

Ontario

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SUMMARY OF QUALIFICATIONS

- Master's in Electrical and Computer Engineering (University of Ottawa, May 2025).
- Mixed-Signal IC Designer with experience in high-speed circuits and transistor-level design.
- Worked with SerDes sub-circuits, including ADC, DAC, serializers/deserializers.
- Familiar with PLL architecture and sub-blocks like VCOs, charge-pumps, and dividers in SerDes systems.
- Skilled in Cadence Virtuoso, Spectre, HSPICE, and physical layout verification (DRC, LVS, QRC).
- Knowledge of CMOS design fundamentals, layout effects, and EM/IR reliability.
- Quick learner with problem-solving skills, eager to contribute to cutting-edge IC design.

EDUCATION

Masters, Electrical and Computers

Sep 2023 – May 2025

University of Ottawa, Ontario

- Courses- Principles of digital communications, Digital logic design, Advanced methods for simulation of large-scale circuits, Signal integrity in high-speed designs and Theory of semiconductor devices.
- Currently extending SERDES design with a custom PLL and CDR chain for signal recovery at 10GHz.
- Current GPA: 8.5/10.

Bachelors, Electronics and Communication

Bangalore University, India

Jul 2017 - Jul 2021

- Courses- VLSI Design, Analog Electronics, Digital circuits, Embedded systems, Microprocessors and VHDL.
- Hand on experience with tools such as PSpice, ModelSIM, Matlab and Vivado.
- Secured first place in an inter-collegiate circuit design competition organized by IEEE.
- GPA: 7.6/10

WORK EXPERIENCE

Graduate Research Assistant

Jun 2024 – Dec 2024

University of Ottawa, Ottawa, ON

- Developed highly efficient MATLAB code for simulating complex threshold voltage equations in BSIM.
- Designed and simulated MOSFET-based circuits in Cadence Virtuoso for analog/mixed-signal applications.
- Performed post-layout verification (DRC, LVS, parasitic extraction) using Cadence Assura and Quantus.
- Conducted SPICE simulations (Spectre, HSPICE) to analyze transistor-level behavior and optimize circuit performance.
- Utilized Design_compiler to generate a gate-level netlist for ALU circuitry and fabricated the design in Cadence Innovus.
- Formulated a floor plan for the I/O pads, and handled component placement and routing to create an IC package.
- Independently debugged and optimized design issues ensuring a 0% error margin in simulations and testing.
- Documented testing procedures and results, ensuring compliance with the needed requirements.

Graduate Teaching Assistant (ELG 4137)

Jan 2024 - Apr 2024

University of Ottawa, Ottawa, ON

- Guided students in Cadence Virtuoso and HSpice-based circuit design and layout verification.
- Adapted Mosfet's knowledge and took tutorials for students, fostering a deeper understanding of VLSI applications.

Assistant System Engineer

Nov 2021 - Aug 2023

Tata Consultancy Services Ltd.

- Drove continuous integration of software builds using Jenkins, achieving a 95% success rate and collaborating with developers to resolve integration roadblocks.
- Developed and executed automated regression tests, improving testing efficiency by 30% and ensuring thorough validation of software components.
- Documented test plans, procedures, and results, and maintained project information using tools such as JIRA and RTC.
- Performed smoke testing on HIL setup with the tools such as ETAS INCA, DSpace ControlDesk, and Lauterbach.

TECHNICAL SKILLS

- Programming languages: C, C++, Python, MATLAB, VHDL, Verilog, knowledge of TCL.
- Simulation & Modeling: MATLAB, Simulink.
- Physical Layout & Verification: Virtuoso Layout Suite, Innovus, Cadence Assura.
- Verification & Automation: DRC, LVS, post-layout extraction, JIRA, Git, Jenkins.
- Mixed-signal circuit Design: DAC, ADC, Serializer, Deserializer, ALU, OPAMP, MUX, Flip Flop.
- CAD Tools: Virtuoso, Innovus, HSpice, Vivado, Design Compiler, EagleCAD, SPECTRE, PSpice.
- Operating Systems: Windows, Linux (CentOS).
- IDEs: Visual Studio, Visual Studio Code, Notepad++, JetBrains.

ACADEMIC PROJECTS

SAR-Based ADC (10GHz Operating Frequency)

- Designed a highly efficient SAR based ADC using Cadence Virtuoso and executed it on CMOS 65nm process.
- Developed the entire ADC block comprising sub blocks such as Comparator, Sample/Hold circuit, DAC and SAR using digital circuits such as D- flip flop, D'Latch, inverter and analog circuits such as Bootstrapped switch.
- Enhanced the critical circuit blocks, including the bootstrapped switch , comparator, and CTLE equalizer circuit to increase the SAR ADC speed from 100MHz to 10GHz for the SerDes Receiver boosting the speed by a factor of 100.
- Currently extending the design with additional modules (CDR, PLL).

SERDES Transceiver

- Designed a high performance SERDES transceiver using Cadence Virtuoso on the CMOS 65nm process.
- Architected and implemented a 4:1 serializer for a high-speed transmitter, including digital logic (MUX, D-FF, D-latch) and analog driver circuits (pre-driver, voltage driver).
- Performed impedance matching analysis and optimization for the transmission channel.
- Performed signal integrity analysis using the Eye diagram for the LVDS transmitter using a PRBS voltage source.

Mini SPICE Simulator

- Developed a circuit simulation tool in C++ with capabilities paralleling commercial SPICE tools.
- Implemented LU decomposition and advanced matrix algorithms for accurate DC and transient analyses.
- Integrated Python's Matplotlib for dynamic waveform visualization.

Analog Circuit Design and Validation with MATLAB and HSPICE

- Modeled and simulated RLC networks and op-amp based amplifier circuits using MATLAB, employing techniques like LU decomposition, Taylor/Padé approximations, and Newton-Raphson methods.
- Validated circuit designs by correlating MATLAB models with HSPICE simulations, including netlist generation and transient/AC response analysis.

CAN Controller Design

- Designed and optimized a CAN transmitter buffer module in Verilog using Xilinx Vivado.
- Developed and executed Verilog test benches to validate design functionality and improve system modularity.

Inclusive Bike for the Physically Disabled

- Integrated and tested embedded electronics to enhance safety and communication features.
- Engineered circuit frameworks and programmed microcontrollers in C on Arduino platform.
- Designed circuit layouts using EagleCAD and refined the system following Agile methodologies.

Smart Door Unlock & Surveillance System

- Implemented face detection algorithms using Python and OpenCV, improving detection accuracy by 20%.
- Developed automated voice note generation for personalized security alerts.

ACHIEVEMENTS AND LEADERSHIP EXPERIENCE

- Facilitated team coordination and communication, ensuring smooth workflow and timely delivery of software projects.
- Delivered high-quality, client-approved software products, consistently meeting all requirements.
- Provided technical support and mentorship to team members, contributing to problem-solving and skill development.