

BIRZEIT UNIVERSITY

FACULTY OF ENGINEERING AND TECHNOLOGY

DEPARTMENT OF ELECTRICAL AND COMPUTER ENGINEERING

CHIP DESIGN VERIFICATION

ENCS5140

**COURSE PROJECT**

**PHASE NO.2 – VERIFICATION PLAN**

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Section 1

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# **1. Description of the Verification Levels**

The verification of this chip will be done at two levels:

* The first verification is done at unit level to ensure that the internal parts of the chip work as expected and doesn’t have bugs. The internal units that need to be checked are the memory and the index register.
* The second verification is done at the top level to verify the functionality of the whole chip and ensure that it works as demonstrated in the chip specifications.

# **2. Functions to be Verified**

The table below list the functions of the DUT that are going to be verified.

|  |  |
| --- | --- |
| **Critical functions** | **Secondary functions** |
| The Compression Algorithm | Reset Function |
| The Decompression Algorithm | Clock Scheduling Function |
| Command Handling Function | Checking Memory Status function |
| Error Detection and Reporting Function | Generating the output (response) function |

# **3. Required Human Resources**

The human resources required are design verification engineers and for this project we (Doha Hmeid and Raghad Afghani) are the human resources.

# **4. Required Tools**

Below are the needed tools for the verification process:

* Simulation engine/environment
* Waveform viewer
* Testbench (will be created using SystemVerilog/UVM)
* Memory – to store the test data and save the simulation results.

# **5. Schedule Details**

The whole verification process must take 2 weeks.

# **6. Specific Tests and Methods**

The verification environment type is grey box, since we are going to check the whole DUT chip and some of it’s internal units like memory and vector index as mentioned earlier.

The verification strategy will include some deterministic test to make sure we covered the corner cases. It will also include pseudo random generated tests to make sure we get the highest coverage ratio possible.

For checking, the testbench waveforms will be used by checking the I/O ports to ensure data correctness.

# **7. Coverage Requirements**

The verification must cover all the functional features of the DUT including the compression and decompression algorithms, input/output ports, command handling, and error detection. And it also must achieve code coverage percentage of more than 90%.

# **8. Completion Criteria**

The verification process is completed when:

* All the test cases are done successfully
* The coverage target is achieved.
* There are no open issues or reviews left for the DUT
* The final regression results are bug-free.

# **9. Test Plan (Matrix)**

|  |  |  |
| --- | --- | --- |
| **Topic** | **Test#** | **Description** |
| Input Command sequences | 1.1 | No Operation: the module remains inactive with no changes to its state or outputs. |
| 1.2 | Compression: searches for existing data, outputs its index if found, or stores it and outputs the new index if not. |
| 1.3 | Decompression: retrieves and outputs data corresponding to the provided index, or reports an error if the index is invalid. |
| 1.4 | Invalid Command: Immediately sets the response to an error state (2'b11), performing no other action. |
| Data compression algorithm | 2.1 | Verify that the compressed output matches the index of stored data in dictionary memory for known inputs. |
| Data decompression algorithm | 3.1 | Verify that the decompressed output matches original data for inputs that have previously been compressed. |
| Error generation | 4.1 | Verify that an error is generated when the data input is empty |
| 4.2 | Verify that an error is generated when compression operation fails |
| 4.3 | Verify that an error is generated when decompression operation fails |
| Ports | 5.1 | Verify that the response port reflects the output correctly |
| Reset | 6.1 | All internal states (memory, index register) are reset to default values upon reset signal. |
| Full system integration | 7.1 | The entire chip works as expected under realistic, complex data patterns and operational conditions. |
| Corner cases | 8.1 | Memory overflow - Verify that an error is generated when the memory is full and a data needs to be written in it (compression case and input not found in memory) |

# **10. Risks and dependencies**

The risks that might affect the verification process are:

* Not meeting the defined verification schedule.
* Incomplete or incorrect test cases.

The verification process depends on the chip specifications and the simulation environment and tools.