Raghav Gupta

Website | GitHub | LinkedIn
raghavgupta@berkeley.edu | 424.272.7363

EDUCATION

UNIVERSITY OF CALIFORNIA, BERKELEY | BS in Electrical Engineering and Computer Science
Expected May 2023 | GPA: 3.96/4.0
Dean's List | Honors to Date

Coursework:
Computer Architecture and Engineering (A) • Advanced Topics in Computer Systems (in-progress) • Introduction to Digital Design and Integrated Circuits (A+) • 22nm SoC for IoT (A) • Great Ideas in Computer Architecture (A) • Operating Systems and System Programming (A)

RESEARCH INTERESTS: COMPUTER ARCHITECTURE

Hardware/Software Co-design • Domain-Specific Architectures and Accelerators • High-Performance/Hyperscale Computing • Profile-Guided Architecture/Microarchitecture

WORK/RESEARCH EXPERIENCE

ADEPT/SLICE LAB AT UC BERKELEY | Undergraduate Student Researcher
Jan 2021 – Present | Berkeley, CA | Website

Working on computer architecture topics with graduate students in Prof. Krste Asanovic's and Prof. Borivoje Nikolic's groups.

Extending FirePerf to Userspace | Original Paper | Poster | Userspace Paper
- An FPGA-accelerated full-system hardware/software performance profiling utility built on top of FireSim
- Provides high-fidelity out-of-band introspection with call stack reconstruction and Flame Graph generation
- Extended FirePerf to support userspace profiling by instrumenting Rocket Chip trace port, obtaining DWARF + hex information, constructing a user binary search space and matching traces to it

FireMarshal Networking | Original Paper
- FireMarshal is an open-source software workload management tool for reliable and reproducible research
- Automates bootable workload image generation and evaluation on FireSim, QEMU, and Spike platforms
- Implemented running multi-node workloads concurrently in QEMU
- Implemented a network interface using Virtual Distributed Ethernet for multi-node workloads emulated in QEMU

Specialized Accelerator for a Hyperscale SoC
- Currently performing initial exploration to accelerate a datacenter tax as part of a Hyperscale SoC

NVIDIA | Power Architect Intern
May 2022 – Aug 2022 | Santa Clara, CA

CPU Power Modeling for Gaming Workloads
- Developed a strategy for application-specific CPU power modeling on production silicon
- Targeted characteristics of gaming workloads and isolated static and dynamic power costs
- Automated data collection, processing, visualization, modeling and summary statistics

TEACHING EXPERIENCE

EECS 151/251A - INTRODUCTION TO DIGITAL DESIGN AND INTEGRATED CIRCUITS | Teaching Assistant
Fall 2022 | Website

- Teaching 1 weekly office hour and 1 weekly lab section using Xilinx PYNQ FPGAs for Berkeley's upper division VLSI course catered towards undergraduates and graduates
- Helping students learn hardware design methods and principles using Verilog, VCS, and waveforms as they implement FSMs, audio synthesis circuits, UART modules and FIFOs on FPGAs
- Supporting students in applying architectural and microarchitectural concepts to design a 3+ stage pipelined RISC-V datapath with L1 data cache, UART/MMIO and optimize it for timing

- Designed a memory controller lab with specification and testbenches as an introduction to working with synchronous memories

EECS16A - DESIGNING INFORMATION DEVICES AND SYSTEMS I | Lab Teaching Assistant and Head Lab Content/Development
Summer 2020 – Spring 2022 | Website

- Taught a weekly lab section of 50+ engineering undergraduates for Berkeley's introductory EECS course for 5 semesters
- Assisted students in building a single pixel camera, resistive and capacitive touchscreens, and an acoustic positioning system
- Trained lab staff and managed lab content for 1000+ students, revamped existing labs, developed new labs and managed the shift to online labs while achieving the requisite learning goals.

CS61C - GREAT IDEAS IN COMPUTER ARCHITECTURE | Teaching Assistant
Summer 2021 | Website

- Taught 2 discussion sections and 1 office hour weekly for Berkeley's introductory computer architecture and systems course
- Developed content and infrastructure for projects on C programming and Logisim datapath design
- Helped design labs on Logisim datapath design, pipelining, and caches

EE290C - 22NM SOC FOR IOT | Course Content Developer
Fall 2022

- Working with Prof. Borivoje Nikolic on an Intel supported project to develop teaching resources for RISC-V SoC tapeout in Intel 16 technology that will eventually be shared as part of Intel's University Shuttle Program
- Developing 2 labs on using the Chipyard framework for SoC development, with a focus on the use of RTL generators (especially custom accelerators), verification in simulation, and the VLSI flow (especially dealing with DRC and LVS)
- Will develop an open-source version with Skywater 130 to function as an asynchronous Chipyard tutorial

PROJECTS

BEARLY ML: SOC FOR MACHINE LEARNING | EE290C
Jan 2022 – May 2022 | Poster
- Designed, verified, and taped-out a RISC-V SoC with ML/DSP accelerators in Intel 16 technology using the Chipyard environment
- Member of 5-person team that developed a sparse-dense matrix multiplication accelerator using the Rocket Custom Coprocessor (RoCC) interface
- Tightly-coupled with a 5 stage, in-order Rocket core with 16KB L1 DCache, 4KB L1 ICache
- Wrote Chisel RTL, performed verification in functional simulation with unit-testing and integration testing with bare-metal C tests, and resolved floor-planning Design Rule Violations
- Maximum frequency: 500 MHz, Achievable Throughput: 2.6 uint8 GOPS

RISC-V CORE ON FPGA | EECS151
Oct 2021 – Dec 2021 | Report
- Team of 2 that designed a 3-stage RISC-V core with UART/MMIO, polyphonic audio synthesizer and BHT-based branch predictor in Verilog
- Won class-wide Apple design contest for performance at a frequency of 70 MHz with a CPI of 1.16 on the matrix multiplication kernel

BRANCH PREDICTOR | Lab Project for CS152
Mar 2021 – Apr 2021 | Report
- Designed and analyzed an 8192-entry tournament predictor using a Gshare predictor, a bimodal predictor, and an arbiter in a 3-person team
- Implemented using the C++ branch predictor framework in BOOM out-of-order core
- Performed >25% better than baseline bimodal predictor

PINTOS | Projects for CS162
Jan 2022 – May 2022
- As a 3-person team, implemented the following features in an x86-based educational OS running as a VM in QEMU/Bochs with extensive debugging in GDB
- Supported user program execution with syscall argument passing, process control syscalls (halt, exec, wait, exit), basic file operation syscalls, and a floating point unit

- Implemented multithreading with an efficient sleep timer, strict priority scheduler with priority donation, and a simplified version of the user-level pthread library and user-level synchronization
- Implemented a Unix FFS-like filesystem with buffer cache, extensible files and support for subdirectories and relative paths

CS61CPU | PROJECT FOR CS61C

Nov 2020

- Designed a 2-stage pipelined RISC-V Datapath using Logisim in a team of 2
- Optimized control logic by simplifying boolean expressions for each signal
- Won class-wide Apple design contest for minimal transistor use

AWARDS

- EECS Oustanding TA Award (2020 - 2021)
- CS61C Project - Apple Design Award (Fall 2020)
- EECS151 Project - Apple Design Award (Fall 2021)
- Edward Frank Kraft Award (Fall 2019)
- Times of India - Spark Scholarship (2018)

ORGANIZATIONS

ETA KAPPA NU | EECS HONOR SOCIETY

Jan 2021 - Present

TUTORING OFFICER

Responsible for managing activities of the tutoring committee, such as organizing and running exam review sessions, planning daily office hours, and supporting learning resources, in Spring 2022.

DECAL ASSISTANT OFFICER

Responsible for facilitating "Going Down the EECS Stack", a course that explores the different fields within the EECS major, in Fall 2021.

CURIOSITY | TUTOR AND CO-FOUNDER

May 2020 - Aug 2020

- Tutored high school students on STEM topics and SAT prep during Summer 2020
- Raised ₹15,000 and donated all funds to COVID-19 and flood relief

SKILLS

Python • C/C++ • Git • Verilog • Chisel • Java • Linux/Bash • GDB • RISC-V • CUDA • Parallel Programming • Vivado • ROS • Machine Learning • Deep Learning • Computer Vision