

# Raghav Gupta

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## EDUCATION

### UNIVERSITY OF CALIFORNIA, BERKELEY | PHD IN COMPUTER SCIENCE

Aug 2023 - Present

Advisor: Prof. Borivoje Nikolic

#### COURSEWORK:

Architectures and Systems for Warehouse-Scale Computers (A)

### UNIVERSITY OF CALIFORNIA, BERKELEY | BS IN ELECTRICAL ENGINEERING AND COMPUTER SCIENCE

Aug 2019 - May 2023 | GPA: 3.95/4.0

High Honors | Dean's List

#### COURSEWORK:

Computer Architecture and Engineering (A) • Operating Systems and System Programming (A) • Introduction to Digital Design and Integrated Circuits (A+) • 22nm SoC for IoT (A) • Advanced Topics in Computer Systems (A-) • Programming Languages and Compilers (A)

## RESEARCH INTERESTS: COMPUTER ARCHITECTURE

Hyperscale Architecture and Systems • Hardware/Software Co-design • Profile-Guided Methods

## RESEARCH EXPERIENCE

### SLICE LAB AT UC BERKELEY | STUDENT RESEARCHER

Jan 2021 - Present | Berkeley, CA | Website

#### MULTI-LEVEL SIMULATION | In-progress

- Building a multi-level simulator that trades-off speed and fidelity in a hierarchy of simulators to enable DSE on large workloads
- Using program analysis to identify critical portions of an execution trace to execute at high fidelity
- Investigating warm-up strategies to approximate cache state

#### ACCELERATING HYPERSCALE RPCs | In-progress

- Investigating orchestration to offload RPCs to a collection of accelerators
- Working on porting the RPC software stack to RISC-V

#### EXTENDING FIREPERF TO USERSPACE | Original Paper | Poster | Userspace Paper

- An FPGA-accelerated full-system hardware/software performance profiling utility built on top of FireSim
- Provides high-fidelity out-of-band introspection with call stack reconstruction and Flame Graph generation
- Extended FirePerf to support userspace profiling by instrumenting Rocket Chip trace port, obtaining DWARF + hex information, constructing a user binary search space and matching traces to it

#### FIREMARSHAL NETWORKING | Original Paper

- FireMarshal is an open-source software workload management tool for reliable and reproducible research
- Automates bootable workload image generation and evaluation on FireSim, QEMU, and Spike platforms
- Implemented running multi-node workloads concurrently in QEMU
- Implemented a network interface using Virtual Distributed Ethernet for multi-node workloads emulated in QEMU

## WORK EXPERIENCE

### NVIDIA | POWER ARCHITECT INTERN

May 2022 - Aug 2022 | Santa Clara, CA

#### CPU POWER MODELING FOR GAMING WORKLOADS

- Developed a strategy for application-specific CPU power modeling on production silicon
- Targeted characteristics of gaming workloads and isolated static and dynamic power costs
- Automated data collection, processing, visualization, modeling and summary statistics

## **OMNISTRATE | SOFTWARE ENGINEERING INTERN**

May 2023 – July 2023 | Remote

### **MONITORING FOR STATEFUL CONTAINERIZED CLOUD APPLICATIONS**

- Developed monitoring infrastructure for stateful containers using the sidecar pattern
- Implemented support for application-specific probes and process metadata checks to trigger alerts and fail-over
- Improved reliability at scale for a public database provider's DBaaS offering

## **TEACHING EXPERIENCE**

### **EE290C - 22NM SOC FOR IOT | TEACHING ASSISTANT**

Fall 2022 - Spring 2023

- Developed teaching resources for RISC-V SoC tapeout, on topics such as the use of RTL generators (especially custom accelerators) and verification in simulation, that were shared as part of Intel's University Shuttle Program
- Managed and supported 3 teams across 2 chips as they designed specialized modules for sparse-dense matrix multiplication, near-cache compute, and Extended Kalman Filter

### **EECS 151/251A - INTRODUCTION TO DIGITAL DESIGN AND INTEGRATED CIRCUITS | TEACHING ASSISTANT**

Fall 2022 | Website

- Taught 1 weekly office hour and 1 weekly lab section using Xilinx PYNQ FPGAs for Berkeley's upper division VLSI course catered towards undergraduates and graduates
- Helped students learn hardware design methods and principles using Verilog, VCS, and waveforms as they implemented FSMs, audio synthesis circuits, UART modules and FIFOs on FPGAs
- Supported students in applying architectural and microarchitectural concepts to design a 3+ stage pipelined RISC-V datapath with L1 data cache, UART/MMIO and optimize it for timing
- Designed a memory controller lab with specification and testbenches as an introduction to working with synchronous memories

### **EECS16A - DESIGNING INFORMATION DEVICES AND SYSTEMS I | LAB TEACHING ASSISTANT AND HEAD LAB CONTENT/DEVELOPMENT**

Summer 2020 – Spring 2022 | Website

- Taught a weekly lab section of 50+ engineering undergraduates for Berkeley's introductory EECS course for 5 semesters
- Assisted students in building a single pixel camera, resistive and capacitive touchscreens, and an acoustic positioning system
- Trained lab staff and managed lab content for 1000+ students, revamped existing labs, developed new labs and managed the shift to online labs while achieving the requisite learning goals.

### **CS61C - GREAT IDEAS IN COMPUTER ARCHITECTURE | TEACHING ASSISTANT**

Summer 2021 | Website

- Taught 2 discussion sections and 1 office hour weekly for Berkeley's introductory computer architecture and systems course
- Developed content and infrastructure for projects on C programming and Logisim datapath design
- Helped design labs on Logisim datapath design, pipelining, and caches

## **PROJECTS**

### **BEARLY ML: SOC FOR MACHINE LEARNING | EE290C**

Jan 2022 – May 2022 | Poster

- Designed, verified, and taped-out a RISC-V SoC with ML/DSP accelerators in Intel 16 technology using the Chipyard environment
- Member of 5-person team that developed a sparse-dense matrix multiplication accelerator using the Rocket Custom Coprocessor (RoCC) interface
- Tightly-coupled with a 5 stage, in-order Rocket core with 16KB L1 DCache, 4KB L1 ICache
- Wrote Chisel RTL, performed verification in functional simulation with unit-testing and integration testing with bare-metal C tests, and resolved floor-planning Design Rule Violations
- Maximum frequency: 500 MHz, Achievable Throughput: 2.6 uint8 GOPS

## PINTOS | PROJECTS FOR CS162

Jan 2022 – May 2022

- As a 3-person team, implemented the following features in an x86-based educational OS running as a VM in QEMU/Bochs with extensive debugging in GDB
- Supported user program execution with syscall argument passing, process control syscalls (halt, exec, wait, exit), basic file operation syscalls, and a floating point unit
- Implemented multithreading with an efficient sleep timer, strict priority scheduler with priority donation, and a simplified version of the user-level pthread library and user-level synchronization
- Implemented a Unix FFS-like filesystem with buffer cache, extensible files and support for subdirectories and relative paths

## PUBLICATIONS AND PRESENTATIONS

- <Anonymized>, <Anonymized>, <Anonymized>, <Anonymized>, <Anonymized>, **Raghav Gupta**, <Anonymized>, et al. **"Partitioning Large-Scale Monolithic Hardware Designs for FireSim."** (Under submission)
- Chi, Yufeng, Franklin Huang, **Raghav Gupta**, Ella Schwarz, Jennifer Zhou, Reza Sajadiany, Animesh Agrawal, et al. **"A Heterogeneous RISC-V SoC for ML Applications in Intel 16 Technology."** Poster presented at HotChips 2023, Stanford, CA, August 27-28, 2023.

## AWARDS

- EECS Outstanding TA Award (2020 - 2021)
- CS61C Project - RISC-V CPU in Logisim - Apple Design Award (Fall 2020)
- EECS151 Project - RISC-V Core on FPGA - Apple Design Award (Fall 2021)
- Edward Frank Kraft Award (Fall 2019)
- Times of India - Spark Scholarship (2018)

## ORGANIZATIONS

### ETA KAPPA NU | EECS HONOR SOCIETY

Jan 2021 - May 2023

#### TUTORING OFFICER

Responsible for managing activities of the tutoring committee, such as organizing and running exam review sessions, planning daily office hours, and supporting learning resources, in Spring 2022.

#### DECAL ASSISTANT OFFICER

Responsible for facilitating "Going Down the EECS Stack", a course that explores the different fields within the EECS major, in Fall 2021.

### CURIOSITY | TUTOR AND CO-FOUNDER

May 2020 - Aug 2020

- Tutored high school students on STEM topics and SAT prep during Summer 2020
- Raised ₹15,000 and donated all funds to COVID-19 and flood relief

## SKILLS

Python • C/C++ • Git • Linux/Bash • Verilog • Chisel • Go • RISC-V • CUDA • Java • Vivado • Docker • Kubernetes • ROS