Raghav Chawla

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Education

Bachelors of Technology with Honors (2014-18) in Electronics & Communication Engineering, (CGPA: 8.293/10)
Indian Institute of Technology, Roorkee

Scored 94.2% in 12th Standard CBSE

Areas of Interest

Semiconductor Devices, Biomedical Circuits, Device-Circuit co-design, Timing Models

Research Publications

- **R. Chawla**, S. Yadav, A. Sharma, B. Kaur, R. Pratap, and A. Bulusu, "*TSV Induced Stress Model and Its Application in Delay Estimation*", in **IEEE SOI-3D-Subthreshold Microelectronics Technology Unified Conference**, October 2018 [Link]
- A. Sharma, N. Alam, **R. Chawla**, and A. Bulusu, "*Modelling the Effect of Variability on the Timing Response of CMOS Inverter-Transmission Gate Structure*", in **IEEE International Symposium on Devices, Circuits and Systems**, March 2018 [Link]
- **R. Chawla**, P. Malik, P. N. Singh, and A. Sharma, "*Timing Calibration in Interleaved Current Steering DACs*", in **IEEE International Symposium on Circuits and Systems (ISCAS)**, 2019 (Submitted) [Link]

Project Presentations

- Presented our prototype 'Dynamic Speed Limit' at **Valeo Innovation Challenge, France**
- Presented our solution for the problem of 'Timing Calibration in Interleaved DACs' to the **TR&D Department at STMicroelectronics and IEEE IIT Roorkee Chapter**
- Presented my project 'Cell Delay Modeling for TSV induced stress in 3D ICs' to **Microelectronics Research Group at IIT Roorkee**
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- **Presented my project on Neuromorphic Circuits in Ideaz, cogni. Runner up in paper presentation**

- Internship Topic present in Training Seminar
- Internship Topic present in IEEE

Experience

Graphics Hardware Engineer | Intel Technology India Pvt. Ltd.

Jun 2018 - Present

- Part of Image Processing Unit (IPU) in Intel India, working as Performance owner and partition owner in the team.
- Responsible for partition optimization from Synthesis to ECOs in terms of layout & performance
- Worked on 7 partitions in 4 tape-ins, focussing on congestion, interface ECO's, full-chip IO, DDR paths and power.
- Worked on the following projects:

Key Projects

Intel Discrete Graphics

Jul 2019 - Present

- Working on two fix function partitions with high gate count, to be used in 1st gen Intel Discrete Graphics.
- Converging critical cross-section paths and Dual Data Rate logic paths using different convergence techniques for high frequencies.

IPU6 SE

Nov 2018 - Jul 2019

- Owned a partition, critical with respect to FV and Power optimization while achieving ~20% improvement in die utilization
- Enhanced the design flow, achieving up to 30% overall runtime reduction
- Debugged false timing & LV violations, due to issues in timing constraints and UPF, affecting multiple partitions.

IPU6

May - Aug 2019

- Worked on full chip IO partition, containing multiple voltage domains and interaction with SOC
- Controlled congestion, using multiple ways, arising due to new tightened Quality checks and high density

Automation of Macro Placement

Jan - Apr 2019

- Designed an algorithm in TCL for automating macro placement, to reduce Turnaround Time.
- Placement based on connectivity with ports, maximum core area, and hierarchy grouping.

Other Projects

- Converged a high macro partition with tighter frequency & process constraint, achieving a utilization improvement of > 15% in IPU5 SEP.
- Working as a secondary performance owner, generating timing ECOs at the section level.

Teaching Assistant | IIT Roorkee — Jan - Apr 2017 & 2018

Taught 'Semiconductor Devices', an introductory course for freshmen undergraduate students, for two semesters as Teaching Assistant for Dr. Anand Bulusu.

Internship

Timing Calibration Algorithm for Interleaved Current Steering DAC | **STMicroelectronics** — May - Jul 2017

- Developed a feedback algorithm for removing timing mismatch problems and improving SNR of interleaved current steering DAC structures.
- Achieved < 0.1% timing error at 4GHz frequency, improving the SNR by more than 24 dB.
- The calibration loop requires a bandwidth of only 200 MHz around the Nyquist frequency

Research Projects

Cell Delay modeling for TSV induced stress in 3D ICs | IIT Roorkee — Jul 2017 - May 2018

- Modeled the variation of stress around a Through Silicon Via (TSV) in 3D Interconnects, due to the difference in thermal expansion of Copper & Silicon wafer and calculating the mobility and threshold variations due to the induced stress
- Developed analytical models for propagation delay of Inverter & 2 I/P NAND gate considering TSV induced variations

Design of Analog Neuromorphic Circuits | IIT Roorkee — May - July 2016

- Studied the design perspectives and characteristics of Neuromorphic Circuits, particularly Motion Detection using VLSI circuits.
- Designed the schematic and layout of a circuit discussed in the research paper- Pulse-Based Analog Velocity Sensor in Cadence.

Delay Modelling of a Static flip flop | IIT Roorkee — Jan - Apr 2017

- Developed an Effective Current model for calculating delay in Inverter and Transmission Gate using only the DC current points of nMOS & pMOS
- Included the effect of process variations in the delay model developed

Study of I-V characteristic variations due to defects in CMOS | IIT Roorkee — Aug- Nov 2016

- Studied the electronic band shifting due to various defects like traps and dopant ions
- Simulated the corresponding change in leakage current in MOSFET due to various forms of gate leakage and drain leakage.
- The simulations were performed in TCAD Sentaurus.

Other Projects

Dynamic Speed Limit | Valeo Innovation Challenge, France — Aug - Nov 2017

- Proposed a novel algorithm to reduce congestion on the roads by determining the road-specific speed limit at a particular time, and verified the results using simulation
- Developed a Machine Learning model that takes into account traffic in the city and the situational factors of a specific road like bicycles, pedestrians, and heavy vehicles to calculate the speed limit

FPGA Implementation of Silicon Neurons | IIT Roorkee — Sept - Nov 2016

- Implemented the behavior of the IZH neuron model (to describe the behavior of a synapse in a neuron) in VHDL and demonstrated the results on FPGA
- Used fixed-point model to describe the behavior.

On Device Activity Recognition | IIT Roorkee — Jan - Mar 2017

- Developed an offline activity recognition system to identify user's behavior and thus, provide health tips & product recommendations accordingly
- Used Convolutional Neural Network to predict activity using the accelerometer sensor of the smartphone

Skills

Computer languages	TCL, Perl, Python, VerilogA
Software Packages	TCAD Sentaurus, Xilinx ISE, HSpice, Synopsys DC, ICC2, PT, Cadence Virtuoso, Git
Honors Courses	VLSI Technology, Digital VLSI Circuit Design, Analog VLSI Circuit Design, VLSI Physical Design, Mixed Signal Circuit Design, Semiconductor Device Modeling
Other Relevant Courses	Fundamentals of Nanoscience and Technology, Signal & Systems, Probability & Statistics, Computer Architecture and Microprocessors, Embedded Engineering Design, Machine Learning (Coursera)

Achievements

- Selected among **7 world finalist** teams in Valeo Innovation Challenge 2017 held in Paris, France
- Selected for the finals of **Make in India Hackathon** held at IIT Bombay
- Winner of the **Best Aesthetic design award** in Srishti 2016 (Annual Hobbies Club Exhibition, IIT Roorkee) for the project- Propeller Clock
- Winner of the inter-college competition during Sankalp 2015 (Annual Social Convention, NSS, IIT Roorkee) for a mobile application on Women Security
- Runner Up in the competition- 'Ideaz' organized by ECE Department, IIT Roorkee during Cognizance 2017
- Represented IIT Roorkee in **Inter IIT Tech Meet 2018** in the event- Engineers' Conclave and won Silver Trophy overall

Positions of Responsibility

- **Timing Performance Owner,** IPU, Intel India
- **Member**, IEEE Student Branch, IIT Roorkee
- **Member, Department Students Council**, Department of E&CE, IIT Roorkee
- **Teaching Assistant**, Department of E&CE, IIT Roorkee
- **Mentor,** Student Mentorship Program, IIT Roorkee

References

Mr. Pratap Narayan Singh
CTO, Vervesmi Microelectronics
Ex - Senior Principal Engineer & Senior Member of Technical Staff, STMicroelectronics, Greater Noida
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