

Name	Value
> i[3:0]	0
o[15:0]	0001
o[15]	0
o[14]	0
o[13]	0
o[12]	0
o[11]	0
o[10]	0
o[9]	0
o[8]	0
o[7]	0
o[6]	0
o[5]	0
o[4]	0
o[3]	0
o[2]	0
o[1]	0
o[0]	1



4to16_using3to8 - [C:/Users/raghava guptha/4to16_using3to8/4to16_using3to8.xpr] - Vivado 2023.2

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ELABORATED DESIGN - xc7a35tcpg236-1

Project Summary x Schematic x 4to16_3to8.v * x

3 Cells 20 I/O Ports 21 Nets

The schematic diagram illustrates a 4-to-16 bit decoder implemented using two 3-to-8 decoders (labeled d1 and d2). The input $i[3:0]$ is connected to a 4-bit bus. The least significant bit of this input, $i[0]$, is connected to the enable input ($en0_i$) of an inverter block labeled RTL_INV . The output of the inverter, O , is connected to the enable input (en) of both decoder blocks $d1$ and $d2$. The remaining three bits of the input, $i[2:0]$, are connected to the data input ($i[2:0]$) of both decoder blocks. The output of decoder $d1$ is $o[7:0]$, and the output of decoder $d2$ is also $o[7:0]$. These two 8-bit outputs are concatenated to form the final 16-bit output $o[15:0]$.

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4to16_using3to8 - [C:/Users/raghava guptha/4to16_using3to8/4to16_using3to8.xpr] - Vivado 2023.2

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ELABORATED DESIGN - xc7a35tcbg236-1

Project SummarySchematic4to16_3to8.v*

C:/Users/raghava guptha/4to16_using3to8/4to16_using3to8.srscs/sources_1/new/4to16_3to8.v

5always @(*)

6begin

7if (en == 1'b1)

8begin

9case(i)

103'b000: o = 8'b00000001;

113'b001: o = 8'b00000010;

123'b010: o = 8'b00000100;

133'b011: o = 8'b00001000;

143'b100: o = 8'b00010000;

153'b101: o = 8'b00100000; // Fixed duplicate value

163'b110: o = 8'b01000000; // Fixed incorrect value

173'b111: o = 8'b10000000;

18endcase

19end

20else

21o = 8'b00000000;

22end

23endmodule

24module dec4to16_dec3to8(i, o);

25input [3:0] i;

26output [15:0] o;

27dec_3to8 d1(i[2:0], o[7:0], ~i[3]);

28dec_3to8 d2(i[2:0], o[15:8], i[3]);

29endmodule

Tcl ConsoleMessagesLogReportsDesign Runs

1:5

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ELABORATED DESIGN - xc7a35tcbg236-1

Project Summary xSchematic x4to16_3to8.v* x

C:/Users/raghava guptha/4to16_using3to8/4to16_using3to8.srscs/sources_1/new/4to16_3to8.v

1 module dec_3to8(i, o, en);
2 input [2:0] i;
3 input en;
4 output reg [7:0] o;
5 always @(*)
6 begin
7 if (en == 1'b1)
8 begin
9 case(i)
10 3'b000: o = 8'b00000001;
11 3'b001: o = 8'b00000010;
12 3'b010: o = 8'b00000100;
13 3'b011: o = 8'b00001000;
14 3'b100: o = 8'b00010000;
15 3'b101: o = 8'b00100000; // Fixed duplicate value
16 3'b110: o = 8'b01000000; // Fixed incorrect value
17 3'b111: o = 8'b10000000;
18 endcase
19 end
20 else
21 o = 8'b00000000;
22 end
23 endmodule
24 module dec4to16_dec3to8(i, o);
25 input [3:0] i;
26 output [15:0] o;

Tcl ConsoleMessagesLogReportsDesign Runs

1:5

Insert




















Verilog

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84°F

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ENG IN

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6/15/2025

Name	Value
>  i[3:0]	0
 en	1
✓  o[15:0]	8000
 [15]	1
 [14]	0
 [13]	0
 [12]	0
 [11]	0
 [10]	0
 [9]	0
 [8]	0
 [7]	0
 [6]	0
 [5]	0
 [4]	0
 [3]	0
 [2]	0
 [1]	0
 [0]	0



4to16_using2to4 - [C:/Users/raghava guptha/4to16_using2to4/4to16_using2to4.xpr] - Vivado 2023.2

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ELABORATED DESIGN - xc7a35tcbg236-1

Project Summary x Schematic x 4to16_2to4.v * x

5 Cells 21 I/O Ports 25 Nets

The schematic diagram illustrates a 4-to-16 bit decoder implemented using four 2-to-4 decoders (labeled d1, d2, d3, d4, and d5). The input is a 4-bit signal $i[3:0]$ and an enable signal en . The output is a 16-bit signal $o[15:0]$. The decoders are connected as follows: d1 takes $i[3:0]$ and en as inputs and outputs $o[3:0]$. d2, d3, d4, and d5 each take $o[3:0]$ and en as inputs and output $o[3:0]$. The outputs of d2, d3, d4, and d5 are connected to the output $o[15:0]$.

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Project Summary x Schematic x 4to16_2to4.v* x

C:/Users/raghava guptha/4to16_using2to4/4to16_using2to4.srscs/sources_1/new/4to16_2to4.v

Q

1 module dec_2to4(a, b, en, o);

2 input a, b, en;

3 output reg [3:0] o;

4 always @(*)

5 begin

6 if (en == 1'b1)

7 begin

8 case({a, b})

9 2'b00: o = 4'b0001;

10 2'b01: o = 4'b0010;

11 2'b10: o = 4'b0100;

12 2'b11: o = 4'b1000;

13 endcase

14 end

15 else

16 o = 4'b0000;

17 end

18 endmodule

19 module dec4to16_dec2to4(i, o, en);

20 input [3:0] i;

21 input en;

22 output [15:0] o;

23 wire [3:0] w; // First stage decoder (decodes upper 2 bits)

24 dec_2to4 d1(i[3], i[2], en, w); // Second stage decoders (decode lower 2 bits)

25 dec_2to4 d2(i[1], i[0], w[0], o[3:0]);

26 dec_2to4 d3(i[3], i[2], w[1], o[7:4]);

27 dec_2to4 d4(i[1], i[0], w[1], o[11:8]);

28 dec_2to4 d5(i[3], i[2], w[1], o[15:12]);

29 endmodule

Tcl Console Messages Log Reports Design Runs

1:8

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