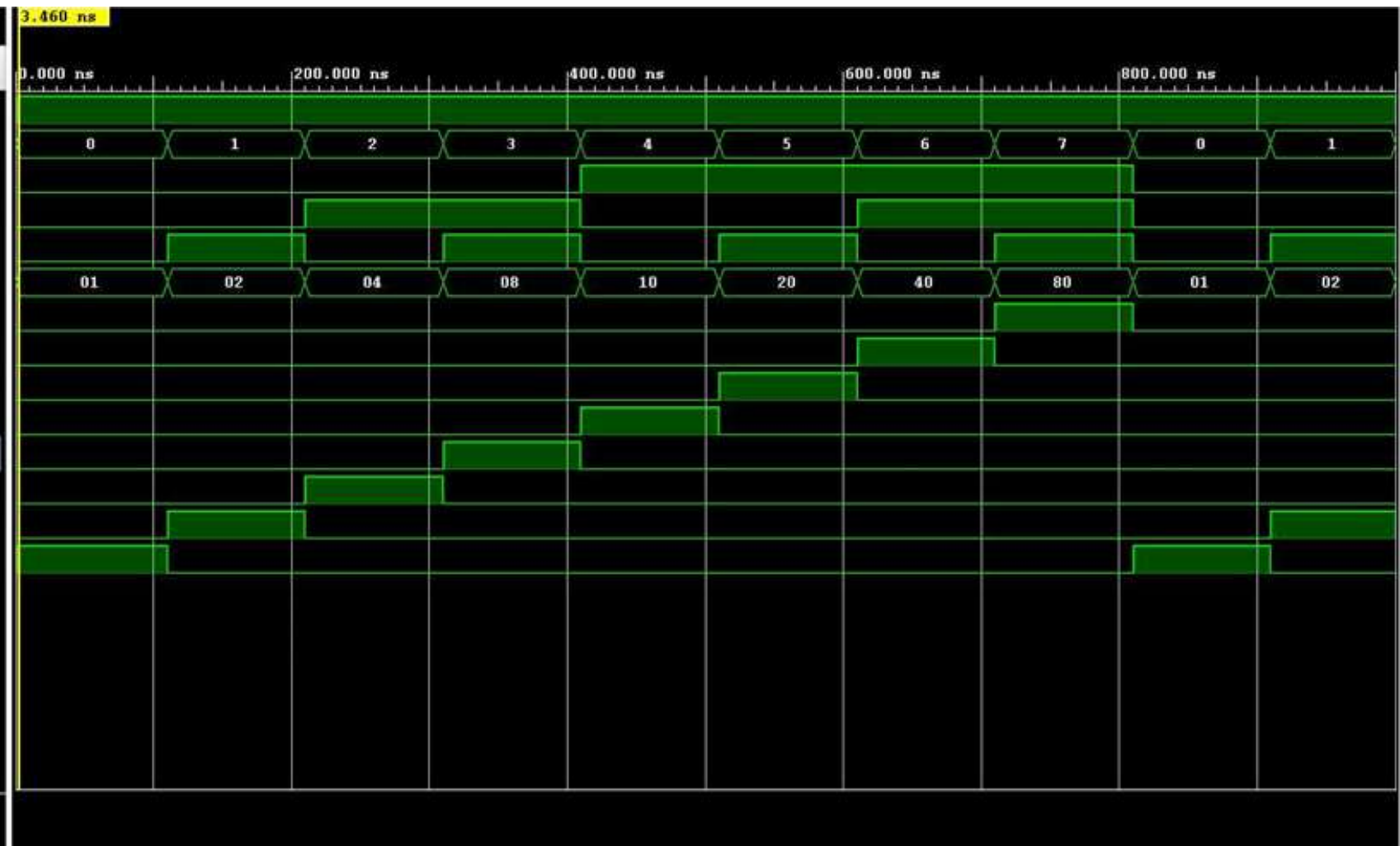


Name	Value
i	1
▼ s[2:0]	0
[2]	0
[1]	0
[0]	0
▼ o[7:0]	01
[7]	0
[6]	0
[5]	0
[4]	0
[3]	0
[2]	0
[1]	0
[0]	1



1to8_1to2 - [C:/Users/raghava guptha/1to8_1to2/1to8_1to2.xpr] - Vivado 2023.2

File Edit Flow Tools Reports Window Layout View Help Q- Quick Access

Ready

Default Layout

Flow Navigator

ELABORATED DESIGN - xc7a35tcbg236-1

Project Summary x Schematic x 1to8_1to2.v x

7 Cells 12 I/O Ports 18 Nets

Sources

Netlist

Source File Properties

PROJECT MANAGER

- Settings
- Add Sources
- Language Templates
- IP Catalog

IP INTEGRATOR

- Create Block Design
- Open Block Design
- Generate Block Design

SIMULATION

- Run Simulation

RTL ANALYSIS

- Run Linter
- Open Elaborated Design
- Report Methodology
- Report DRC
- Report Noise
- Schematic

Schematic

Diagram showing a 1-to-8 decoder circuit implemented using seven 2-to-1 demultiplexers (d1 to d7). The input is a 3-bit signal s[2:0]. The output is an 8-bit signal o[7:0]. The circuit is structured as follows:

- Input s[2:0] is connected to the 'i' input of demux_2tol d1.
- Output o[1:0] of d1 is connected to the 'i' inputs of demux_2tol d2 and d3.
- Output o[1:0] of d2 is connected to the 'i' inputs of demux_2tol d4 and d5.
- Output o[1:0] of d3 is connected to the 'i' inputs of demux_2tol d6 and d7.
- Output o[1:0] of d4 is connected to output o[7:0].
- Output o[1:0] of d5 is connected to output o[7:0].
- Output o[1:0] of d6 is connected to output o[7:0].
- Output o[1:0] of d7 is connected to output o[7:0].

Tcl Console Messages Log Reports Design Runs

1to8_1to2 - [C:/Users/raghava guptha/1to8_1to2/1to8_1to2.xpr] - Vivado 2023.2

FileEditFlowToolsReportsWindowLayoutViewHelpQ- Quick Access

Ready

Default Layout

Flow Navigator

PROJECT MANAGER

Settings

Add Sources

Language Templates

IP Catalog

IP INTEGRATOR

Create Block Design

Open Block Design

Generate Block Design

SIMULATION

Run Simulation

RTL ANALYSIS

Run Linter

Open Elaborated Design

Report Methodology

Report DRC

Report Noise

Schematic

ELABORATED DESIGN - xc7a35tcbg236-1

Sources

Netlist

Source File Properties

Project Summary xSchematic x1to8_1to2.v * x

C:/Users/raghava guptha/1to8_1to2/1to8_1to2.srscs/sources_1/new/1to8_1to2.v

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25

module demux_2tol(i, s, o);

input i, s;

output reg [1:0] o;

always @(*)

begin

case(s)

1'b0: o = {1'b0, i};

1'b1: o = {i, 1'b0};

endcase

end

endmodule

module demux1to8(i, s, o);

input i;

input [2:0] s;

output [7:0] o;

wire [5:0] w;

demux_2tol d1(i, s[2], w[1:0]);

demux_2tol d2(w[0], s[1], w[3:2]);

demux_2tol d3(w[1], s[1], w[5:4]);

demux_2tol d4(w[2], s[0], o[1:0]);

demux_2tol d5(w[3], s[0], o[3:2]);

demux_2tol d6(w[4], s[0], o[5:4]);

demux_2tol d7(w[5], s[0], o[7:6]);

endmodule

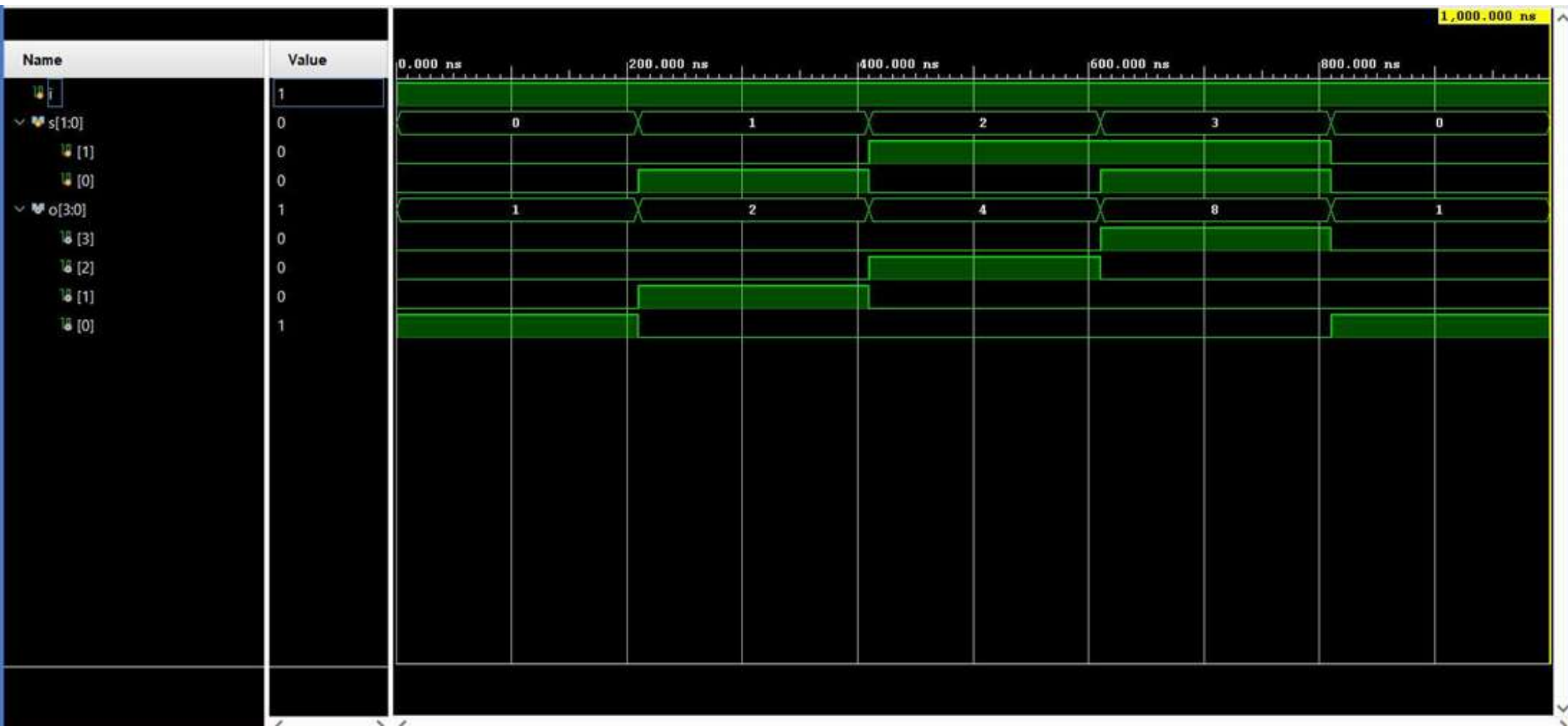
Tcl ConsoleMessagesLogReportsDesign Runs

1:5InsertVerilog

84°FPartly cloudy

Search

7:15 PM6/15/2025



1to4_1to2 - [C:/Users/raghava guptha/1to4_1to2/1to4_1to2.xpr] - Vivado 2023.2

File Edit Flow Tools Reports Window Layout View Help Q- Quick Access Ready

Flow Navigator

- PROJECT MANAGER
 - Settings
 - Add Sources
 - Language Templates
 - IP Catalog
- IP INTEGRATOR
 - Create Block Design
 - Open Block Design
 - Generate Block Design
- SIMULATION
 - Run Simulation
- RTL ANALYSIS
 - Run Linter
 - Open Elaborated Design
 - Report Methodology
 - Report DRC
 - Report Noise
 - Schematic

ELABORATED DESIGN - xc7a35tcbg236-1

Project Summary x Schematic x 1to4_1to2.v x

3 Cells 7 I/O Ports 9 Nets

The schematic shows three 2-to-1 demux_2to1 blocks (d1, d2, d3) connected in a cascaded manner. The input 'i' and select signal 's[1:0]' are connected to the first block (d1). The output 'o[1:0]' of d1 is connected to the input 'i' of the second block (d2). The output 'o[1:0]' of d2 is connected to the input 'i' of the third block (d3). The output 'o[1:0]' of d3 is connected to the final output 'o[3:0]'.

Tcl Console Messages Log Reports Design Runs

1to4_1to2 - [C:/Users/raghava guptha/1to4_1to2/1to4_1to2.xpr] - Vivado 2023.2

File Edit Flow Tools Reports Window Layout View Help Q- Quick Access Ready

Flow Navigator

- PROJECT MANAGER
 - Settings
 - Add Sources
 - Language Templates
 - IP Catalog
- IP INTEGRATOR
 - Create Block Design
 - Open Block Design
 - Generate Block Design
- SIMULATION
 - Run Simulation
- RTL ANALYSIS
 - Run Linter
 - Open Elaborated Design
 - Report Methodology
 - Report DRC
 - Report Noise
 - Schematic

ELABORATED DESIGN - xc7a35tcpg236-1

Sources

Netlist

Source File Properties

Project Summary x Schematic x 1to4_1to2.v x

C:/Users/raghava guptha/1to4_1to2/1to4_1to2.srscs/sources_1/new/1to4_1to2.v

```
1 module demux_2tol(i, s, o);
2     input i, s;
3     output reg [1:0] o;
4
5     always @(*)
6     begin
7         case(s)
8             1'b0: o = {1'b0, i};
9             1'b1: o = {i, 1'b0};
10        endcase
11    end
12 endmodule
13
14 module demux1to4_2tol(i, s, o);
15     input i;
16     input [1:0] s;
17     output [3:0] o;
18     wire [1:0] w;
19
20     demux_2tol d1(i, s[1], w);
21     demux_2tol d2(w[0], s[0], o[1:0]);
22     demux_2tol d3(w[1], s[0], o[3:2]);
23 endmodule
```

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