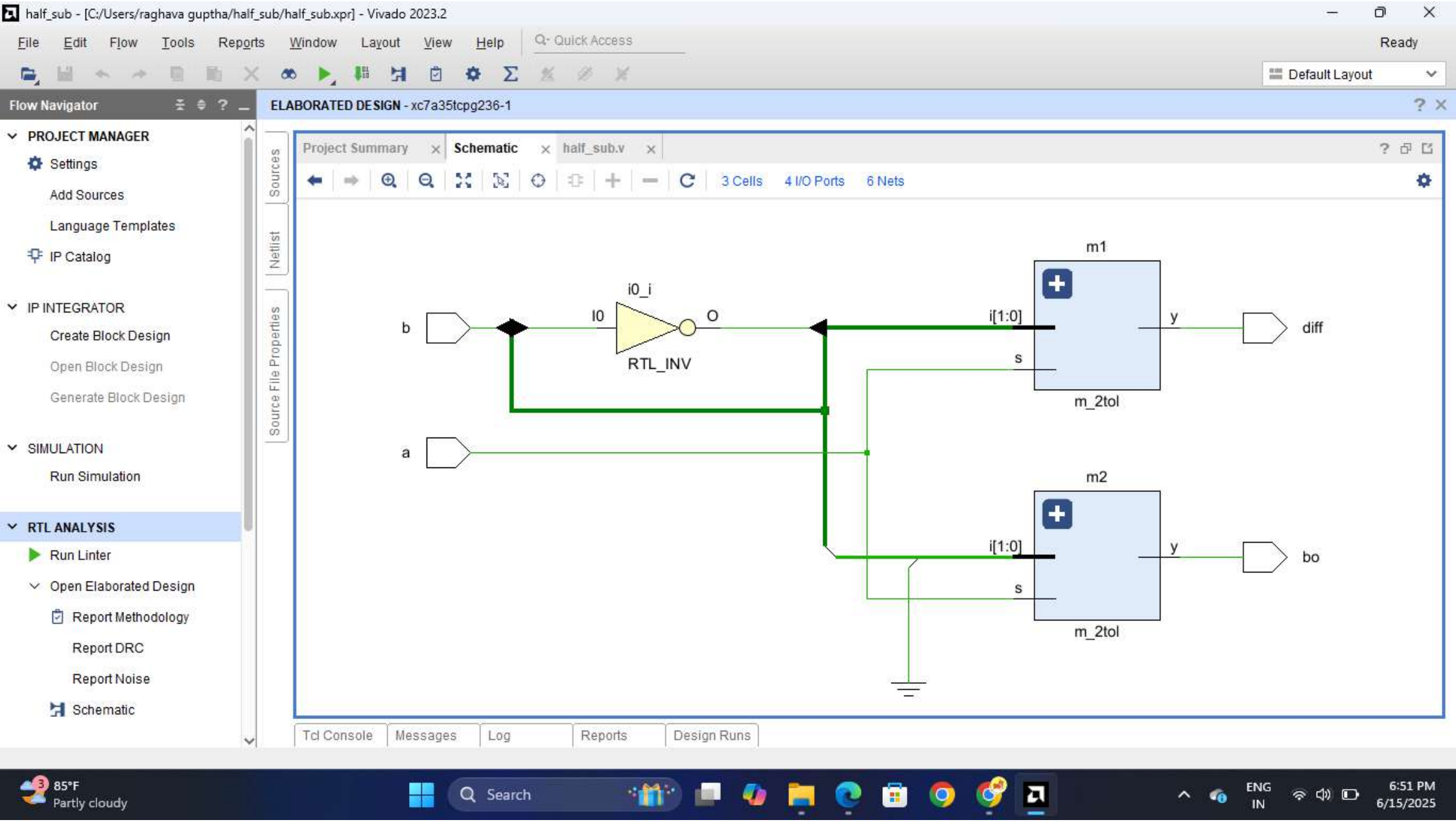

0.000 ns
Name
Value
a
0
b
0
diff
0
bo
0
0.000 ns
50.000 ns
100.000 ns
150.000 ns
200.000 ns
250.000 ns
300.000 ns
350.000 ns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3 Cells
4 I/O Ports
6 Nets
b
a
i0_i
I0
O
RTL_INV
m1
i[1:0]
s
y
diff
m_2tol
m2
i[1:0]
s
y
bo
m_2tol
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IN
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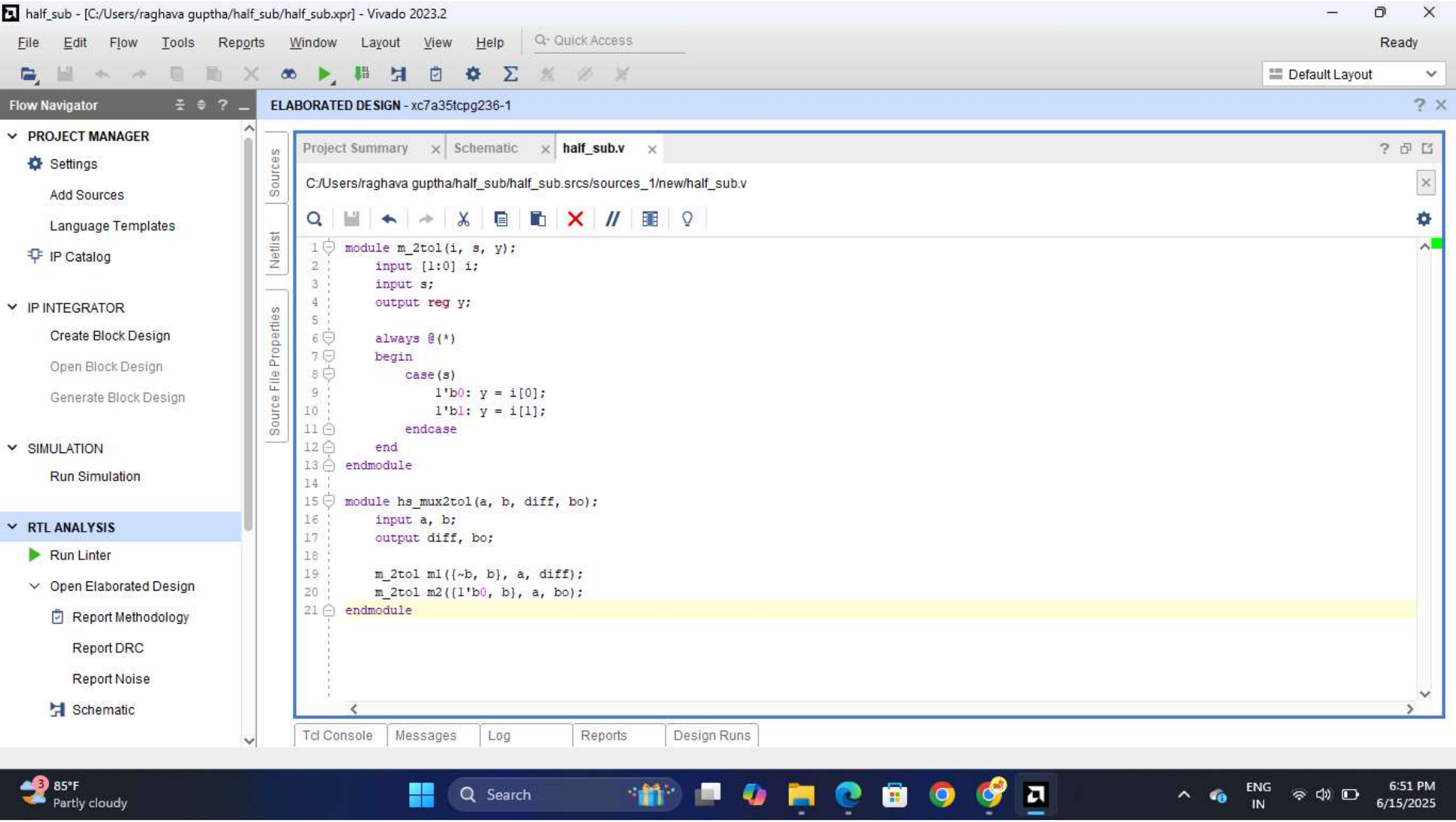
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C:/Users/raghava guptha/half_sub/half_sub.srcs/sources_1/new/half_sub.v
1 module m_2tol(i, s, y);
2 input [1:0] i;
3 input s;
4 output reg y;
5
6 always @(*)
7 begin
8 case(s)
9 1'b0: y = i[0];
10 1'b1: y = i[1];
11 endcase
12 end
13 endmodule
14
15 module hs_mux2tol(a, b, diff, bo);
16 input a, b;
17 output diff, bo;
18
19 m_2tol m1({~b, b}, a, diff);
20 m_2tol m2({1'b0, b}, a, bo);
21 endmodule
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85°F
Partly cloudy
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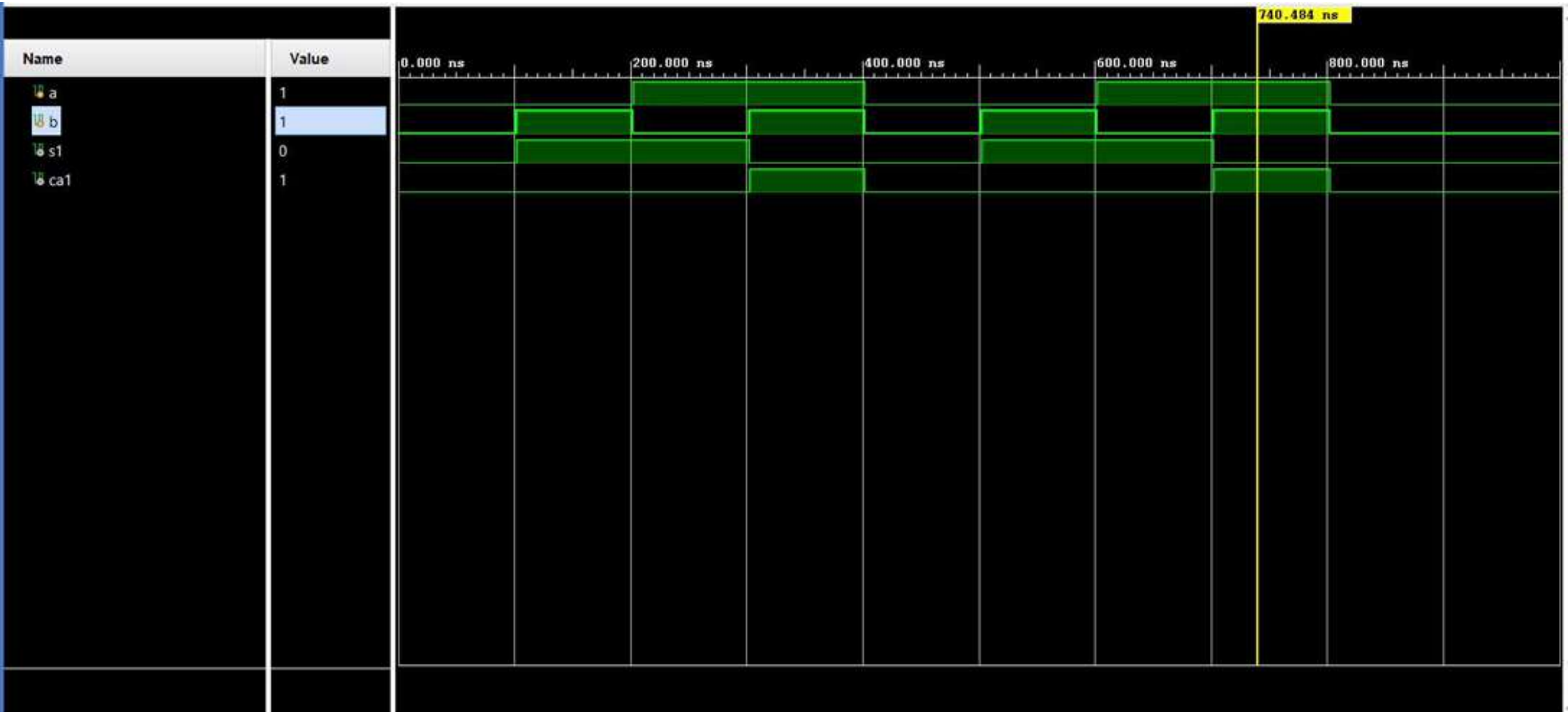
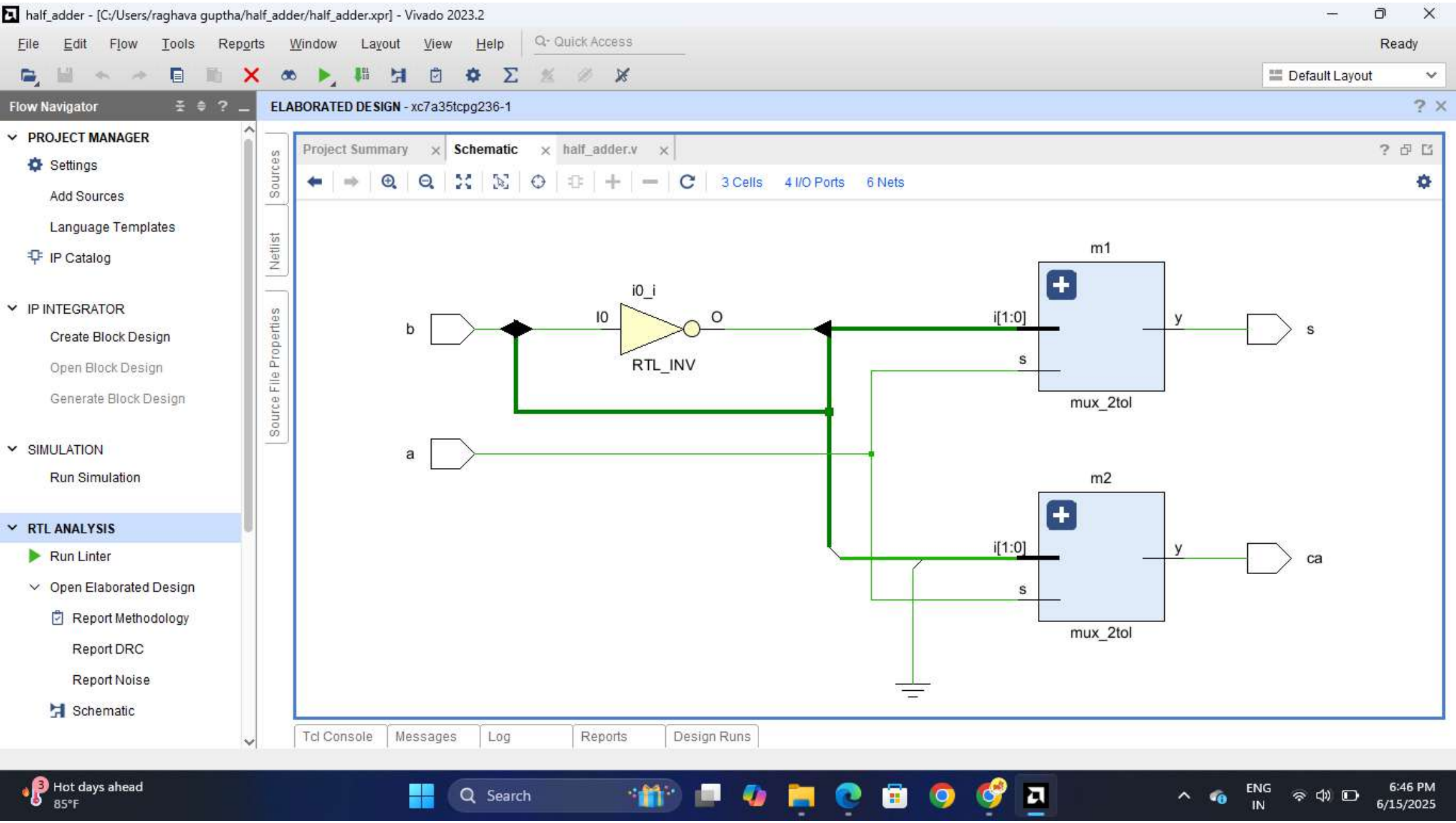

Name
Value
a
1
b
1
s1
0
ca1
1
0.000 ns
200.000 ns
400.000 ns
600.000 ns
740.484 ns
800.000 ns


half_adder - [C:/Users/raghava guptha/half_adder/half_adder.xpr] - Vivado 2023.2
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half_adder.v
3 Cells
4 I/O Ports
6 Nets
b
a
i0_i
I0
O
RTL_INV
m1
i[1:0]
s
y
mux_2tol
s
m2
i[1:0]
s
y
mux_2tol
ca
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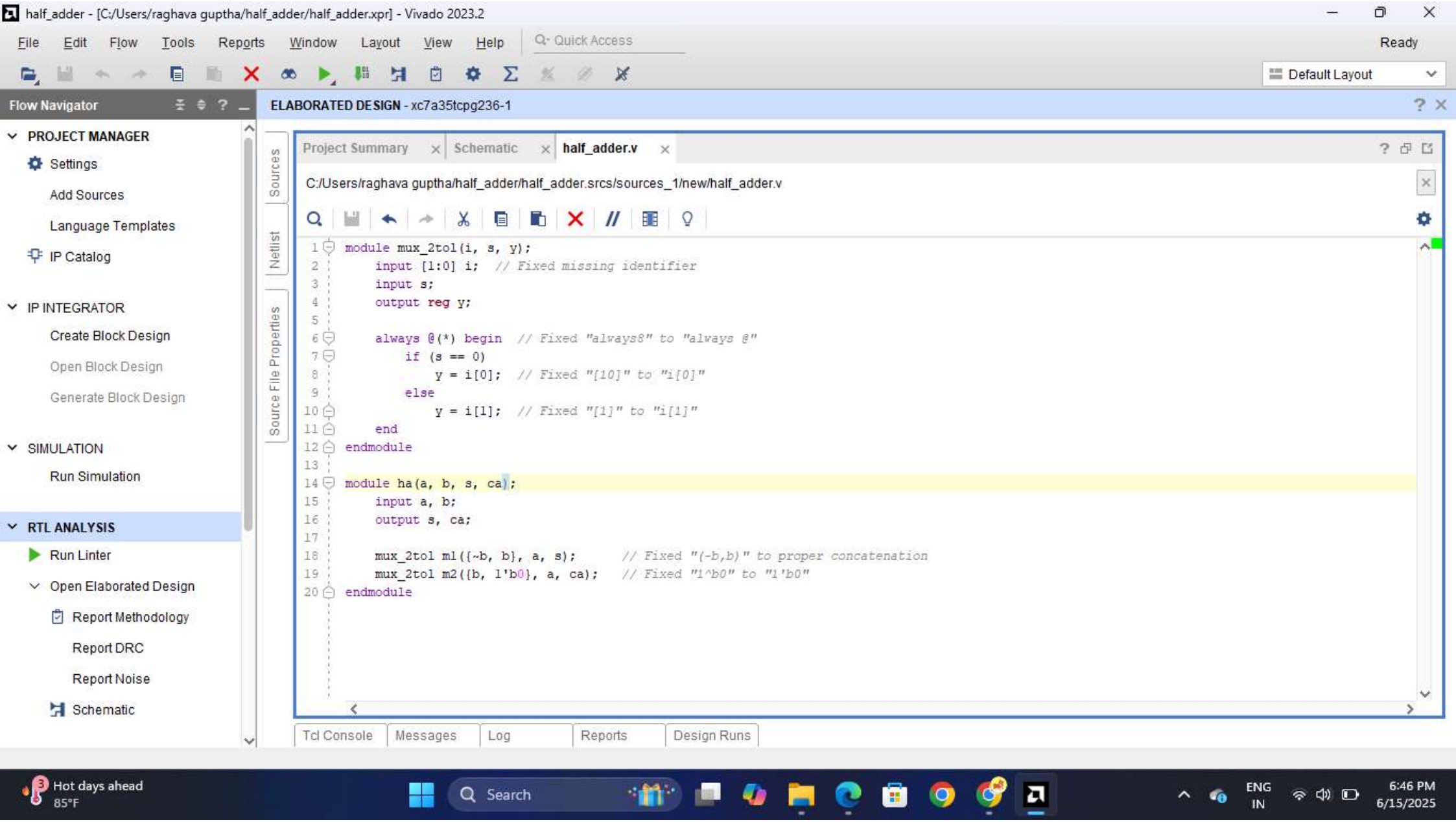
half_adder - [C:/Users/raghava guptha/half_adder/half_adder.xpr] - Vivado 2023.2
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half_adder.v
C:/Users/raghava guptha/half_adder/half_adder.srcs/sources_1/new/half_adder.v
1 module mux_2tol(i, s, y);
2 input [1:0] i; // Fixed missing identifier
3 input s;
4 output reg y;
5
6 always @(*) begin // Fixed "always8" to "always @"
7 if (s == 0)
8 y = i[0]; // Fixed "[10]" to "i[0]"
9 else
10 y = i[1]; // Fixed "[1]" to "i[1]"
11 end
12 endmodule
13
14 module ha(a, b, s, ca);
15 input a, b;
16 output s, ca;
17
18 mux_2tol m1({~b, b}, a, s); // Fixed "(-b,b)" to proper concatenation
19 mux_2tol m2({b, 1'b0}, a, ca); // Fixed "1^b0" to "1'b0"
20 endmodule
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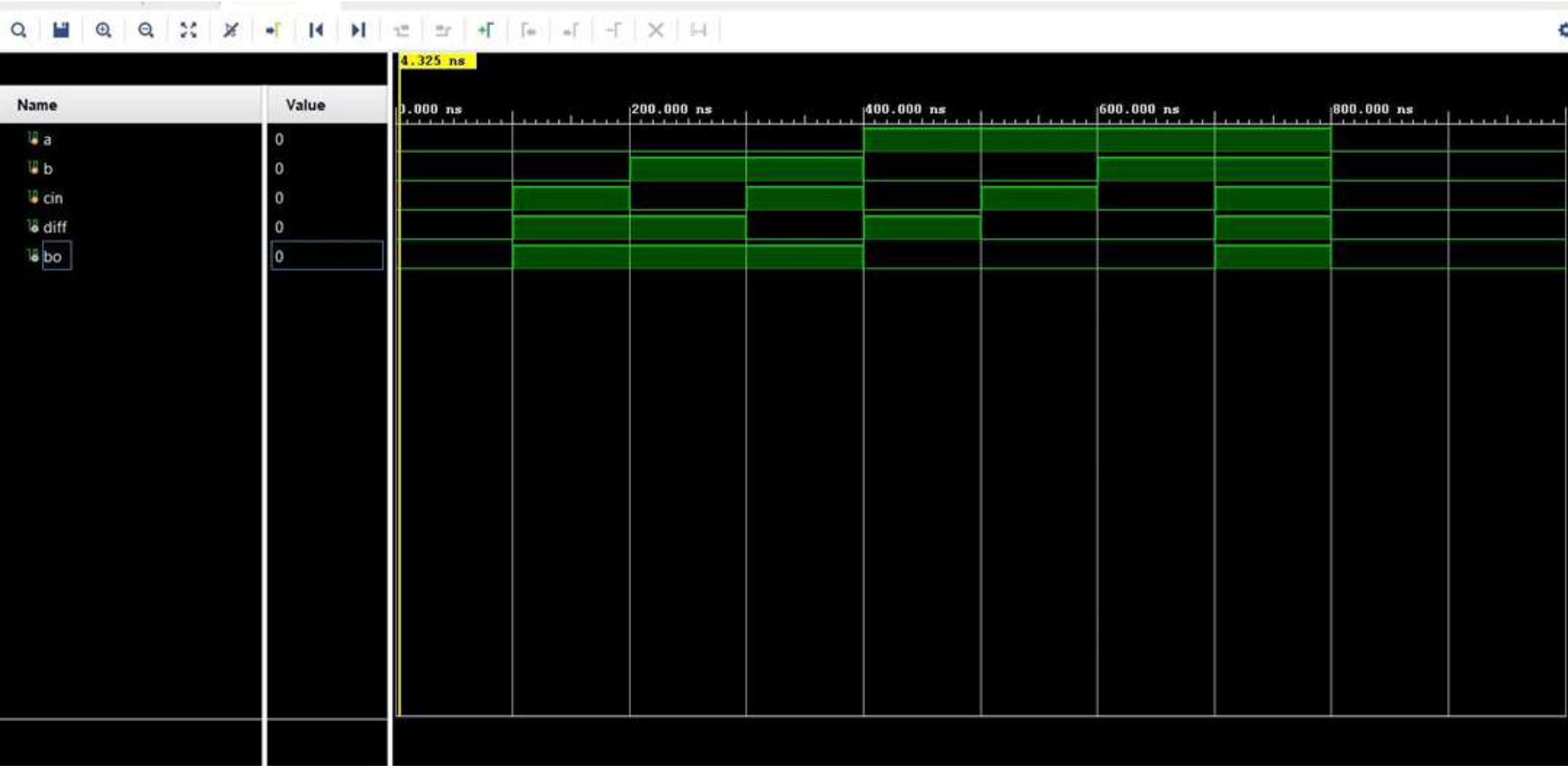
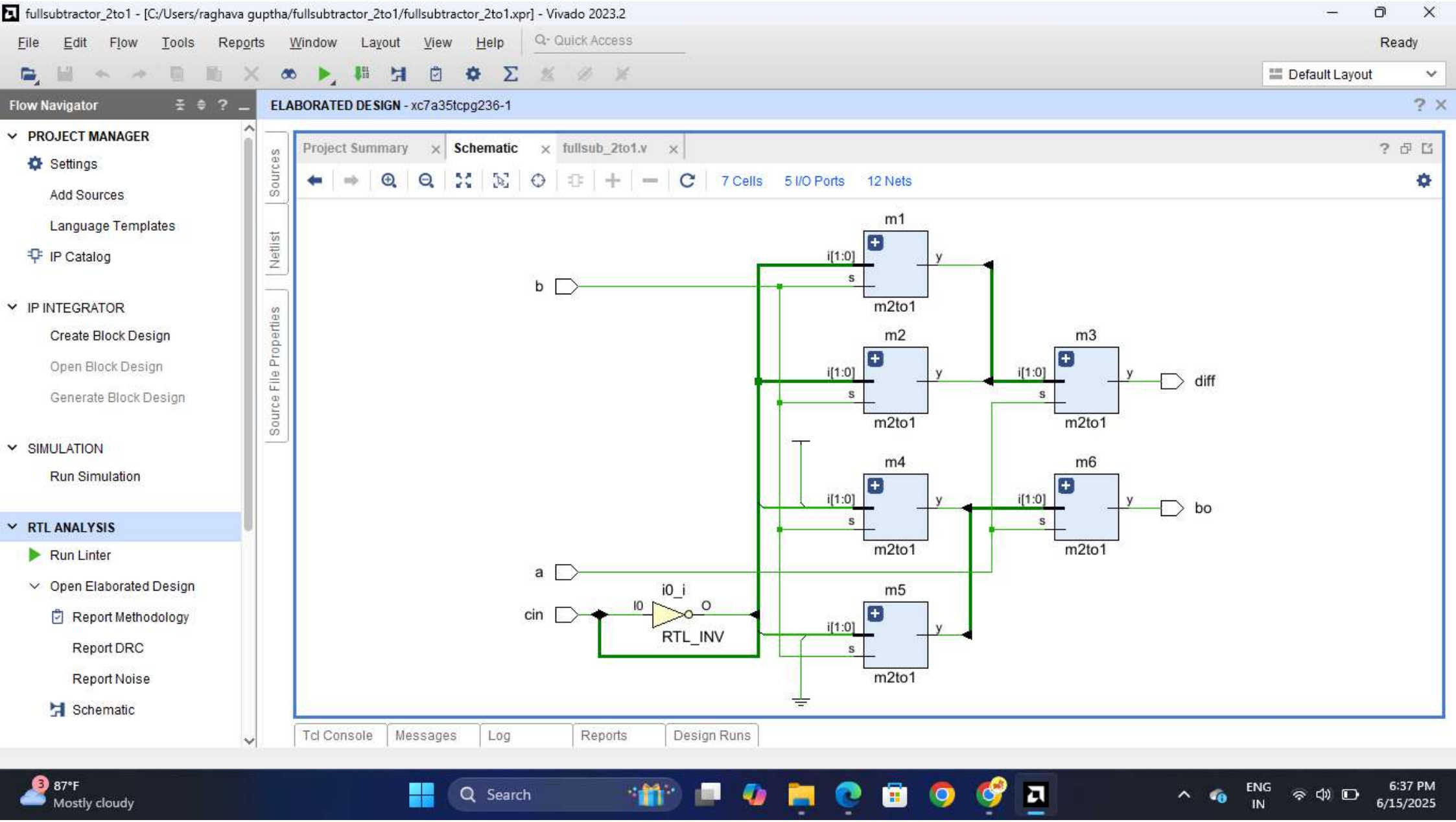

4.325 ns
Name
Value
a
0
b
0
cin
0
diff
0
bo
0
0.000 ns
200.000 ns
400.000 ns
600.000 ns
800.000 ns


fullsubtractor_2to1 - [C:/Users/raghava guptha/fullsubtractor_2to1/fullsubtractor_2to1.xpr] - Vivado 2023.2
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fullsub_2to1.v
7 Cells
5 I/O Ports
12 Nets
m1
m2
m3
m4
m5
m6
m2to1
i[1:0]
s
y
b
a
cin
diff
bo
i0_i
I0
O
RTL_INV
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Mostly cloudy
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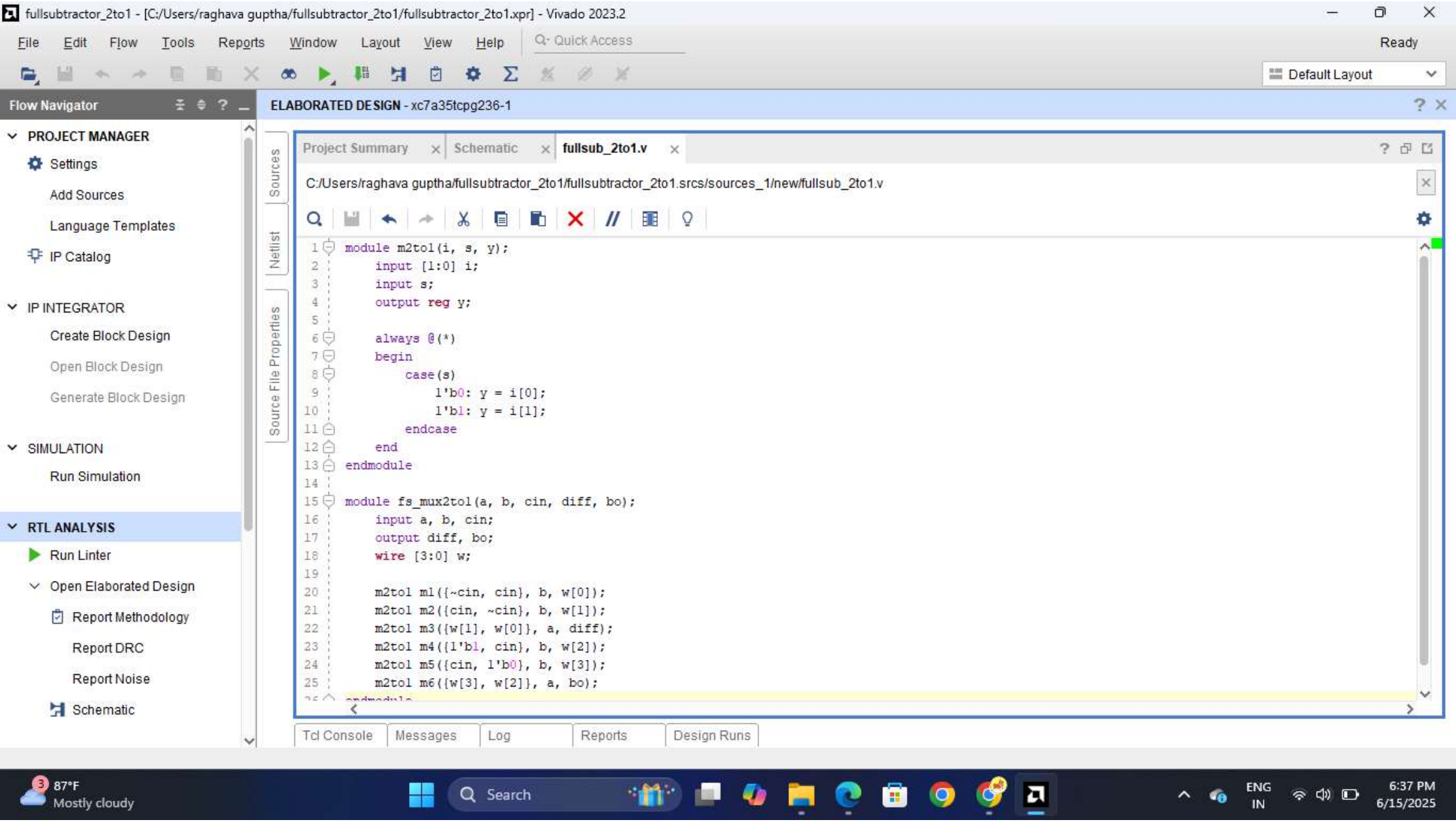
fullsubtractor_2to1 - [C:/Users/raghava guptha/fullsubtractor_2to1/fullsubtractor_2to1.xpr] - Vivado 2023.2
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1 module m2to1(i, s, y);
2 input [1:0] i;
3 input s;
4 output reg y;
5
6 always @(*)
7 begin
8 case(s)
9 1'b0: y = i[0];
10 1'b1: y = i[1];
11 endcase
12 end
13 endmodule
14
15 module fs_mux2to1(a, b, cin, diff, bo);
16 input a, b, cin;
17 output diff, bo;
18 wire [3:0] w;
19
20 m2to1 m1({~cin, cin}, b, w[0]);
21 m2to1 m2({cin, ~cin}, b, w[1]);
22 m2to1 m3({w[1], w[0]}, a, diff);
23 m2to1 m4({1'b1, cin}, b, w[2]);
24 m2to1 m5({cin, 1'b0}, b, w[3]);
25 m2to1 m6({w[3], w[2]}, a, bo);
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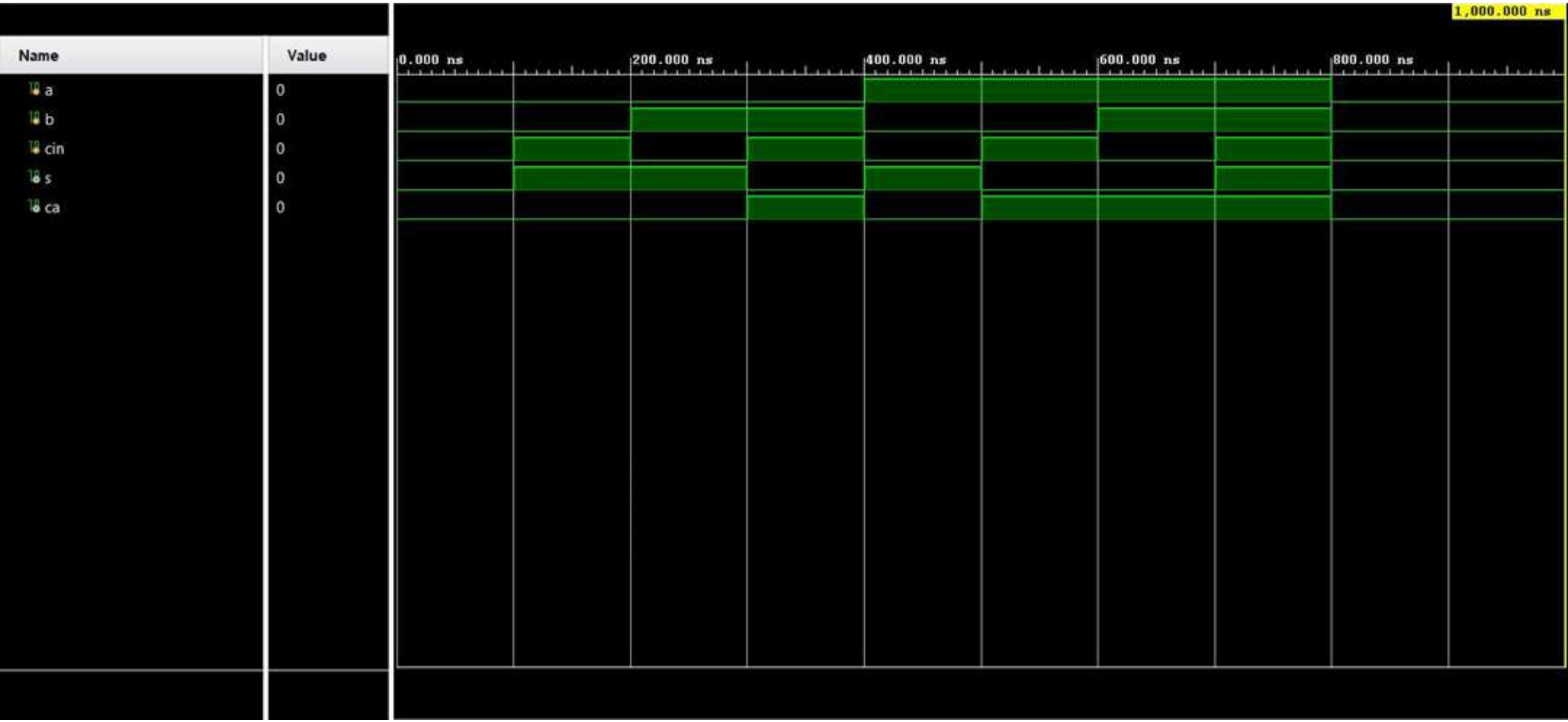
Name
Value
a
0
b
0
cin
0
s
0
ca
0
0.000 ns
200.000 ns
400.000 ns
600.000 ns
800.000 ns
1,000.000 ns

fulladder_2to1 - [C:/Users/raghava guptha/fulladder_2to1/fulladder_2to1.xpr] - Vivado 2023.2

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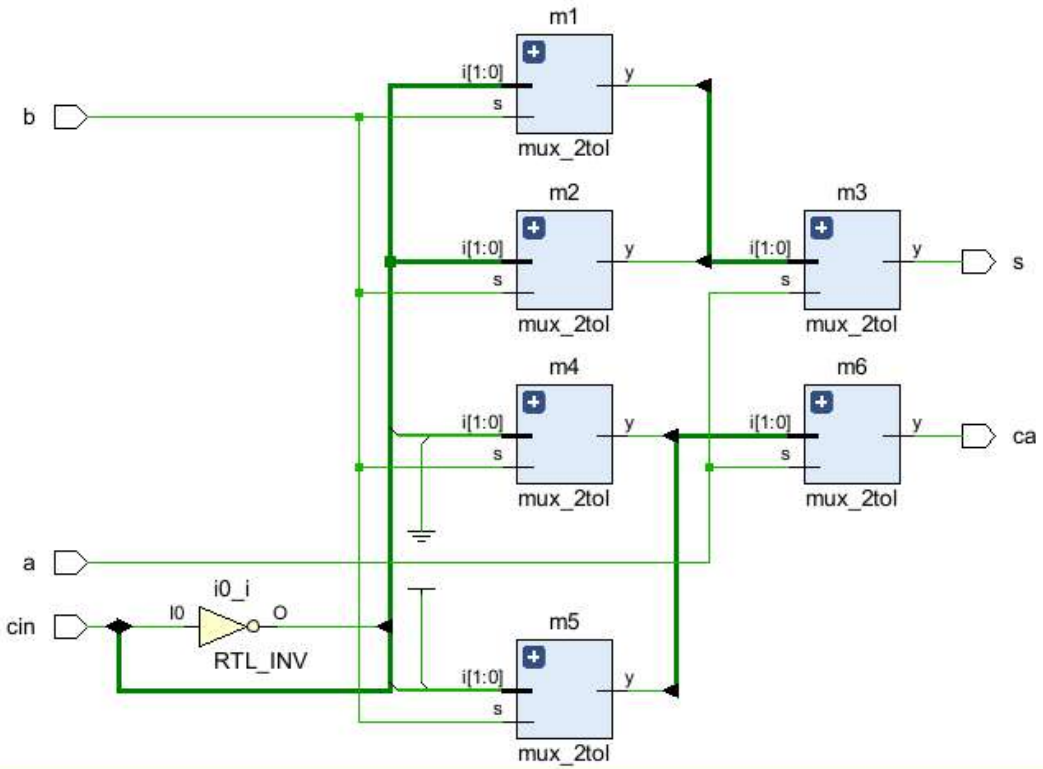
7 Cells 5 I/O Ports 12 Nets



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87°F Mostly cloudy

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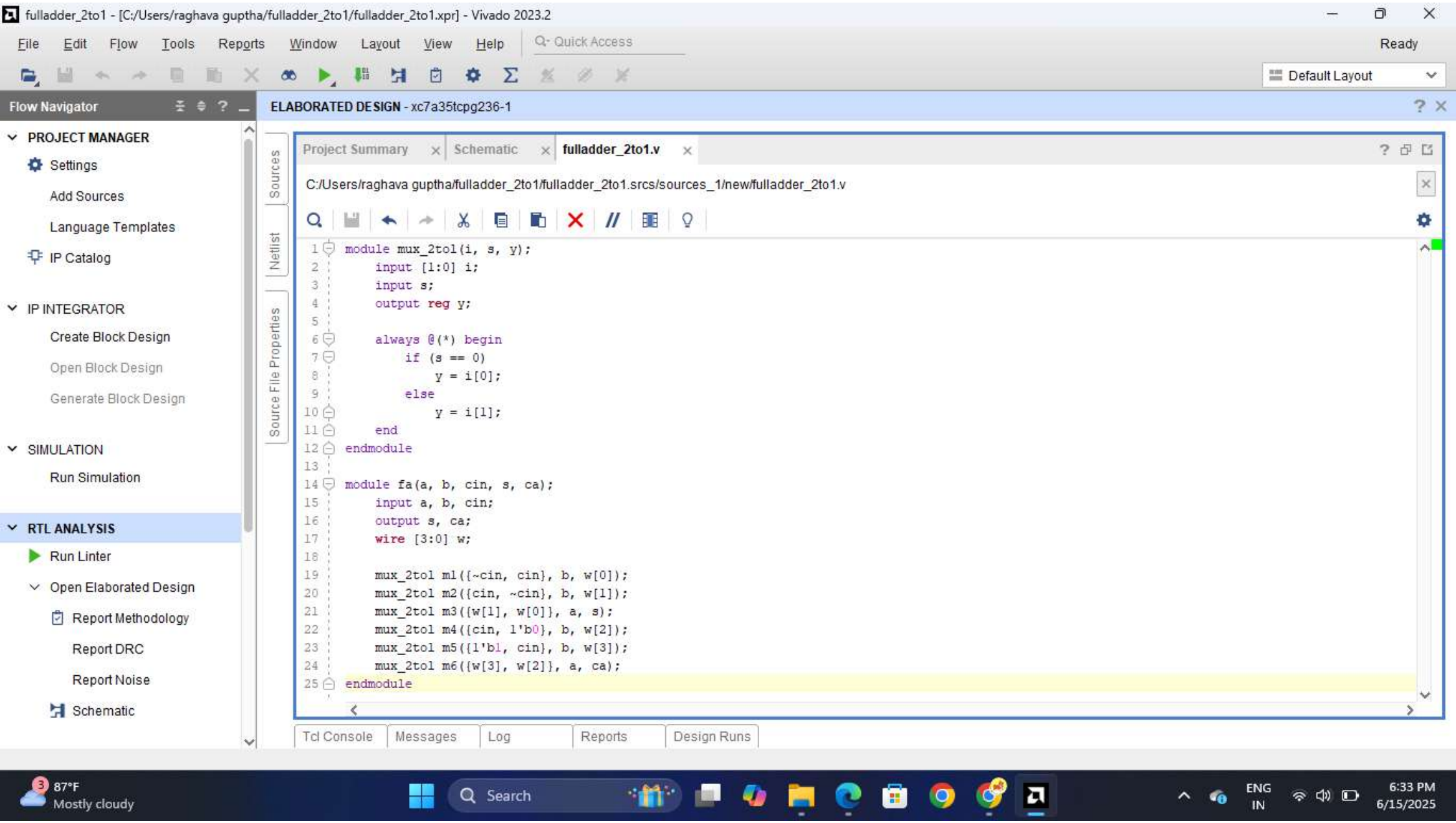
fulladder_2to1 - [C:/Users/raghava guptha/fulladder_2to1/fulladder_2to1.xpr] - Vivado 2023.2
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1 module mux_2to1(i, s, y);
2 input [1:0] i;
3 input s;
4 output reg y;
5
6 always @(*) begin
7 if (s == 0)
8 y = i[0];
9 else
10 y = i[1];
11 end
12 endmodule
13
14 module fa(a, b, cin, s, ca);
15 input a, b, cin;
16 output s, ca;
17 wire [3:0] w;
18
19 mux_2to1 m1({~cin, cin}, b, w[0]);
20 mux_2to1 m2({cin, ~cin}, b, w[1]);
21 mux_2to1 m3({w[1], w[0]}, a, s);
22 mux_2to1 m4({cin, 1'b0}, b, w[2]);
23 mux_2to1 m5({1'b1, cin}, b, w[3]);
24 mux_2to1 m6({w[3], w[2]}, a, ca);
25 endmodule
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