



2to4dec\_2to1mux - [C:/Users/raghava guptha/2to4dec\_2to1mux/2to4dec\_2to1mux.xpr] - Vivado 2023.2

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5 Cells 6 I/O Ports 8 Nets

The schematic diagram shows a 2-to-4 decoder and a 2-to-1 multiplexer circuit. The input  $i[1:0]$  is connected to an RTL\_INV block, which outputs  $i0_i$ . The input  $i[1:0]$  is also connected to the 's' (select) input of four m2to1 multiplexer blocks (m1, m2, m3, m4). The outputs 'y' of these multiplexers are connected to the output  $o[3:0]$ .

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```
1 module m2to1(i, s, y);
2     input [1:0] i;
3     input s;
4     output reg y;
5
6     always @(*)
7     begin
8         case(s)
9             1'b0: y = i[0];
10            1'b1: y = i[1];
11        endcase
12    end
13 endmodule
14
15 module dec2to4_m2to1(i, o);
16     input [1:0] i;
17     output [3:0] o;
18
19     m2to1 m1({1'b0, ~i[0]}, i[1], o[0]);
20     m2to1 m2({1'b0, i[0]}, i[1], o[1]);
21     m2to1 m3({~i[0], 1'b0}, i[1], o[2]);
22     m2to1 m4({i[0], 1'b0}, i[1], o[3]);
23 endmodule
```

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