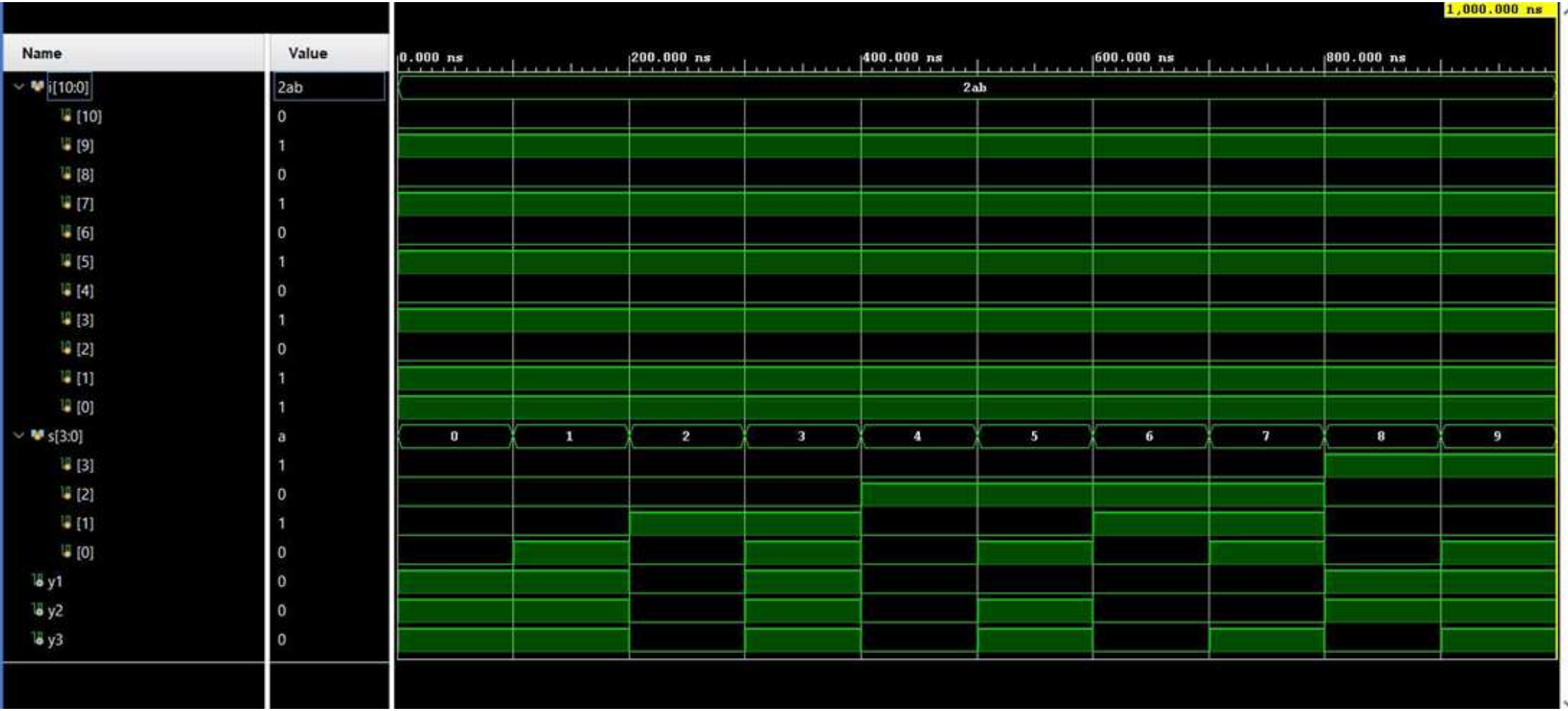
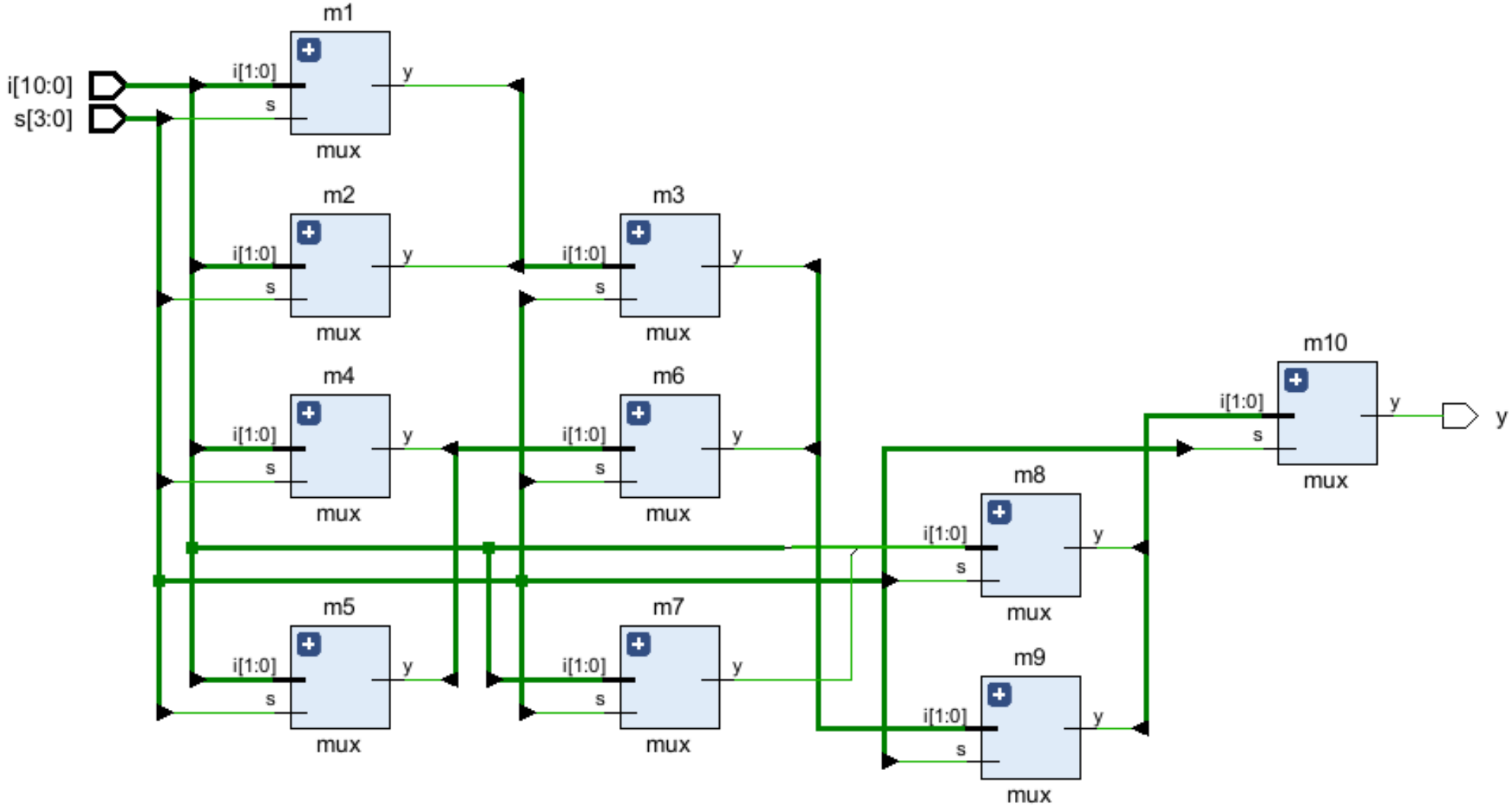

Name
Value
i[10:0]
2ab
[10]
0
[9]
1
[8]
0
[7]
1
[6]
0
[5]
1
[4]
0
[3]
1
[2]
0
[1]
1
[0]
1
s[3:0]
a
[3]
1
[2]
0
[1]
1
[0]
0
y1
0
y2
0
y3
0
0.000 ns
200.000 ns
400.000 ns
600.000 ns
800.000 ns
1,000.000 ns
2ab
0
1
2
3
4
5
6
7
8
9


i[10:0]
s[3:0]
m1
i[1:0]
s
y
mux
m2
m3
m4
m6
m5
m7
m8
m9
m10
y

muxs - [C:/Users/raghava guptha/muxs/muxs.xpr] - Vivado 2023.2

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C:/Users/raghava guptha/muxs/muxs.srcs/sources_1/new/muxs.v

```
1  module mux(i, s, y);  // 2-to-1 MUX
2      input [1:0] i;
3      input s;
4      output reg y;
5   always @(*) begin
6          case (s)
7              0: y = i[0];
8              1: y = i[1];
9          endcase
10     end
11 endmodule
12 module mux_5tol(i, s, y);  // 5-to-1 MUX using mux...
23 module mux_7tol(i, s, y);  // 7-to-1 MUX using mux
24     input [6:0] i;
25     input [2:0] s;
26     output y;
27     wire [4:0] w;
28     mux m1(i[1:0], s[0], w[0]);
29     mux m2(i[3:2], s[0], w[1]);
30     mux m3(i[5:4], s[0], w[2]);
31     mux m4({i[6], w[0]}, s[0], w[3]);
32     mux m5({w[1], w[2]}, s[1], w[4]);
33     mux m6({w[3], w[4]}, s[2], y);
34 endmodule
35 module mux_11tol(i, s, y);  // 11-to-1 MUX using mux
```

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52:1 Insert Verilog

87°F Mostly cloudy

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6:24 PM 6/15/2025

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C:/Users/raghava guptha/muxs/muxs.srcs/sources_1/new/muxs.v

```
29      mux m2(i[3:2], s[0], w[1]);
30      mux m3(i[5:4], s[0], w[2]);
31      mux m4({i[6], w[0]}, s[0], w[3]);
32      mux m5({w[1], w[2]}, s[1], w[4]);
33      mux m6({w[3], w[4]}, s[2], y);
34  endmodule
35  module mux_11tol(i, s, y);  // 11-to-1 MUX using mux
36      input [10:0] i;
37      input [3:0] s;
38      output y;
39      wire [8:0] w;
40      mux m1(i[1:0], s[0], w[0]);
41      mux m2(i[3:2], s[0], w[1]);
42      mux m3({w[0], w[1]}, s[1], w[5]);
43      mux m4(i[5:4], s[0], w[2]);
44      mux m5(i[7:6], s[0], w[3]);
45      mux m6({w[2], w[3]}, s[1], w[6]);
46
47      mux m7(i[9:8], s[0], w[4]);
48      mux m8({w[4], i[10]}, s[1], w[7]);
49
50      mux m9({w[5], w[6]}, s[2], w[8]);
51      mux m10({w[8], w[7]}, s[3], y);
52  endmodule
53
```

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52:1 Insert Verilog