



half\_sub - [C:/Users/raghava guptha/half\_sub/half\_sub.xpr] - Vivado 2023.2

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ELABORATED DESIGN - xc7a35tcbg236-1

Project Summary x Schematic x half\_sub.v x

3 Cells 4 I/O Ports 6 Nets

The schematic diagram shows a half-subtractor circuit. It consists of two 2-to-1 multiplexers, m1 and m2, and an RTL\_INV block. Input 'b' is connected to a multiplexer (black diamond) and the 'i0' input of the RTL\_INV block. The output of the multiplexer is connected to the 'i0' input of the RTL\_INV block. The output of the RTL\_INV block is connected to the 'i[1:0]' input of both m1 and m2. The 's' input of both m1 and m2 is connected to the output of the RTL\_INV block. The 'y' output of m1 is connected to the 'diff' output, and the 'y' output of m2 is connected to the 'bo' output. A ground symbol is connected to the 's' input of m2.

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Project Summary xSchematic xhalf\_sub.v x

C:/Users/raghava guptha/half\_sub/half\_sub.srsrcs/sources\_1/new/half\_sub.v

Q

1 module m\_2tol(i, s, y);

2 input [1:0] i;

3 input s;

4 output reg y;

5

6 always @(\*)

7 begin

8 case(s)

9 1'b0: y = i[0];

10 1'b1: y = i[1];

11 endcase

12 end

13 endmodule

14

15 module hs\_mux2tol(a, b, diff, bo);

16 input a, b;

17 output diff, bo;

18

19 m\_2tol m1({~b, b}, a, diff);

20 m\_2tol m2({1'b0, b}, a, bo);

21 endmodule

Tcl ConsoleMessagesLogReportsDesign Runs

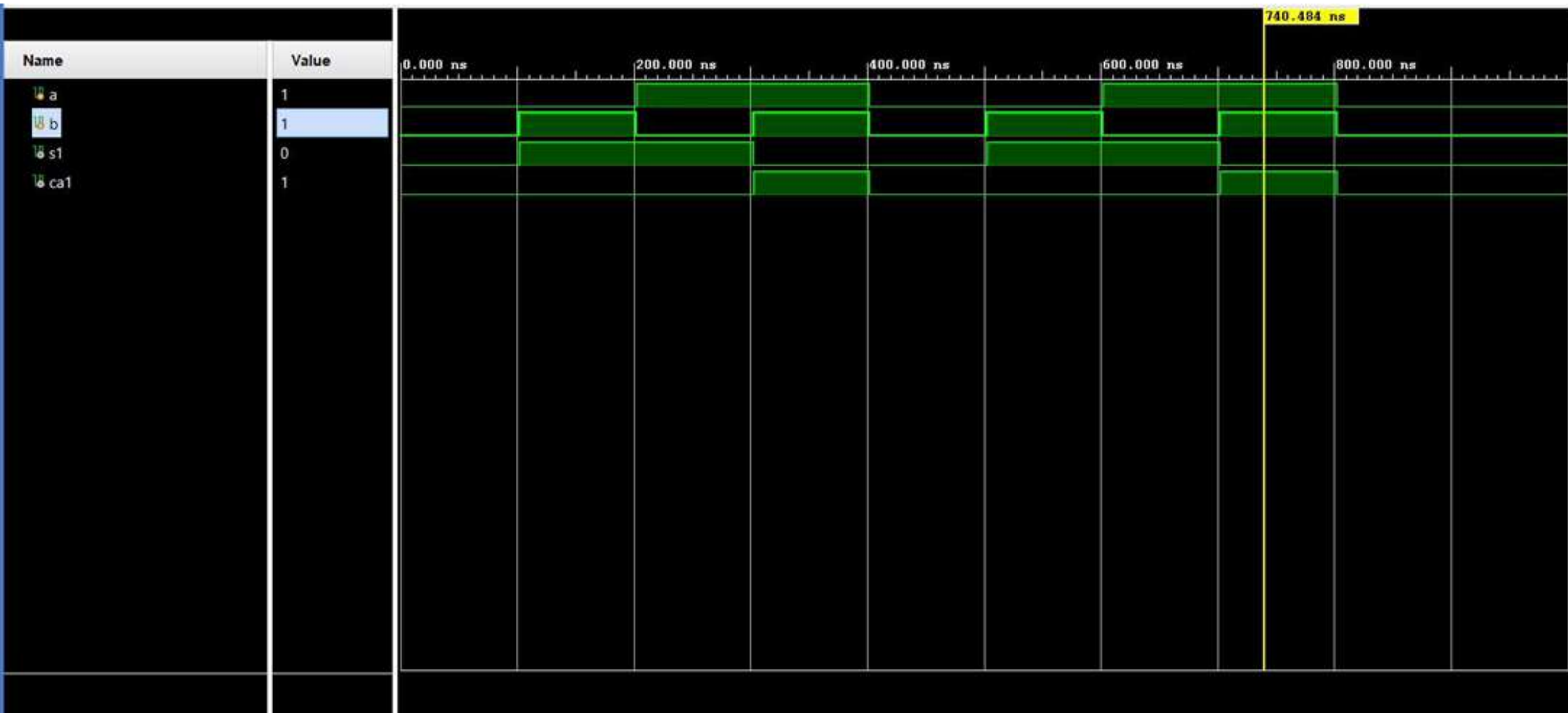
85°F

Partly cloudy

Search

6:51 PM

6/15/2025



half\_adder - [C:/Users/raghava guptha/half\_adder/half\_adder.xpr] - Vivado 2023.2

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Project Summary x Schematic x half\_adder.v x

3 Cells 4 I/O Ports 6 Nets

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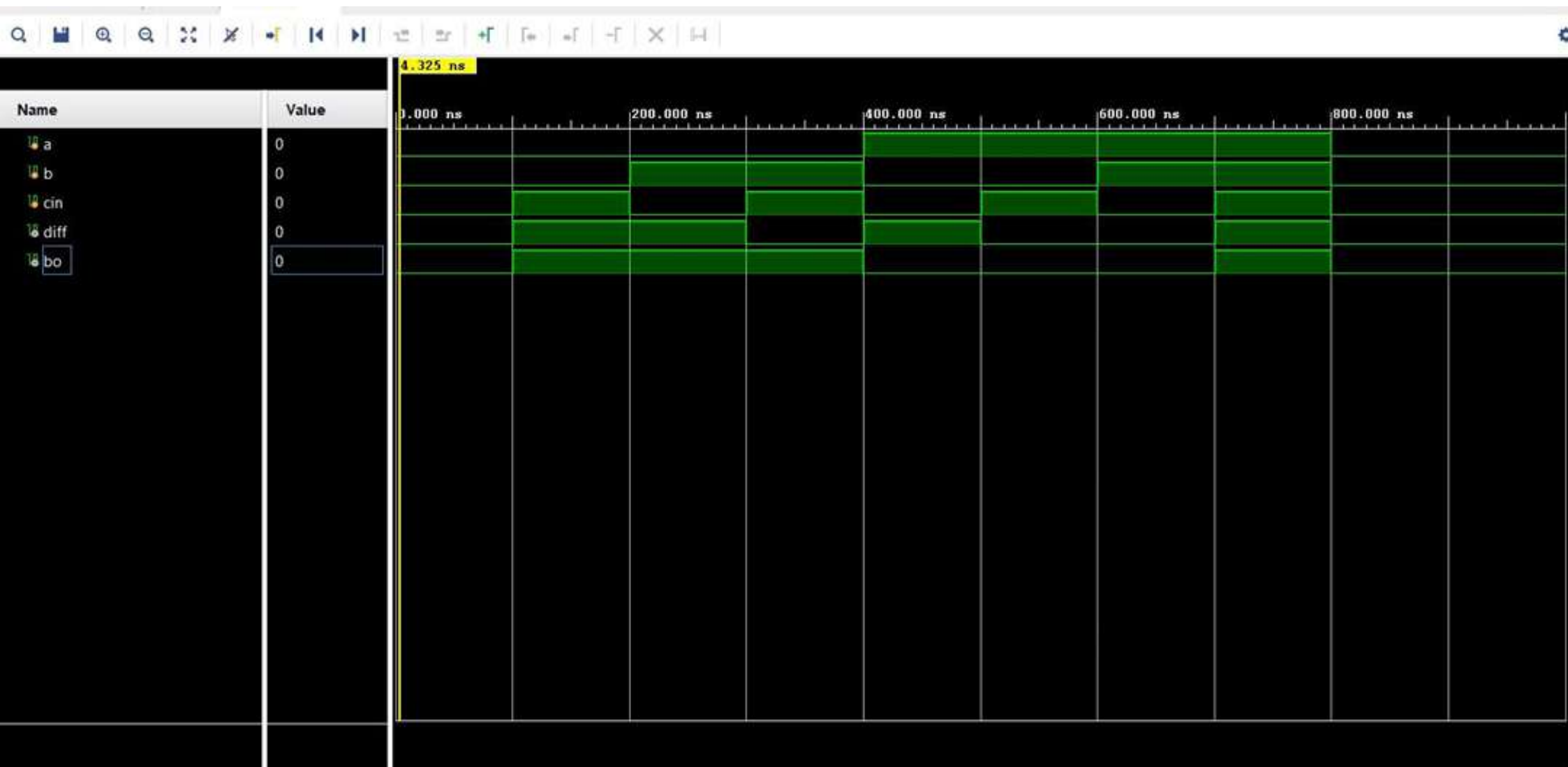
Source File Properties

Project Summary x Schematic x half\_adder.v x

C:/Users/raghava guptha/half\_adder/half\_adder.srscs/sources\_1/new/half\_adder.v

```
1 module mux_2to1(i, s, y);
2     input [1:0] i; // Fixed missing identifier
3     input s;
4     output reg y;
5
6     always @(*) begin // Fixed "always8" to "always @"
7         if (s == 0)
8             y = i[0]; // Fixed "[10]" to "i[0]"
9         else
10            y = i[1]; // Fixed "[1]" to "i[1]"
11        end
12    endmodule
13
14 module ha(a, b, s, ca);
15     input a, b;
16     output s, ca;
17
18     mux_2to1 m1({~b, b}, a, s); // Fixed "(-b,b)" to proper concatenation
19     mux_2to1 m2({b, 1'b0}, a, ca); // Fixed "1^b0" to "1'b0"
20 endmodule
```

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fullsubtractor\_2to1 - [C:/Users/raghava guptha/fullsubtractor\_2to1/fullsubtractor\_2to1.xpr] - Vivado 2023.2

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7 Cells 5 I/O Ports 12 Nets

The schematic diagram illustrates a 2-bit full subtractor implemented using five 2-to-1 multiplexers (m1 to m5). The inputs are 'a' (2-bit), 'b' (2-bit), and 'cin' (1-bit). The circuit uses an RTL\_INV block to invert 'cin'. The outputs are 'diff' (2-bit) and 'bo' (1-bit). The multiplexers are configured as follows:

- m1: i[1:0] = b, s = cin, y = diff[1:0]
- m2: i[1:0] = b, s = cin, y = diff[1:0]
- m3: i[1:0] = b, s = cin, y = diff[1:0]
- m4: i[1:0] = b, s = cin, y = diff[1:0]
- m5: i[1:0] = b, s = cin, y = diff[1:0]

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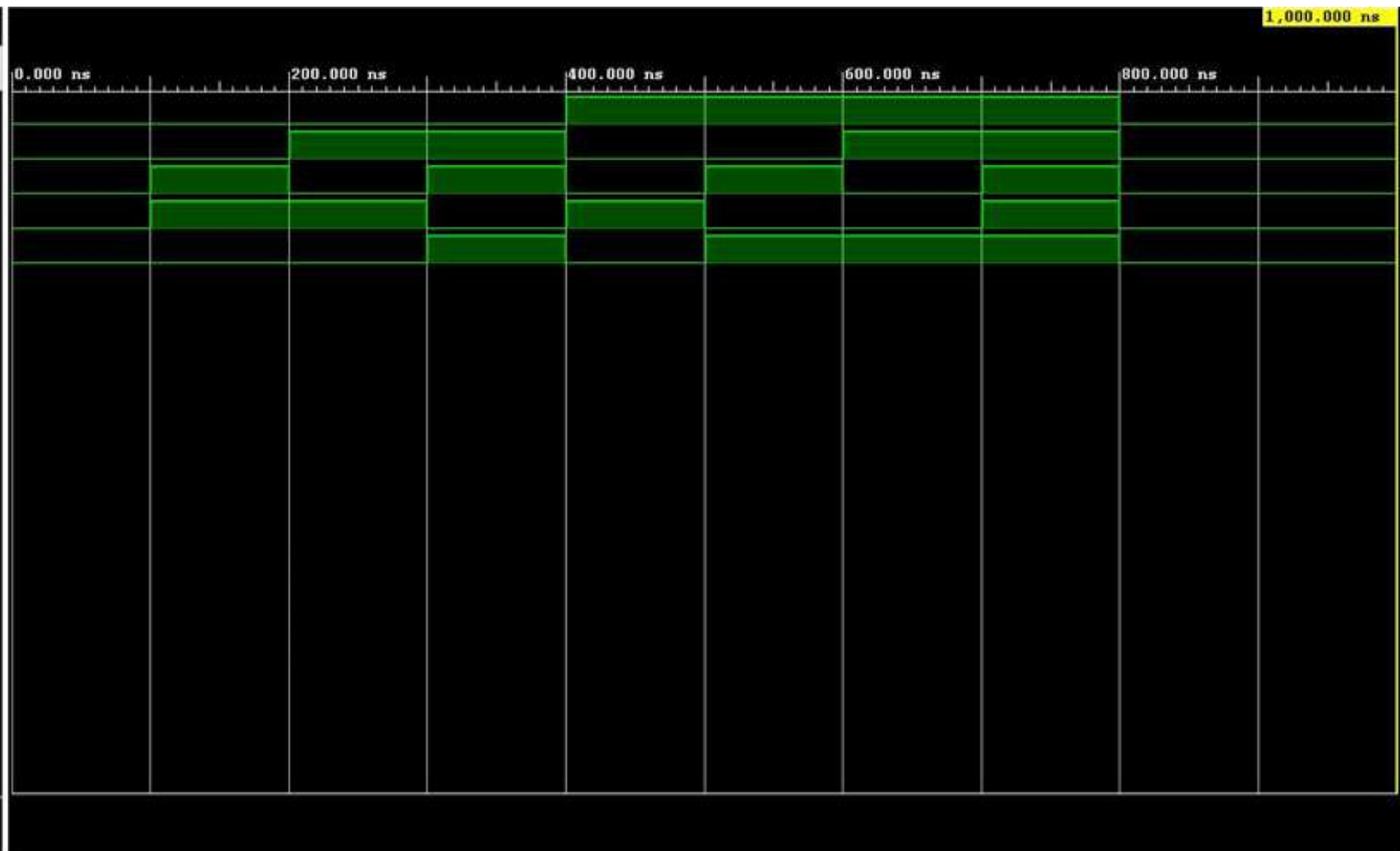
Project Summary x Schematic x fullsub\_2to1.v x

C:/Users/raghava guptha/fullsubtractor\_2to1/fullsubtractor\_2to1.srcs/sources\_1/new/fullsub\_2to1.v

```
1 module m2to1(i, s, y);
2     input [1:0] i;
3     input s;
4     output reg y;
5
6     always @(*)
7     begin
8         case(s)
9             1'b0: y = i[0];
10            1'b1: y = i[1];
11        endcase
12    end
13 endmodule
14
15 module fs_mux2to1(a, b, cin, diff, bo);
16     input a, b, cin;
17     output diff, bo;
18     wire [3:0] w;
19
20     m2to1 m1({~cin, cin}, b, w[0]);
21     m2to1 m2({cin, ~cin}, b, w[1]);
22     m2to1 m3({w[1], w[0]}, a, diff);
23     m2to1 m4({1'b1, cin}, b, w[2]);
24     m2to1 m5({cin, 1'b0}, b, w[3]);
25     m2to1 m6({w[3], w[2]}, a, bo);
26 endmodule
```

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Name	Value
 a	0
 b	0
 cin	0
 s	0
 ca	0



ELABORATED DESIGN - xc7a35tcpg236-1

- Project Summary x Schematic x fulladder\_2to1.v x ? [ ]

- 
 7 Cells   5 I/O Ports   12 Nets

- ist 

- |     | mux    | 2tol   |
|-----|--------|--------|
| 1   | 0.0000 | 0.0000 |
| 2   | 0.0000 | 0.0000 |
| 3   | 0.0000 | 0.0000 |
| 4   | 0.0000 | 0.0000 |
| 5   | 0.0000 | 0.0000 |
| 6   | 0.0000 | 0.0000 |
| 7   | 0.0000 | 0.0000 |
| 8   | 0.0000 | 0.0000 |
| 9   | 0.0000 | 0.0000 |
| 10  | 0.0000 | 0.0000 |
| 11  | 0.0000 | 0.0000 |
| 12  | 0.0000 | 0.0000 |
| 13  | 0.0000 | 0.0000 |
| 14  | 0.0000 | 0.0000 |
| 15  | 0.0000 | 0.0000 |
| 16  | 0.0000 | 0.0000 |
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| 59  | 0.0000 | 0.0000 |
| 60  | 0.0000 | 0.0000 |
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| 65  | 0.0000 | 0.0000 |
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| 69  | 0.0000 | 0.0000 |
| 70  | 0.0000 | 0.0000 |
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| 74  | 0.0000 | 0.0000 |
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| 77  | 0.0000 | 0.0000 |
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| 90  | 0.0000 | 0.0000 |
| 91  | 0.0000 | 0.0000 |
| 92  | 0.0000 | 0.0000 |
| 93  | 0.0000 | 0.0000 |
| 94  | 0.0000 | 0.0000 |
| 95  | 0.0000 | 0.0000 |
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| 98  | 0.0000 | 0.0000 |
| 99  | 0.0000 | 0.0000 |
| 100 | 0.0000 | 0.0000 |

[illegible]

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C:/Users/raghava guptha/fulladder\_2to1/fulladder\_2to1.srcs/sources\_1/new/fulladder\_2to1.v

```
1 module mux_2to1(i, s, y);
2     input [1:0] i;
3     input s;
4     output reg y;
5
6     always @(*) begin
7         if (s == 0)
8             y = i[0];
9         else
10            y = i[1];
11        end
12    endmodule
13
14 module fa(a, b, cin, s, ca);
15     input a, b, cin;
16     output s, ca;
17     wire [3:0] w;
18
19     mux_2to1 m1({~cin, cin}, b, w[0]);
20     mux_2to1 m2({cin, ~cin}, b, w[1]);
21     mux_2to1 m3({w[1], w[0]}, a, s);
22     mux_2to1 m4({cin, 1'b0}, b, w[2]);
23     mux_2to1 m5({1'b1, cin}, b, w[3]);
24     mux_2to1 m6({w[3], w[2]}, a, ca);
25 endmodule
```

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