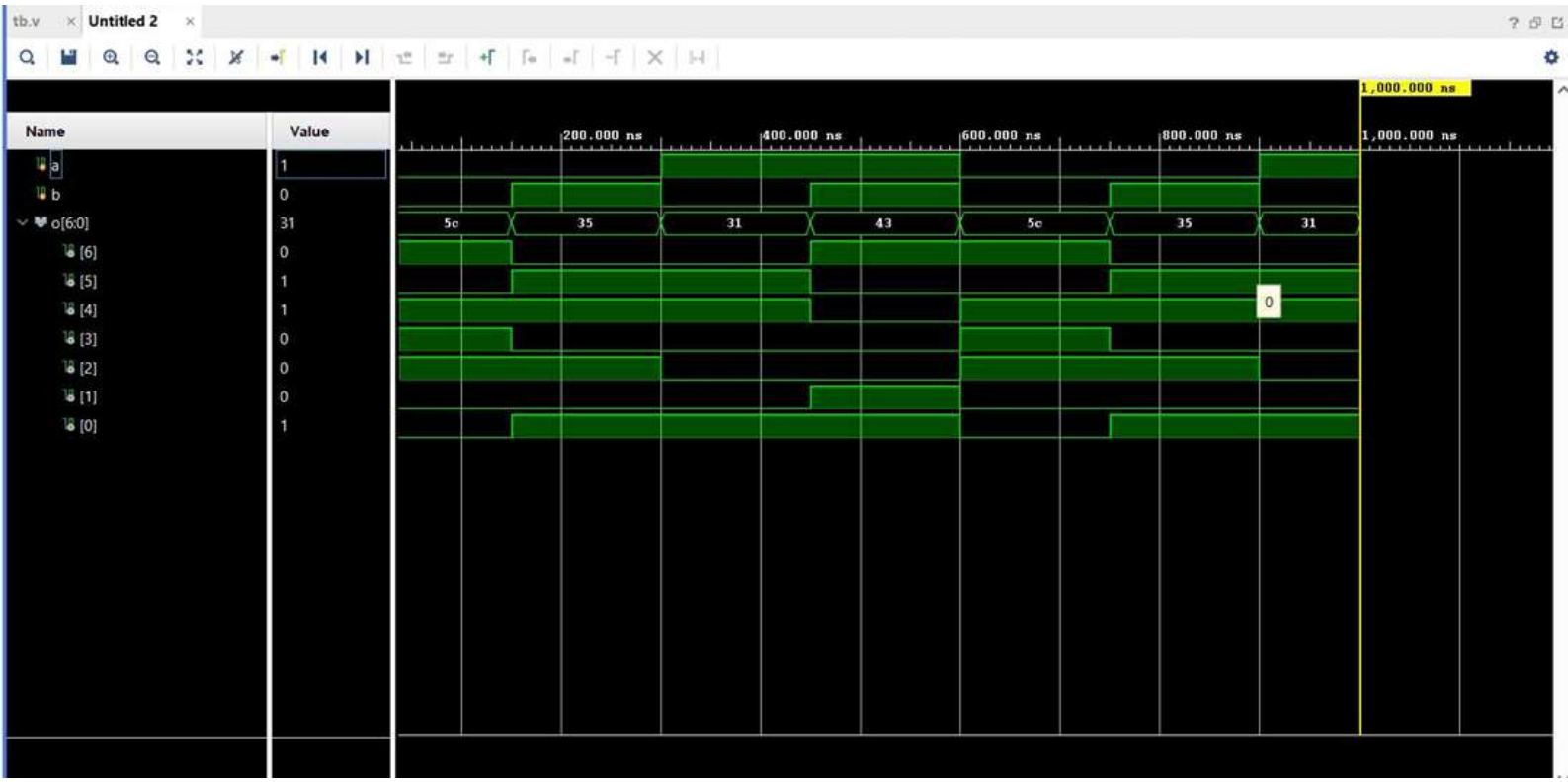
tb.v
Untitled 2
Name
Value
a
1
b
0
o[6:0]
31
[6]
0
[5]
1
[4]
1
[3]
0
[2]
0
[1]
0
[0]
1
200.000 ns
400.000 ns
600.000 ns
800.000 ns
1,000.000 ns
1,000.000 ns
5c
35
31
43
5c
35
31
0

program_for_logic_gates - [C:/Users/raghava guptha/program_for_logic_gates/program_for_logic_gates.xpr] - Vivado 2023.2

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Default Layout

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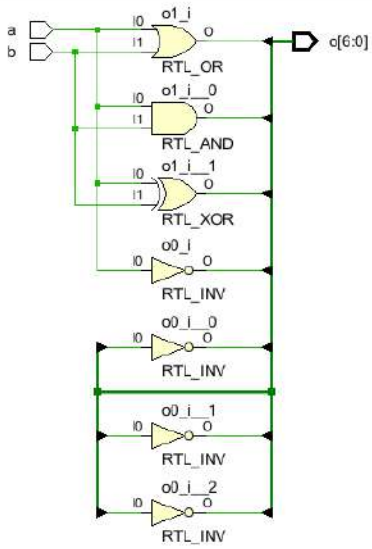
  - Create Block Design
  - Open Block Design
  - Generate Block Design
- SIMULATION
  - Run Simulation
- RTL ANALYSIS
  - Run Linter
  - Open Elaborated Design
    - Report Methodology
    - Report DRC
    - Report Noise
    - Schematic
- SYNTHESIS
  - Run Synthesis
  - Open Synthesized Design

ELABORATED DESIGN - xc7a35tcpg236-1

Sources | Netlist | Source File Properties

Project Summary | Schematic | logicgates.v | aligates_tb.v

7 Cells 9 I/O Ports 9 Nets



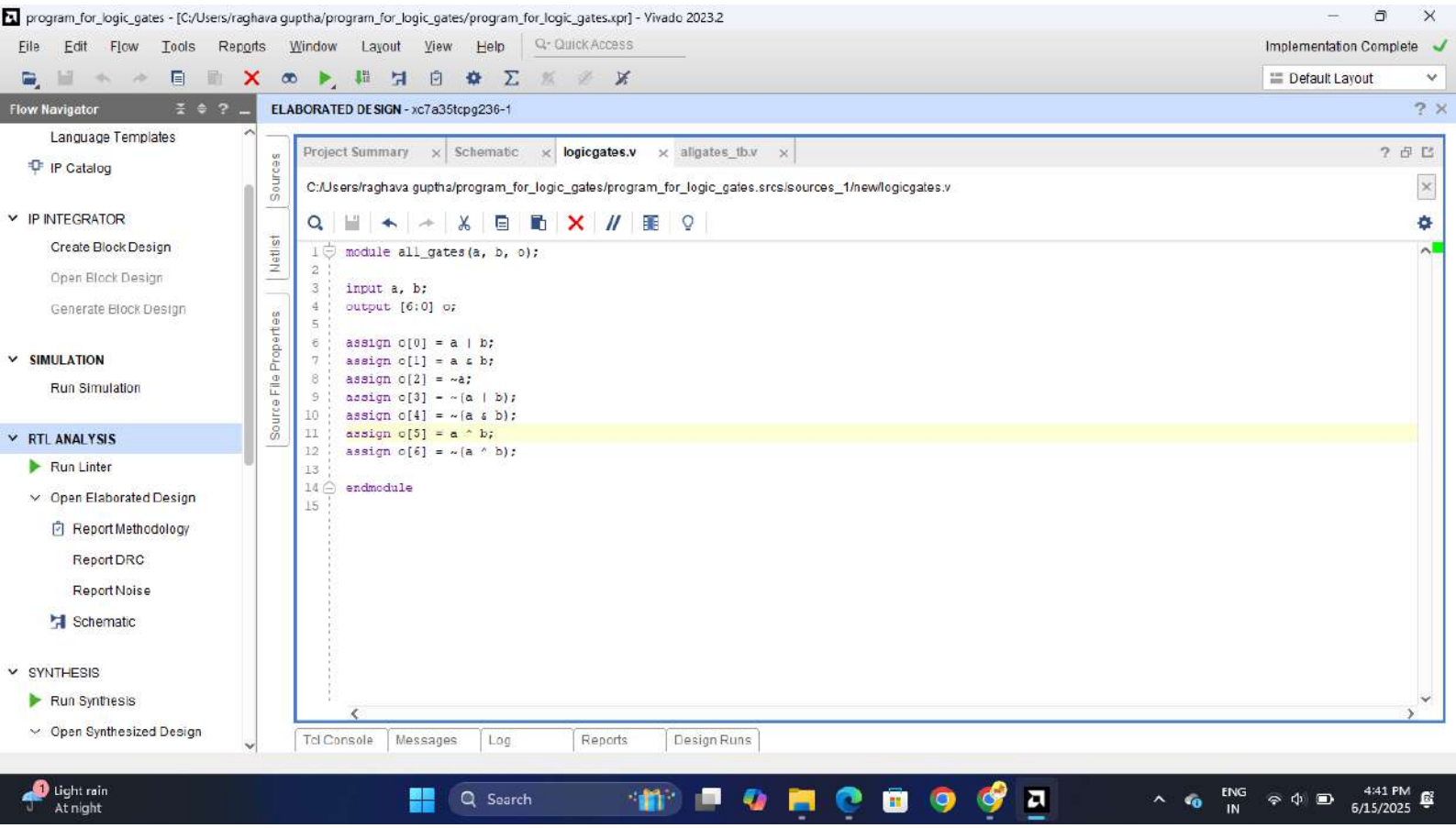
Tcl Console | Messages | Log | Reports | Design Runs

Light rain At night

Search

ENG IN

4:41 PM 6/15/2025


program_for_logic_gates - [C:/Users/raghava guptha/program_for_logic_gates/program_for_logic_gates.xpr] - Vivado 2023.2
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logicgates.v
allgates_tb.v
C:/Users/raghava guptha/program_for_logic_gates/program_for_logic_gates.srcs/sources_1/new/logicgates.v
1 module all_gates(a, b, o);
2
3 input a, b;
4 output [6:0] o;
5
6 assign o[0] = a | b;
7 assign o[1] = a & b;
8 assign o[2] = ~a;
9 assign o[3] = ~(a | b);
10 assign o[4] = ~(a & b);
11 assign o[5] = a ^ b;
12 assign o[6] = ~(a ^ b);
13
14 endmodule
15
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