












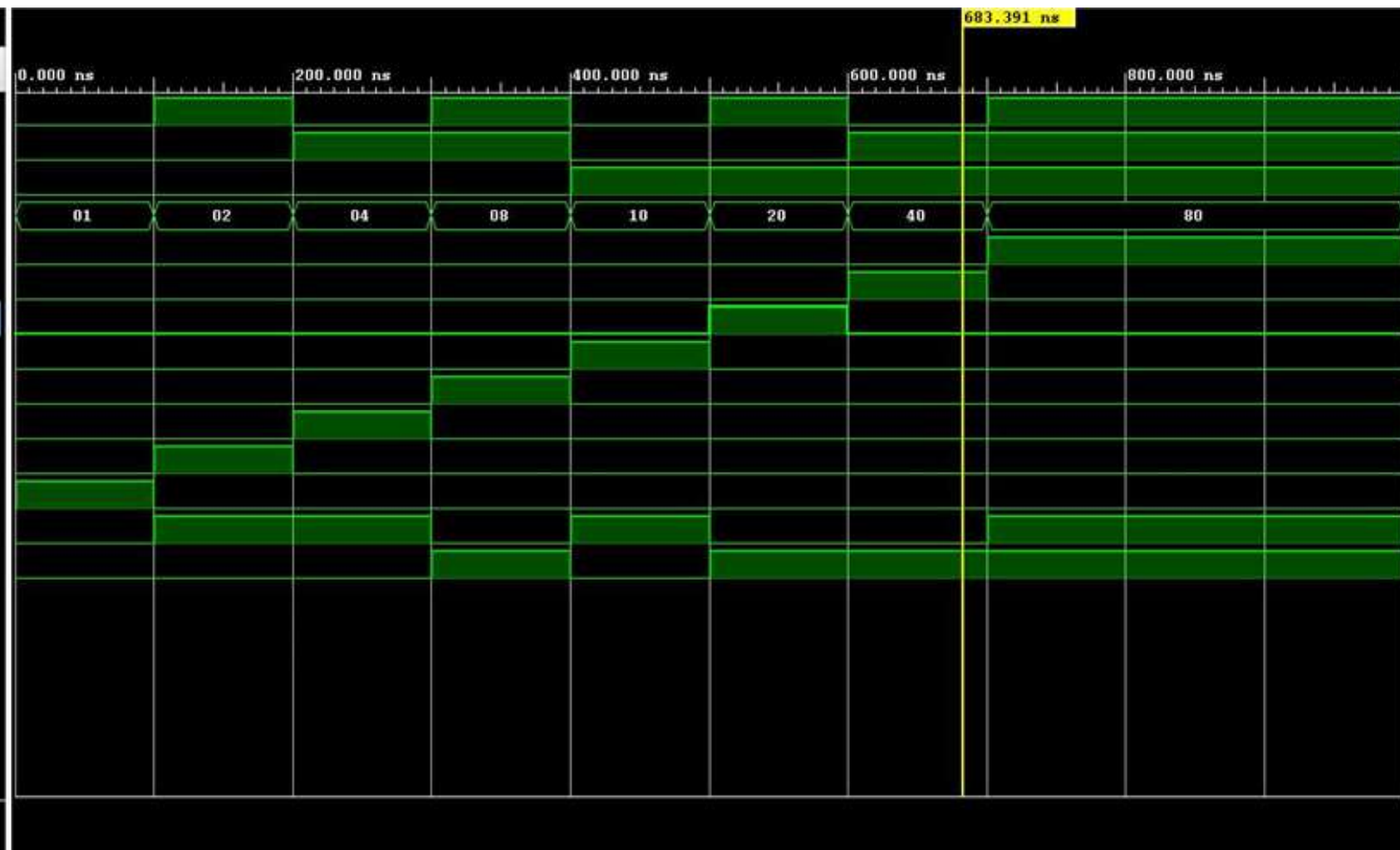


Name	Value
 a	0
 b	1
 cin	1
▼  o[7:0]	40
 [7]	0
 [6]	1
 [5]	0
 [4]	0
 [3]	0
 [2]	0
 [1]	0
 [0]	0
 s	0
 ca	1



fa_2to4decoder - [C:/Users/raghava guptha/fa_2to4decoder/fa_2to4decoder.xpr] - Vivado 2023.2

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ELABORATED DESIGN - xc7a35tcpg236-1

Project Summary x Schematic x fa_2to4decoder.v* x

9 Cells 13 I/O Ports 18 Nets

The schematic diagram illustrates a 2-to-4 decoder circuit. It features two 2-to-4 decoders, d1 and d2, and three RTL_OR blocks. The inputs are b, a, and cin. b and a are connected to the 'a' and 'b' inputs of d1 and d2. cin is connected to the 'en' input of d1 and the 'en0_i' input of an RTL_INV block. The output of RTL_INV is connected to the 'en' input of d2. The outputs of d1 and d2 are connected to the inputs of three RTL_OR blocks. The outputs of these RTL_OR blocks are connected to the inputs of three more RTL_OR blocks, which produce the final outputs: ca, o[7:0], and s.

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fa_2to4decoder.v *

C:/Users/raghava guptha/fa_2to4decoder/fa_2to4decoder.srscs/sources_1/new/fa_2to4decoder.v

7

begin

8

case({a, b})

9

2'b00: o = 4'b0001;

10

2'b01: o = 4'b0010;

11

2'b10: o = 4'b0100;

12

2'b11: o = 4'b1000;

13

endcase

14

end

15

else

16

o = 4'b0000;

17

end

18

endmodule

19

module fa_dec2to4(a, b, cin, o, s, ca);

20

input a, b, cin;

21

output [7:0] o;

22

output reg s, ca;

23

24

dec_2to4 d1(b, a, ~cin, o[3:0]);

25

dec_2to4 d2(b, a, cin, o[7:4]);

26

always @(*)

27

begin

28

s = o[1] | o[2] | o[4] | o[7];

29

ca = o[3] | o[5] | o[6] | o[7];

30

end

31

endmodule

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83°F

Partly cloudy

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ENG IN

1:5

Insert

Verilog

7:40 PM

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Schematic x

fa_2to4decoder.v * x

C:/Users/raghava guptha/fa_2to4decoder/fa_2to4decoder.srcs/sources_1/new/fa_2to4decoder.v

1 module dec_2to4(a, b, en, o);

2 input a, b, en;

3 output reg [3:0] o;

4 always @(*)

5 begin

6 if (en == 1'b1)

7 begin

8 case({a, b})

9 2'b00: o = 4'b0001;

10 2'b01: o = 4'b0010;

11 2'b10: o = 4'b0100;

12 2'b11: o = 4'b1000;

13 endcase

14 end

15 else

16 o = 4'b0000;

17 end

18 endmodule

19 module fa_dec2to4(a, b, cin, o, s, ca);

20 input a, b, cin;

21 output [7:0] o;

22 output reg s, ca;

23

24 dec_2to4 d1(b, a, ~cin, o[3:0]);

25 dec_2to4 d2(b, a, cin, o[7:4]);

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ha_2to4decoder - [C:/Users/raghava guptha/ha_2to4decoder/ha_2to4decoder.xpr] - Vivado 2023.2

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Project Summary x Schematic x ha_2to4decoder.v * x

2 Cells 9 I/O Ports 8 Nets

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Project SummarySchematicha_2to4decoder.v*

C:/Users/raghava guptha/ha_2to4decoder/ha_2to4decoder.srsrcs/sources_1/new/ha_2to4decoder.v

1module dec_2to4(a, b, en, c);
2input a, b, en;
3output reg [3:0] c;
4always @(*)
5begin
6if (en == 1'b1)
7begin
8case({a, b})
92'b00: c = 4'b0001;
102'b01: c = 4'b0010;
112'b10: c = 4'b0100;
122'b11: c = 4'b1000;
13default: c = 4'b0000;
14endcase
15end
16else
17c = 4'b0000;
18end
19endmodule
20
21module ha_dec2to4(a, b, en, c, s, ca);
22input a, b, en;
23output [3:0] c;
24output s, ca;
25dec_2to4 d(a, b, en, c);
26

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Search

24:5
Insert
Verilog

7:37 PM
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