



| Name | Value |
|--------|-------|
| a | 0 |
| b | 0 |
| y[3:0] | 6 |
| [3] | 0 |
| [2] | 1 |
| [1] | 1 |
| [0] | 0 |



xor_using_2to1 - [C:/Users/raghava guptha/xor_using_2to1/xor_using_2to1.xpr] - Vivado 2023.2

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Ready

Default Layout

Flow Navigator

ELABORATED DESIGN - xc7a35tcpg236-1

Project Summary x Schematic x xor_using_2to1.v x

5 Cells 6 I/O Ports 9 Nets

Sources

Netlist

Source File Properties

PROJECT MANAGER

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IP INTEGRATOR

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SIMULATION

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RTL ANALYSIS

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 - Report Methodology
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 - Report Noise
 - Schematic

Schematic

RTL_INV

m1_xor

m2_xnor

m3_nand

m4_and

y[3:0]

```
graph LR
    a((a)) --- i0_1_1[i[0:1]]
    a --- i0_1_2[i[0:1]]
    a --- i0_1_3[i[0:1]]
    a --- i0_1_4[i[0:1]]
    b((b)) --- i0_1_1
    b --- i0_1_2
    b --- i0_1_3
    b --- i0_1_4
    b --- rtl_inv[RTL_INV]
    rtl_inv --- i0_1_2
    rtl_inv --- i0_1_3
    rtl_inv --- i0_1_4
    i0_1_1 --- m1_xor[m1_xor]
    i0_1_2 --- m2_xnor[m2_xnor]
    i0_1_3 --- m3_nand[m3_nand]
    i0_1_4 --- m4_and[m4_and]
    m1_xor --- y3_0[y[3:0]]
    m2_xnor --- y3_0
    m3_nand --- y3_0
    m4_and --- y3_0
```

xor_using_2to1 - [C:/Users/raghava guptha/xor_using_2to1/xor_using_2to1.xpr] - Vivado 2023.2

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Flow Navigator

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Sources

Netlist

Source File Properties

Project Summary x Schematic x xor_using_2to1.v x

C:/Users/raghava guptha/xor_using_2to1/xor_using_2to1.srcs/sources_1/new/xor_using_2to1.v

```
1 module mux_2to1(input [0:1] i, output reg y, input s);
2     always @(*)
3     begin
4         if (s == 0)
5             y = i[0];
6         else
7             y = i[1];
8     end
9 endmodule
10
11 module gates_2to1mux(input a, b, output [3:0] y);
12     mux_2to1 m1_xor({b, ~b}, y[0], a);
13     mux_2to1 m2_xnor({~b, b}, y[1], a);
14     mux_2to1 m3_nand({1'b1, b}, y[2], a);
15     mux_2to1 m4_and({0, b}, y[3], a);
16 endmodule
17
```

Tcl Console Messages Log Reports Design Runs