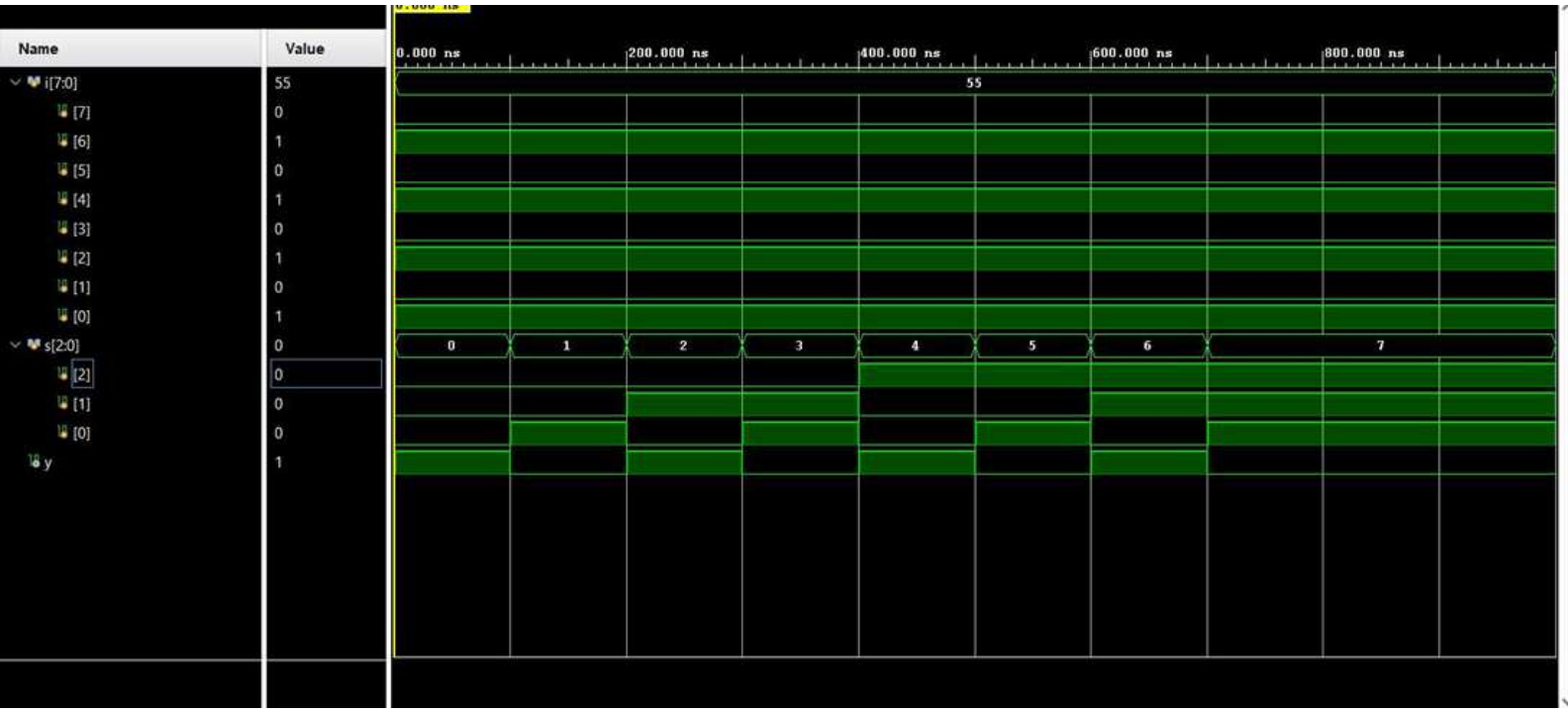
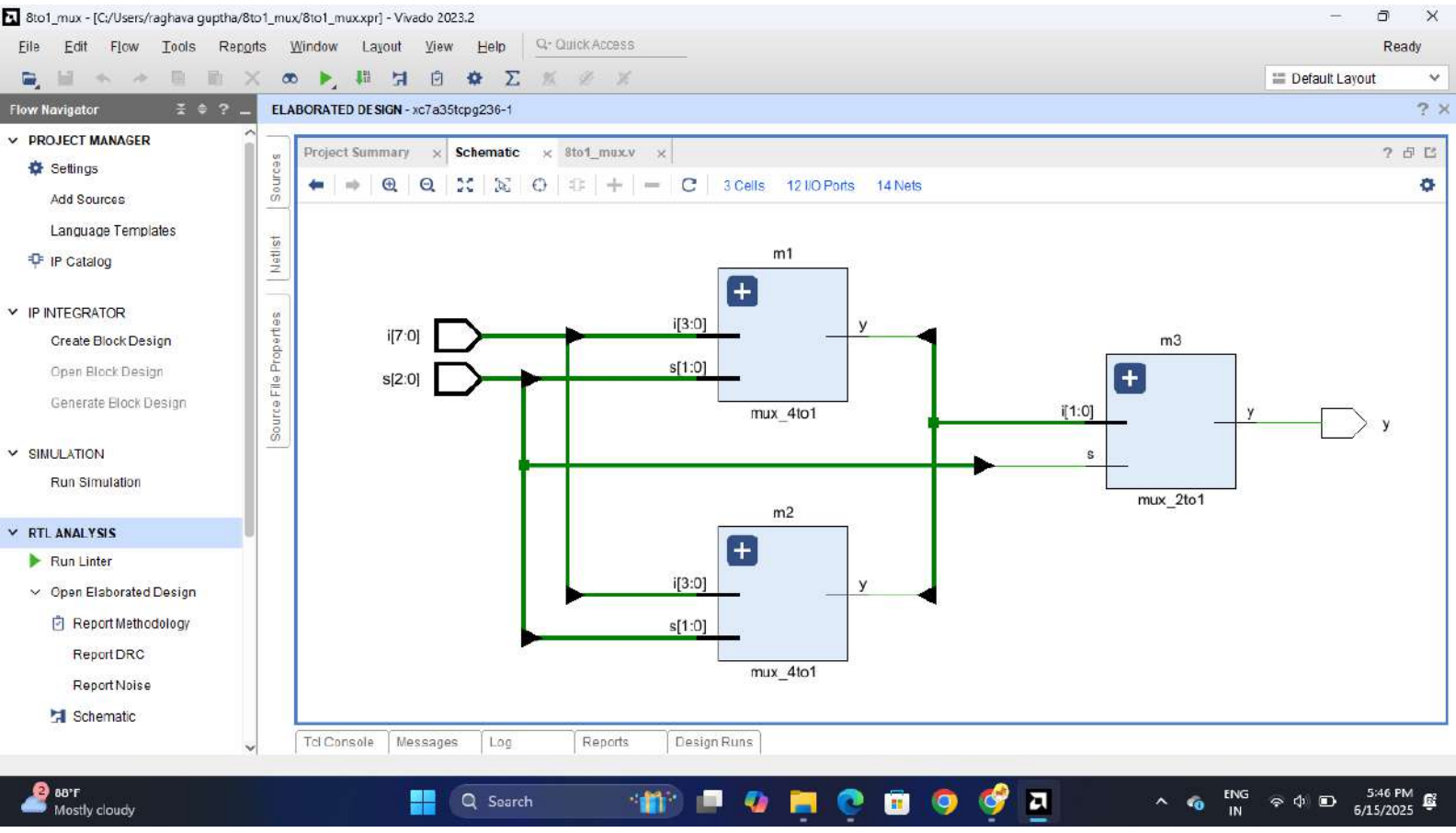

Name
Value
i[7:0]
55
[7]
0
[6]
1
[5]
0
[4]
1
[3]
0
[2]
1
[1]
0
[0]
1
s[2:0]
0
[2]
0
[1]
0
[0]
0
y
1
0.000 ns
200.000 ns
400.000 ns
600.000 ns
800.000 ns
55
0
1
2
3
4
5
6
7


8to1_mux - [C:/Users/raghava guptha/8to1_mux/8to1_mux.xpr] - Vivado 2023.2
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8to1_mux.v
3 Cells
12 I/O Ports
14 Nets
m1
i[7:0]
s[2:0]
i[3:0]
s[1:0]
y
mux_4to1
m3
i[1:0]
s
y
mux_2to1
y
m2
i[3:0]
s[1:0]
y
mux_4to1
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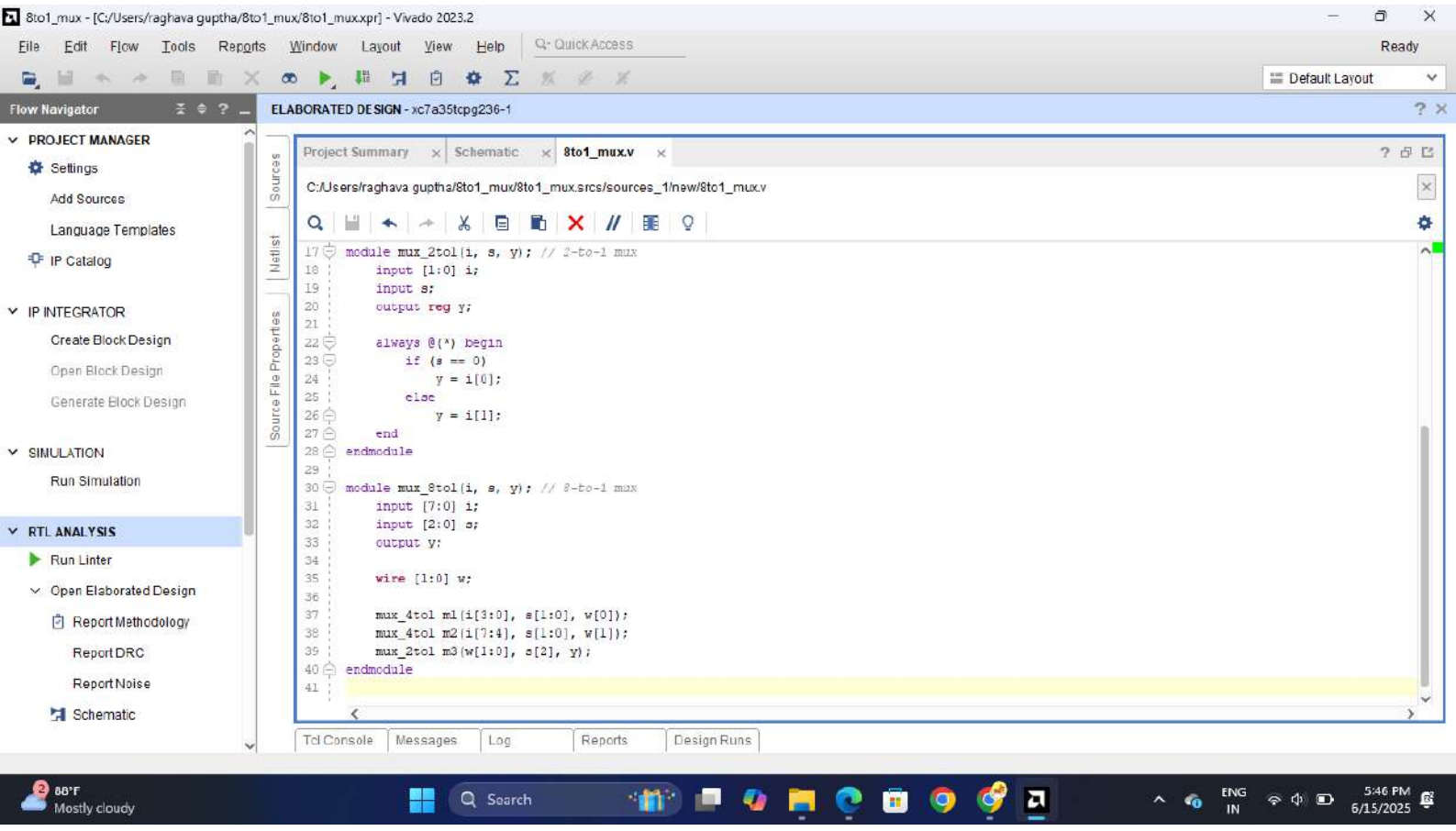
88°F
Mostly cloudy
Search
ENG
IN
5:46 PM
6/15/2025


8to1_mux - [C:/Users/raghava guptha/8to1_mux/8to1_mux.xpr] - Vivado 2023.2
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C:/Users/raghava guptha/8to1_mux/8to1_mux.srcs/sources_1/new/8to1_mux.v
Sources
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17 module mux_2to1(i, s, y); // 2-to-1 mux
18 input [1:0] i;
19 input s;
20 output reg y;
21
22 always @(*) begin
23 if (s == 0)
24 y = i[0];
25 else
26 y = i[1];
27 end
28 endmodule
29
30 module mux_8to1(i, s, y); // 8-to-1 mux
31 input [7:0] i;
32 input [2:0] s;
33 output y;
34
35 wire [1:0] w;
36
37 mux_4to1 m1(i[3:0], s[1:0], w[0]);
38 mux_4to1 m2(i[7:4], s[1:0], w[1]);
39 mux_2to1 m3(w[1:0], s[2], y);
40 endmodule
41
Tcl Console
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Design Runs
88°F
Mostly cloudy
Search
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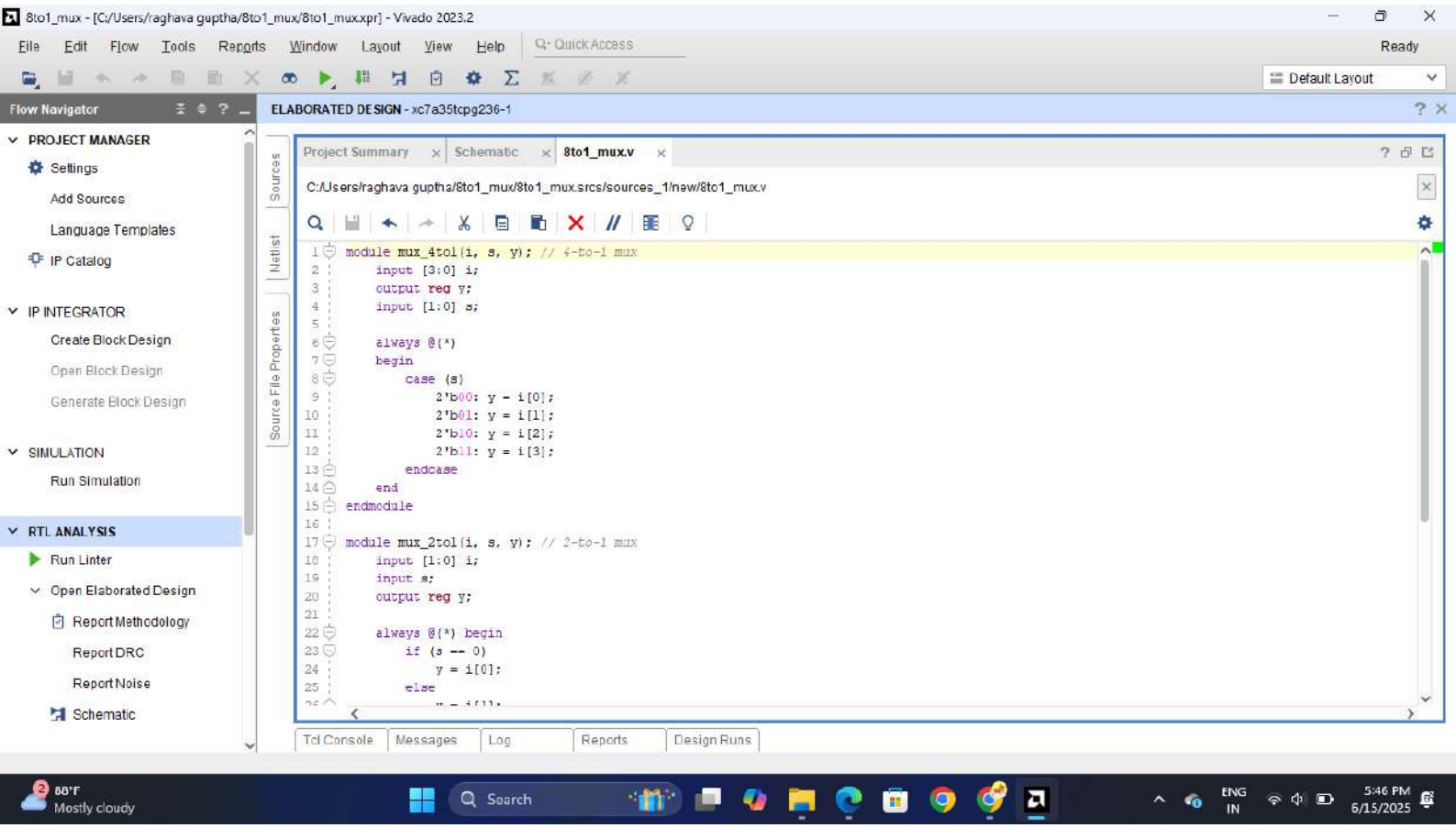
5:46 PM
6/15/2025


8to1_mux - [C:/Users/raghava guptha/8to1_mux/8to1_mux.xpr] - Vivado 2023.2
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8to1_mux.v
C:/Users/raghava guptha/8to1_mux/8to1_mux.srcs/sources_1/new/8to1_mux.v
1 module mux_4to1(i, s, y); // 4-to-1 mux
2 input [3:0] i;
3 output reg y;
4 input [1:0] s;
5
6 always @(*)
7 begin
8 case (s)
9 2'b00: y = i[0];
10 2'b01: y = i[1];
11 2'b10: y = i[2];
12 2'b11: y = i[3];
13 endcase
14 end
15 endmodule
16
17 module mux_2to1(i, s, y); // 2-to-1 mux
18 input [1:0] i;
19 input s;
20 output reg y;
21
22 always @(*) begin
23 if (s == 0)
24 y = i[0];
25 else
Tcl Console
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Mostly cloudy
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ENG
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5:46 PM
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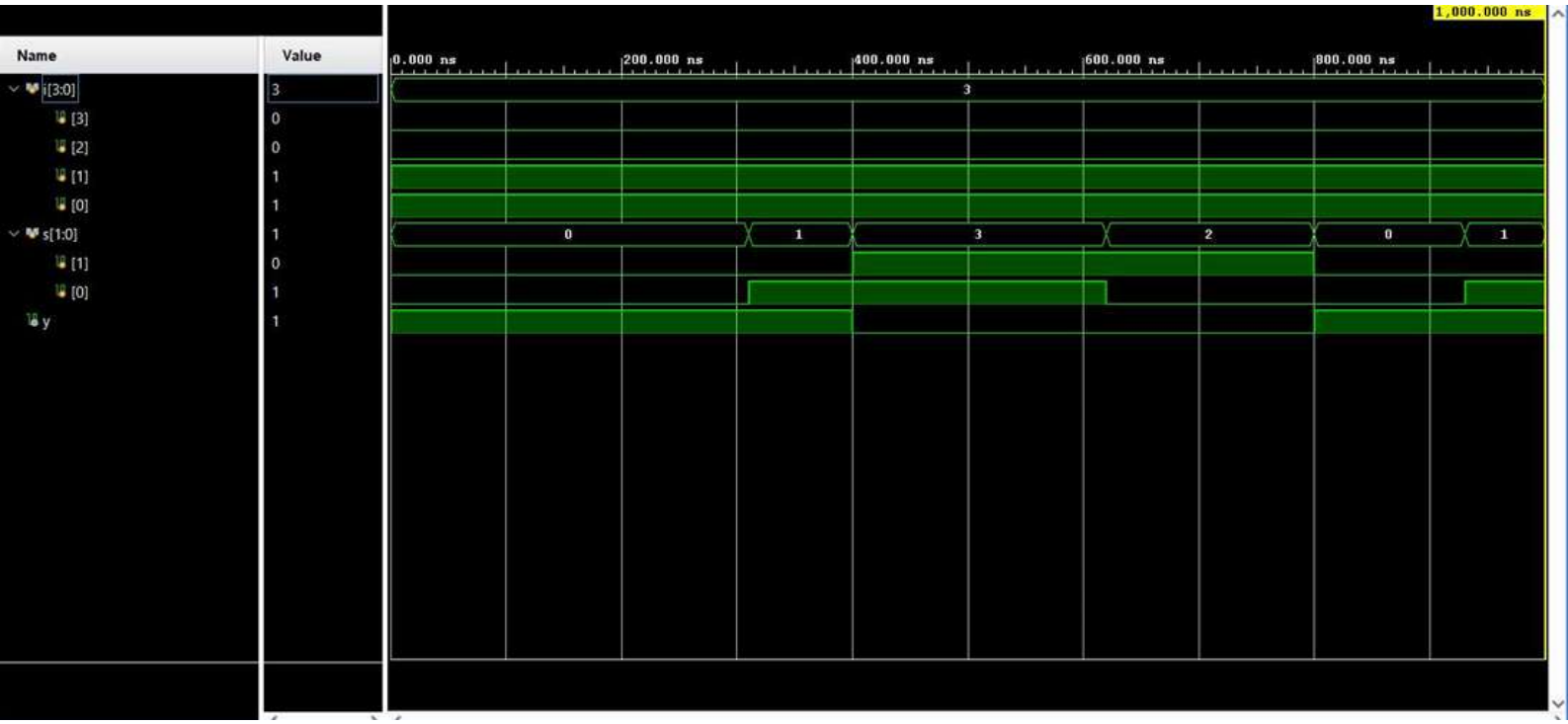
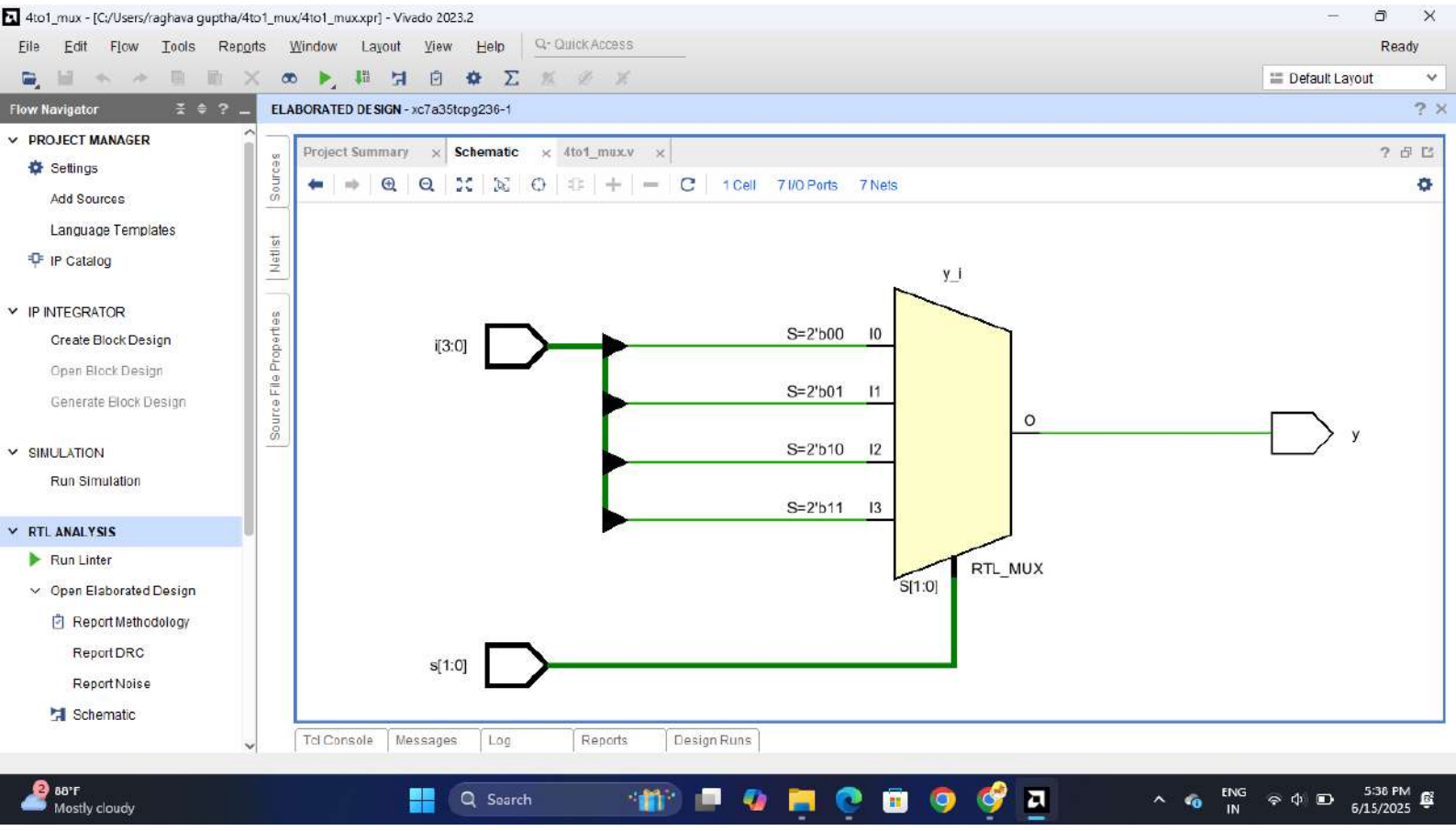

Name
Value
i[3:0]
3
[3]
0
[2]
0
[1]
1
[0]
1
s[1:0]
1
[1]
0
[0]
1
y
1
0.000 ns
200.000 ns
400.000 ns
600.000 ns
800.000 ns
1,000.000 ns
3
0
1
3
2
0
1


4to1_mux - [C:/Users/raghava guptha/4to1_mux/4to1_mux.xpr] - Vivado 2023.2
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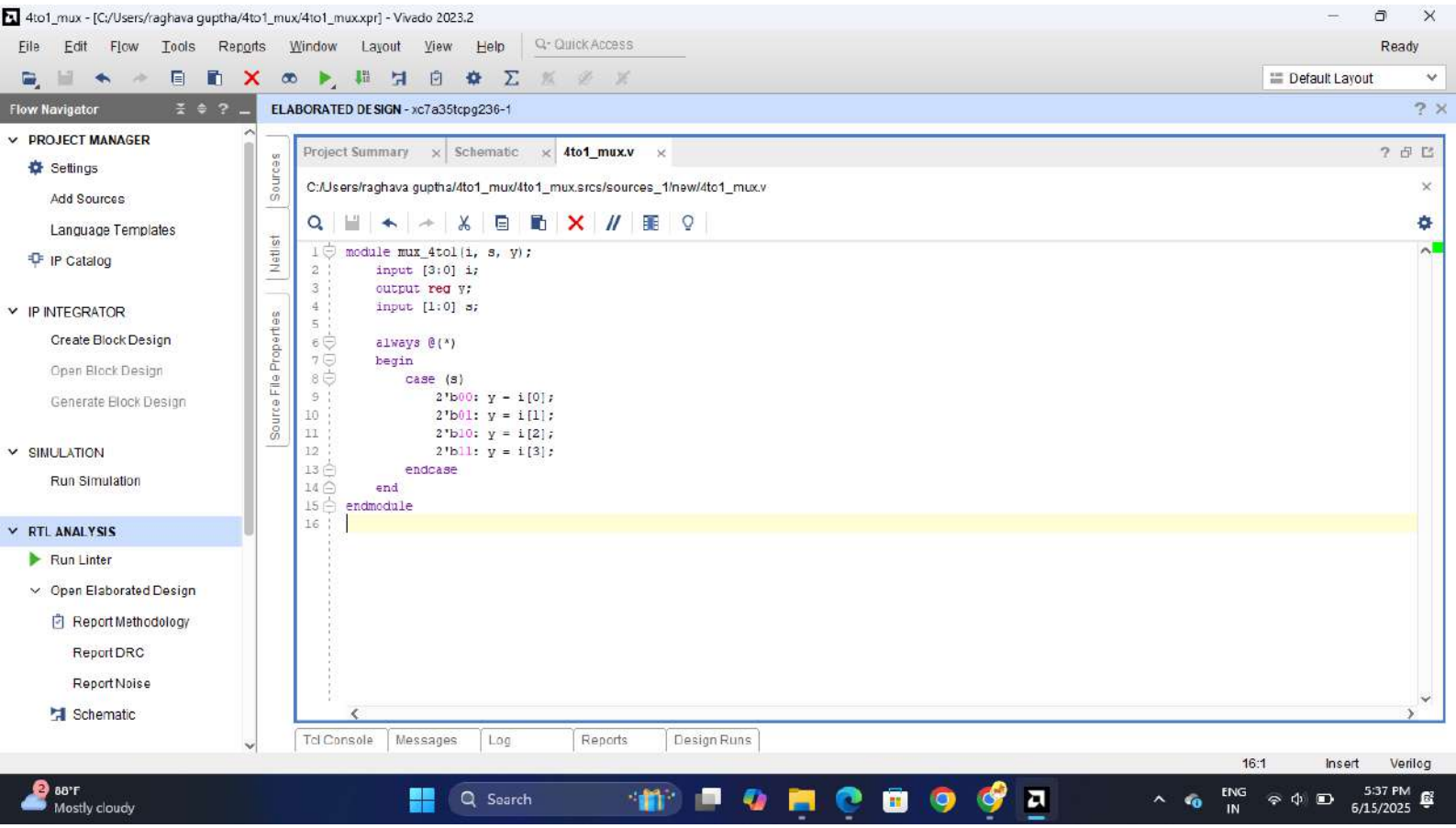
4to1_mux.v
1 Cell
7 I/O Ports
7 Nets
y_i
i[3:0]
S=2'b00
I0
S=2'b01
I1
S=2'b10
I2
S=2'b11
I3
O
y
RTL_MUX
S[1:0]
s[1:0]
Tcl Console
Messages
Log
Reports
Design Runs
88°F
Mostly cloudy
Search
ENG
IN
5:38 PM
6/15/2025


4to1_mux - [C:/Users/raghava guptha/4to1_mux/4to1_mux.xpr] - Vivado 2023.2
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module mux_4to1(i, s, y);
input [3:0] i;
output reg y;
input [1:0] s;
always @(*)
begin
case (s)
2'b00: y = i[0];
2'b01: y = i[1];
2'b10: y = i[2];
2'b11: y = i[3];
endcase
end
endmodule
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16:1
Insert
Verilog
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