
Name
Value
a
0
b
0
eq
1
lt
0
gt
0
0.000 ns
200.000 ns
400.000 ns
600.000 ns
800.000 ns
1,000.000 ns

comp_1bit - [C:/Users/raghava guptha/comp_1bit/comp_1bit.xpr] - Vivado 2023.2

File Edit Flow Tools Reports Window Layout View Help Quick Access Ready

Default Layout

Flow Navigator

PROJECT MANAGER
- Settings
- Add Sources
- Language Templates
- IP Catalog

IP INTEGRATOR
- Create Block Design
- Open Block Design
- Generate Block Design

SIMULATION
- Run Simulation

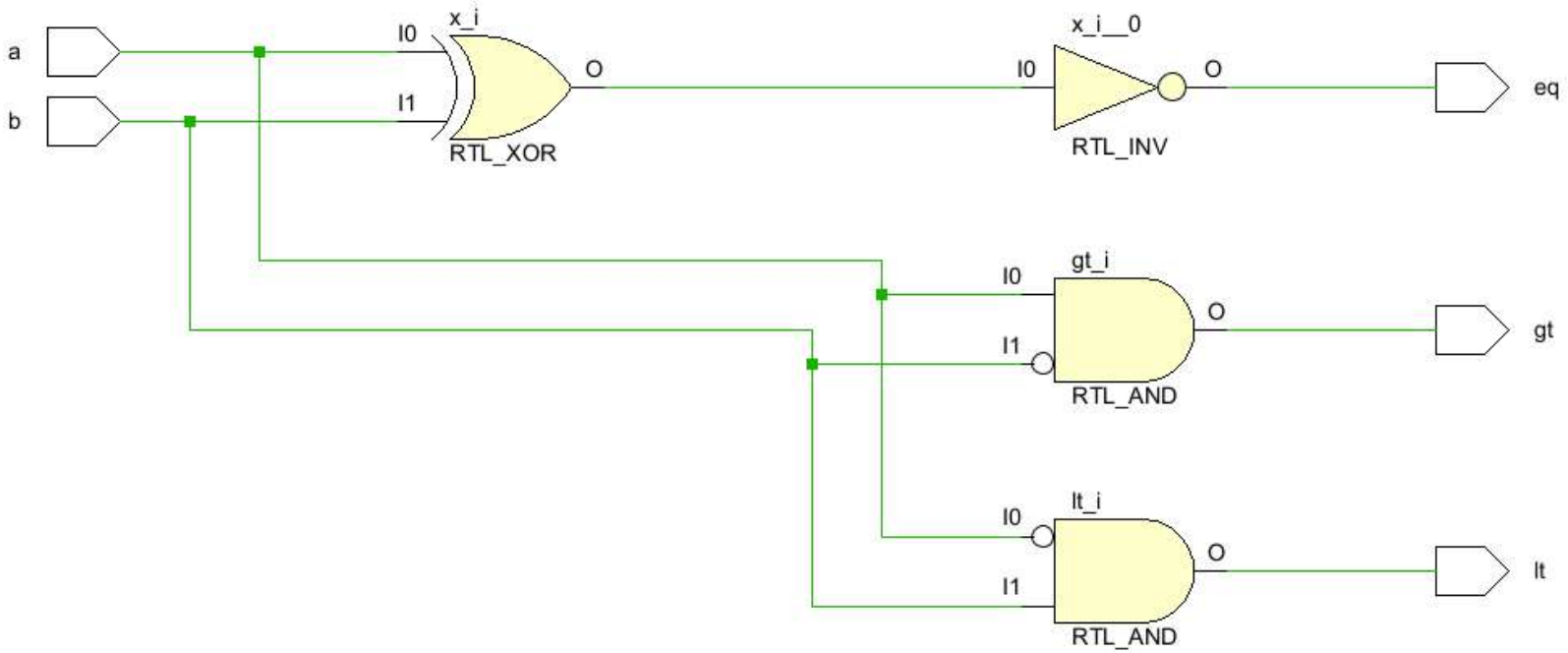
RTL ANALYSIS
- Run Linter
- Open Elaborated Design
  - Report Methodology
  - Report DRC
  - Report Noise
  - Schematic

ELABORATED DESIGN - xc7a35tcpg236-1

Sources | Netlist | Source File Properties

Project Summary | Schematic | comp_1bit.v

4 Cells 5 I/O Ports 6 Nets



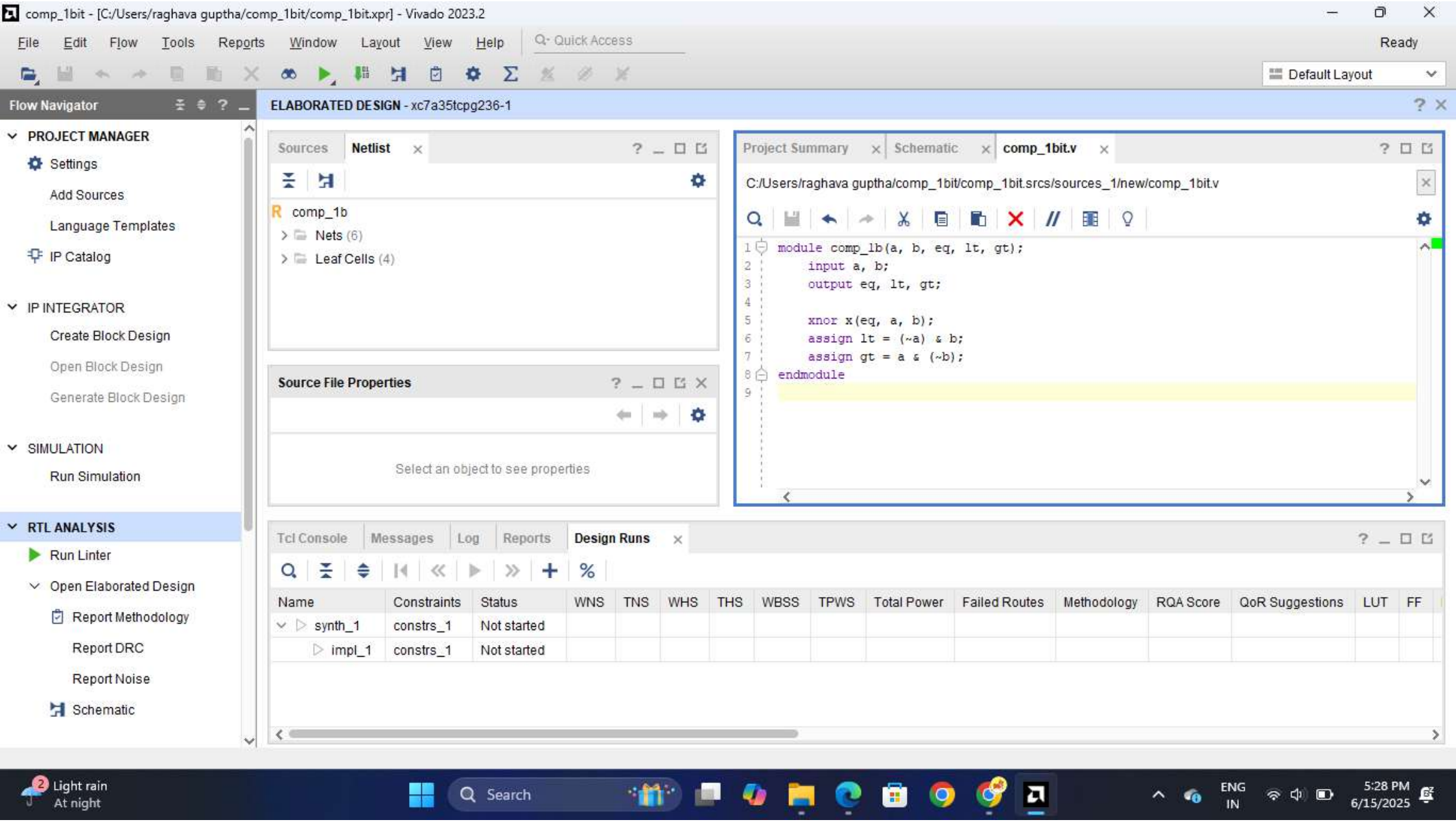
Tcl Console | Messages | Log | Reports | Design Runs

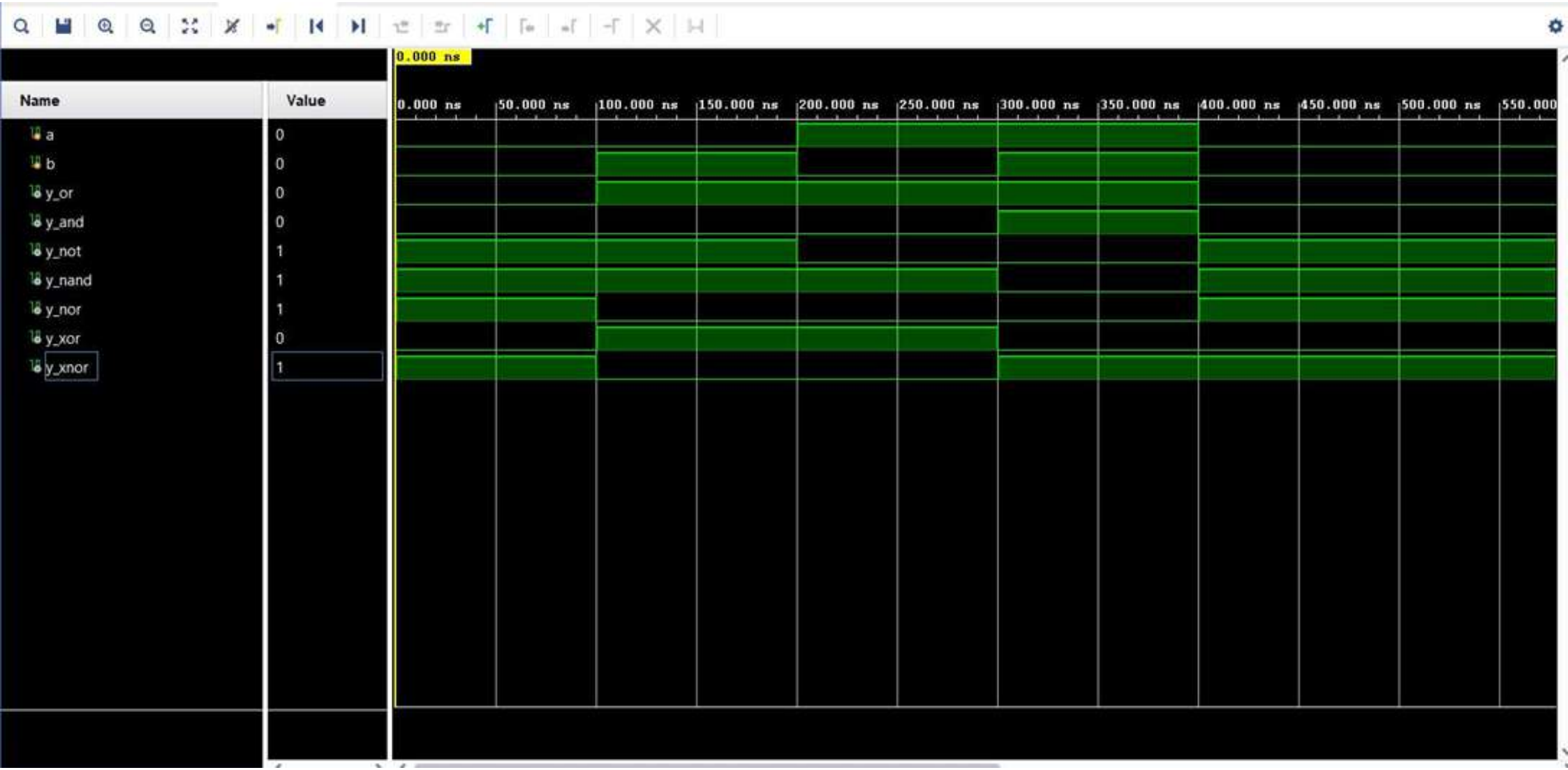
Light rain At night

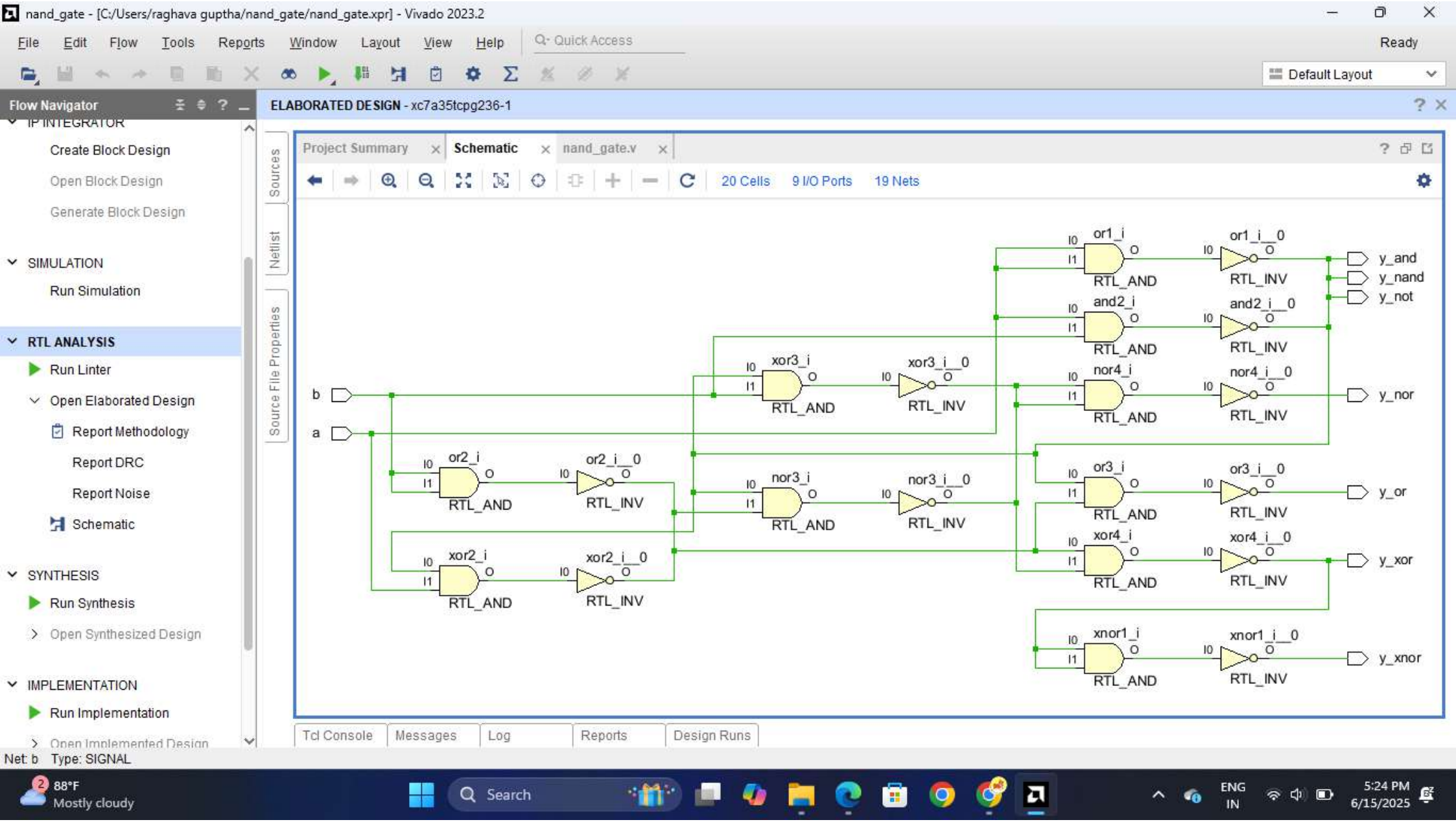
Search

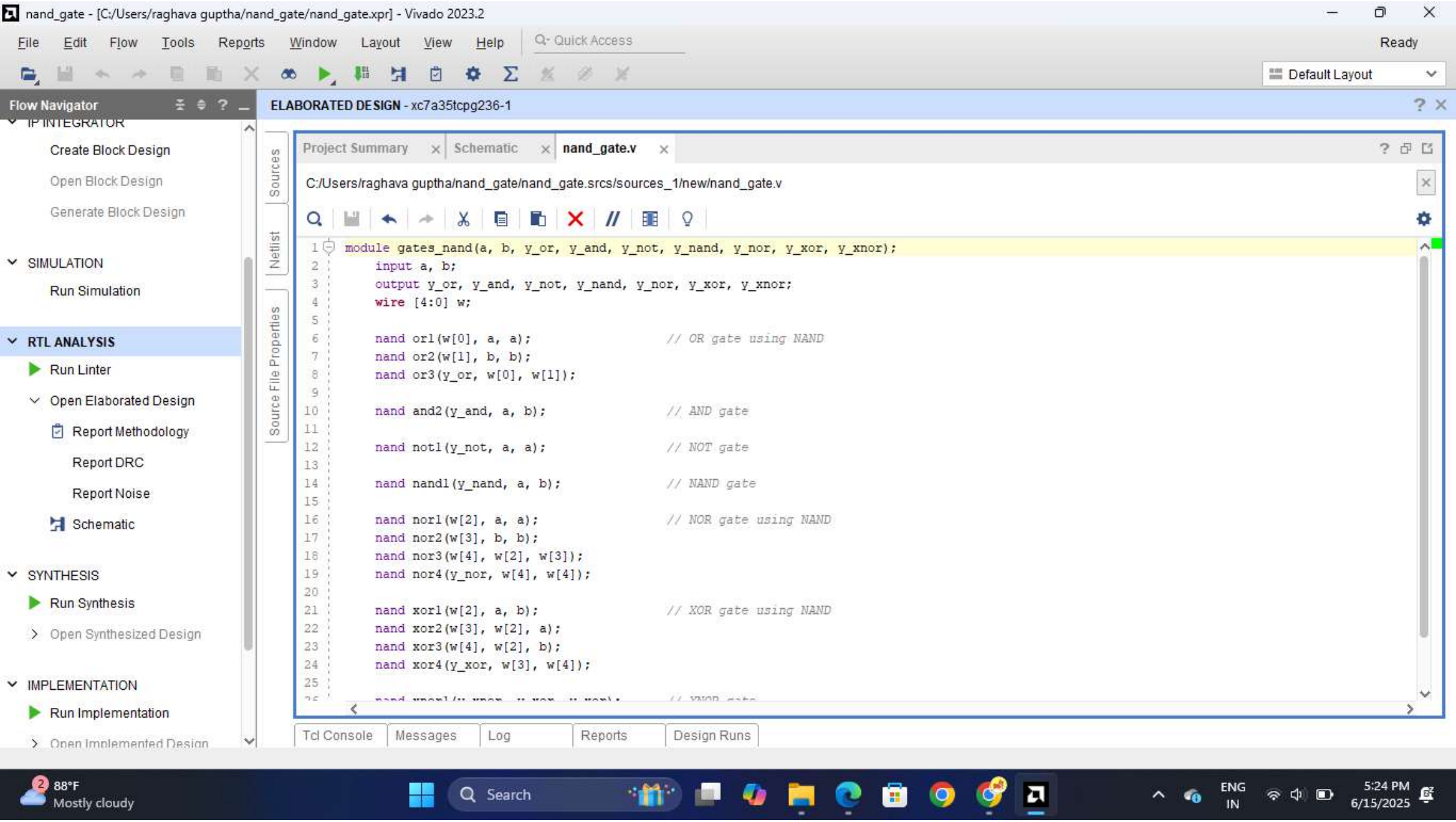
ENG IN

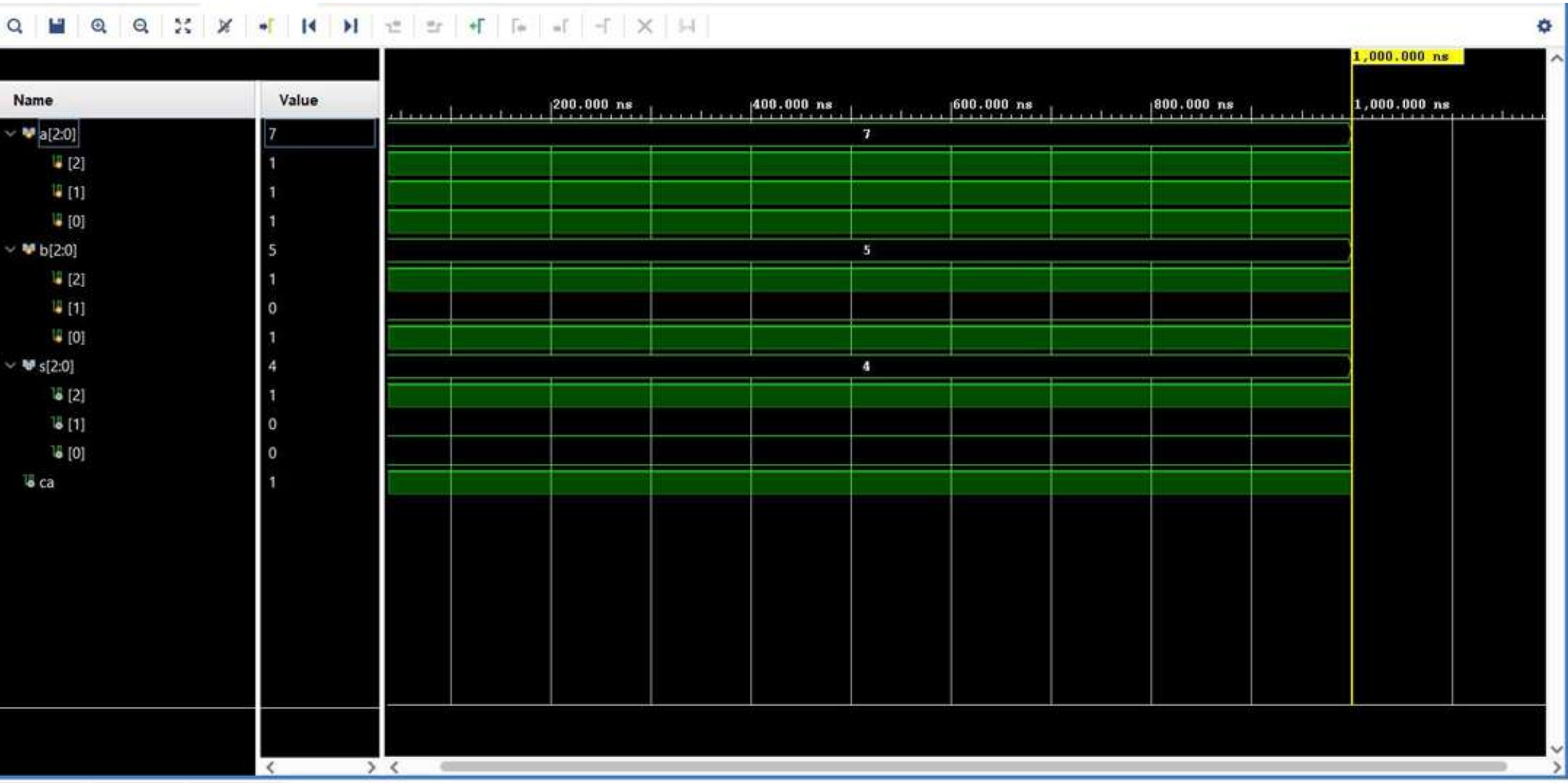
5:28 PM 6/15/2025


comp_1bit - [C:/Users/raghava guptha/comp_1bit/comp_1bit.xpr] - Vivado 2023.2
File Edit Flow Tools Reports Window Layout View Help
Quick Access
Ready
Default Layout
Flow Navigator
PROJECT MANAGER
Settings
Add Sources
Language Templates
IP Catalog
IP INTEGRATOR
Create Block Design
Open Block Design
Generate Block Design
SIMULATION
Run Simulation
RTL ANALYSIS
Run Linter
Open Elaborated Design
Report Methodology
Report DRC
Report Noise
Schematic
ELABORATED DESIGN - xc7a35tcpg236-1
Sources
Netlist
comp_1b
Nets (6)
Leaf Cells (4)
Source File Properties
Select an object to see properties
Project Summary
Schematic
comp_1bit.v
C:/Users/raghava guptha/comp_1bit/comp_1bit.srcs/sources_1/new/comp_1bit.v
1 module comp_1b(a, b, eq, lt, gt);
2 input a, b;
3 output eq, lt, gt;
4
5 xnor x(eq, a, b);
6 assign lt = (~a) & b;
7 assign gt = a & (~b);
8 endmodule
9
Tcl Console
Messages
Log
Reports
Design Runs
Name Constraints Status WNS TNS WHS THS WBSS TPWS Total Power Failed Routes Methodology RQA Score QoR Suggestions LUT FF
synth_1 constrs_1 Not started
impl_1 constrs_1 Not started
Light rain
At night
Search
ENG
IN
5:28 PM
6/15/2025


0.000 ns
Name
Value
0.000 ns
50.000 ns
100.000 ns
150.000 ns
200.000 ns
250.000 ns
300.000 ns
350.000 ns
400.000 ns
450.000 ns
500.000 ns
550.000
a
0
b
0
y_or
0
y_and
0
y_not
1
y_nand
1
y_nor
1
y_xor
0
y_xnor
1


nand_gate - [C:/Users/raghava guptha/nand_gate/nand_gate.xpr] - Vivado 2023.2
File Edit Flow Tools Reports Window Layout View Help
Quick Access
Ready
Default Layout
Flow Navigator
IP INTEGRATOR
Create Block Design
Open Block Design
Generate Block Design
SIMULATION
Run Simulation
RTL ANALYSIS
Run Linter
Open Elaborated Design
Report Methodology
Report DRC
Report Noise
Schematic
SYNTHESIS
Run Synthesis
Open Synthesized Design
IMPLEMENTATION
Run Implementation
ELABORATED DESIGN - xc7a35tcpg236-1
Sources
Netlist
Source File Properties
Project Summary
Schematic
nand_gate.v
20 Cells
9 I/O Ports
19 Nets
b
a
or1_i
or1_i__0
and2_i
and2_i__0
nor4_i
nor4_i__0
xor3_i
xor3_i__0
or2_i
or2_i__0
nor3_i
nor3_i__0
or3_i
or3_i__0
xor2_i
xor2_i__0
xor4_i
xor4_i__0
xnor1_i
xnor1_i__0
RTL_AND
RTL_INV
y_and
y_nand
y_not
y_nor
y_or
y_xor
y_xnor
Tcl Console
Messages
Log
Reports
Design Runs
Net: b Type: SIGNAL
88°F
Mostly cloudy
Search
ENG
IN
5:24 PM
6/15/2025


nand_gate - [C:/Users/raghava guptha/nand_gate/nand_gate.xpr] - Vivado 2023.2
File Edit Flow Tools Reports Window Layout View Help
Quick Access
Ready
Default Layout
Flow Navigator
IP INTEGRATOR
Create Block Design
Open Block Design
Generate Block Design
SIMULATION
Run Simulation
RTL ANALYSIS
Run Linter
Open Elaborated Design
Report Methodology
Report DRC
Report Noise
Schematic
SYNTHESIS
Run Synthesis
Open Synthesized Design
IMPLEMENTATION
Run Implementation
Open Implemented Design
ELABORATED DESIGN - xc7a35tcpg236-1
Sources
Netlist
Source File Properties
Project Summary
Schematic
nand_gate.v
C:/Users/raghava guptha/nand_gate/nand_gate.srcs/sources_1/new/nand_gate.v
1 module gates_nand(a, b, y_or, y_and, y_not, y_nand, y_nor, y_xor, y_xnor);
2 input a, b;
3 output y_or, y_and, y_not, y_nand, y_nor, y_xor, y_xnor;
4 wire [4:0] w;
5
6 nand or1(w[0], a, a); // OR gate using NAND
7 nand or2(w[1], b, b);
8 nand or3(y_or, w[0], w[1]);
9
10 nand and2(y_and, a, b); // AND gate
11
12 nand not1(y_not, a, a); // NOT gate
13
14 nand nand1(y_nand, a, b); // NAND gate
15
16 nand nor1(w[2], a, a); // NOR gate using NAND
17 nand nor2(w[3], b, b);
18 nand nor3(w[4], w[2], w[3]);
19 nand nor4(y_nor, w[4], w[4]);
20
21 nand xor1(w[2], a, b); // XOR gate using NAND
22 nand xor2(w[3], w[2], a);
23 nand xor3(w[4], w[2], b);
24 nand xor4(y_xor, w[3], w[4]);
25
Tcl Console
Messages
Log
Reports
Design Runs
88°F
Mostly cloudy
Search
ENG
IN
5:24 PM
6/15/2025


Name
Value
a[2:0]
7
[2]
1
[1]
1
[0]
1
b[2:0]
5
[2]
1
[1]
0
[0]
1
s[2:0]
4
[2]
1
[1]
0
[0]
0
ca
1
200.000 ns
400.000 ns
600.000 ns
800.000 ns
1,000.000 ns
1,000.000 ns
7
5
4

ass3_rca - [C:/Users/raghava guptha/ass3_rca/ass3_rca.xpr] - Vivado 2023.2

File Edit Flow Tools Reports Window Layout View Help Quick Access Ready

Default Layout

Flow Navigator

PROJECT MANAGER
- Settings
- Add Sources
- Language Templates
- IP Catalog

IP INTEGRATOR
- Create Block Design
- Open Block Design
- Generate Block Design

SIMULATION
- Run Simulation

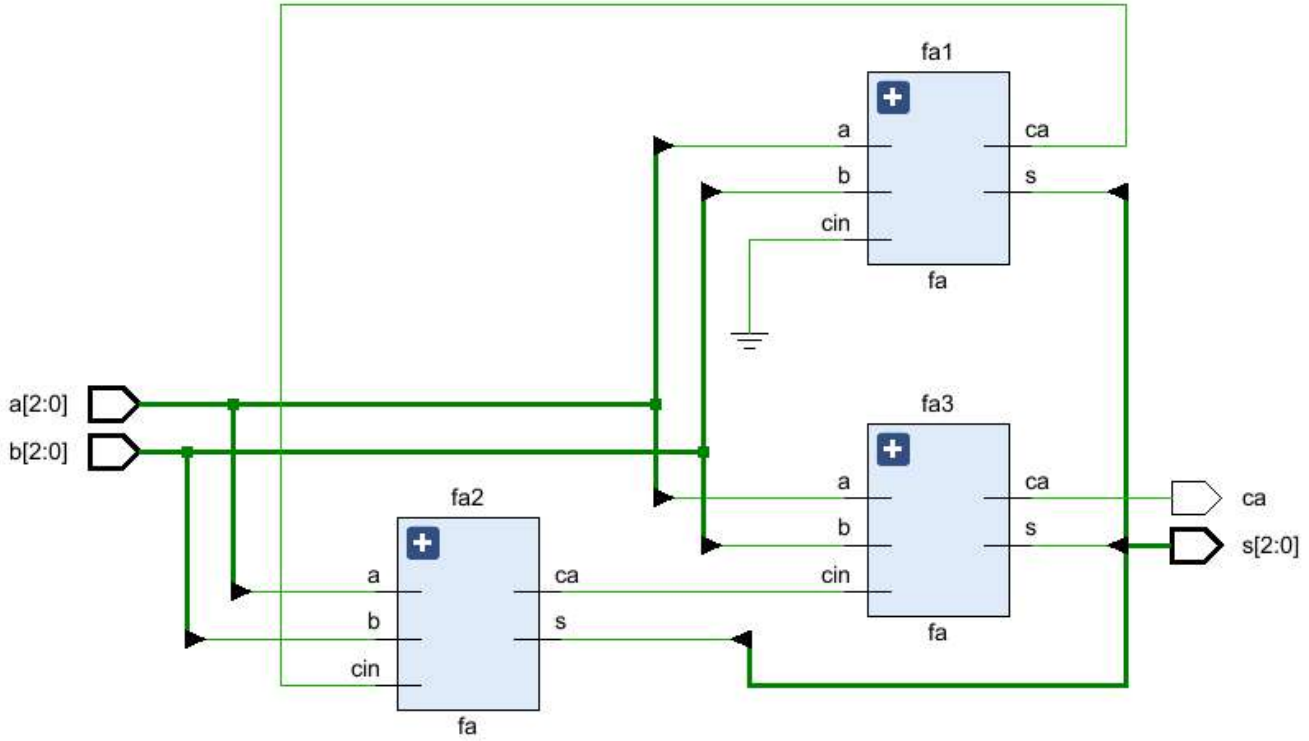
RTL ANALYSIS
- Run Linter
- Open Elaborated Design
  - Report Methodology
  - Report DRC
  - Report Noise
  - Schematic

ELABORATED DESIGN - xc7a35tcpg236-1

Sources | Netlist | Source File Properties

Project Summary | Schematic | rca.v | repple_carrey_adder.v

3 Cells 10 I/O Ports 13 Nets



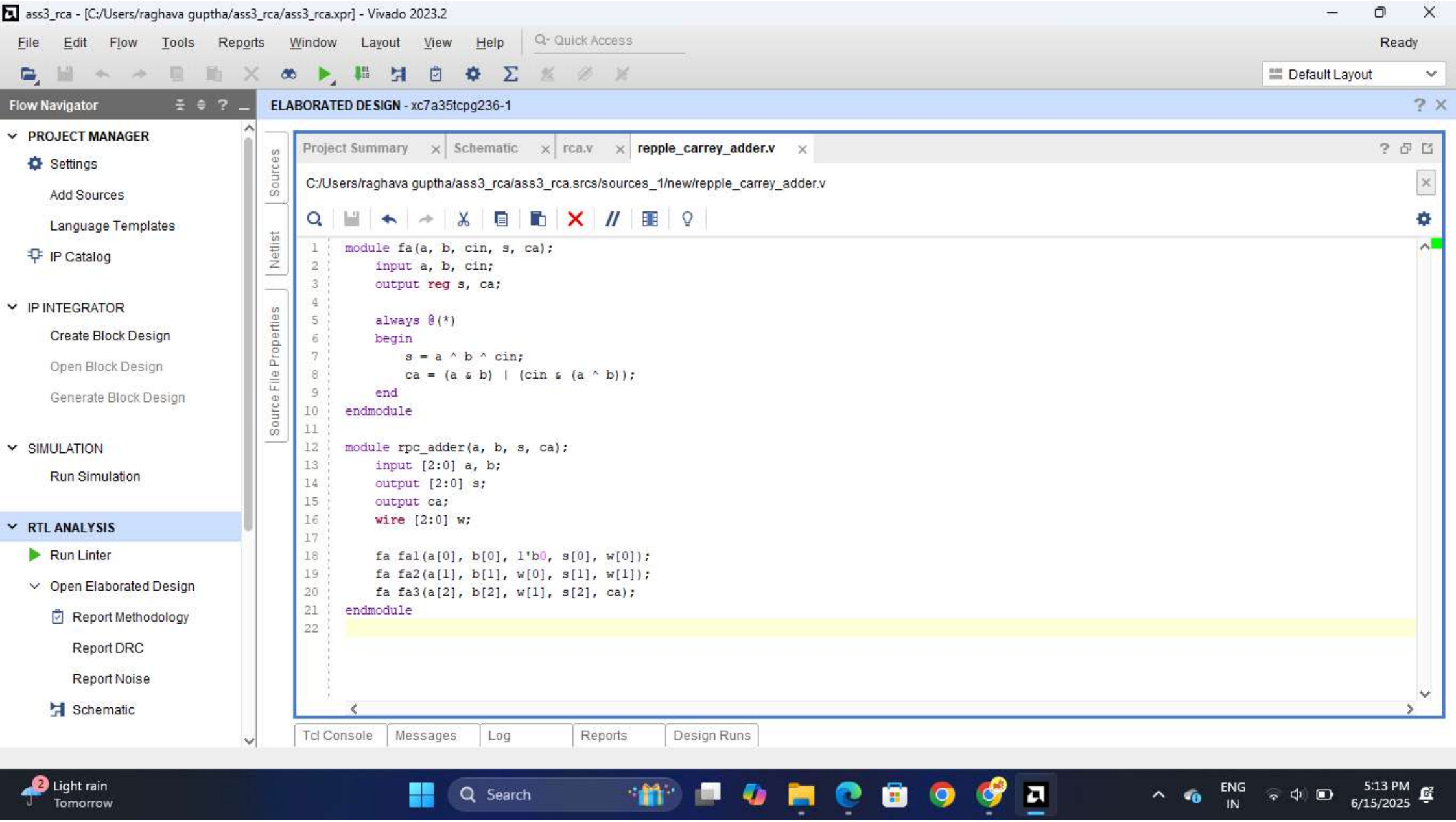
Tcl Console | Messages | Log | Reports | Design Runs

Light rain Tomorrow

Search

ENG IN

5:13 PM 6/15/2025


ass3_rca - [C:/Users/raghava guptha/ass3_rca/ass3_rca.xpr] - Vivado 2023.2
File Edit Flow Tools Reports Window Layout View Help
Quick Access
Ready
Default Layout
Flow Navigator
PROJECT MANAGER
Settings
Add Sources
Language Templates
IP Catalog
IP INTEGRATOR
Create Block Design
Open Block Design
Generate Block Design
SIMULATION
Run Simulation
RTL ANALYSIS
Run Linter
Open Elaborated Design
Report Methodology
Report DRC
Report Noise
Schematic
ELABORATED DESIGN - xc7a35tcpg236-1
Sources
Netlist
Source File Properties
Project Summary
Schematic
rca.v
repple_carrey_adder.v
C:/Users/raghava guptha/ass3_rca/ass3_rca.srcs/sources_1/new/repple_carrey_adder.v
1 module fa(a, b, cin, s, ca);
2 input a, b, cin;
3 output reg s, ca;
4
5 always @(*)
6 begin
7 s = a ^ b ^ cin;
8 ca = (a & b) | (cin & (a ^ b));
9 end
10 endmodule
11
12 module rpc_adder(a, b, s, ca);
13 input [2:0] a, b;
14 output [2:0] s;
15 output ca;
16 wire [2:0] w;
17
18 fa fa1(a[0], b[0], 1'b0, s[0], w[0]);
19 fa fa2(a[1], b[1], w[0], s[1], w[1]);
20 fa fa3(a[2], b[2], w[1], s[2], ca);
21 endmodule
22
Tcl Console
Messages
Log
Reports
Design Runs
Light rain
Tomorrow
Search
ENG
IN
5:13 PM
6/15/2025