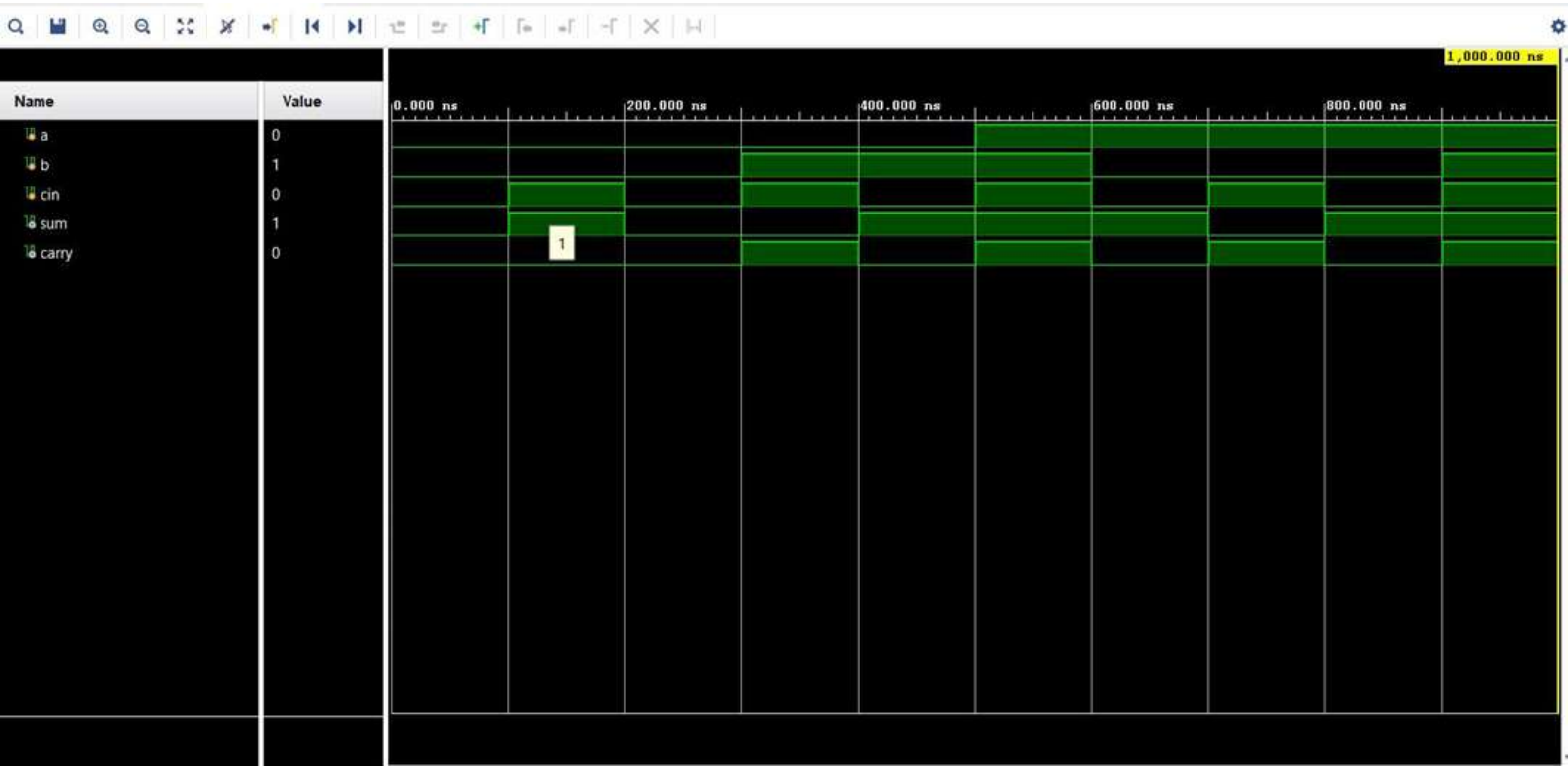
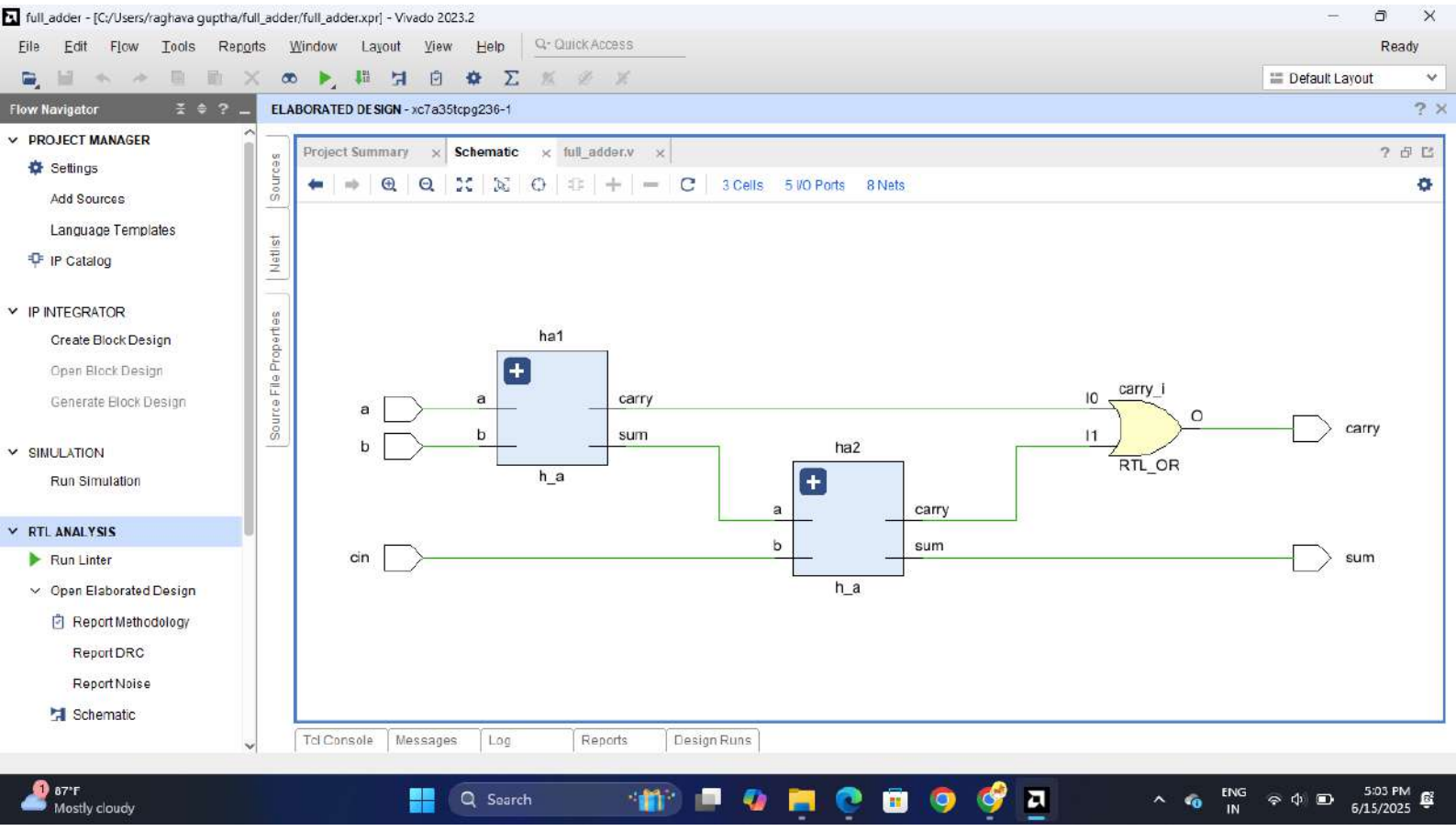
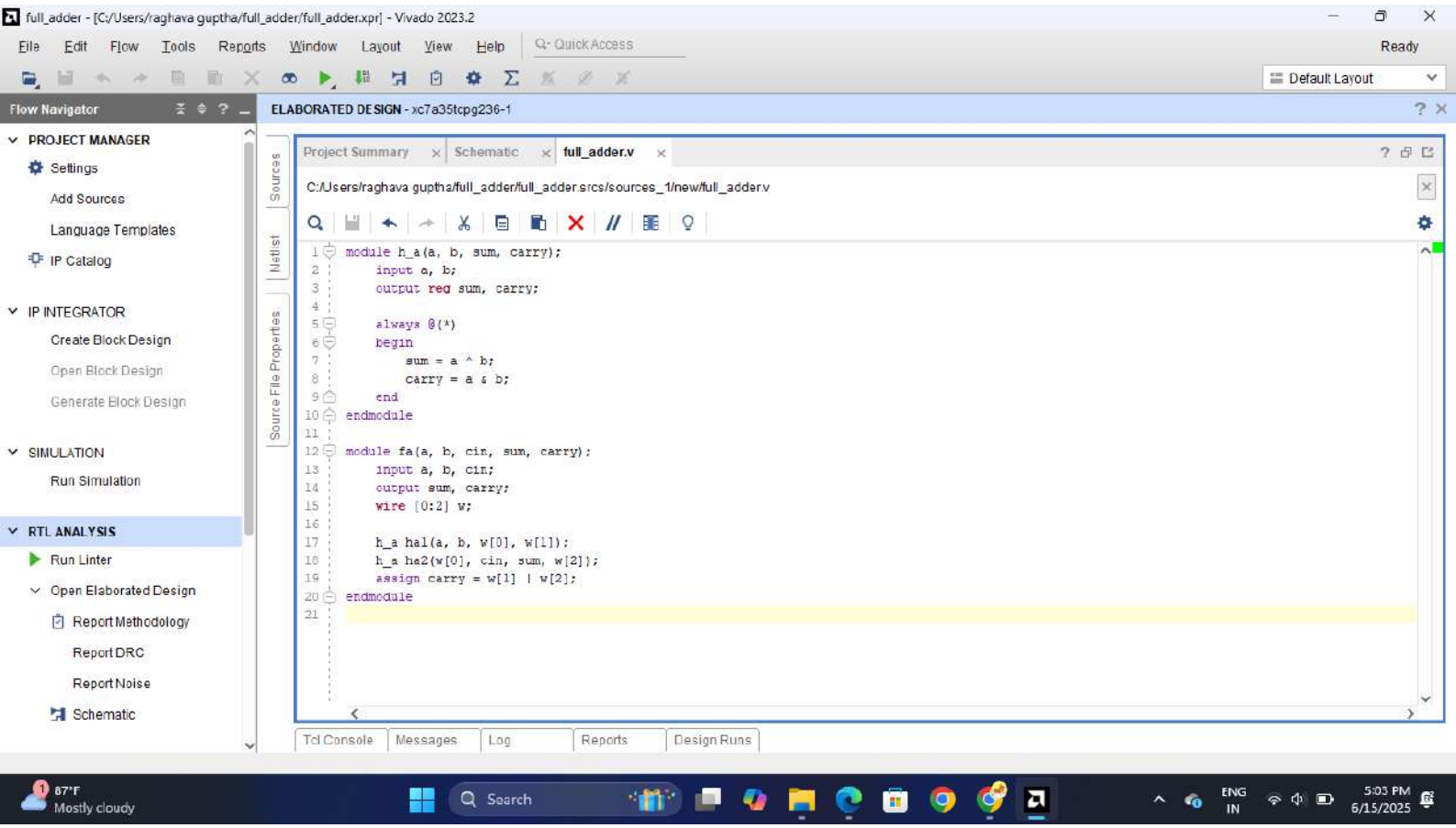
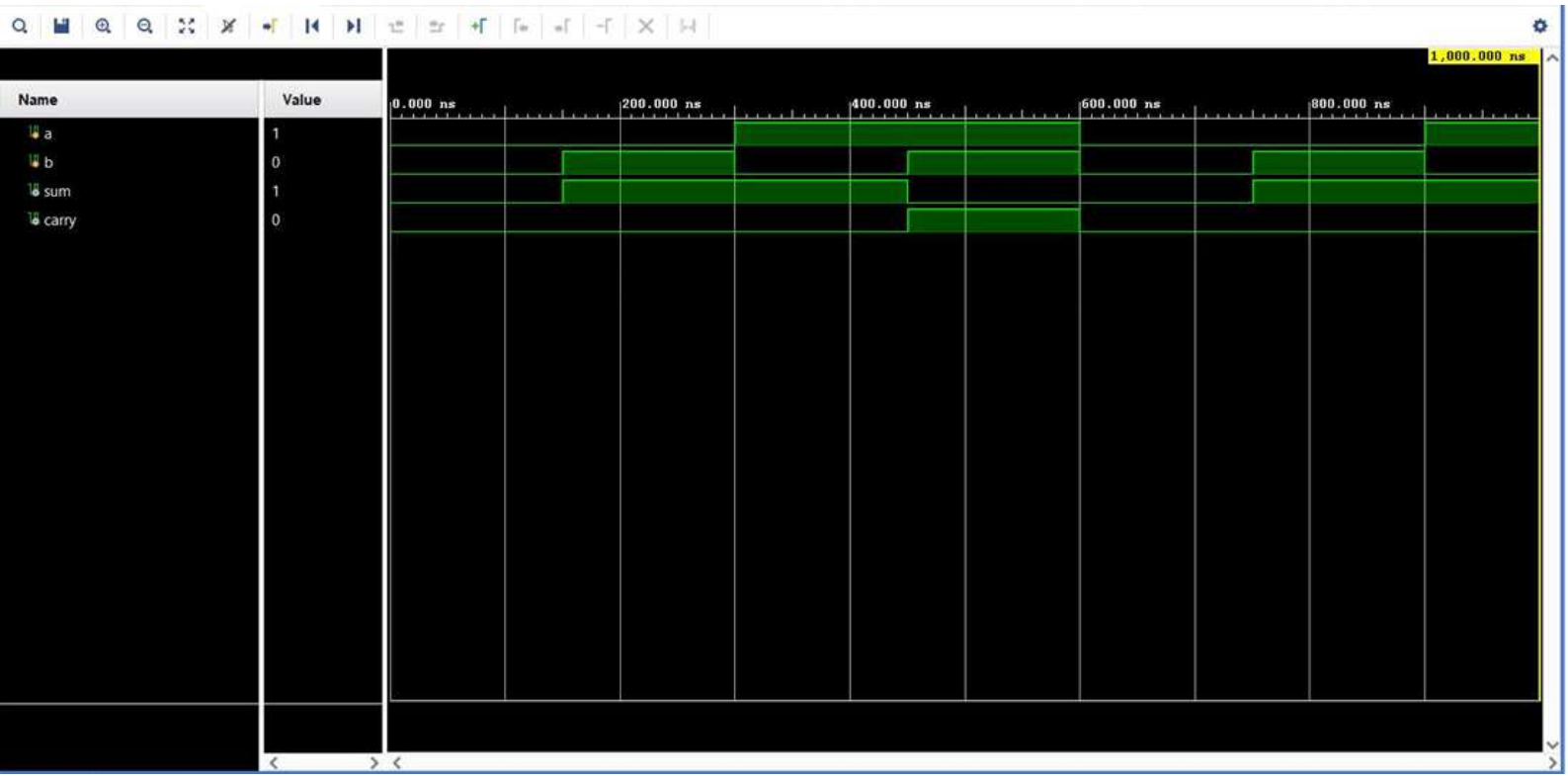
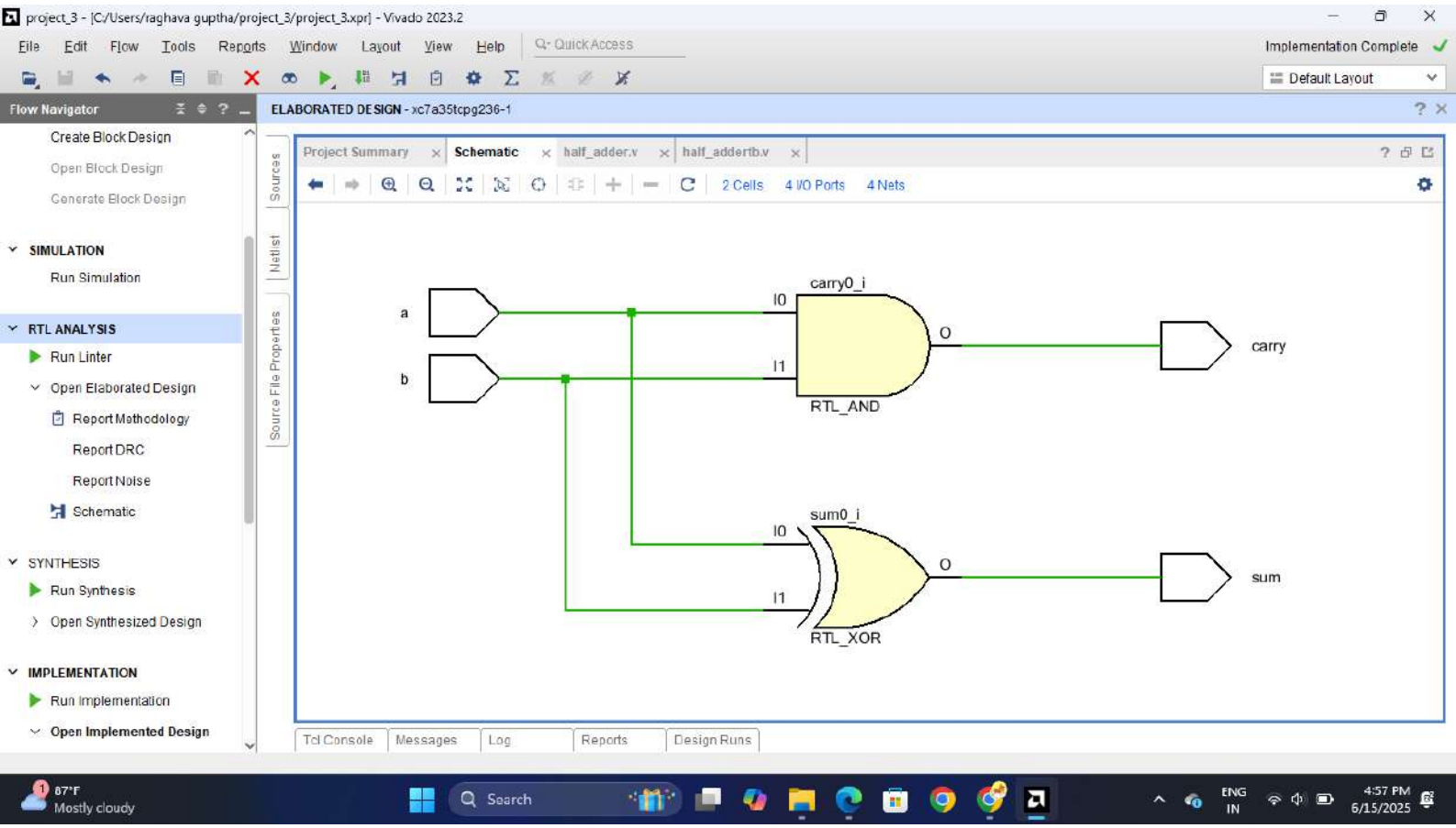
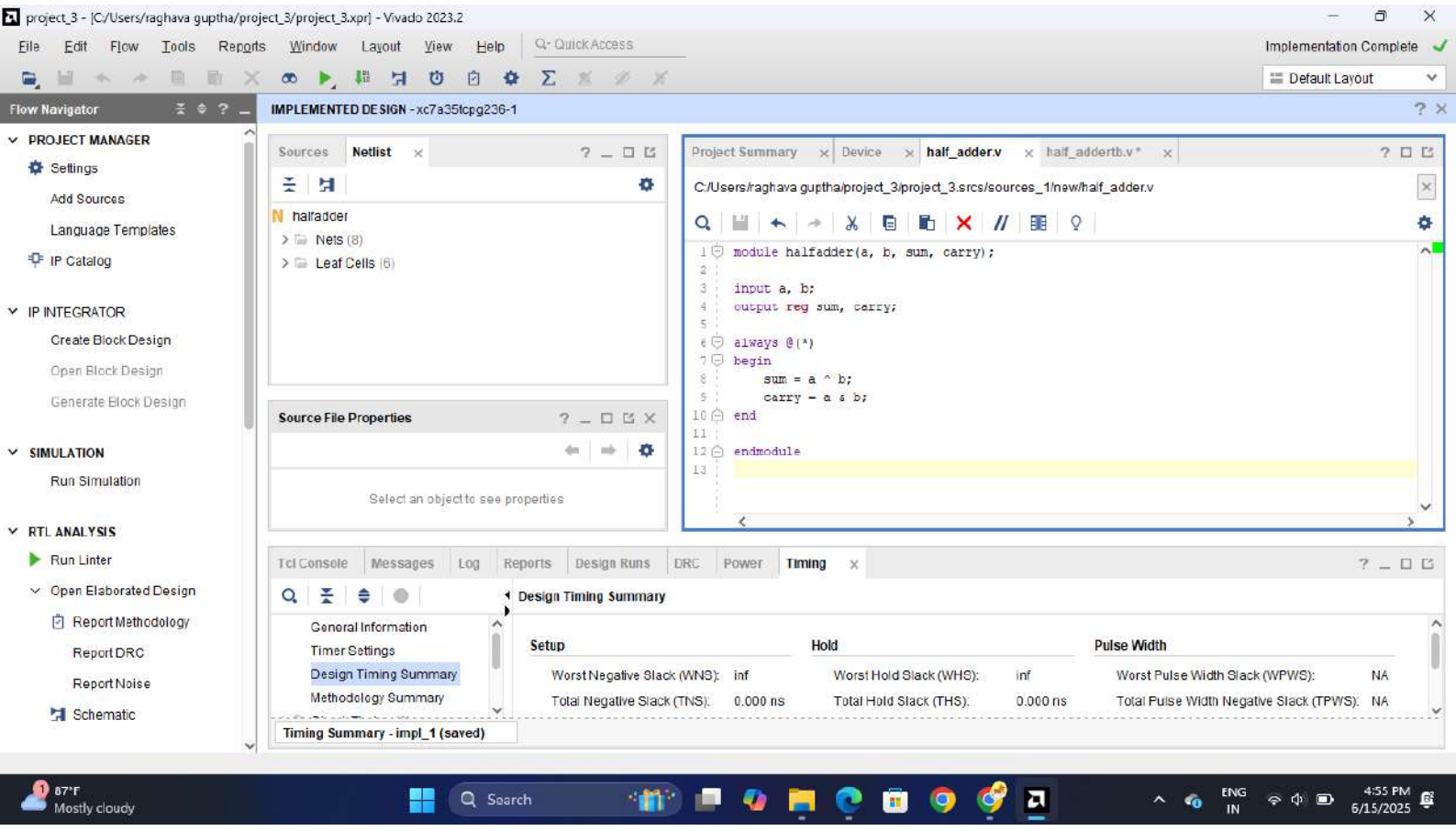

Name
Value
a
0
b
1
cin
0
sum
1
carry
0
0.000 ns
200.000 ns
400.000 ns
600.000 ns
800.000 ns
1,000.000 ns
1




full_adder - [C:/Users/raghava guptha/full_adder/full_adder.xpr] - Vivado 2023.2
File Edit Flow Tools Reports Window Layout View Help
Quick Access
Ready
Default Layout
Flow Navigator
PROJECT MANAGER
Settings
Add Sources
Language Templates
IP Catalog
IP INTEGRATOR
Create Block Design
Open Block Design
Generate Block Design
SIMULATION
Run Simulation
RTL ANALYSIS
Run Linter
Open Elaborated Design
Report Methodology
Report DRC
Report Noise
Schematic
ELABORATED DESIGN - xc7a35tcpg236-1
Project Summary
Schematic
full_adder.v
C:/Users/raghava guptha/full_adder/full_adder.srcs/sources_1/new/full_adder.v
Sources
Netlist
Source File Properties
1 module h_a(a, b, sum, carry);
2 input a, b;
3 output reg sum, carry;
4
5 always @(*)
6 begin
7 sum = a ^ b;
8 carry = a & b;
9 end
10 endmodule
11
12 module fa(a, b, cin, sum, carry);
13 input a, b, cin;
14 output sum, carry;
15 wire [0:2] w;
16
17 h_a ha1(a, b, w[0], w[1]);
18 h_a ha2(w[0], cin, sum, w[2]);
19 assign carry = w[1] | w[2];
20 endmodule
21
Tcl Console
Messages
Log
Reports
Design Runs
87°F
Mostly cloudy
Search
ENG
IN
5:03 PM
6/15/2025


Name
Value
a
1
b
0
sum
1
carry
0
0.000 ns
200.000 ns
400.000 ns
600.000 ns
800.000 ns
1,000.000 ns


project_3 - [C:/Users/raghava guptha/project_3/project_3.xpr] - Vivado 2023.2
File Edit Flow Tools Reports Window Layout View Help
Quick Access
Implementation Complete
Default Layout
Flow Navigator
ELABORATED DESIGN - xc7a35tcpg236-1
Create Block Design
Open Block Design
Generate Block Design
SIMULATION
Run Simulation
RTL ANALYSIS
Run Linter
Open Elaborated Design
Report Methodology
Report DRC
Report Noise
Schematic
SYNTHESIS
Run Synthesis
Open Synthesized Design
IMPLEMENTATION
Run Implementation
Open Implemented Design
Sources
Netlist
Source File Properties
Project Summary
Schematic
half_adder.v
half_addertb.v
2 Cells
4 I/O Ports
4 Nets
a
b
carry0_i
I0
I1
O
RTL_AND
carry
sum0_i
I0
I1
O
RTL_XOR
sum
Tcl Console
Messages
Log
Reports
Design Runs
87°F
Mostly cloudy
Search
ENG
IN
4:57 PM
6/15/2025


project_3 - [C:/Users/raghava guptha/project_3/project_3.xpr] - Vivado 2023.2
File Edit Flow Tools Reports Window Layout View Help
Quick Access
Implementation Complete
Default Layout
Flow Navigator
IMPLEMENTED DESIGN - xc7a35tcpg236-1
PROJECT MANAGER
Settings
Add Sources
Language Templates
IP Catalog
IP INTEGRATOR
Create Block Design
Open Block Design
Generate Block Design
SIMULATION
Run Simulation
RTL ANALYSIS
Run Linter
Open Elaborated Design
Report Methodology
Report DRC
Report Noise
Schematic
Sources
Netlist
halfadder
Nets (8)
Leaf Cells (6)
Source File Properties
Select an object to see properties
Project Summary
Device
half_adder.v
half_addertb.v *
C:/Users/raghava guptha/project_3/project_3.srcs/sources_1/new/half_adder.v
1 module halfadder(a, b, sum, carry);
2
3 input a, b;
4 output reg sum, carry;
5
6 always @(*)
7 begin
8 sum = a ^ b;
9 carry = a & b;
10 end
11
12 endmodule
13
Tcl Console
Messages
Log
Reports
Design Runs
DRC
Power
Timing
Design Timing Summary
General Information
Timer Settings
Design Timing Summary
Methodology Summary
Setup
Worst Negative Slack (WNS): inf
Total Negative Slack (TNS): 0.000 ns
Hold
Worst Hold Slack (WHS): inf
Total Hold Slack (THS): 0.000 ns
Pulse Width
Worst Pulse Width Slack (WPWS): NA
Total Pulse Width Negative Slack (TPWS): NA
Timing Summary - impl_1 (saved)
87°F
Mostly cloudy
Search
ENG
IN
4:55 PM
6/15/2025