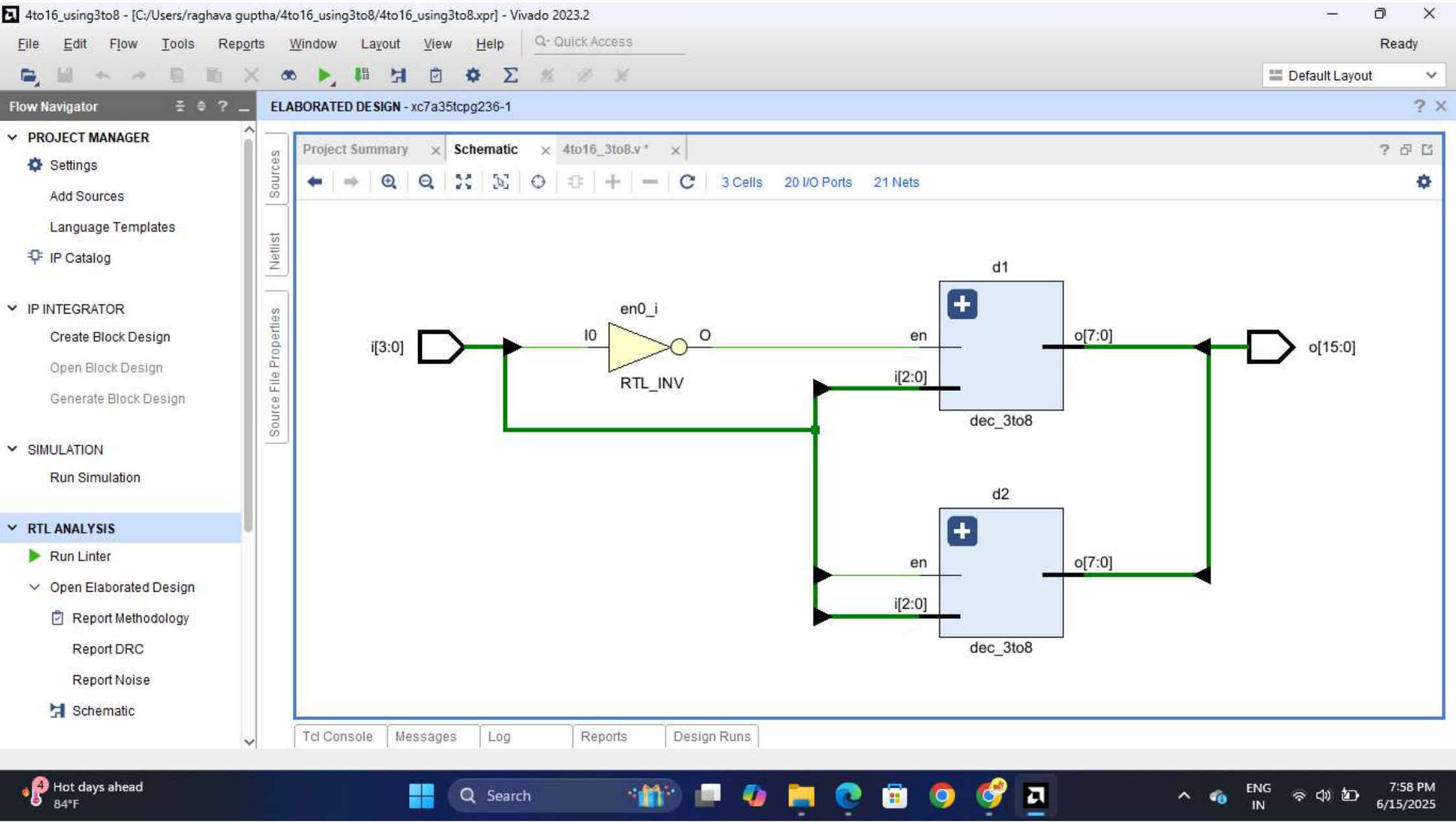
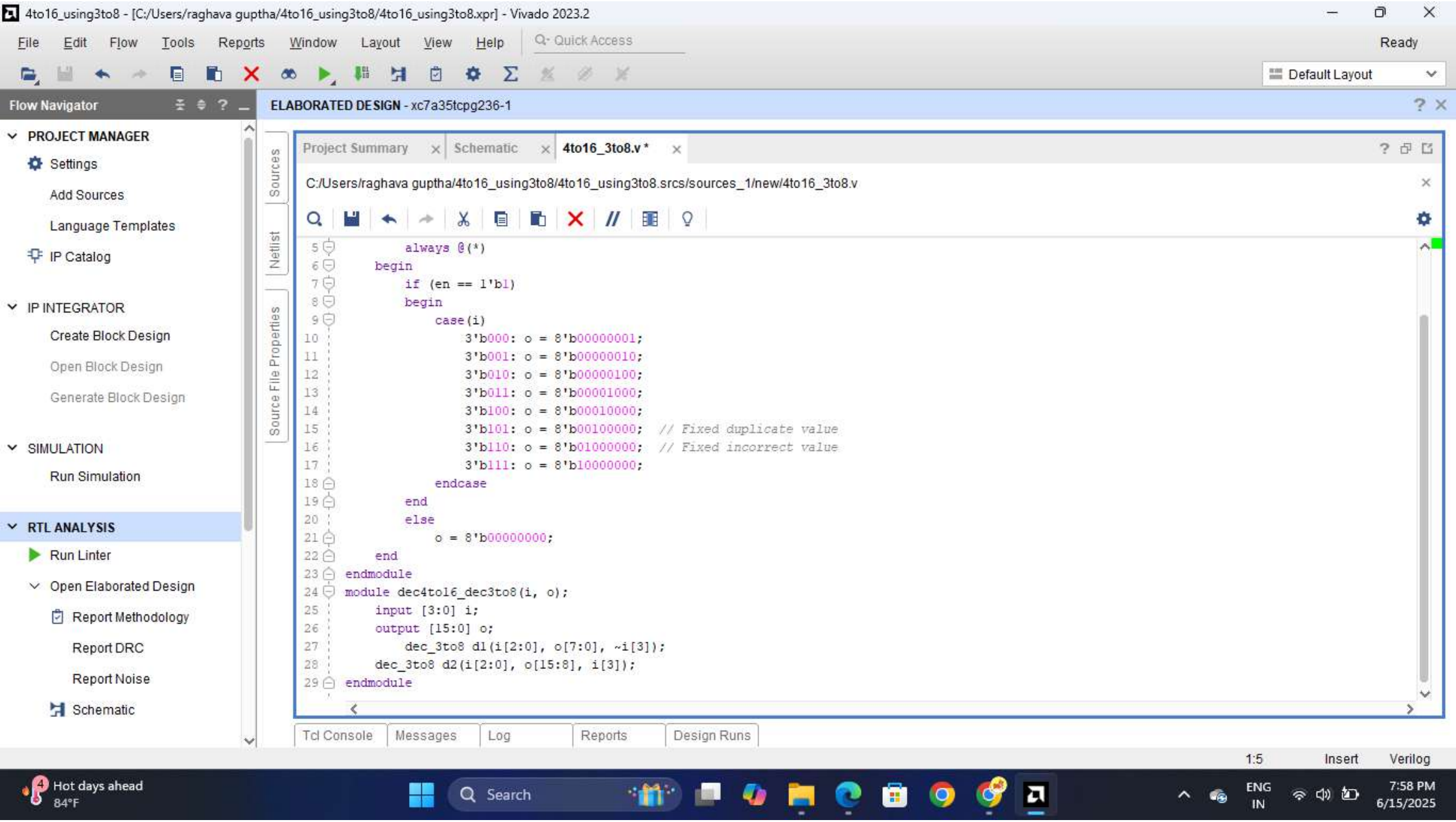

0.000 ns
Name
Value
i[3:0]
0
o[15:0]
0001
[15]
0
[14]
0
[13]
0
[12]
0
[11]
0
[10]
0
[9]
0
[8]
0
[7]
0
[6]
0
[5]
0
[4]
0
[3]
0
[2]
0
[1]
0
[0]
1
0.000 ns
200.000 ns
400.000 ns
600.000 ns
800.000 ns
1,000.000 ns
1,200.000 ns
1,400.000 ns
0 1 2 3 4 5 6 7 8 9 a b c d e f
0001 0002 0004 0008 0010 0020 0040 0080 0100 0200 0400 0800 1000 2000 4000 8000


4to16_using3to8 - [C:/Users/raghava guptha/4to16_using3to8/4to16_using3to8.xpr] - Vivado 2023.2
File Edit Flow Tools Reports Window Layout View Help
Quick Access
Ready
Default Layout
Flow Navigator
PROJECT MANAGER
Settings
Add Sources
Language Templates
IP Catalog
IP INTEGRATOR
Create Block Design
Open Block Design
Generate Block Design
SIMULATION
Run Simulation
RTL ANALYSIS
Run Linter
Open Elaborated Design
Report Methodology
Report DRC
Report Noise
Schematic
ELABORATED DESIGN - xc7a35tcpg236-1
Sources
Netlist
Source File Properties
Project Summary
Schematic
4to16_3to8.v *
3 Cells
20 I/O Ports
21 Nets
i[3:0]
en0_i
I0
O
RTL_INV
d1
en
i[2:0]
o[7:0]
dec_3to8
o[15:0]
d2
en
i[2:0]
o[7:0]
dec_3to8
Tcl Console
Messages
Log
Reports
Design Runs
Hot days ahead
84°F
Search
ENG
IN
7:58 PM
6/15/2025


4to16_using3to8 - [C:/Users/raghava guptha/4to16_using3to8/4to16_using3to8.xpr] - Vivado 2023.2
File Edit Flow Tools Reports Window Layout View Help
Quick Access
Ready
Default Layout
Flow Navigator
PROJECT MANAGER
Settings
Add Sources
Language Templates
IP Catalog
IP INTEGRATOR
Create Block Design
Open Block Design
Generate Block Design
SIMULATION
Run Simulation
RTL ANALYSIS
Run Linter
Open Elaborated Design
Report Methodology
Report DRC
Report Noise
Schematic
ELABORATED DESIGN - xc7a35tcpg236-1
Sources
Netlist
Source File Properties
Project Summary
Schematic
4to16_3to8.v *
C:/Users/raghava guptha/4to16_using3to8/4to16_using3to8.srcs/sources_1/new/4to16_3to8.v
5 always @(*)
6 begin
7 if (en == 1'b1)
8 begin
9 case(i)
10 3'b000: o = 8'b00000001;
11 3'b001: o = 8'b00000010;
12 3'b010: o = 8'b00000100;
13 3'b011: o = 8'b00001000;
14 3'b100: o = 8'b00010000;
15 3'b101: o = 8'b00100000; // Fixed duplicate value
16 3'b110: o = 8'b01000000; // Fixed incorrect value
17 3'b111: o = 8'b10000000;
18 endcase
19 end
20 else
21 o = 8'b00000000;
22 end
23 endmodule
24 module dec4to16_dec3to8(i, o);
25 input [3:0] i;
26 output [15:0] o;
27 dec_3to8 d1(i[2:0], o[7:0], ~i[3]);
28 dec_3to8 d2(i[2:0], o[15:8], i[3]);
29 endmodule
Tcl Console
Messages
Log
Reports
Design Runs
1:5
Insert
Verilog
Hot days ahead
84°F
Search
ENG
IN
7:58 PM
6/15/2025

4to16_using3to8 - [C:/Users/raghava guptha/4to16_using3to8/4to16_using3to8.xpr] - Vivado 2023.2

File Edit Flow Tools Reports Window Layout View Help Quick Access Ready

Default Layout

Flow Navigator

PROJECT MANAGER
- Settings
- Add Sources
- Language Templates
- IP Catalog

IP INTEGRATOR
- Create Block Design
- Open Block Design
- Generate Block Design

SIMULATION
- Run Simulation

RTL ANALYSIS
- Run Linter
- Open Elaborated Design
  - Report Methodology
  - Report DRC
  - Report Noise
  - Schematic

ELABORATED DESIGN - xc7a35tcpg236-1

Sources | Netlist | Source File Properties

Project Summary | Schematic | 4to16_3to8.v *

C:/Users/raghava guptha/4to16_using3to8/4to16_using3to8.srcs/sources_1/new/4to16_3to8.v

```
1  module dec_3to8(i, o, en);
2      input [2:0] i;
3      input en;
4      output reg [7:0] o;
5          always @(*)
6      begin
7          if (en == 1'b1)
8          begin
9              case(i)
10                 3'b000: o = 8'b00000001;
11                 3'b001: o = 8'b00000010;
12                 3'b010: o = 8'b00000100;
13                 3'b011: o = 8'b00001000;
14                 3'b100: o = 8'b00010000;
15                 3'b101: o = 8'b00100000;  // Fixed duplicate value
16                 3'b110: o = 8'b01000000;  // Fixed incorrect value
17                 3'b111: o = 8'b10000000;
18             endcase
19         end
20         else
21             o = 8'b00000000;
22     end
23 endmodule
24 module dec4to16_dec3to8(i, o);
25     input [3:0] i;
```

input

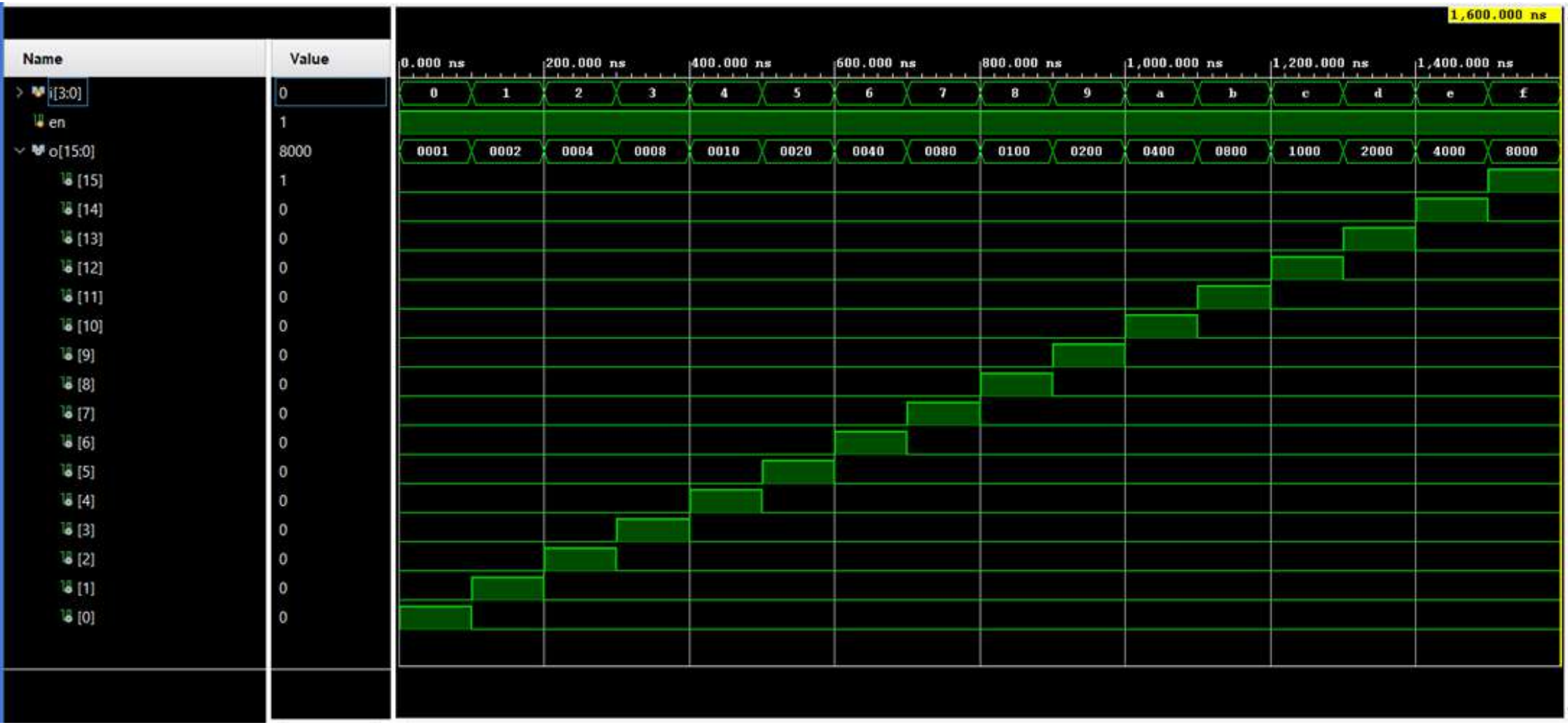
Tcl Console | Messages | Log | Reports | Design Runs

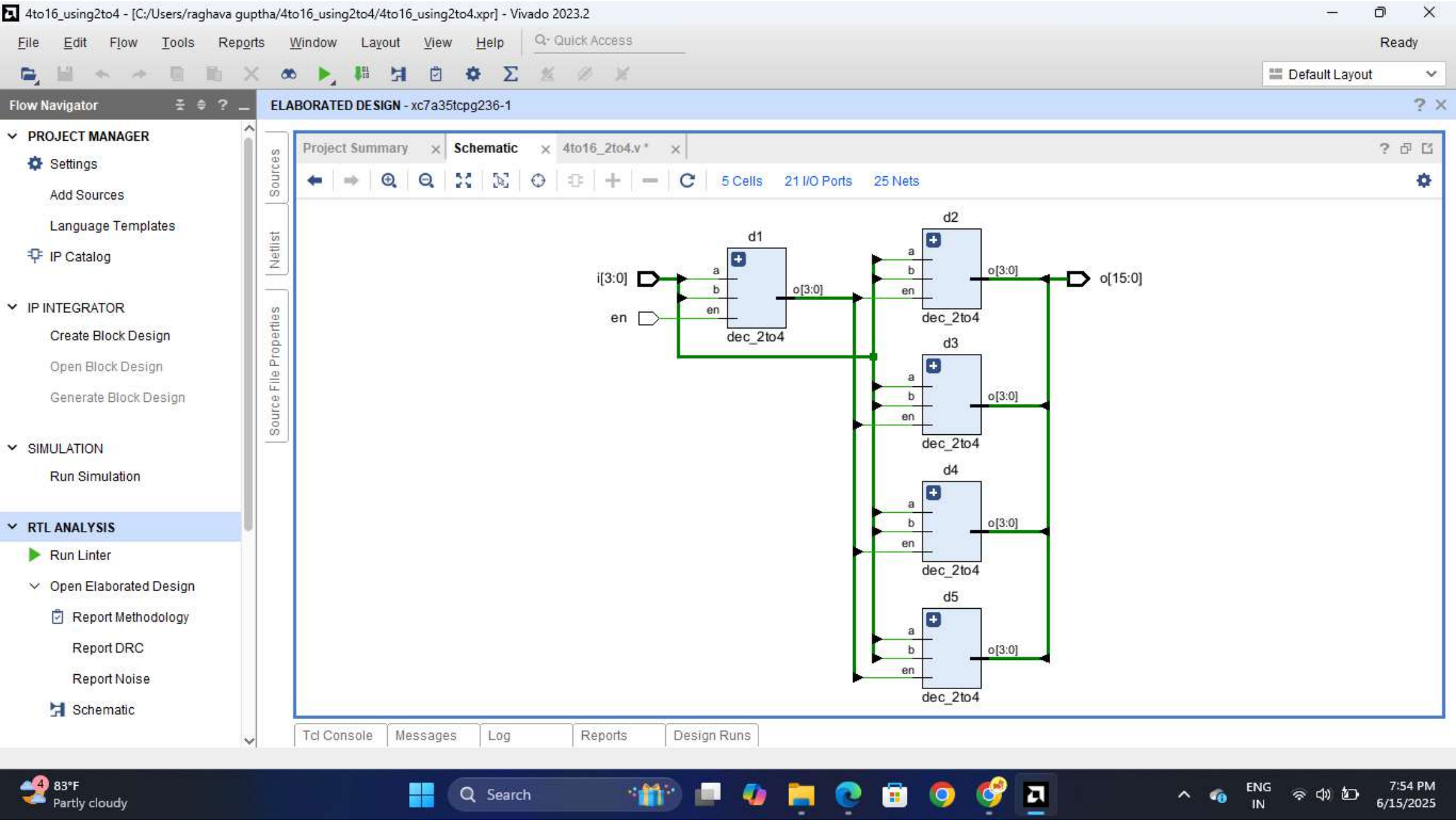
1:5 Insert Verilog

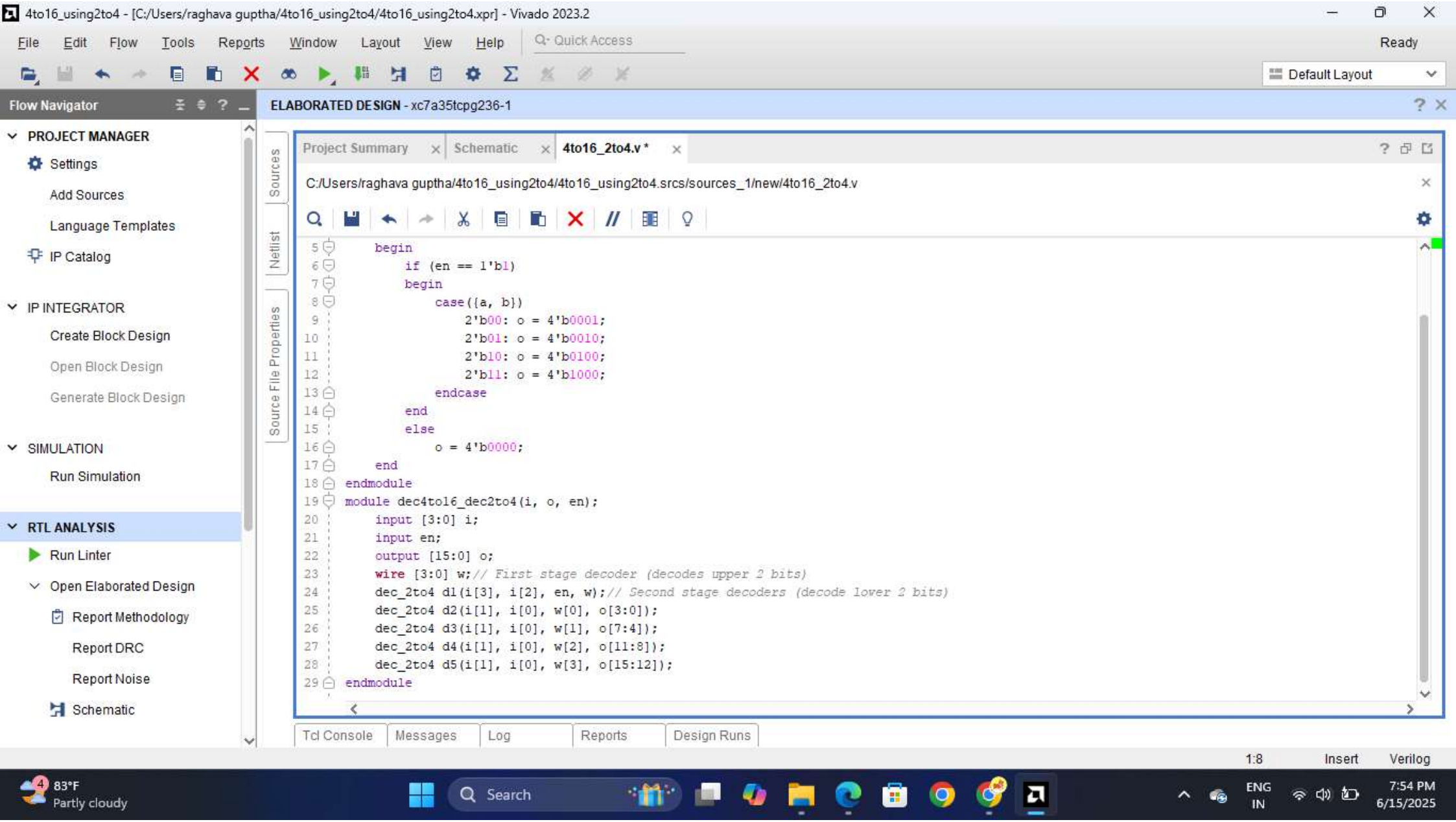
Hot days ahead 84°F

Search

ENG IN 7:58 PM 6/15/2025


Name
Value
i[3:0]
0
en
1
o[15:0]
8000
[15]
1
[14]
0
[13]
0
[12]
0
[11]
0
[10]
0
[9]
0
[8]
0
[7]
0
[6]
0
[5]
0
[4]
0
[3]
0
[2]
0
[1]
0
[0]
0
1,600.000 ns
0.000 ns
200.000 ns
400.000 ns
600.000 ns
800.000 ns
1,000.000 ns
1,200.000 ns
1,400.000 ns
0 1 2 3 4 5 6 7 8 9 a b c d e f
0001 0002 0004 0008 0010 0020 0040 0080 0100 0200 0400 0800 1000 2000 4000 8000


4to16_using2to4 - [C:/Users/raghava guptha/4to16_using2to4/4to16_using2to4.xpr] - Vivado 2023.2
File Edit Flow Tools Reports Window Layout View Help
Quick Access
Ready
Default Layout
Flow Navigator
PROJECT MANAGER
Settings
Add Sources
Language Templates
IP Catalog
IP INTEGRATOR
Create Block Design
Open Block Design
Generate Block Design
SIMULATION
Run Simulation
RTL ANALYSIS
Run Linter
Open Elaborated Design
Report Methodology
Report DRC
Report Noise
Schematic
ELABORATED DESIGN - xc7a35tcpg236-1
Sources
Netlist
Source File Properties
Project Summary
Schematic
4to16_2to4.v *
5 Cells
21 I/O Ports
25 Nets
d1
d2
d3
d4
d5
i[3:0]
en
a
b
en
o[3:0]
o[15:0]
dec_2to4
Tcl Console
Messages
Log
Reports
Design Runs
83°F
Partly cloudy
Search
ENG
IN
7:54 PM
6/15/2025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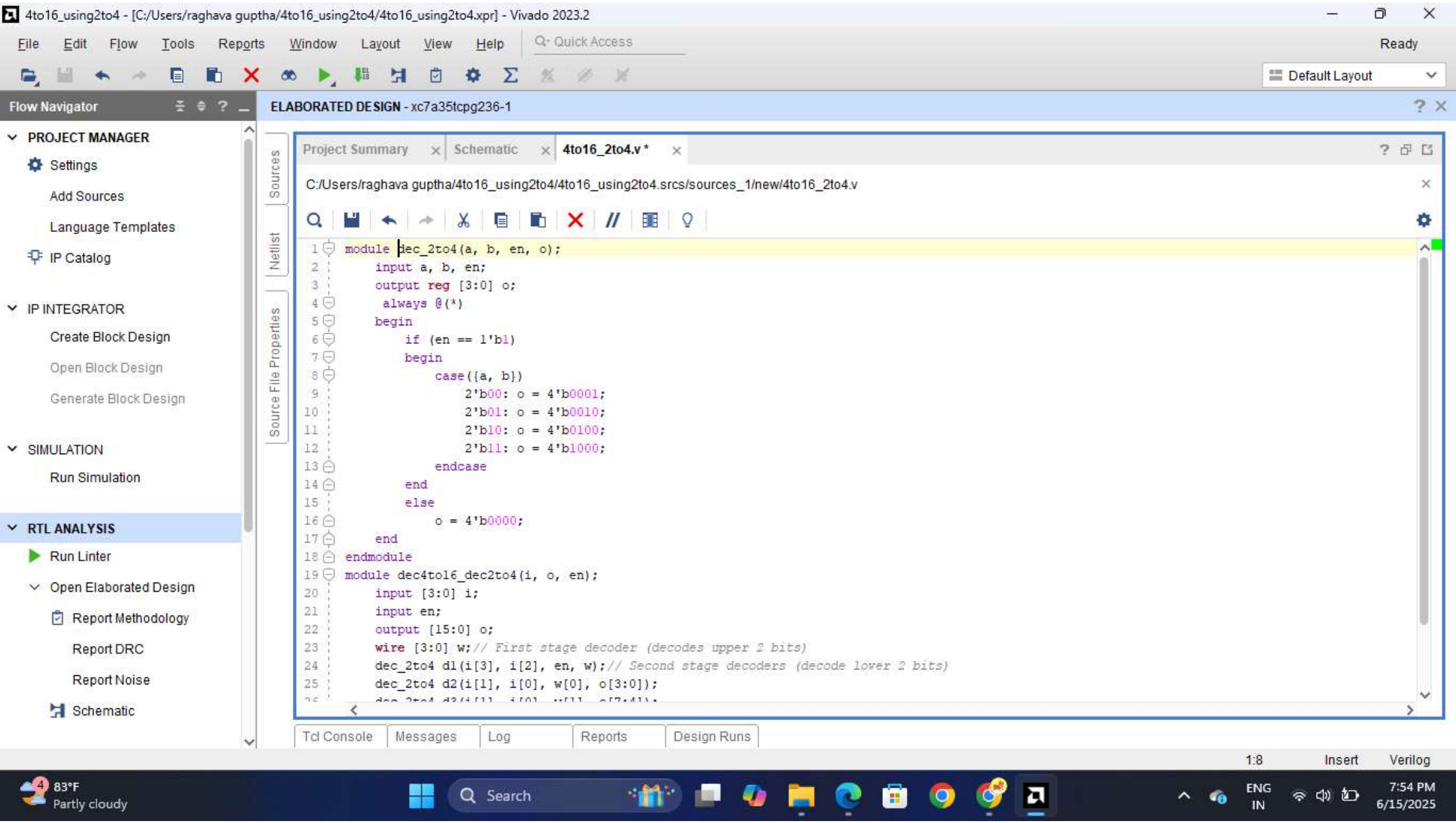
File Edit Flow Tools Reports Window Layout View Help
Quick Access
Ready
Default Layout
Flow Navigator
PROJECT MANAGER
Settings
Add Sources
Language Templates
IP Catalog
IP INTEGRATOR
Create Block Design
Open Block Design
Generate Block Design
SIMULATION
Run Simulation
RTL ANALYSIS
Run Linter
Open Elaborated Design
Report Methodology
Report DRC
Report Noise
Schematic
ELABORATED DESIGN - xc7a35tcpg236-1
Sources
Netlist
Source File Properties
Project Summary
Schematic
4to16_2to4.v *
C:/Users/raghava guptha/4to16_using2to4/4to16_using2to4.srcs/sources_1/new/4to16_2to4.v
5 begin
6 if (en == 1'b1)
7 begin
8 case({a, b})
9 2'b00: o = 4'b0001;
10 2'b01: o = 4'b0010;
11 2'b10: o = 4'b0100;
12 2'b11: o = 4'b1000;
13 endcase
14 end
15 else
16 o = 4'b0000;
17 end
18 endmodule
19 module dec4to16_dec2to4(i, o, en);
20 input [3:0] i;
21 input en;
22 output [15:0] o;
23 wire [3:0] w;// First stage decoder (decodes upper 2 bits)
24 dec_2to4 d1(i[3], i[2], en, w);// Second stage decoders (decode lower 2 bits)
25 dec_2to4 d2(i[1], i[0], w[0], o[3:0]);
26 dec_2to4 d3(i[1], i[0], w[1], o[7:4]);
27 dec_2to4 d4(i[1], i[0], w[2], o[11:8]);
28 dec_2to4 d5(i[1], i[0], w[3], o[15:12]);
29 endmodule
Tcl Console
Messages
Log
Reports
Design Runs
1:8
Insert
Verilog
83°F
Partly cloudy
Search
ENG
IN
7:54 PM
6/15/2025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File Edit Flow Tools Reports Window Layout View Help
Quick Access
Ready
Default Layout
Flow Navigator
PROJECT MANAGER
Settings
Add Sources
Language Templates
IP Catalog
IP INTEGRATOR
Create Block Design
Open Block Design
Generate Block Design
SIMULATION
Run Simulation
RTL ANALYSIS
Run Linter
Open Elaborated Design
Report Methodology
Report DRC
Report Noise
Schematic
ELABORATED DESIGN - xc7a35tcpg236-1
Sources
Netlist
Source File Properties
Project Summary
Schematic
4to16_2to4.v *
C:/Users/raghava guptha/4to16_using2to4/4to16_using2to4.srcs/sources_1/new/4to16_2to4.v
1 module dec_2to4(a, b, en, o);
2 input a, b, en;
3 output reg [3:0] o;
4 always @(*)
5 begin
6 if (en == 1'b1)
7 begin
8 case({a, b})
9 2'b00: o = 4'b0001;
10 2'b01: o = 4'b0010;
11 2'b10: o = 4'b0100;
12 2'b11: o = 4'b1000;
13 endcase
14 end
15 else
16 o = 4'b0000;
17 end
18 endmodule
19 module dec4to16_dec2to4(i, o, en);
20 input [3:0] i;
21 input en;
22 output [15:0] o;
23 wire [3:0] w;// First stage decoder (decodes upper 2 bits)
24 dec_2to4 d1(i[3], i[2], en, w);// Second stage decoders (decode lower 2 bits)
25 dec_2to4 d2(i[1], i[0], w[0], o[3:0]);
Tcl Console
Messages
Log
Reports
Design Runs
1:8
Insert
Verilog
83°F
Partly cloudy
Search
ENG
IN
7:54 PM
6/15/2025