VIGNAN's INSTITUTE OF INFORMATION TECHNOLOGY
(AUTONOMOUS)
(Approved by AICTE - New Delhi & Affiliated to JNTUGV, Vizianagaram)
Beside VSEZ, Duvvada, Vadlapudi Post, Gajuwaka, Visakhapatnam - 530 049.

A REPORT

On

INTERNSHIP

Name of the Student: Gogula Raghava Guptha

Name of the College: Vignan's Institute of Information Technology (A)

Registration Number: 22L31A0457

Period of Internship: 6 weeks (25-05-2025 to 10-07-2025)

Year: III B.Tech

Name and Address of the Intern Organization: Sense Semiconductor & It Solutions Pvt.Ltd, Mangalagiri,Guntur,Andhra Pradesh

An Internship Report

on

FPGA BASED VLSI DEGISN

Submitted in partial fulfilment of the requirements for the award of the degree of

Bachelor of Technology
In
Depart of Electronics and Communication Engineering

By

G. Raghava Guptha
(Roll No. 22L31A0457)

Under the Faculty Guidance of
DR. A.SAMPATH DAKSHINA MURTHY
Associate Professor

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

VIGNAN'S INSTITUTE OF INFORMATION TECHNOLOGY (A)

DUVVADA, VISAKHAPATNAM

JUNE, 2025

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Vignan's Institute of Information Technology (A)

Department of Electronics and Communication Engineering

Student Declaration

I, **G.Raghava Guptha**, am third-year student of Bachelor of Technology with Reg. No.: **22L31A0457** in the department of **Electronics and Communication Engineering (ECE)**, Vignan's Institute of Information Technology (A), Duvvada, Visakhapatnam. I hereby declare that the presented report of the internship titled "**FPGA BASED VLSI DESIGN**" is uniquely prepared by me after successful completion of a summer internship from 29-05-2025 to 12-06-2025 in **"Sense Semiconductor & It Solutions PVT LTD"** under the faculty guidance of **Dr. A.Sampath Dakshina Murthy**, Associate Professor, department of Electronics and Communication Engineering, Vignan's Institute of Information Technology (A), Duvvada, Visakhapatnam, during the academic year **2025**.

I also confirm that the report is only prepared for my academic requirement, not for any other purpose. It might not be used in the interest of the opposite party of the corporation.

G.Raghava Guptha

Regd. No.: 22L31A0457

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Department of Electronics and Communication Engineering

CERTIFICATE

This is to certify that **Gogula Raghava Guptha** bearing Regd. No. **22L31A0457** has completed the internship at **Sense Semiconductor & It Solutions Pvt.Ltd** on **"FPGA BASED VLSI DESIGN"** under the faculty guidance of **Dr. A.SAMPATH DAKSHINA MURTHY**, Associate Professor. He is also submitted the internship report to the department during the academic year **2024-25**, in partial fulfilment of the requirements for the award of the degree of Bachelor of Technology in the department of Electronics and communication Engineering, Vignan's Institute of Information Technology (A), Duvvada, Visakhapatnam.

Faculty Supervisor

Dr. A.Sampath Dakshina Murthy

Dept. Internship coordinator

Dr. M..Karuna.

Head of the Department
Dr. R.Uma Maheswari

ABSTRACT

Internships in FPGA-based VLSI (Very Large-Scale Integration) design offer invaluable hands-on experience, bridging the gap between academic learning and practical application. FPGA (Field-Programmable Gate Array) technology plays a vital role in modern VLSI systems, enabling rapid prototyping, custom hardware development, and efficient design verification across industries ranging from consumer electronics to aerospace and telecommunications. This abstract explores the significance, structure, and outcomes of internships in this specialized field.

Internships in FPGA-based VLSI are crucial for developing technical expertise and industry-ready skills. They provide students and aspiring professionals with real-world exposure, allowing them to apply theoretical knowledge to practical hardware design challenges. Interns gain insight into digital system design, hardware description languages (HDLs) like Verilog or VHDL, simulation, synthesis, and implementation on FPGA platforms — all of which are critical for advancing innovation in modern electronic systems.

In conclusion, internships in FPGA-based VLSI are a pivotal component of engineering education and career development. They offer a comprehensive learning experience that equips aspiring engineers with the skills and knowledge necessary to excel in the fast-evolving VLSI domain. Through hands-on projects and professional mentorship, interns are well-prepared to contribute to advancements in semiconductor technology and meet the growing demands of the electronics industry.

Acknowledgements

I would like to express my heartfelt gratitude to all those who supported and guided me throughout my internship journey.

First and foremost, I sincerely thank **Dr. A.SAMPATH DAKSHINA MURTHY,** Associate Professor, my internship mentor, for his consistent support in monitoring my daily attendance and weekly reports with patience and dedication.

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My sincere thanks to **Dr. M.Karuna**, Associate Professor and Department Internship Coordinator at Vignan's Institute of Information Technology, for offering continuous support and guidance in gathering information and assisting with the timely submission of reports.

I am also grateful to **Dr. R.Uma Maheswari**, Associate Professor and Head of the Department, Electronics and Communication Engineering, for providing essential information, advising me on suitable companies, and helping me analyze internship opportunities effectively.

I would like to sincerely acknowledge **Dr. A.Naga Jyothi**, Dean Academics, for her encouragement and support in facilitating academic coordination related to the internship program.

Lastly, I extend my special thanks to our respected Principal, **Dr. J.Sudhakar**, Professor, for granting me the opportunity to participate in this summer internship program and encouraging me to gain industrial knowledge and experience.

Contents

CHAPTER 1: EXECUTIVE SUMMARY

1.1 Learning Objectives:

The primary learning objectives of this internship were focused on bridging theoretical academic knowledge with practical industry applications in the field of FPGA-based VLSI Design. The key objectives were:

- To understand FPGA architecture, VLSI design flow, and hardware description languages (HDLs) like Verilog and VHDL.
- To develop proficiency in simulation, synthesis, and implementation tools such as Xilinx Vivado and ModelSim.
- To learn real-time problem-solving techniques in FPGA-based digital system design.
- To understand the professional workflow in the semiconductor industry, including documentation, reporting, and collaboration.
- To enhance communication, teamwork, and technical presentation skills in an engineering environment.

1.2 Outcomes Achieved:

By the end of the internship, the following outcomes were successfully achieved:

- Acquired strong foundational knowledge of FPGA-based digital circuit design and verification processes.
- Gained hands-on experience in writing, simulating, and debugging Verilog HDL code for digital systems.
- Implemented multiple digital modules such as counters, multiplexers, UART communication, and finite state machines (FSMs) on FPGA platforms.
- Learned how to utilize Xilinx Vivado and ModelSim for simulation, timing analysis, and synthesis.
- Developed a deeper understanding of industry standards in VLSI design, including constraints handling and optimization techniques.
- Improved professional communication, project reporting, and technical documentation skills.

1.3 Business Sector and Internship Organization:

The internship was completed in the Semiconductor and Electronics Industry, specifically focusing on VLSI Design and FPGA Prototyping. The organization,, specializes in delivering solutions in digital IC design, FPGA development, and embedded systems. It serves industries such as telecommunications, automotive, consumer electronics, and aerospace, contributing significantly to hardware innovation and system integration.

1.4 Overview of Activities:

During the internship, the following key activities were carried out:

- Studied FPGA architectures and design methodologies relevant to modern VLSI practices.
- Worked on hardware description languages (HDLs) to model digital systems.
- Designed and simulated digital circuits through *Verilog/VHDL* using industry-standard EDA tools.
- Performed synthesis, implementation, and hardware testing on FPGA development boards.
- Participated in verification and debugging of RTL designs to ensure functionality and timing accuracy.
- Contributed to technical documentation, project reports, and presentations as part of the team's workflow.
- Attended technical workshops and training sessions related to FPGA technologies and VLSI advancements.

CHAPTER 2: OVERVIEW OF THE ORGANIZATION

A. Introduction of the Organization

Sense Semiconductor & IT Solutions Pvt. Ltd is a leading company specializing in FPGA-based VLSI design and embedded systems solutions. The company focuses on delivering high-quality services in ASIC/FPGA design, digital system verification, embedded hardware development, and prototyping solutions for a wide range of industries including consumer electronics, automotive, aerospace, medical devices, and telecommunications. With expertise in advanced technologies and hardware development, the organization aims to bridge the gap between concept and silicon through reliable and efficient engineering practices.

B. Vision, Mission, and Values of the Organization

Vision:

To become a global leader in FPGA and VLSI-based technology solutions, fostering innovation and contributing to advancements in the electronics and semiconductor industries.

Mission:

- To deliver cutting-edge solutions in VLSI design and embedded systems.
- To offer reliable, high-performance hardware solutions aligned with customer requirements.
- To continuously invest in research, innovation, and employee development.

Core Values:

* Innovation and Excellence

* Integrity and Transparency

* Customer Satisfaction

* Commitment to Quality

* Teamwork and Continuous Learning

C. Policy of the Organization in Relation to the Intern Role

The organization believes in nurturing young engineering talent by offering structured internship programs. Interns are treated as part of the project teams and are provided with practical exposure to real-time FPGA/VLSI design projects. The policy focuses on hands-on learning, knowledge sharing, and professional mentorship to help interns transition from academic environments to industry-ready roles.

D. Organizational Structure

Typical Structure:

Board of Directors

|

Chief Executive Officer (CEO)

|

Technical Director / CTO

|

Project Managers / Design Leads

|

Senior Engineers / Verification Engineers

|

Junior Engineers / Interns / Trainees

The intern typically reports to the Design Lead or Senior Engineer, who assigns tasks, reviews progress, and provides technical guidance throughout the internship period.

E. Roles and Responsibilities of the Employees in which the Intern is Placed

The intern was placed within the FPGA/VLSI Design Team, whose key responsibilities include:

- Designing digital hardware systems using Verilog, VHDL, and related tools.
- Performing simulations, synthesis, and timing analysis for FPGA implementation.
- Debugging and verifying hardware modules on FPGA development boards.
- Collaborating with verification teams to ensure system-level compliance.
- Preparing technical reports and documentation for each project milestone.

The intern’s daily tasks aligned with these responsibilities under the guidance of senior engineers.

F. Performance of the Organization in Terms of Turnover, Profits, Market Reach, and Market Value

Sense Semiconductor & IT Solutions Pvt. Ltd has shown consistent growth in revenue and market recognition within the FPGA/VLSI sector.

Turnover: Approximately e.g., ₹X crores or \$X million annually.

Profitability: Steady year-on-year growth due to niche specialization in semiconductor solutions.

Market Reach: Active collaborations with clients from India, USA, Europe, and Asia-Pacific regions.

Market Value: Recognized as a reliable partner for innovative VLSI and FPGA-based solutions, contributing significantly to industries requiring high-performance digital systems.

G. Future Plans of the Organization

- To expand research capabilities in AI-integrated hardware solutions using FPGA and VLSI technologies.
- To develop IP cores for commercial use in specific industries like automotive and telecommunications.
- To strengthen global partnerships and enter new international markets.
- To enhance employee development through advanced training programs in next-generation semiconductor technologies.
- To focus on sustainable and energy-efficient hardware designs as part of future product offerings.

CHAPTER 3: INTERNSHIP PART

3.1 Details of Working Conditions

The internship was conducted in a professional office environment equipped with modern computing facilities and FPGA development tools. The workspace was well-organized and designed to promote focus and productivity, with access to technical resources, reference materials, and dedicated lab spaces for hardware testing.

- Working hours typically followed standard office timing: 9:30 AM to 5:30 PM.
- A dedicated workstation with all necessary software tools was provided.
- Interns had access to guidance from experienced engineers and team leads.
- Safety protocols and organizational policies were strictly followed within the premises.
- Opportunities were provided to attend technical discussions, review meetings, and knowledge-sharing sessions.

3.2 Weekly Work Schedule

Day	Activities
Monday	Design discussions, review of weekly objectives, project planning
Tuesday	Coding in Verilog/VHDL, simulations, debugging
Wednesday	Hardware implementation on FPGA boards, lab testing
Thursday	Verification processes, timing analysis, synthesis
Friday	Documentation, reporting, meetings with mentors
Saturday	Knowledge sessions, additional tasks, technical presentations (if applicable)
Sunday	Weekly holiday

3.3 Equipment Used

During the internship, the following tools, software, and equipment were utilized:

Hardware:

- Xilinx Spartan / Artix / Zynq FPGA development boards.
- Oscilloscopes and Logic Analyzers for signal verification.
- Power supplies, Multimeters for hardware testing.

Software Tools:

- Xilinx Vivado Design Suite (for synthesis, implementation, and simulation)
- ModelSim (for HDL simulation and debugging)
- Quartus Prime (if applicable)
- Git / SVN(for version control)
- Microsoft Office / Google Workspace* (for documentation and reporting)

3.4 Tasks Performed:

Throughout the internship period, the following key tasks and responsibilities were undertaken:

- Studied and understood the FPGA architecture and VLSI design flow.
- Wrote Verilog and VHDL code for various digital design modules such as counters, ALUs, multiplexers, and UARTs.
- Performed simulation, synthesis, and implementation of hardware designs using Xilinx Vivado and ModelSim.
- Conducted verification, debugging, and timing analysis to ensure accurate hardware functionality.
- Assisted in the development of testbenches for functional verification of digital circuits.
- Deployed designs on FPGA development boards and validated their real-time performance.
- Participated in team discussions on design strategies and optimization techniques.
- Prepared technical documentation, design reports, and project summaries as per industry standards.

ACTIVITY LOG FOR WEEK-1

Day	Date	Brief description of the daily activity	Learning Outcome	Person In-Charge Signature
Day-1	29-05-25	Introduction to VLSI design and **Verilog basics** (Module 1).	Understood fundamental Verilog constructs and design principles.	
Day-2	30-05-25	Designed and simulated basic logic gates and combinational circuits in Verilog (Module 1).	Gained hands-on experience in Verilog coding for simple combinational logic.	
Day-3	31-05-25	Explored dataflow and structural modeling for combinational designs (Module 1).	Developed proficiency in different Verilog modeling styles.	
Day-4	02-06-25	Implemented adders and subtractors using Verilog (Module 2).	Understood arithmetic circuit implementation in Verilog.	
Day-5	03-06-25	Designed and simulated multiplexers and demultiplexers (Module3).	Learned about MUX/DEMUX as universal logic.	
Day-6	04-06-25	Performed functional simulations of combinational circuits using **ModelSim**.	Gained initial experience with ModelSim for verifying Verilog designs.	

WEEKLY REPORT

WEEK – 1 (From Date: 29-05-2025 to Date: 04-06-2025)

Objective of the Activity Done:

To establish a strong foundation in Hardware Description Languages (HDLs) by learning Verilog constructs, combinational logic design, and basic simulation techniques. This week aimed at enabling the intern to translate digital circuit concepts into synthesizable Verilog code.

Detailed Report:

This week commenced with an in-depth introduction to FPGA-based VLSI design, company overview, and internship objectives. The initial focus was on mastering Module 1: Verilog Constructs and Combinational Design-I, covering fundamental Verilog syntax, data types, and operators. Practical sessions involved designing and simulating basic logic gates (AND, OR, NOT, XOR) and more complex combinational circuits like half-adders and full-adders. We explored different modeling styles: behavioral, dataflow, and structural, understanding their applications and advantages. Subsequently, Module 2: Verilog Constructs and Combinational Design-II was covered, which focused on advanced combinational circuit design, specifically the implementation of arithmetic circuits like adders and subtractors. The week concluded with Module 3: Multiplexers and Demultiplexers as Universal Logic and Realizations, where we designed and simulated MUX and DEMUX circuits, understanding their role in universal logic implementation. All designs were rigorously simulated using ModelSim to verify functional correctness, providing hands-on experience with industry-standard simulation tools.

ACTIVITY LOG FOR WEEK-2

Day	Date	Brief description of the daily activity	Learning Outcome	Person In-Charge Signature
Day-7	05-06-25	Designed and simulated encoders and decoders in Verilog (Module 4).	Understood encoder/decoder principles and implementation.	
Day-8	06-06-25	Learned about event queues and Verilog design guidelines for synthesis (Module5).	Improved Verilog coding practices for robust designs.	
Day-9	07-06-25	Designed and simulated basic flip-flops and latches in Verilog (Module 6).	Understood fundamental sequential logic elements.	
Day-10	09-06-25	Implemented synchronous and asynchronous counters using synthesizable Verilog (Module 7).	Developed skills in designing various counter types.	
Day-11	10-06-25	Designed and simulated shift registers at the RTL level (Module 8).	Understood shift register concepts and Verilog implementation.	
Day-12	11-06-25	Explored advanced shift register applications and refined simulation techniques (Module8).	Enhanced understanding of sequential circuit applications and debugging.	

WEEKLY REPORT

WEEK – 2 (From Date: 05-06-2025 to Date: 11-06-2025)

Objective of the Activity Done:

To advance understanding of digital design by learning sequential logic concepts, FSMs, and the RTL design of registers and counters, along with refining Verilog coding practices for robust and synthesizable designs.

Detailed Report:

Building upon the combinational logic foundation, this week transitioned into sequential circuit design. We started with Module 4: Decoders and Encoders and its Realizations, designing and simulating these critical combinational blocks. A significant portion of the week was dedicated to Module 5: Event Queue and Design Guidelines, where we delved into the intricacies of event-driven simulation and learned crucial synthesizable Verilog coding practices and design guidelines, essential for efficient hardware implementation. The core of the week involved Module 6: Basics of Sequential Design Using Verilog, where we designed and simulated fundamental memory elements like D-flip-flops and latches. This led into Module 7: Synchronous Counter and Asynchronous Counters Design Using Synthesizable Constructs, where we designed various types of counters (e.g., up/down counters, BCD counters) using synthesizable Verilog. The latter part of the week focused on Module 8: RTL Design of Shift Registers, where we implemented different types of shift registers (SISO, PISO, SIPO, PIPO) and explored their applications, further enhancing our RTL design capabilities. Simulations in ModelSim were integral for verifying the timing and functionality of these sequential circuits.

ACTIVITY LOG FOR WEEK-3

Day	Date	Brief description of the daily activity	Learning Outcome	Person In-Charge Signature
Day-13	12-06-25	Introduced to **Finite State Machines (FSMs)** and design principles (Module 9).	Understood FSM theory for control logic.	
Day-14	13-06-25	Designed and simulated a simple FSM in Verilog.	Gained practical experience in FSM implementation.	
Day-15	14-06-25	Understood **Datapath and Controller** separation in digital design (Module 10).	Learned about structural decomposition in complex designs.	
Day-16	16-06-25	Overview of **FPGA Architecture and Design Flow** using **Xilinx Vivado** (Module 11).	Understood the complete FPGA design process.	
Day-17	17-06-25	Performed **synthesis** of a Verilog design in Vivado.	Gained hands-on experience with the synthesis stage.	
Day-18	18-06-25	Learned **implementation (place and route)** and **bitstream generation** in Vivado.	Understood physical design mapping and FPGA programming.	

WEEKLY REPORT

WEEK – 3 (From Date: 12-06-2025 to Date: 18-06-2025)

Objective of the Activity Done:

To introduce the methodology of designing Finite State Machines (FSMs) for control logic, understand the architectural aspects of FPGAs, and gain initial hands-on experience with the complete FPGA design flow using industry-standard tools like Xilinx Vivado.

Detailed Report:

This week began with a comprehensive study of Module 9: Finite State Machines Using Verilog. We explored the principles of FSM design, including Mealy and Moore machine models, state encoding techniques, and state transition diagrams. Practical exercises involved designing and simulating simple FSMs for control logic, such as a sequence detector. Following this, Module 10: Datapath And Controller was covered, emphasizing the crucial architectural separation of data processing (datapath) and control logic (controller) in complex digital systems. A major highlight of the week was the introduction to Module 11: FPGA Architecture and Design Flow. We gained an overview of the internal structure of FPGAs (Configurable Logic Blocks, I/O Blocks, Routing Resources) and the complete FPGA design flow using the Xilinx Vivado Design Suite. Hands-on sessions with Vivado included performing synthesis of a small Verilog design to generate a gate-level netlist, and subsequently, learning about the implementation (place and route) process, which maps the design onto the physical FPGA fabric. The week concluded with the generation of a bitstream, the final file used to program the FPGA.

ACTIVITY LOG FOR WEEK-4

Day	Date	Brief description of the daily activity	Learning Outcome	Person In-Charge Signature
Day-19	19-06-25	Studied **Static Timing Analysis** and timing constraints (Module 12).	Understood the importance of timing for FPGA performance.	
Day-20	20-06-25	Performed timing analysis in Vivado and resolved basic timing issues.	Gained practical skills in analyzing and optimizing timing.	
Day-21	21-06-25	Explored **RAM and ROM Memories** and their integration in FPGAs (Module 13).	Learned about on-chip memory elements.	
Day-22	23-06-25	Began **FIFO Design and Implementation** as a case study (Module 14).	Understood the concept and need for FIFO buffers.	
Day-23	24-06-25	Designed and simulated a basic FIFO buffer in Verilog.	Gained hands-on experience in designing a practical data buffering circuit.	
Day-24	25-06-25	Final project review, report preparation, and presentation of the FIFO design.	Consolidated learning and enhanced technical communication skills.	

WEEKLY REPORT

WEEK – 4 (From Date:19-06-25 to Date: 25-06-25)

Objective of the Activity Done:

To understand crucial aspects of high-performance digital design, including static timing analysis, memory integration, and practical system-level design through a case study, culminating in the complete design and implementation of a complex digital component.

Detailed Report:

The final week focused on critical aspects of practical FPGA design. We delved into Module 12: Static Timing Analysis, understanding the importance of timing closure for reliable and high-speed operation. Key concepts like setup time, hold time, clock period, and timing constraints (SDC) were thoroughly discussed. Practical exercises in Vivado involved analyzing timing reports for previously synthesized designs and identifying and resolving basic timing violations. Next, Module 13: RAM And ROM Memories provided insights into different types of on-chip memories available in FPGAs (Block RAMs, Distributed RAMs) and their efficient utilization in Verilog designs. The culmination of the internship was Module 14: Case Study: FIFO Design and Implementation. We learned the fundamental concept and applications of First-In, First-Out (FIFO) buffers, critical for data synchronization and buffering between asynchronous domains. The major activity involved designing and simulating a complete FIFO buffer (including full/empty flags, write/read pointers) in Verilog. This comprehensive case study allowed us to integrate knowledge from all previous modules, from combinational and sequential logic to FSMs for control, and apply it within the full FPGA design flow. The week concluded with a final review of all learned concepts, preparation of the internship report, and a presentation of the implemented FIFO design.

CHAPTER 4: OUTCOMES DESCRIPTION

4.1 People Interactions

Throughout the internship, interaction with colleagues, mentors, and team leads was highly professional and collaborative. Senior engineers provided valuable guidance, especially in areas related to *FPGA design, verification, and debugging practices*. Regular meetings, discussions, and technical reviews allowed for open communication and knowledge sharing. The work environment encouraged asking questions, participating in problem-solving discussions, and learning through peer interaction.

Worked under the guidance of Senior FPGA Engineers and Project Leads.

Participated in weekly project reviews and technical discussions.

Collaborated with verification teams and hardware engineers to ensure smooth project execution.

4.2 Facilities Available and Maintenance

- The organization provided modern, well-maintained facilities that supported efficient learning and work:
- Dedicated workstations equipped with licensed software tools like Vivado, ModelSim, and Quartus.
- Access to FPGA development boards and necessary hardware testing equipment (oscilloscopes, logic analyzers, etc.).
- High-speed internet connectivity and access to internal knowledge repositories.
- A well-maintained lab environment for practical hardware testing with clean and organized setups.
- Regular maintenance ensured that all equipment remained functional and up-to-date.

4.3 Clarity of Job Roles

From the beginning of the internship, job roles and responsibilities were clearly communicated. The scope of work, expectations, timelines, and deliverables were outlined in alignment with the organization's project needs.

Clear understanding of daily and weekly objectives.

Defined responsibilities related to HDL coding, simulation, FPGA implementation, and documentation.

Regular feedback from supervisors helped align efforts with project goals.

4.4 Motivation

The internship environment was motivating and growth-oriented. Factors contributing to motivation included:

- Exposure to industry-relevant tools and real-world project challenges.
- Encouragement from mentors to explore, innovate, and learn independently.
- A structured environment that recognized efforts and provided constructive feedback.
- Opportunities to present work during internal reviews and technical sessions, which boosted confidence and technical communication skills.

4.5 Space and Ventilation

The workspace provided by the organization was well-planned with ample space, proper lighting, and ventilation to ensure a comfortable working environment:

- Separate workstations and lab areas with ergonomic furniture.
- Proper air conditioning and ventilation systems maintained a comfortable atmosphere.
- Clean and hygienic premises contributing to a productive work environment.

Describe the real time technical skills you have acquired (*in terms of the job-related skills and hands on experience)*

Real-Time Technical Skills Acquired

During my internship in **FPGA-based VLSI design**, I gained extensive practical experience and developed several job-related technical skills that have strengthened my capabilities as an aspiring VLSI engineer:

Digital System Design:

- Designed and implemented digital circuits and finite state machines for various applications.
- Understood trade-offs between area, speed, and power consumption in hardware designs.

Hardware Description Languages (HDLs):

- Gained proficiency in writing, testing, and debugging designs using **Verilog** (and/or VHDL).
- Developed modular, reusable code following industry best practices.

FPGA Toolchains and Platforms:

- Hands-on experience with FPGA development tools (e.g., Xilinx Vivado, Quartus Prime).
- Performed synthesis, place-and-route, timing analysis, and bitstream generation.
- Implemented and tested designs on FPGA boards, observing and validating real-time hardware behavior.

Simulation and Verification:

- Created testbenches to verify functionality before deployment.
- Used simulation tools to debug and validate designs against specifications.

Rapid Prototyping:

- Translated design specifications into working prototypes on FPGA.
- Iteratively improved designs based on simulation results and real hardware testing.

Industry Practices and Documentation:

- Learned professional design flow, including version control, requirement analysis, and design documentation.
- Understood IP integration and reuse within complex systems.

Team Collaboration:

- Collaborated with mentors and peers to debug challenging issues.
- Participated in code reviews and design discussions, improving both technical and communication skills.

Describe the managerial skills you have acquired (*in terms of planning, leadership, team work, behaviour, workmanship, productive use of time, weekly improvement in competencies, goal setting, decision making, performance analysis, etc.*

Managerial Skills Acquired

During my internship, I developed a range of managerial and professional skills that complemented my technical growth and prepared me for industry roles:

Planning and Goal Setting:

- Broke down complex design tasks into manageable milestones.
- Set short-term weekly targets aligned with overall project timelines, ensuring steady progress.

Leadership and Initiative:

- Took the lead in small project components, guiding peers in debugging and design decisions.
- Shared knowledge about HDL coding practices and FPGA tool usage with team members.

Teamwork and Collaboration:

- Worked closely with fellow interns and mentors to achieve common goals.
- Learned to communicate ideas clearly, listen to feedback, and adjust designs based on team input.

Behaviour and Professionalism:

- Maintained a positive, solution-focused attitude even when faced with design challenges.
- Practiced punctuality, accountability, and respect within the workplace.

Workmanship and Attention to Detail:

- Ensured code and documentation met industry standards for clarity and maintainability.
- Conducted thorough reviews to catch errors early, improving overall design quality.

Productive Use of Time:

- Prioritized tasks effectively, focusing on critical path activities.
- Balanced learning new concepts with delivering tangible results each week.

Weekly Improvement in Competencies:

- Reflected on weekly performance to identify areas for improvement, such as refining Verilog coding style or enhancing simulation skills.
- Actively sought feedback to continuously elevate design quality and efficiency.

Decision Making and Problem Solving:

- Made informed design choices by weighing trade-offs between area, speed, and power.
- Used simulation results and testing data to guide design revisions.

Performance Analysis:

- Regularly reviewed project metrics and personal progress to ensure alignment with goals.
- Documented lessons learned and best practices to improve future project phases.

Describe how you could improve your communication skills (*in terms of improvement in oral communication, written communication, conversational abilities, confidence levels while communicating, anxiety management, understanding others, getting understood by others, extempore speech, ability to articulate the key points, closing the conversation, maintaining niceties and protocols, greeting, thanking and appreciating others, etc.,)*

Oral Communication and Conversational Abilities:

- Practice speaking clearly and confidently during meetings and technical discussions.
- Engage in group discussions and presentations to become more comfortable expressing ideas aloud.

Written Communication:

- Focus on writing concise, well-structured reports, design documentation, and emails.
- Learn to adapt writing style for different audiences, from technical peers to non-technical stakeholders.

Confidence Levels and Anxiety Management:

- Participate in mock presentations and team briefings to build speaking confidence.
- Use relaxation techniques and thorough preparation to reduce nervousness before speaking.

Understanding Others and Being Understood:

- Improve active listening skills by giving full attention, asking clarifying questions, and summarizing others' points to confirm understanding.
- Use simple, clear language to ensure my own ideas are conveyed accurately.

Extempore Speech and Articulation:

- Practice speaking on impromptu topics to develop spontaneity and fluency.
- Learn to quickly outline key points mentally to keep communication organized and focused.

Closing Conversations and Maintaining Niceties:

- Be mindful to end discussions professionally by summarizing action items and next steps.
- Remember to greet colleagues appropriately, thank them for their contributions, and acknowledge their ideas.

Greeting, Thanking, and Appreciating Others:

- Cultivate the habit of showing appreciation during team work, which helps build a positive environment.
- Use polite language and respectful tone consistently, whether in emails or face-to-face communication.

Describe how you could enhance your abilities in group discussions, participation in teams, contribution as a team member, leading a team/activity.

To enhance my abilities in group discussions, team participation, and leadership, I plan to work on several key areas. First, I aim to participate more actively in discussions by preparing in advance, researching relevant topics, and expressing my ideas clearly and confidently. At the same time, I want to become a better listener who pays close attention to others' viewpoints and builds constructively on them. As a team member, I intend to take initiative by volunteering for tasks that match my skills while remaining ready to support teammates in other areas as needed. I believe sharing knowledge, offering constructive feedback, and being open to feedback myself will strengthen collaboration and improve team outcomes. To work effectively within a group, I will focus on communicating openly and respectfully, adapting to different working styles, and recognizing each member's strengths to encourage balanced participation. As I take on opportunities to lead, I aim to set clear

goals, delegate tasks thoughtfully, and motivate team members through positive reinforcement and open dialogue. Guiding discussions to stay focused on objectives while making sure everyone feels heard will also be a priority. Finally, I plan to observe experienced leaders, reflect on my own performance, and seek feedback from peers and mentors to continuously improve my teamwork and leadership skills. Through these efforts, I hope to become a more confident, effective, and supportive participant and leader in any team setting.

Describe the technological developments you have observed and relevant to the subject area of training *(focus on digital technologies relevant to your job role)*

During my internship in FPGA-based VLSI design, I observed several significant technological developments that are reshaping the field of digital design and semiconductor engineering. One of the most notable trends is the rapid evolution of FPGA architectures, including the integration of high-speed transceivers, hardened processor cores, and AI/ML acceleration blocks, which allow for more powerful and versatile hardware designs. Advances in high-level synthesis (HLS) tools have also made it easier to translate algorithmic descriptions directly into optimized hardware, significantly reducing development time. In addition, the growing adoption of system-on-chip (SoC) FPGA platforms has enabled designers to combine programmable logic with embedded processors, supporting complex applications in real-time signal processing, edge computing, and communications. I also noticed improvements in simulation and verification tools, such as more accurate timing analysis and formal verification, which help detect design errors earlier and increase reliability. The shift towards hardware/software co-design, where FPGA logic is closely integrated with software running on embedded processors, further highlights the need for engineers to be proficient in both hardware description languages like Verilog/VHDL and software development tools. Together, these developments are enabling faster prototyping, higher design efficiency, and the creation of more complex, high-performance digital systems—trends that are highly relevant to modern roles in VLSI design and embedded systems engineering.

Internship Completion Certificate, Photo with geo tag

Photo with Internal Mentor:

Certificate:

SENSE SEMICONDUCTOR & IT SOLUTIONS PVT. LTD.
Mangalagiri, Andhra Pradesh
An ISO 9001:2015 Certified Organization

CERTIFICATE
OF INTERNSHIP

This is to Certify that

Mr./Ms

GOGULA RAGHAVA GUPTHA

with ID No. 22L31A0457 From Vignan's Institute of information technology,

Has successfully completed Summer Internship Program - 2025 in the domain of FPGA BASED VLSI DESIGN

from 25-05-2025 to 10-07-2025. During the program he/she demonstrated a strong understanding of the trainning modules. He/She actively participated & completed Hands-on industry projects & displayed excellent problem-solving skills, strong communication abilities, & dedication towards project completion. This certificate is awarded in recognition of his/her commitment to professional development & successful completion of the Internship.

P. Tejeswara
Internship Mentor
SSIT Solutions Pvt. Ltd.

Certificate No.
SSIT-2025- 2380

HRD Manager
SSIT Solutions Pvt. Ltd.

Recognized by:

Date of Certification:
09-07-2025

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