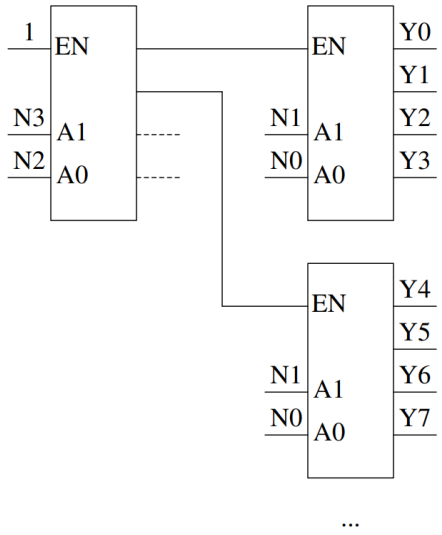
HOMEWORK 8 SOLUTIONS

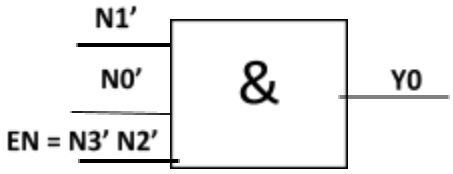
1.

4-to-16 binary decoder using 2-to-4 binary decoders:

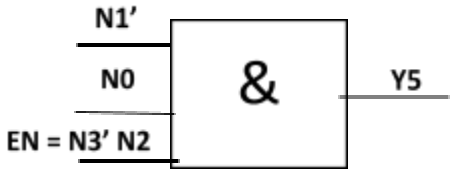


Based on internal structure of the 2-to-4 decoders used:

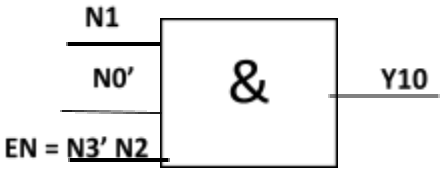
Y0 = N3' N2' N1' N0'



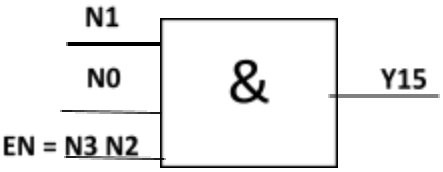
Y5 = N3' N2 N1' N0



Y10 = N3’ N2 N1 N0’



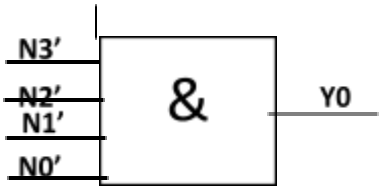
Y15 = N3 N2 N1 N0



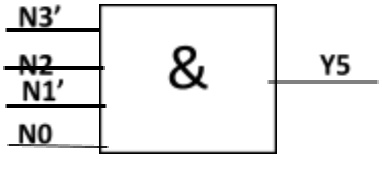
Based on internal structure of the 4-to-16 decoders used:

(Here EN = 1)

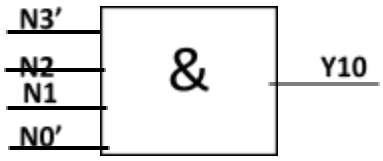
Y0 = N3’ N2’ N1’ N0’



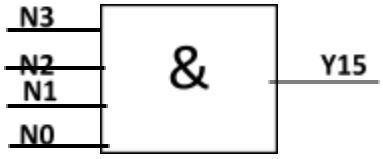
Y5 = N3’ N2 N1’ N0



Y10 = N3’ N2 N1 N0’

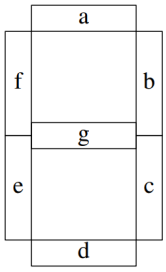


Y15 = N3 N2 N1 N0



2.

Reference 7-segment display:



Here are some examples: (Truth table can include any 4 capital letters)

A

C

E

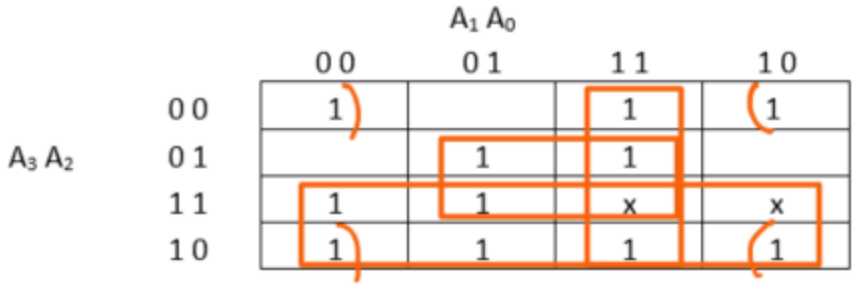
F

Truth table:

digit/alphabet	A_3	A_2	A_1	A_0	Ya	Yb	Yc	Yd	Ye	Yf	Yg
0	0	0	0	0	1	1	1	1	1	1	0
1	0	0	0	1	0	1	1	0	0	0	0
2	0	0	1	0	1	1	0	1	1	0	1
3	0	0	1	1	1	1	1	1	0	0	1
4	0	1	0	0	0	1	1	0	0	1	1
5	0	1	0	1	1	0	1	1	0	1	1
6	0	1	1	0	0	0	1	1	1	1	1
7	0	1	1	1	1	1	1	0	0	0	0
8	1	0	0	0	1	1	1	1	1	1	1
9	1	0	0	1	1	1	1	0	0	1	1
A	1	0	1	0	1	1	1	0	1	1	1
C	1	0	1	1	1	0	0	1	1	1	0
E	1	1	0	0	1	0	0	1	1	1	1
F	1	1	0	1	1	0	0	0	1	1	1
-	1	1	1	0	x	x	x	x	x	x	x
-	1	1	1	1	x	x	x	x	x	x	x

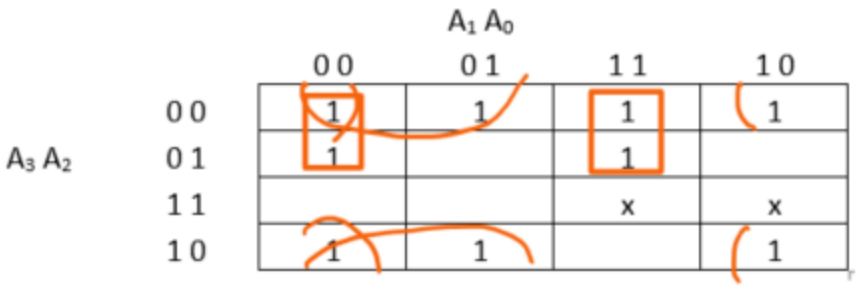
Logical Expression two output functions: (Logical expressions for any 2 Ys are sufficient.)

Y_a :



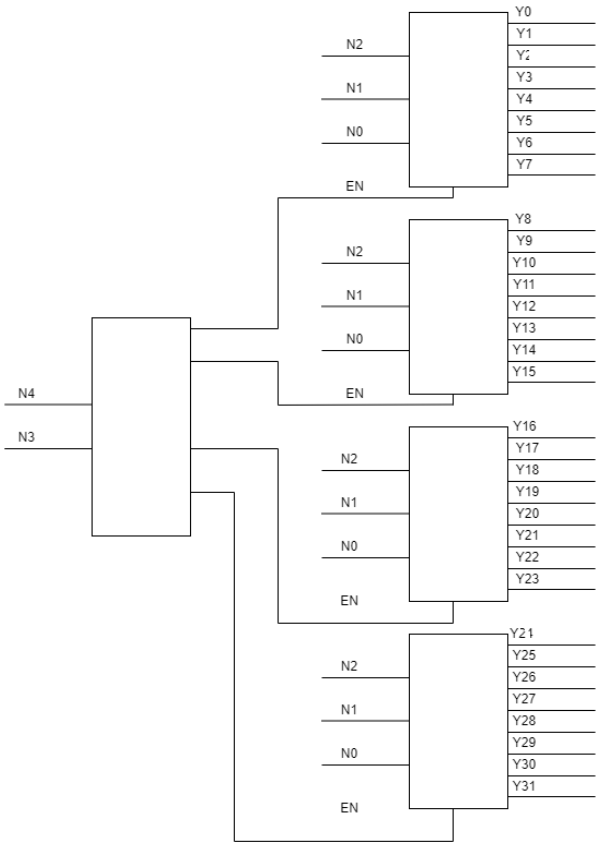
$Y_a = A_3 + A_2\,A_0 + A_1\,A_0 + A_2'\,A_0'$

Y_b :

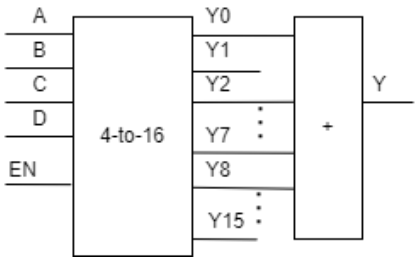


$Y_b = A_2'\,A_1' + A_2'\,A_0' + A_3'\,A_1\,A_0' + A_3'\,A_1\,A_0$

3.


N4
N3
N2
N1
N0
EN
Y0
Y1
Y2
Y3
Y4
Y5
Y6
Y7
Y8
Y9
Y10
Y11
Y12
Y13
Y14
Y15
Y16
Y17
Y18
Y19
Y20
Y21
Y22
Y23
Y25
Y26
Y27
Y28
Y29
Y30
Y31

4.


A
B
C
D
EN
4-to-16
Y0
Y1
Y2
Y7
Y8
Y15
+
Y

5.

Decoder is a digital circuit with ‘n’ inputs and 2^n outputs.

Demultiplexer is a digital circuit with 1 input, ‘n’ address lines and 2^n outputs.

Demultiplexer can be made using a decoder with following connections:

The input signal of the demultiplexer can be connected to the enable signal of the decoder and the ‘n’ address lines of the demultiplexer can be connected to the inputs of the decoder.

6.

Let I15 I14 … I0 be the input signals to the 16-to-4 encoder,

Let Y3 Y2 Y1 Y0 be the output signals of the 16-to-4 encoder

Y0 = I1 + I3+ I5+ I7 + I9 + I11 + I13 + I15

Y1 = I2 + I3 + I6 + I7 + I10 + I11 + I14 + I15

Y2 = I4 + I5 + I6 + I7 + I12 + I13 + I14 + I15

Y3 = I8 + I9 + I10 + I11 + I12 + I13 + I14 + I15

Let I31 I30 … I0 be the input signals to the 32-to-5 encoder,

Let Y4 Y5 Y3 Y2 Y1 Y0 be the output signals of the 32-to-5 encoder,

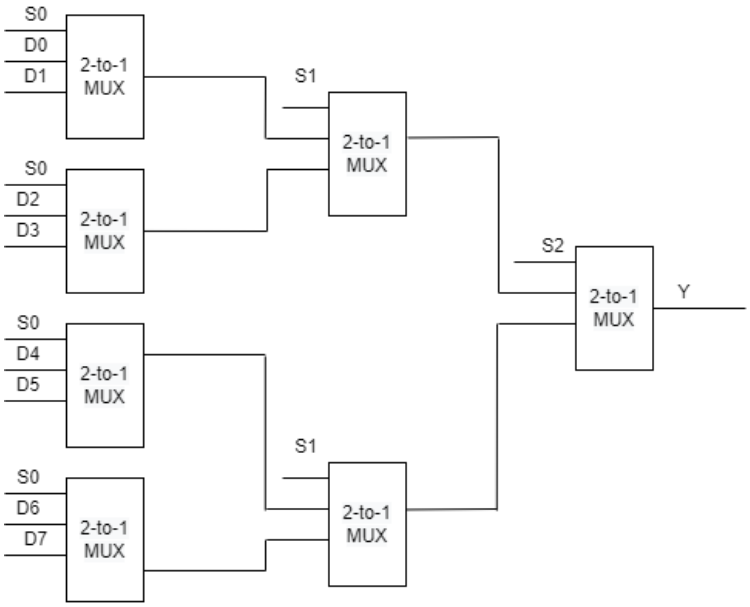
Y0 = I1 + I3+ I5+ I7 + I9 + I11 + I13 + I15 + I17 + I19 + I21 + I23 + I25 + I27 + I29 + I31

Y1 = I2 + I3 + I6 + I7 + I10 + I11 + I14 + I15 + I18 + I19 + I22 + I23 + I26 + I27 + I30 + I31

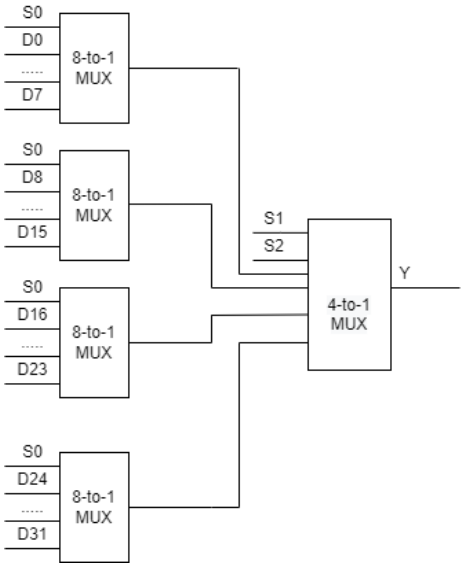
Y2 = I4 + I5 + I6 + I7 + I12 + I13 + I14 + I15 + I20 + I21 + I22 + I23 + I28 + I29 + I30 + I31

Y3 = I8 + I9 + I10 + I11 + I12 + I13 + I14 + I15 + I24 + I25 + I26 + I27 + I28 + I29 + I30 + I31

7.


S0
D0
D1
2-to-1 MUX
S0
D2
D3
2-to-1 MUX
S0
D4
D5
2-to-1 MUX
S0
D6
D7
2-to-1 MUX
S1
2-to-1 MUX
S1
2-to-1 MUX
S2
2-to-1 MUX
Y

8.


S0
D0
.....
D7
8-to-1 MUX
S0
D8
.....
D15
8-to-1 MUX
S0
D16
.....
D23
8-to-1 MUX
S0
D24
.....
D31
8-to-1 MUX
S1
S2
4-to-1 MUX
Y

9.

Let the 3 input signals be A, B, C

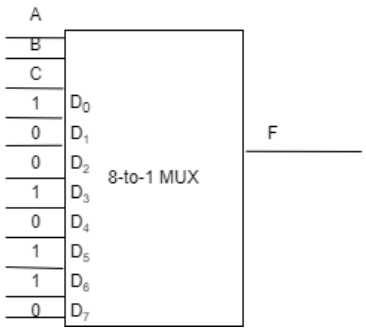
$S_2 = A$

$S_1 = B$

$S_0 = C$

F = ABC' + AB'C + A'BC + A'B'C'

- $D_0 = D_3 = D_5 = D_6 = 1$, $D_1 = D_2 = D_4 = D_7 = 0$



10.

F = PQ'R' + P'QR'

F will be logic high only if I0, I1 of M2 are logic high and are selected by select signals R, S. Hence R, S can be 00 or 01. This implies R needs to be logic low.

For I0, I1 of M2 to be logic high, P, Q need to select I1 or I2 of M1. Hence PQ can be 01 or 10.

Hence F = PQ'R' + P'QR'.