ECE 27000 Introduction to Digital System Design
Spring 2022
Exam 3, April 21, 2022

S O L U T I O N

Last Name: _____ First Name: _____

Purdue ID: _____

Lab Section (Number or Day and Time): _____

As a boilermaker pursuing academic excellence, I pledge to be honest and true in all that I do. Accountable together - we are Purdue.

I certify that I have neither given nor received unauthorized aid on this exam.

Signed: _____

Solve the following problems. The number of points for each problem is shown in the table below.

Use only the space provided to solve each problem, and copy the answers to the space marked "Answer:..."

Problem	Outcome	Points
1	3,4	/ 20
2	3	/ 20
3	4	/ 20
4	4	/ 20
5	3	/ 20
Total		/ 100

Problem 1

Design a state table for a finite-state machine with the following specification.
The finite-state machine has two inputs, X_1 and X_2, and one output, Z.
The input sequence on X_1 represents a binary number N_1 with the least-significant bit appearing first. Similarly, the input sequence on X_2 represents a binary number N_2 with the least-significant bit appearing first.
The output Z should represent the arithmetic sum $N_1 + N_2$ (the carry-out does not show up on the output).
For example, the following input and output sequences may be obtained.

X_1	0	1	0	1	1	0	0	0
X_2	0	0	1	1	1	1	0	0
Z	0	1	1	0	1	0	1	0

Name the initial state of the machine A, and additional states (if needed) B, C, $\cdots$.

Answer (state table):

			S*,Z		
meaning	S	X1X2=00	01	10	11
carry in 0	A	A,0	A,1	A,1	B,0
carry in 1	B	A,1	B,0	B,0	B,1

Problem 2

Apply state minimization to the following state table. Show the subsets of equivalent states, and find a reduced state table.

	S*,Z	
S	X=0	X=1
S0	S0,1	S1,0
S1	S1,0	S2,0
S2	S2,0	S3,1
S3	S3,1	S4,0
S4	S4,0	S5,0
S5	S5,0	S3,1

Name the states of the reduced machine A, B, C, $\cdots$, using as many states as needed.

Answer (equivalent states, and reduced state table):

P0=(S0,S1,S2,S3,S4,S5)

P1=(S0,S3)(S1,S4)(S2,S5)

P2:

S0,S3$\xrightarrow{0}$S0,S3; S0,S3$\xrightarrow{1}$S1,S4

S1,S4$\xrightarrow{0}$S1,S4; S1,S4$\xrightarrow{1}$S2,S5

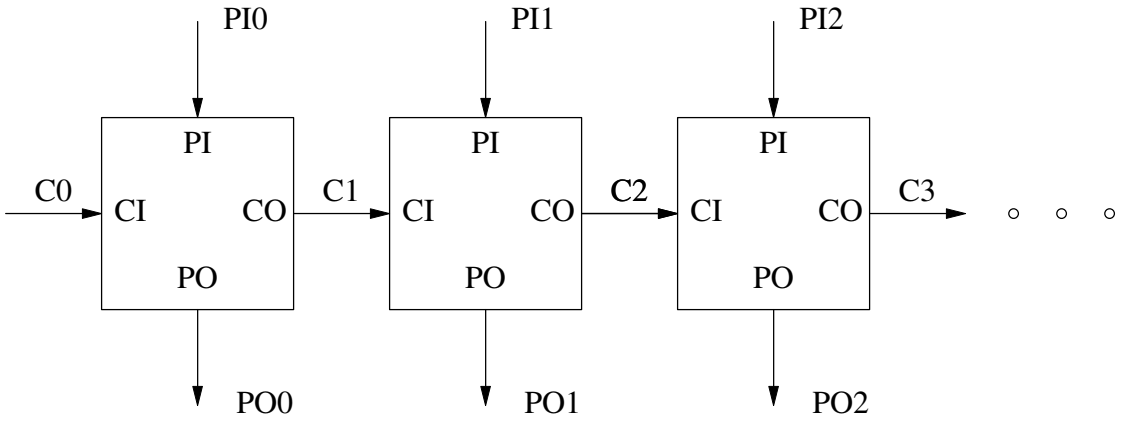
S2,S5$\xrightarrow{0}$S2,S5; S2,S5$\xrightarrow{1}$S3,S3

P2=P1

		S*,Z	
	S	X=0	X=1
S0,S3	A	A,1	B,0
S1,S4	B	B,0	C,0
S2,S5	C	C,0	A,1

Problem 3

Show the truth table of a basic building block in an iterative circuit that has the structure below and the following functionality.
The primary input $PI_i = X_i$ is bit i of an n-bit number X.
There are no primary outputs. The outputs of the iterative circuit are the cascading outputs of logic block $n - 1$.
The iterative circuit computes the number of 1's in X modulo 4 (the result is the remainder of division by 4).
For example, with $n = 8$, $X = 10110110$ has five 1's, and five modulo 4 is equal to one.
Note that the figure is that of a general iterative circuit. It is not specific to this problem, and it does not show numbers of primary inputs, primary outputs, cascading inputs, or cascading outputs.



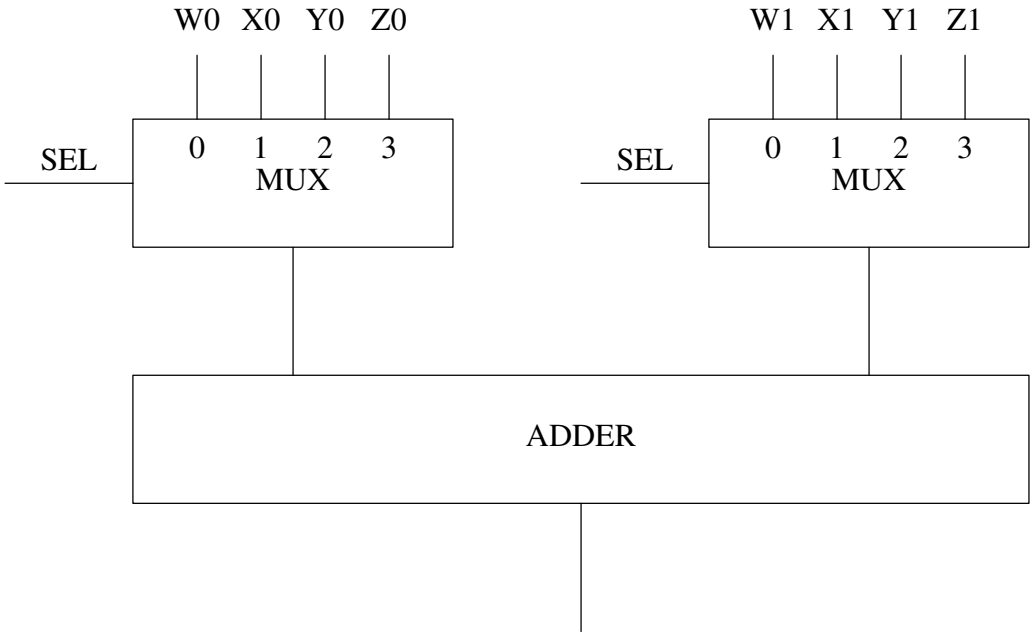
Answer (truth table of a basic building block):

Xi	Ci1	Ci0	C(i+1)1	C(i+1)0	X0...Xi mod 4
0	0	0	0	0	0
0	0	1	0	1	1
0	1	0	1	0	2
0	1	1	1	1	3
1	0	0	0	1	1
1	0	1	1	0	2
1	1	0	1	1	3
1	1	1	0	0	0

Problem 4

A 32-bit ADDER is available. The ADDER needs to be used for computing one of four possible arithmetic sums. The possible operands are 32-bit numbers called W_0, W_1, X_0, X_1, Y_0, Y_1, Z_0 and Z_1. The sum to be computed is specified by a 2-bit select input called *SEL* as follows.
If *SEL* = 00, the ADDER computes the sum $W_0 + W_1$.
If *SEL* = 01, the ADDER computes the sum $X_0 + X_1$.
If *SEL* = 10, the ADDER computes the sum $Y_0 + Y_1$.
If *SEL* = 11, the ADDER computes the sum $Z_0 + Z_1$.
Show a figure of the ADDER and the logic around it that allows the four sums to be computed as required. Specify inputs clearly. You may show an n-bit signal as a single line to simplify the figure.

Answer (logic diagram that includes the ADDER):



Problem 5

Find a synchronizing sequence for the finite-state machine with the following state table.

	S*,Z	
S	X=0	X=1
A	B,0	A,0
B	C,0	A,1
C	D,1	B,0
D	A,1	B,1

Answer (synchronizing sequence): 11