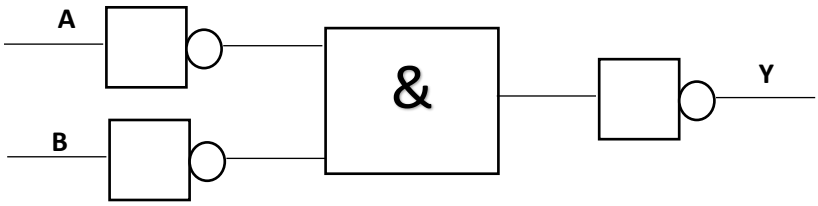
PRACTICE1 – SOLUTIONS

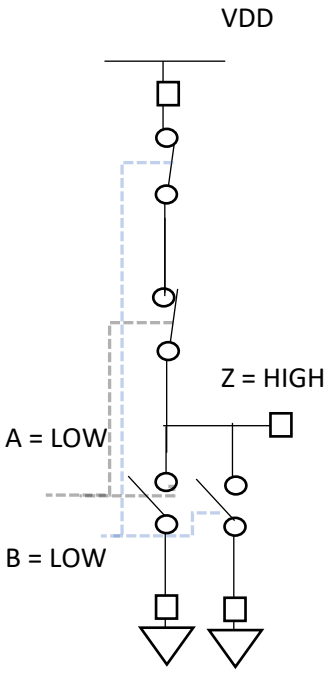
1)

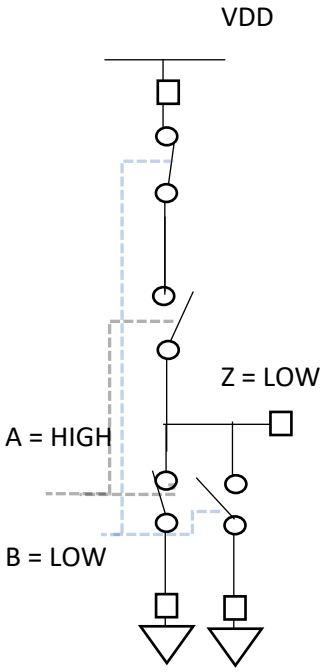


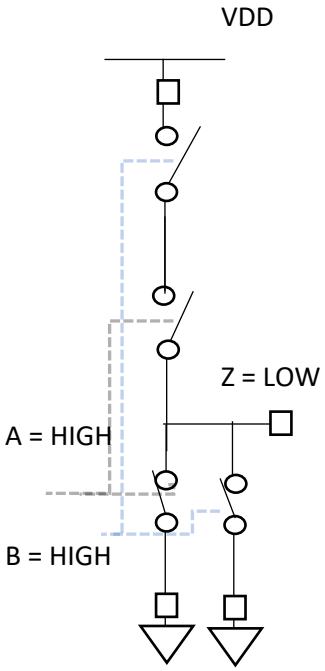
A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1

An OR circuit gives the same output behavior, that is, Y = A + B.

2)




VDD
Z = LOW
A = HIGH
B = LOW


VDD
Z = LOW
A = HIGH
B = HIGH

3)

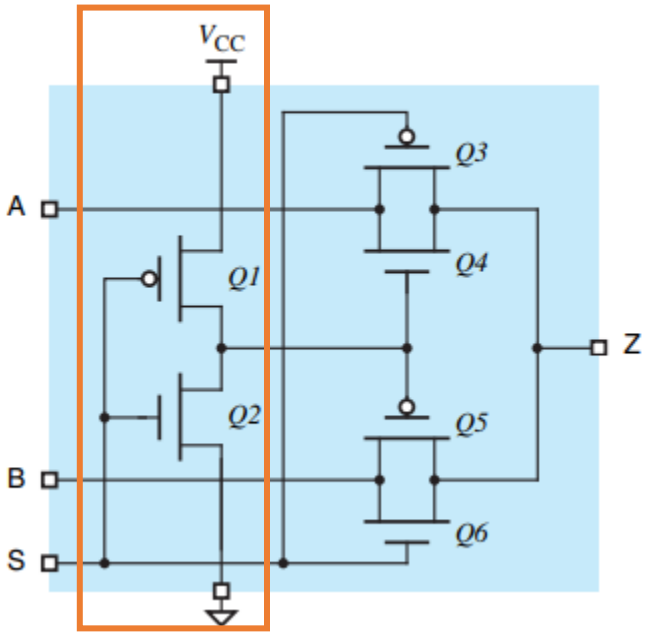
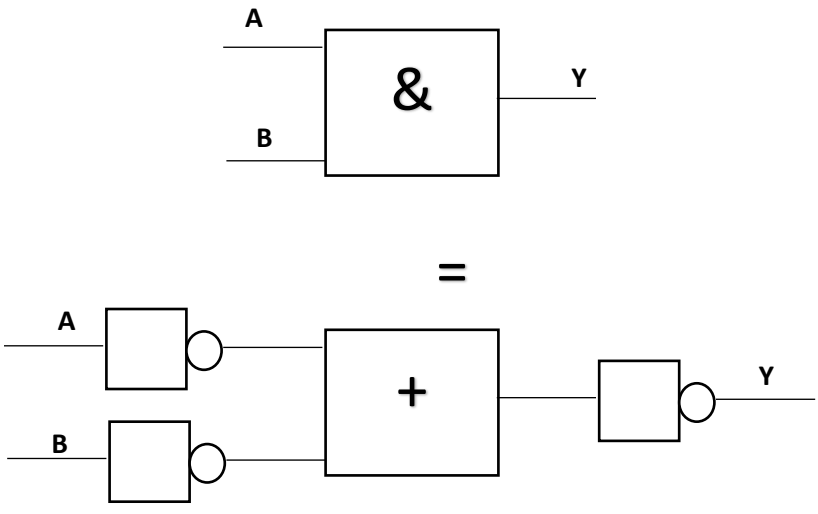


Figure 1-19
Multiplexer design using CMOS transmission gates.

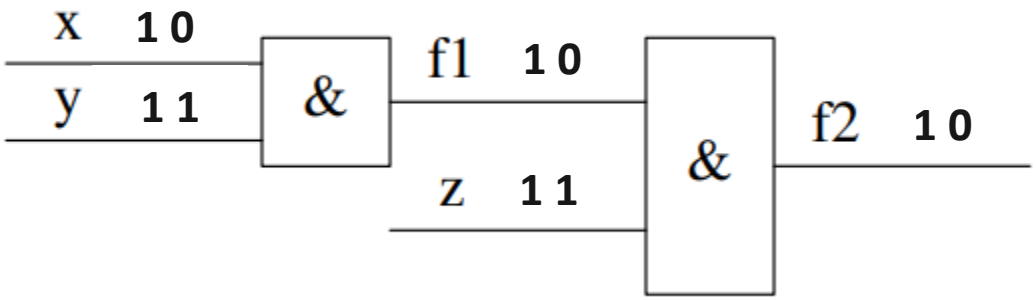
The part of the circuit highlighted with the orange box acts as an inverter. Hence, transistors Q1, Q2 form an inverter.

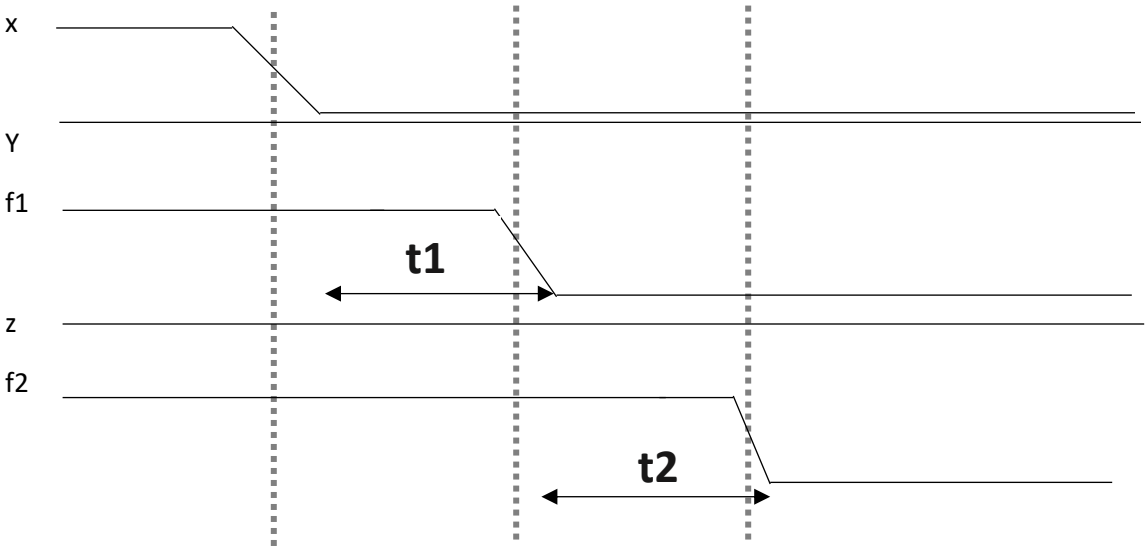
4)



Y = A . B = (A' + B') '

5)





t1: propagation delay from x to f1

t1: propagation delay from f1 to f2

6)