Homework 11-12 Solutions

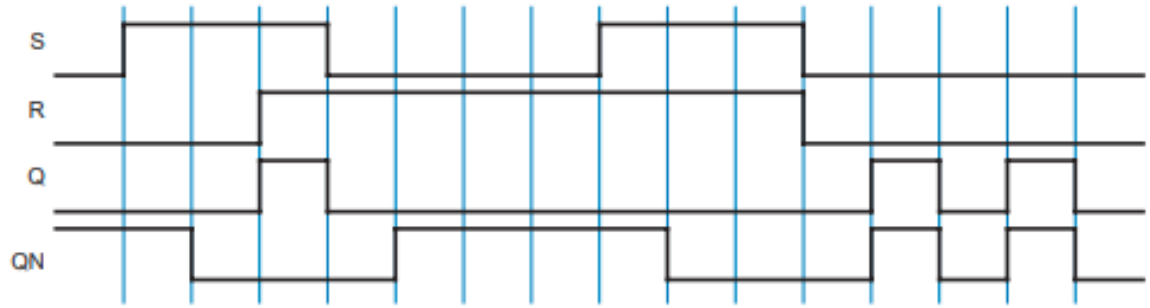
1. As per the truth table of S'R' latch in the notes/text book, we have if S_L = 0, Q is always 1, depending on R_L, value of QN is changing. In that case, we have below inputs/outputs:

S_L = 0 and R_L = 1 is Q = 1 and QN = 0;

S_L = 0 and R_L = 0 is Q = 1 and QN = 1;

S_L = 1 and R_L = 1 is Q = 0 and QN = 1 or Q = 1 and QN = 0; based on which gate takes the first output value and passes it to the other.

2. The latch oscillates if S and R are negated simultaneously. The below behavior is seen when established with the given waveforms as inputs to S and R for our S-R latch.

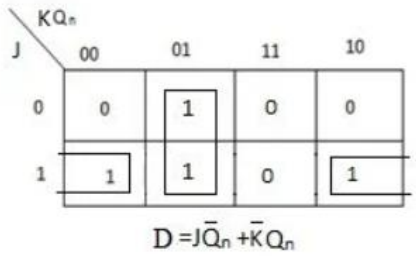


3. To convert D flipflop into a JK flip flop, as per the given requirement, we shall first build a conversion table of values as below.

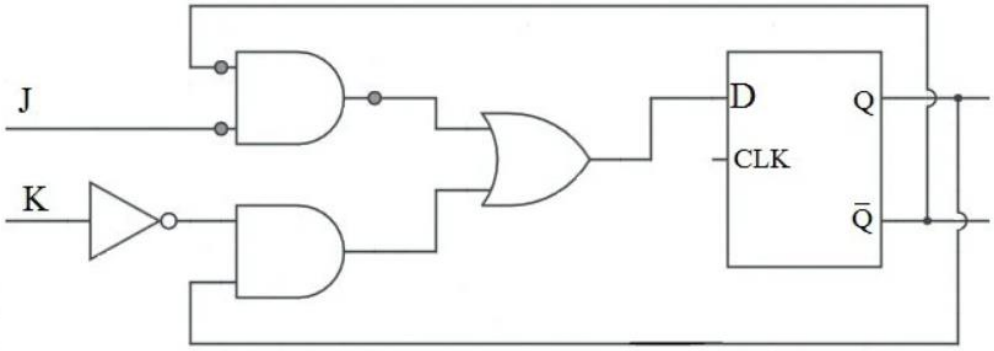
J	K	Q_n	Q_{n+1}	D
0	0	0	0	0
0	0	1	1	1
0	1	0	0	0
0	1	1	0	0
1	0	0	1	1
1	0	1	1	1
1	1	0	1	1
1	1	1	0	0

X—Dont care

Now, using a K-Map, find the relation for 'D' in terms of J, K and Qn as below.



From this equation, we can build the circuit diagram of a JK flip flop using D flipflop as shown below.



4. Given to consider a T-Flipflop. We know the truth table of T-flipflop is as below.

T	Q_n	Q_{n+1}
0	0	0
0	1	1
1	0	1
1	1	0

Here, it is given that T = 1 always, and from the above table, we can observe that, if T = 1, Qn+1 = ~Qn since this is a toggle flipflop. So, the same value either 1 or 0, comes again after 1 clock cycle every time as in the way 1010101010…. or 0101010101…. is obtained.

Hence, if the given input clock frequency is 240Hz, let's say if we consider initial value of Q is 1, then after 1 additional clock cycle, 1 again is obtained at Q which gives me the frequency of 240Hz/2 = 120 Hz is the frequency of our output signal.

5. Given the clock frequency is 50 MHz. So, Timeperiod is 20 ns (1/50MHz).

As per the setup time margin equation, we have Tffpd(max) + Tcomb(max) + Tsetup <= Tclk

Just substituting the provided numbers from the question, we have,

2 ns + 1 ns + 2 ns <= 20 ns

5 ns <= 20 ns, So there is no set up time violation in the given circuit.

As per the hold time margin equation, we have Tffpd(min) + Tcomb(min) >= Thold

1 ns + 0.5 ns >= 1 ns

1.5 ns >= 1 ns So there is no hold time violation also in the given circuit.

Setup time margin = 20-5 = 15 ns

Hold time margin = 1.5 – 1 = 0.5 ns

6. In the given diagram, we can observe that Q2 and Q3 are connected to a XNOR gate and the output of the XNOR gate is given to CLEAR' pin of the counter which is an active low pin. So, if CLEAR' = 0, the counter will be reset. Else continue normally.

So, to find the maximum value the counter can count, we need to find when will the counter be cleared. In other words, at what values of Q0, Q1, Q2, Q3, the counter gets cleared.

So, the CLEAR' = Q3 XNOR Q2 which means, if Q3 = Q2, then output of the gate will be 1, else 0.

So, our requirement is to get the gate output as 0, which gives Q3 not equal to Q2.

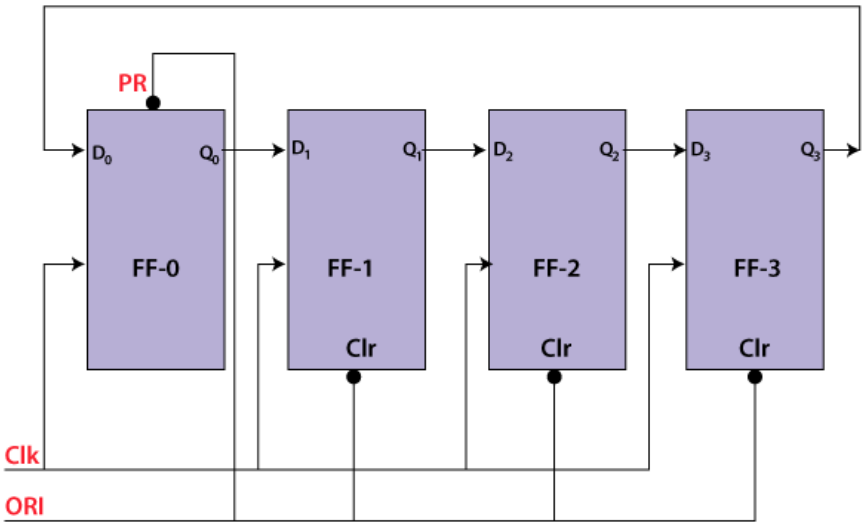
This means that, when the Q3 not equal to Q2 occurs at the first time, while starting from 0000, for synchronous clear counter (which works on every clock edge), the clear occurs after the clock edge. This situation occurs for 0100 first time so this is counting till value 4. So, this is a mod-5 counter.

7. So, we need a 4-bit ring counter. Let's say if our counter starts from 0000. Now, as per the lecture notes/text book, a 1 propagates through the number of digits for each clock cycle as the counter moves forward. So, from initial state of all 0000 at Q pin of the flipflops, since we need a 1 to propagate around, we can take the Q pin of the last flip flop and connect it as the input of our 1^{st} flip flop in the sequence as all are D-Flipflops only and its output is equal to the input at the clock edge sampling.

From this logic, we can simply construct a 4-bit ring counter by serially connecting 4 DFF's and Q pin of 4^{th} DFF to input of 1^{st} DFF as shown below and parallelly we take the outputs at each Q pin of the D flipflops.

This is a typical application of shift register.

PR = 0, then Q = 1; CLR = 0, then Q = 0; ORI is an active low input in the below diagram

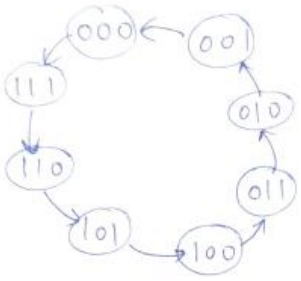


8. 3-bit ripple down counter can be implemented using T flipflop as shown below. For instance, we can use the excitation table of a TFF and the state diagram and characteristic table as shown below for a 3-bit ripple down counter using negative edge triggered TFF's.

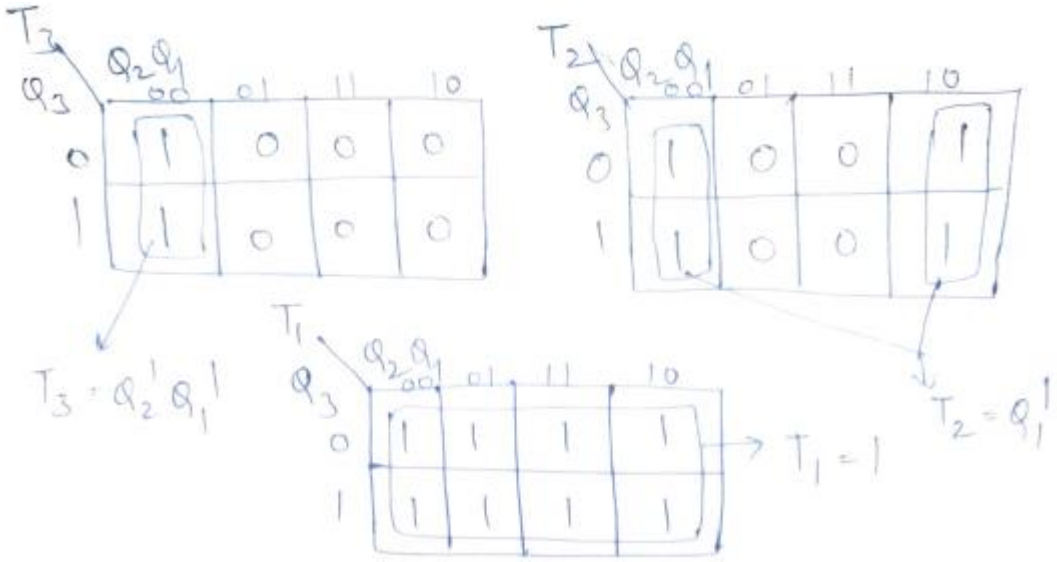
Excitation Table of T-FF

Q_n	Q_{n+1}	T
0	0	0
0	1	1
1	0	1
1	1	0

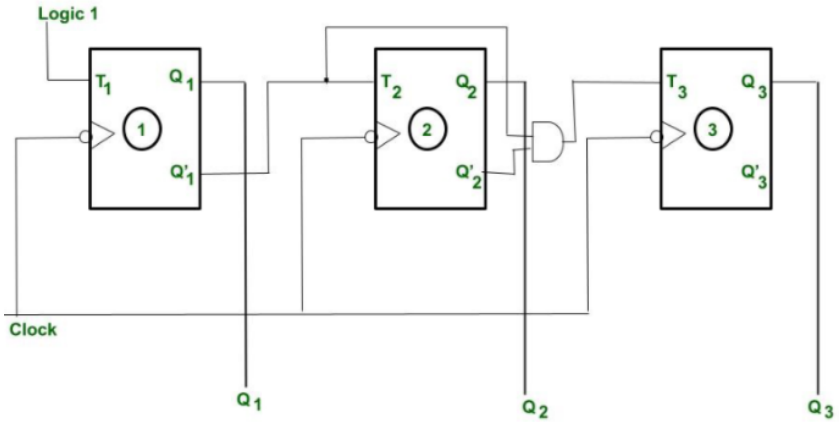
State Diagram



Previous state			Next state					
Q_3	Q_2	Q_1	Q_3	Q_2	Q_1	T_3	T_2	T_1
0	0	0	1	1	1	1	1	1
0	0	1	0	0	0	0	0	1
0	1	0	0	0	1	0	1	1
0	1	1	0	1	0	0	0	1
1	0	0	0	1	1	1	1	1
1	0	1	1	0	0	0	0	1
1	1	0	1	0	1	0	1	1
1	1	1	1	1	0	0	0	1



Based on the outcomes of above K-maps, we need to draw the circuit diagram using the T-Flipflops.



9. 011010… Take the reset state of the circuit and note the value of QA for every clock edge.

10. (a) As per the diagram, we have Dnext = Q0 XOR Q2 XOR Q3

So, we have the 4-bit values after each clock pulse as shown here.

Q0	Q1	Q2	Q3
1	0	0	0
1	1	0	0
1	1	1	0
0	1	1	1
0	0	1	1
0	0	0	1
1	0	0	0

(b) As from the above table, we see that if 1000 is to be occurring in 2 clocks, we can clearly observe that we should initialize the shift register to 0011.