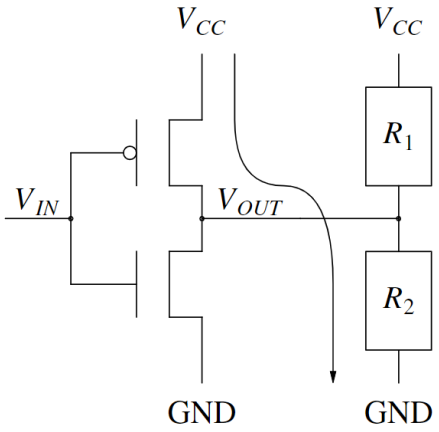
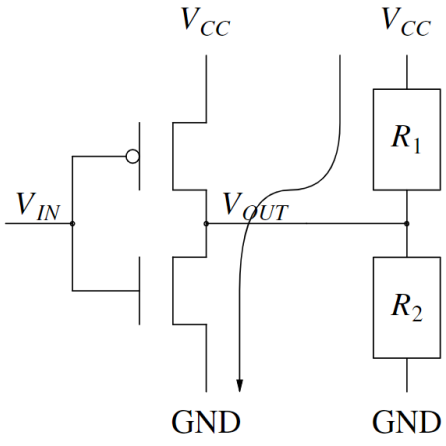
HOMEWORK 6
SOLUTIONS

1. Since both the NMOS and PMOS transistors have some resistance associated with them under ON conditions, a resistive load changes the output voltage due to voltage divider action.
   For a LOW input voltage, the output voltage is lower than the actual output HIGH (5V).
   For a HIGH input voltage, the output voltage is higher than the actual output LOW (0V).

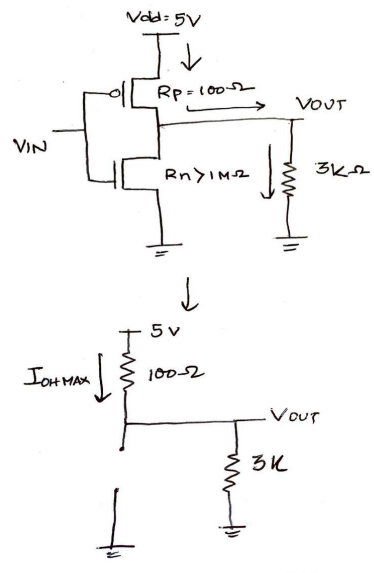


When PMOS is ON (Vin = 0V)



When NMOS is ON (Vin = 5V)

2. I_{OHMAX} is the maximum current that the output can source when it is HIGH while still maintaining an output voltage no lesser than VOHmin.For the output to be high the PMOS has to be turned ON. The NMOS is OFF and thus has very high resistance.



$$V_{OUT} = \frac{3K}{3100\Omega} \times 5V$$

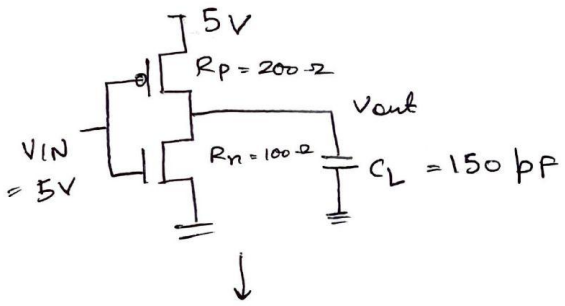
$$\Rightarrow \frac{30}{31} \times 5$$

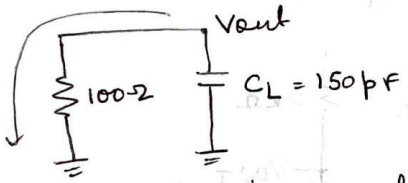
$$\Rightarrow 4.83\,V$$

$$I_{OHMAX} = \frac{(5-4.83)V}{100\Omega}$$

$$= 1.7\,mA$$

3.





By Kirchoff's voltage law.

$$\frac{d}{dt}(C V_{out}) = -\frac{V_{out}}{R}$$

$$\Rightarrow C\frac{dV_{out}}{dt} = -\frac{V_{out}}{R}$$

$$\Rightarrow RC\frac{dV_{out}}{V_{out}} = -dt$$

$$\Rightarrow \int_{0.8V_{DD}}^{0.2V_{DD}} \frac{dv_{out}}{V_{out}} = -\int_{0}^{t_{fall}} \frac{dt}{RC}$$

$$= \int_{0.2V_{DD}}^{0.8V_{DD}} \frac{dv_{out}}{V_{out}} = \int_{0}^{t_{fall}} \frac{dt}{RC}$$

$$\Rightarrow \ln 4 = \frac{t_{fall}}{RC}$$

$$\Rightarrow t_{fall} = 100 \times 150 \times 10^{-12} \times \ln 4$$

$$= 20.8\,ns$$

4. i) Dissipation due to direct current path - This happens when the input voltage undergoes a transition and both the PMOS and NMOS transistors are ON for a short interval of time as the input voltage is not close to 0V or Vdd.

$P_T = C_{PD} * Vdd^2 * f$

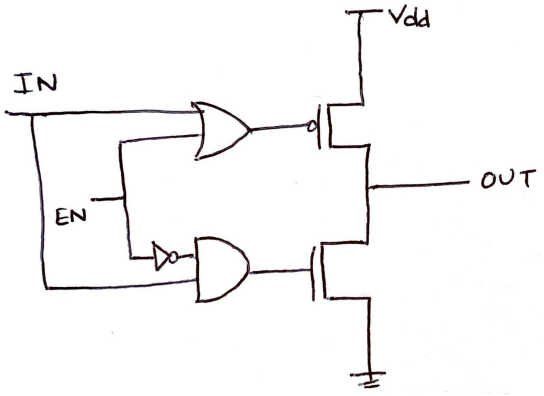
where f is the transition frequency and C_{PD} is a constant that represents the physical effects that occur in the device.

ii) Dissipation due to capacitive load at the output - The energy dissipated due to charging and discharging of the output capacitor, which can be a combination of internal capacitance, interconnect capacitance, and external load capacitance.

$P_L = C_L * Vdd^2 * f$

Where f is the transition frequency and C_L is the load capacitance.

5. The high-impedance output state is created by turning off both the PMOS and NMOS transistors using the EN signal.



6. We can connect tri-state buffers at the output of each device before connecting to the bus. A decoder logic can be used to set the enable signals of the tri-state buffers thus ensuring that only one device is accessing the bus at a time. The outputs of all the other devices are held in a high-impedance (Z) state.

7. module Mux21 (A,B,S,Y) ;
   output Y;
   input A, B, S;
   assign Y = S?B:A; (or Y = S?A:B)
   endmodule

8. Y = 5'b0X011

9. 3*4+6+4 = 22

10. reg [31:0] A [0:127]
    assign B = A[5]