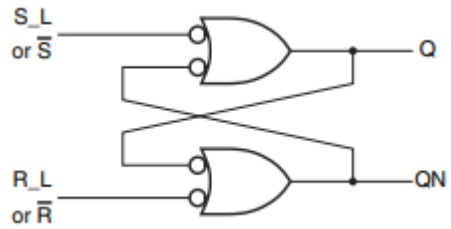
ECE 270 (Spring 2022)

Homework 11-12

Due on 04/08/2022 (Friday) by 11:59 pm on BrightSpace.

1. The following values are applied to S_L and R_L inputs of the NAND latch shown in the below figure in the same sequence indicated below.

(S_L = 0, R_L = 1) → (S_L = 0, R_L = 0) → (S_L = 1, R_L = 1).



What is the corresponding stable Q, QN outputs for each of the input value sets in the above sequence?

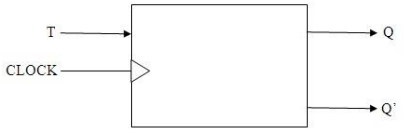
2. Sketch the outputs of a NOR based S-R latch for the input waveforms shown in the figure below.

Assume that input and output rise and fall times are zero, that the propagation delay of a NOR gate is 10 ns, and that each time division below is 10 ns.

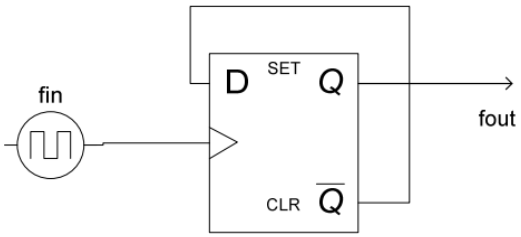
3. A positive-edge-triggered J-K flip-flop has two control inputs J and K that control the device's behavior at the rising edge of CLK. If only J is asserted, the Q output is set to 1; if only K is asserted, Q is cleared to 0; if both are asserted, Q is toggled; and if neither is asserted, Q is not changed.

Show how to build a J-K flip-flop using a D flip-flop and combinational logic.

4. A simple T flip-flop is given as shown below. If the input frequency of clock signal driving this flip-flop is 240 Hz and T=1 always, what is the frequency of the output signal Q ?



5. In a digital circuit, if the set up-time margin is negative, then the circuit is said to have a set up time violation. Similarly, if the hold-time margin is negative, the circuit is said to have a hold time violation.

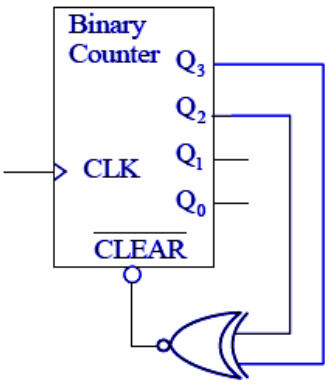


Consider the fin (frequency) of the clock as 50 MHz. T_{ffpd} (min) = 1 ns, T_{ffpd} (max) = 2 ns, T_{comb} (min) = 0.5 ns, T_{comb} (max) = 1 ns, T_{setup} = 2 ns, T_{hold} = 1 ns.

Now, Please check if the above circuit has any set-up time or hold time violations with the given values of T_{ffd}, T_{comb}, T_{setup} and T_{hold} values as above. If yes, provide the values of respective set up-time or hold time margins.

6. A modulo-n counter counts the values from 0 to n-1 in the decimal system. For example, a modulo-4 counter can be used to count the values from 0 to 3.

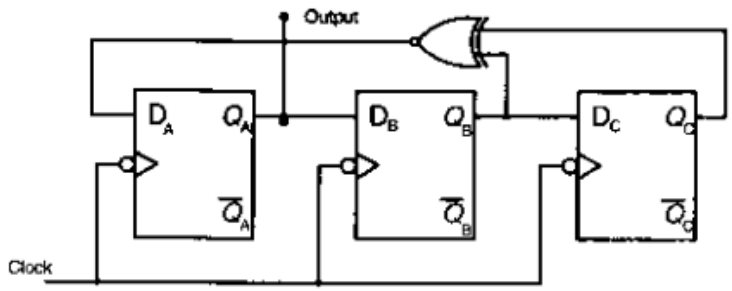
The figure below shows a modulo-n binary counter which works on every positive clock edge. Find the value of ‘n’ in this modulo-n counter ? (Assume Q3,Q2,Q1,Q0 are the outputs of your 4 flip flops which decodes as binary to decimal values upto n-1 with Q3 as MSB and Q0 as LSB)



7. Draw a 4-bit ring counter using D-Flipflops and give the output values of each flipflop for each clock cycle.

8. Implement a 3-bit ripple down counter using T-Flip Flop by showing the characteristic table and the final circuit diagram containing proper inputs/flipflops.

9. Assuming all the flip-flops are in reset condition initially, what is the sequence observed at the output Q_A in the circuit shown for each clock cycle. Provide your answer for at least 6 clock cycles.



10. A 4-bit shift register, which shifts data right Q0→ Q1→ Q2→ Q3, is shown in the below figure. The initial value for Q0, Q1, Q2, Q3 is 1000.

(a) Write the 4-bit values for Q0, Q1, Q2 and Q3 after each clock pulse until the pattern 1000 reappears.

(b) To what value should the shift register be initialized so that the pattern 1000 occurs after 2 clock pulses?