Chapter 3. Switching Algebra and Combinational Logic (Part 3)

Timing Hazards

Until now we analyzed combinational logic circuits assuming that their inputs have been stable for a long time relative to the delays of the circuit.

Equivalently, we assumed a zero delay between an input change and an output change.

The actual delay from an input change to an output change is nonzero.

Suppose that an input combination A_1 produces an output combination Z_1.
Suppose that an input combination $A_2 \neq A_1$ produces an output combination Z_2 from C.

When the input combination is changed from A_1 to A_2, we expect the output combination to change from Z_1 to Z_2.

Because of circuit delays the change does not happen instantaneously.
During the transition from Z_1 to Z_2 the outputs may go through combinations that are different from Z_1 and different from Z_2.

A momentary pulse on an output to which A_1 and A_2 assign the same value is called a *glitch*.
A glitch can cause unwanted circuit behavior.
For example, a traffic light changing momentarily to green when it is supposed to be red.
A *hazard* is the possibility that the circuit will produce a glitch.

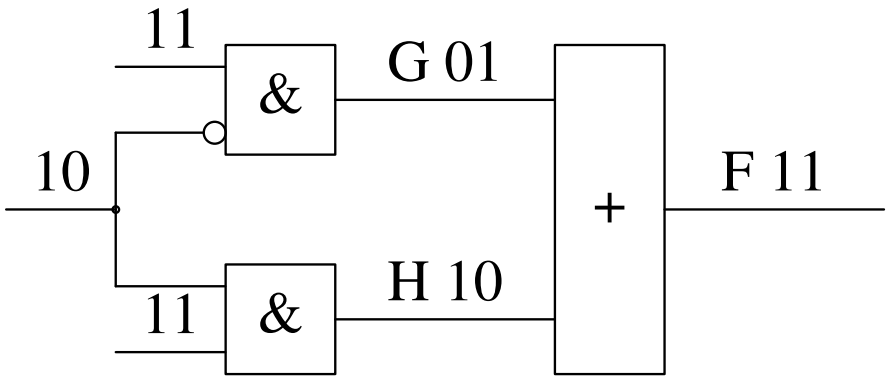
The occurrence of glitches depends on the circuit delays and it cannot be computed accurately from the logic description of the circuit.
However, the possibility that they will occur can be predicted from the logic description of the circuit.
It is also possible to design a circuit so as to avoid hazards.

Static Hazards

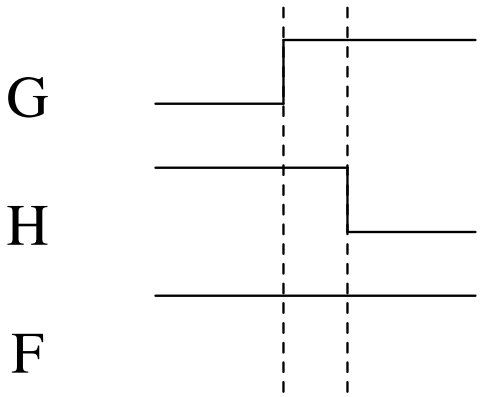
A *static-1 hazard* is the possibility that the circuit output will have a momentary 0 pulse when it is supposed to be stable at 1.

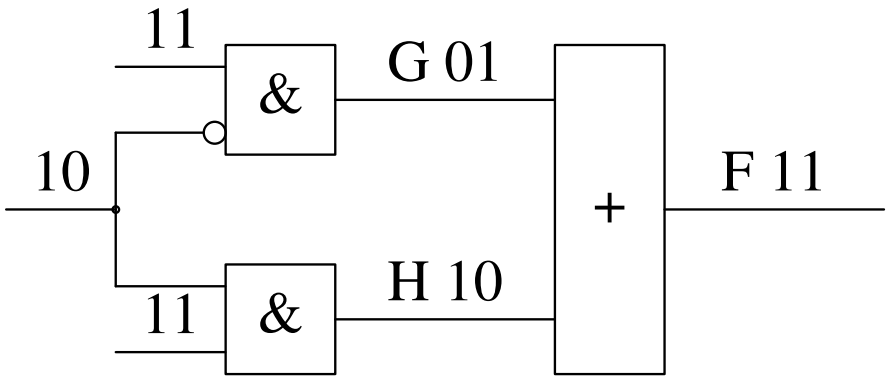
Definition: A static-1 hazard is a pair of input combinations that (a) differ in only one input variable, and (b) both give a 1 output; such that it is possible for a momentary 0 output to occur during a transition in the differing input variables.

Example:

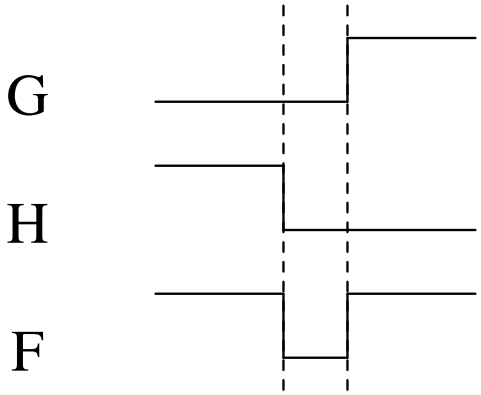


Timing scenario 1:





Timing scenario 2:

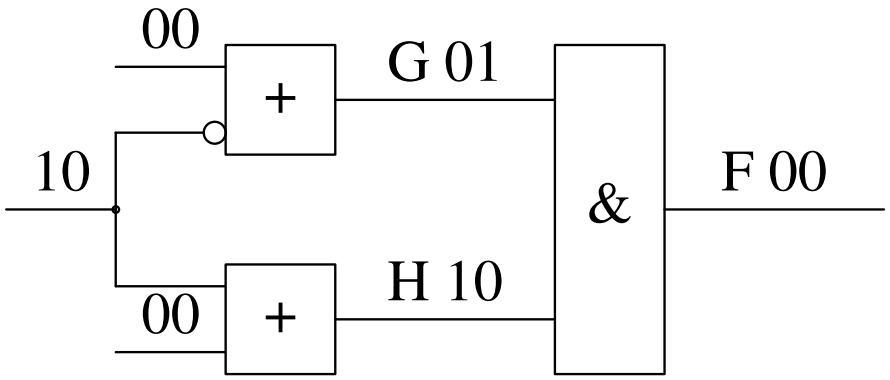


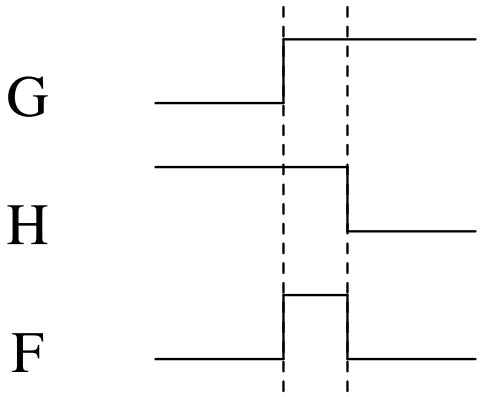
This scenario is likely because the inverter adds a delay to the change on G.

A *static-0 hazard* is the possibility that the circuit output will have a momentary 1 pulse when it is supposed to be stable at 0.

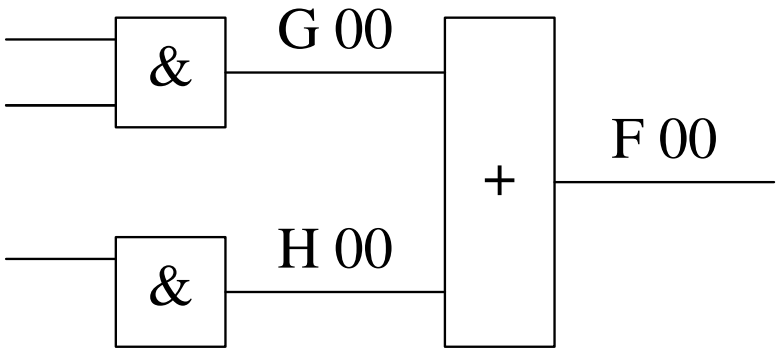
Definition: A static-0 hazard is a pair of input combinations that (a) differ in only one input variable, and (b) both give a 0 output; such that it is possible for a momentary 1 output to occur during a transition in the differing input variables.

Example: The dual of the previous example.





Considering a two-level sum-of-products (AND-OR) circuit:
A static-0 hazard is not created at the output of the OR gate.



For a static-0 hazard to be created on G or H, an AND gate would have to be driven by an input and its complement. This is never necessary.

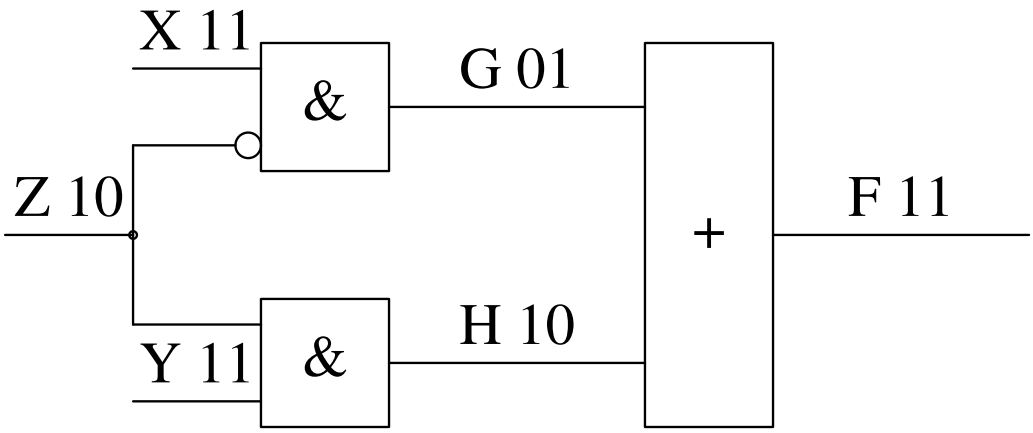
Therefore, in an AND-OR circuit we are concerned about static-1 harzards.
For the dual reasons, in an OR-AND circuit we are concerned about static-0 hazards.

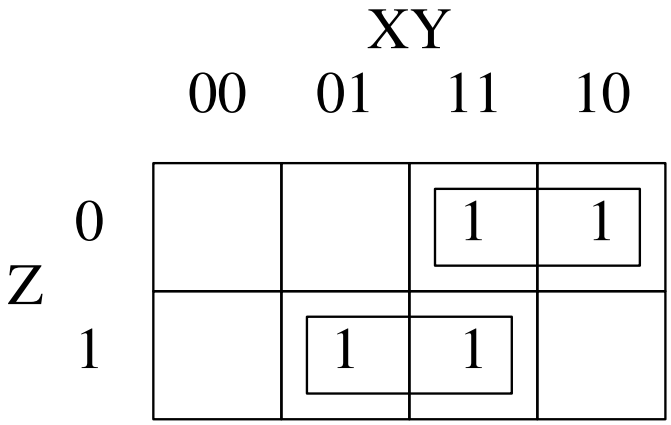
Finding Static Hazards from K-Maps

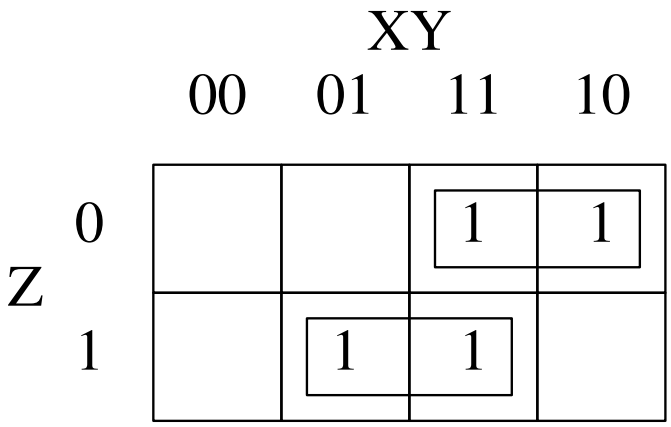
A K-map allows us to find static hazards in a two-level sum-of-products or product-of-sums circuit.

We need a K-map in which the product terms corresponding to the AND gates of the circuit are circled.

Example:







From the K-map, there is no single product term in the circuit that covers both XYZ = 111 and XYZ = 110.

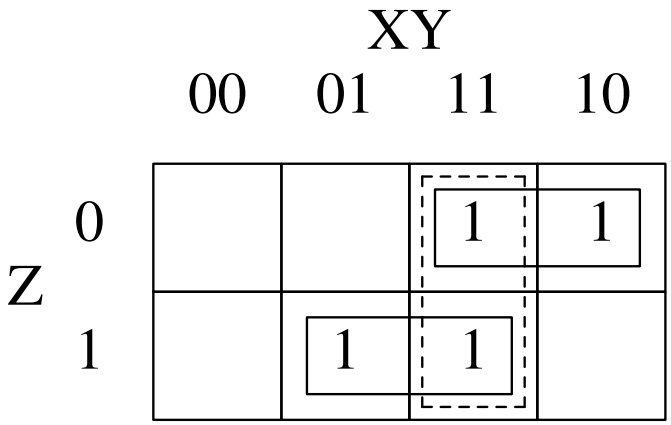
Therefore, there are two different AND gates that cause the output to be 1 for 111 and 110.

If one of the AND gates changes from 0 to 1 before the other, a glitch can occur.

We conclude that a static-1 hazard occurs if adjacent minterms are not covered by a single product term.

The way to eliminate the hazard is to add another AND gate to cover the adjacent minterms.

In the example, the required AND gate implements the product term XY.



In the corresponding circuit, every pair of adjacent minterms is covered by a single AND gate.

Consequently, every single input change where the output should remain 1 is covered by a single AND gate. This gate will remain at 1 when the input change occurs.

No static-1-hazard exists.

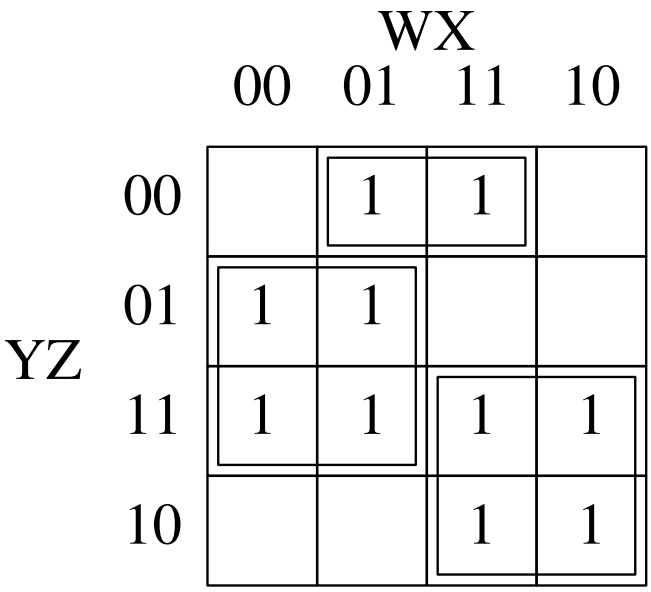
The same can be achieved by applying the switching algebra theorem
(T11) $X \cdot Y + X' \cdot Z + Y \cdot Z = X \cdot Y + X' \cdot Z$

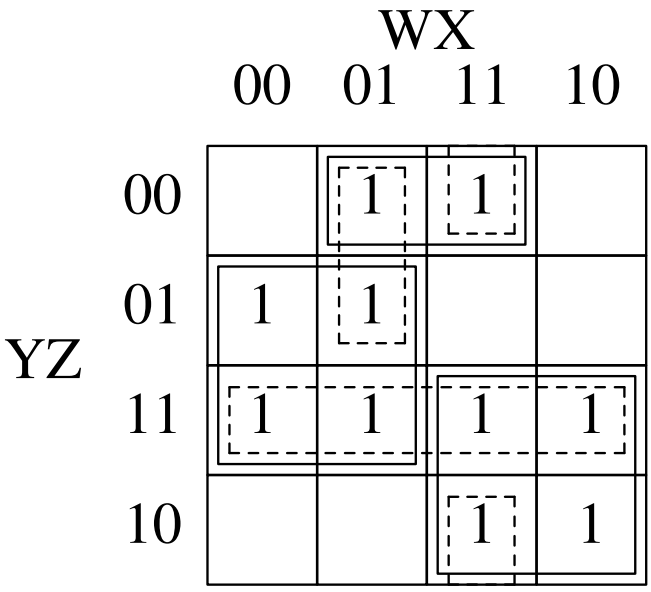
In the previous example:
$F = X \cdot Z' + Y \cdot Z = X \cdot Z' + Y \cdot Z + X \cdot Y$.

With an OR gate at the output and no single input driving the same gate twice, an AND-OR circuit does not have static-0 hazards.

Similar analysis can be done for OR-AND circuits.

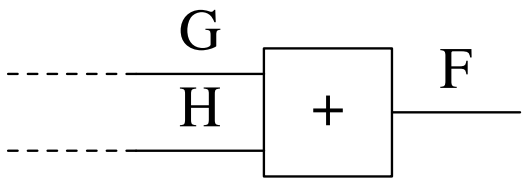
The next example illustrates that adjacent minterms should be covered by prime implications.

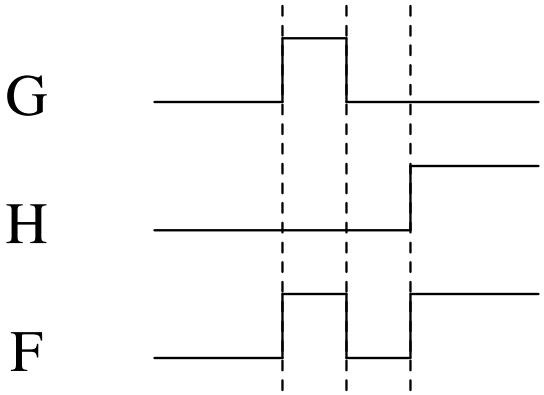




Dynamic Hazards

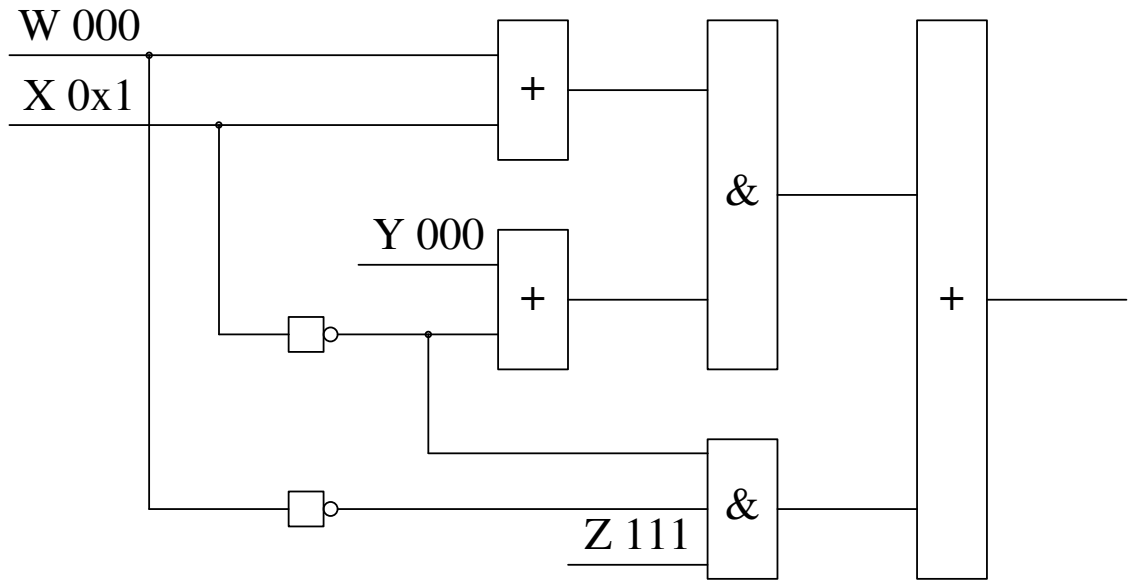
A *dynamic hazard* is the possibility that an output will change more than once as a result of a single input change.
Dynamic hazards occur in multi-level circuits.

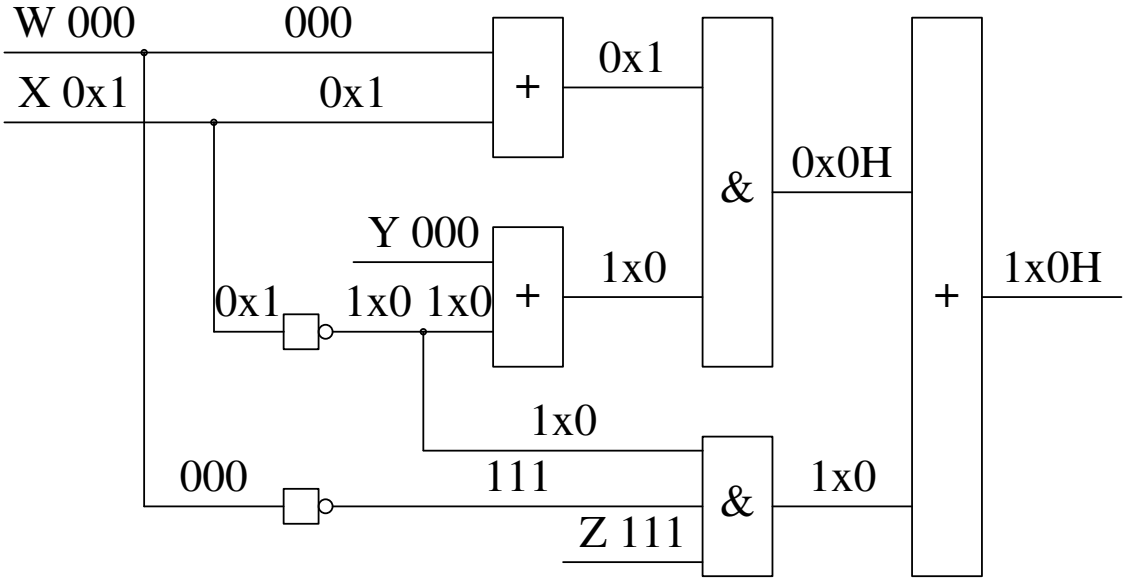




Example of hazard analysis in a multi-level circuit:

The input changes from WXYZ = 0001 to WXYZ = 0101.




W 000
000
X 0x1
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