ECE 27000 Introduction to Digital System Design
Spring 2022
Exam 2, March 24, 2022

S O L U T I O N

Last Name: _____ First Name: _____

Lab Section (Number or Day and Time): _____

As a boilermaker pursuing academic excellence, I pledge to be honest and true in all that I do. Accountable together - we are Purdue.

I certify that I have neither given nor received unauthorized aid on this exam.

Signed: _____

Solve the following problems. The number of points for each problem is shown in the table below.

Use only the space provided to solve each problem, and copy the answers to the space marked "Answer:..."

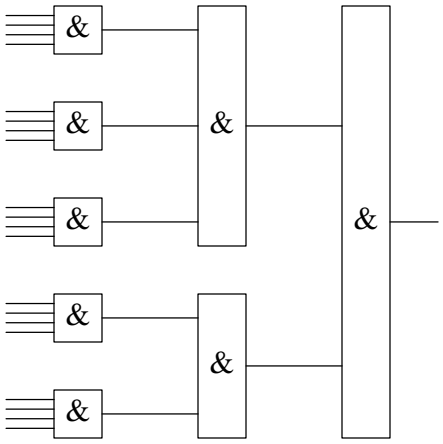
Problem	Outcome	Points
1	1	/ 20
2	1	/ 20
3	2	/ 20
4	2	/ 20
5	2	/ 20
Total		/ 100

Problem 1

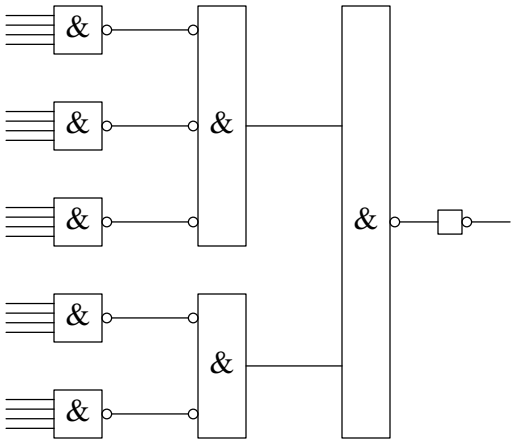
It is given that the fanin of CMOS NAND and NOR gates is four. Design a 20-input AND gate using only NAND and NOR gates that satisfy the fanin constraint. You are allowed to use inverters. However, you should use as few inverters as possible.

Answer (20-input AND gate designed using NAND gates, NOR gates and inverters as specified in the question):

Assuming AND gates with the same fanin constraint are available:

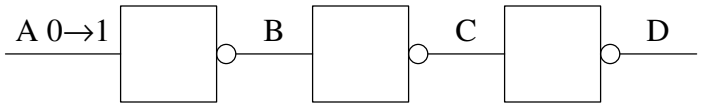


After adding inverters to use NAND and NOR gates:

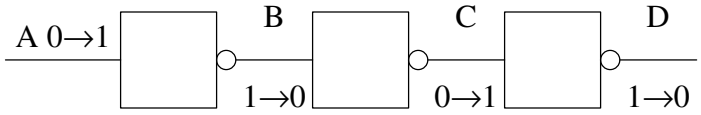


Problem 2

The propagation delays for an inverter are defined as follows.
t_{p10} - the time between an input change and the corresponding output change when the output is changing from 1 to 0.
t_{p01} - the time between an input change and the corresponding output change when the output is changing from 0 to 1.
Find the time between the change on A and the change on D for the following circuit.
Assume that only the propagation delays of the inverters affect this time, and transition times are zero.



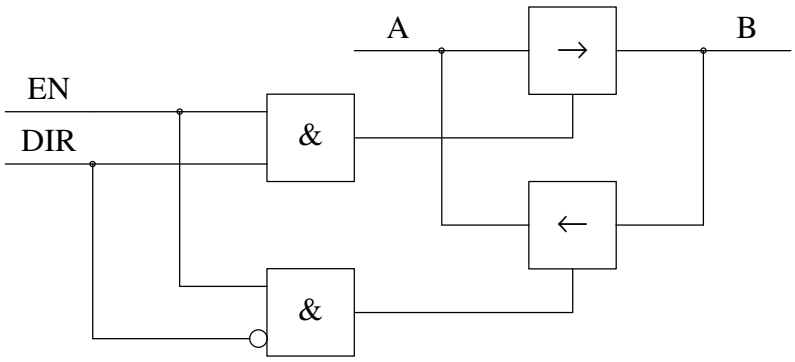
Answer (time between the change on A and the change on D expressed in terms of t_{p10} and t_{p01}):



$2 \cdot t_{p10} + t_{p01}$

Problem 3

The following bus tranceiver connects buses A and B. Fill the table below with values for EN and DIR to implement the operations shown in the table. The operations occur in the order they appear in the table. To avoid unwanted effects, only one value of EN or DIR should be changed from one operation to the next.



Note: the following symbols are equivalent.

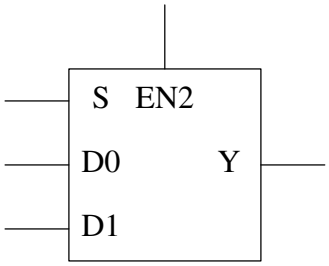
operation	EN	DIR
data flows from A to B	1	1
data does not flow between A and B	0	1
data does not flow between A and B	0	0
data flows from B to A	1	0
data does not flow between A and B	0	0
data does not flow between A and B	0	1
data flows from A to B	1	1

Answer (enter the values of EN and DIR in the table above).

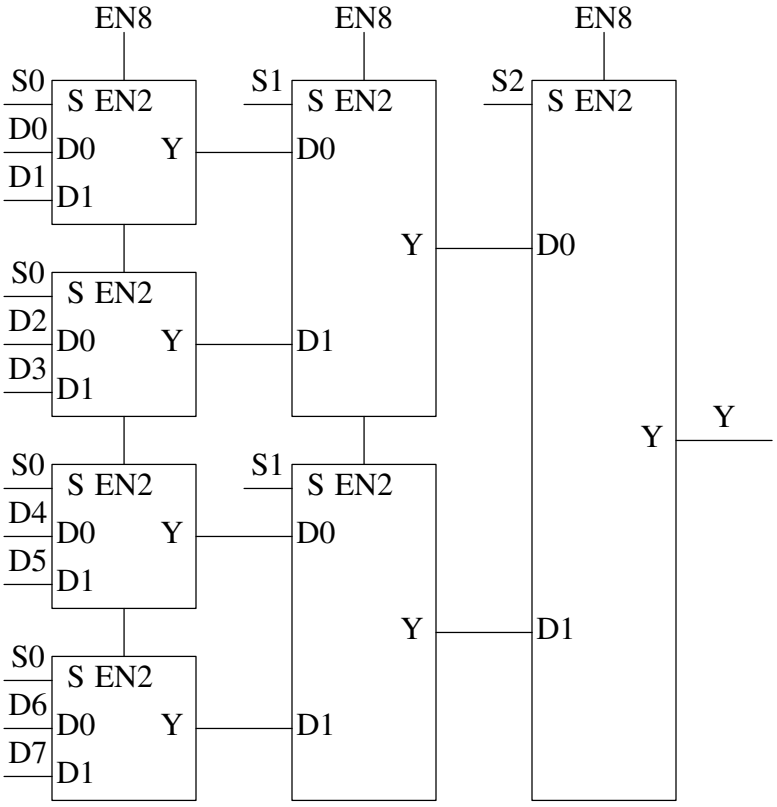
Explanation: Data flows from A to B when EN=1 and DIR=1. Data does not flow when EN=0 and DIR=x. To transition from 11 to 0x with only EN changing, use DIR=1. Continue in the same manner.

Problem 4

Design an 8-input 1-bit multiplexer using only 2-input 1-bit multiplexers.
The control inputs of the 8-input 1-bit multiplexer are S0, S1 and S2. Its data inputs are D0, D1, $\cdots$, D7. Its enable input is EN8.
Note: the function of a 2-input 1-bit multiplexer with control input S, data inputs D0 and D1, and enable input EN2, is $Y = EN2 \cdot (S' \cdot D0 + S \cdot D1)$.
Use the following logic symbol for a 2-input 1-bit multiplexer.



Answer (8-input 1-bit multiplexer design using only 2-input 1-bit multiplexers with the logic symbol given above):



Problem 5

An XNOR gate implements the function $Z = (X \oplus Y)'$.
Prove that if the values of Y and Z are known, it is possible to compute the value of X.
Show the equation for X as a function of Y and Z.

Answer ($X = \cdots$):

$X = (Y \oplus Z)' = Y' \oplus Z = Y \oplus Z'$.

Proof:
Truth table of an XNOR gate:

X	Y	Z
0	0	1
0	1	0
1	0	0
1	1	1

Using the truth table to write X as a function of Y and Z:

Y	Z	X
0	0	1
0	1	0
1	0	0
1	1	1

$X = (Y \oplus Z)'$.
Using perfect induction to prove that $X = (Y \oplus Z)'$:

X	Y	Z	Y	Z	$(Y \oplus Z)'$
0	0	1	0	1	0
0	1	0	1	0	0
1	0	0	0	0	1
1	1	1	1	1	1