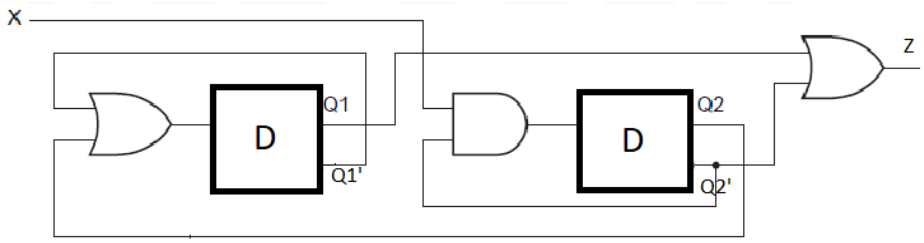
ECE 270 (Spring 2022)

Homework 10

Due on 04/1/2022 (Friday) by 11:59 pm on BrightSpace.

1. Write the transition and output table for the sequential circuit shown below. Assign symbolic names to the states and draw a state table.



2. A state diagram depicts the transition of states from one state to the next and the output, for a given input. Each state is represented by a circle in the diagram.Write the state table and draw the state diagram for a sequence detector that detects an overlapping 1001 sequence.

3. Write a state table and draw the state diagram to detect the non-overlapping sequence 0101.

4. Draw the state diagram for a sequential circuit that returns 1 when it detects three consecutive inputs to be 0.

5. From the state table shown below, perform state minimization to attain optimum number of states.

Present state	Input X = 0	Input X = 1
	Next state, Output	
A	B, 0	C,1
B	D,0	F,1
C	F,0	E,0

D	B,0	G,1
E	F,0	C,0
F	E,0	D,0
G	F,0	G,0

6. For the state table shown below, perform state minimization, state assignment, and write each next-state function in terms of the present states and inputs. The states can be assigned in an orderly manner. Eg: A = 000, B = 001 etc.

Present state	Input X = 0	Input X = 1
	Next state, Output	
A	A, 0	B,0
B	C,0	B,0
C	D,0	B,0
D	A,0	E,0
E	C,0	B,1

7. A synchronous up-down counter is a circuit that increments its count at every clock edge, when the UP input is enabled to 1. When UP is 0, it decrements its count. Write the transition and excitation table for a 3 bit counter circuit considering it uses D flip-flops.
8. A traffic signal cycles from GREEN to YELLOW, YELLOW to RED and RED to GREEN. In each cycle GREEN is turned on for 70s, YELLOW for 5s and RED for 75s. The traffic light has to be implemented using a Finite State Machine (FSM). The clock used in the circuit has a time perios of 5s. What is the minimum number of flipflops required to implement this FSM.
9. Draw a mealy machine state diagram to find 2’s complement of any binary number. The machine has a single input, and a single output; a number appears on the input one bit at a time starting from the least-significant bit; the output is the 2's complement of the input being produced one bit at a time.

10. What is the difference between a Moore and a Mealy machine? Write a behavioral verilog code for the moore machine shown in the state table below:

Present state	Input X = 0	Input X = 1	Output Z
S0	S0	S1	0
S1	S2	S0	0
S2	S3	S2	0
S3	S1	S0	1