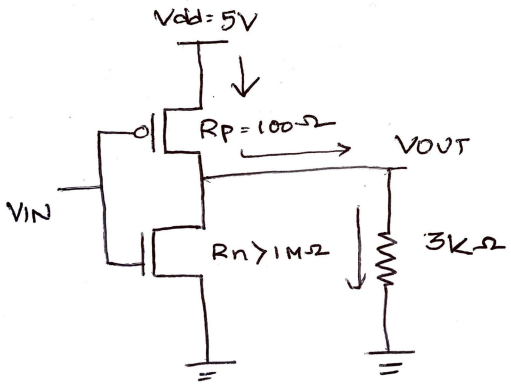
ECE 270 (Spring 2022)

Homework 6

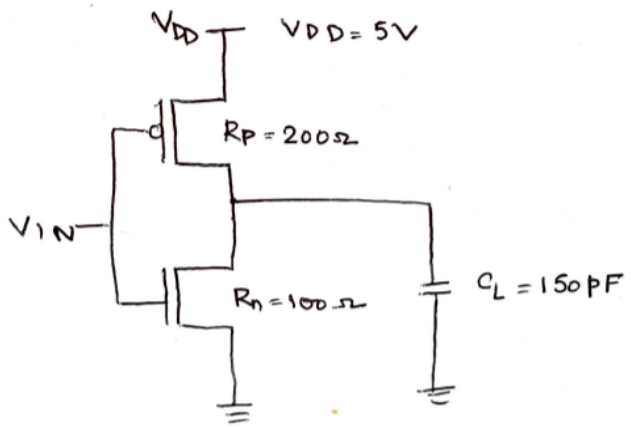
Due on 02/25/2022 (Friday) by 11:59 pm on BrightSpace.

1. Explain the effects of a resistive load on the output voltage of a CMOS inverter.
2. Determine the I_{OHMAX} and V_{OUT} in the following circuit. R_P is the ON-state resistance of the PMOS and whereas R_n is the OFF-state resistance of the NMOS transistor.

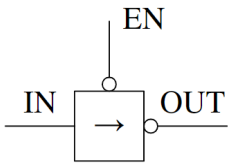


3. If fall time is defined as the time taken by the output voltage to go from 80% of the maximum value to 20%, then what is the fall time for the following inverter circuit considering a capacitive load? R_P and R_n are the ON-state resistance of the PMOS and NMOS transistors respectively.

   Hint: Use the formula $V_{OUT} = V_{DD}.\ e^{-t/(R_n C_L)}$



4. What are the two components of dynamic power in a CMOS circuit?
5. Shown below is a tri-state inverter and its functionality. How can we create a tri-state inverter device using CMOS transistors? Explain with a circuit diagram.



EN	OUT
1	Z
0	IN’

6. Consider multiple devices connected to the same bus. How can we ensure that only one device accesses the bus at a time? Explain.
7. Using the conditional operator, write a simple behavioral Verilog code for a 2:1 multiplexer circuit.
8. What is the value of Y in the following Verilog code:

```
A = 5’b0X011;
if (A === 3’b0X1)
    Y = (A << 2) | 01001;
else
    Y = A;
```

9. Based on the below Verilog statements, how many bits are there in the variable Y?

```
Reg [15:0] A;
Reg [3:0] B;
Y = {3{B}, A[13:8], 4’b0};
```

10. Write the Verilog syntax to declare an array A of 128 32-bit vectors. Assign the 5th element of the array to a register B.