ECE 270 (Spring 2022)

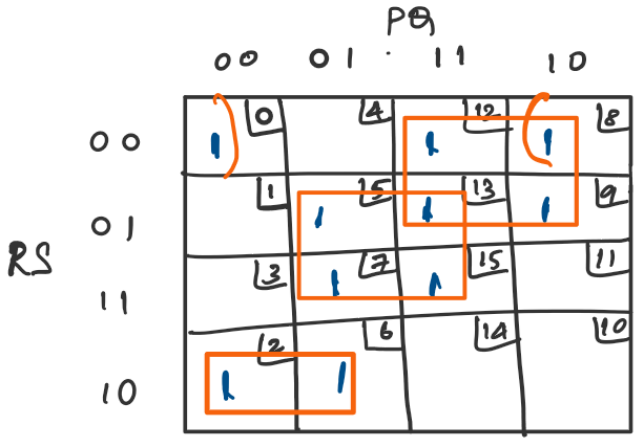
Homework 5

Due on 02/18/2022 (Friday) by 11:59 pm on BrightSpace.

1. Draw the Prime Implicants table for f (X, Y, Z) = ∑ (0, 1, 2, 5, 6, 7) and minimize the sum expression.

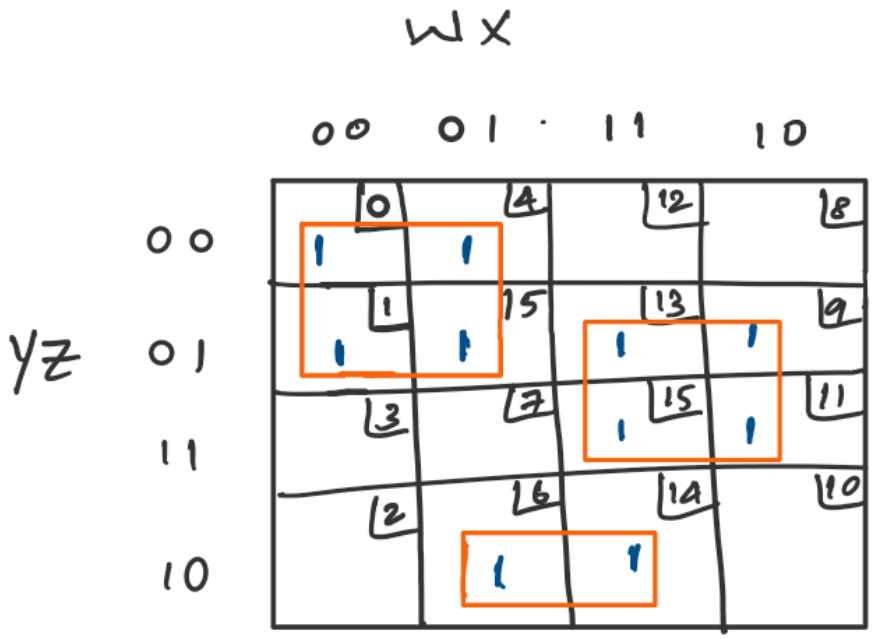
2. Do static zero hazards occur in a Sum of Products circuit? Justify.

3. Identify all the static hazards in the AND-OR circuit implementation of F (P, Q, R, S) described by the K-Map below. Each product term from the K-Map corresponds to an AND gate in the circuit.



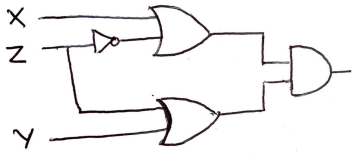
4. Write a sum-of-products expression after removing static hazards from the minimized logic function F deduced in question 3.

5. Find all the static hazards in the AND-OR circuit whose AND gates are represented by circled terms on the K-Map below.

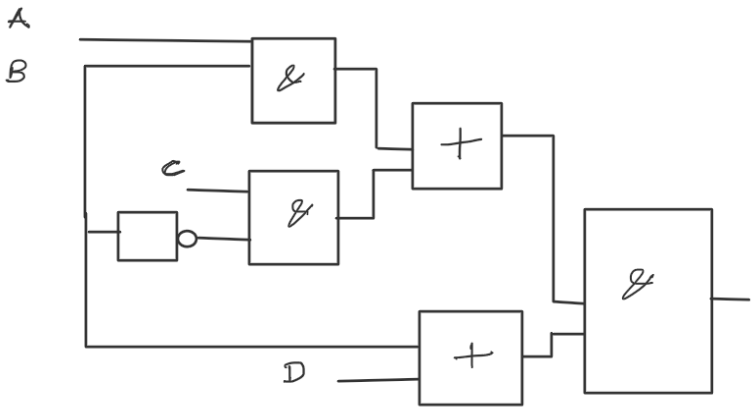


6. Draw a hazard-free AND-OR circuit diagram for the minimized logic function from the K-Map in question 5.

7. In the following circuit, consider inputs X and Y to be held constantly at logic "0" and Z to be transitioning from logic "0" to logic "1" (rising transition). Assume that all the gates have the same propagation delays (including the inverter), and neglect transition times. Draw a timing diagram to show the output of every logic gate. What type of static hazard is exhibited by the circuit?



8. Do you observe a hazard in the circuit below as input changes from ABCD = 1110 to ABCD = 1010? Explain.



9. Provide a circuit implementation of 12 input NOR gate, keeping in mind the fan-in limits for the logic gates (fan-in limit for NOR gate = 4, NAND gate = 6). Minimize the use of inverters in the implementation.

10. Find the DC Noise Margins for a circuit whose V_{OHmin} = 4.9 V, V_{IHmin} = 3.5 V, V_{ILmax} = 1.5 V, V_{OLmax} = 0.1V.