Read:
Chapter 4 (Digital Design Practices).

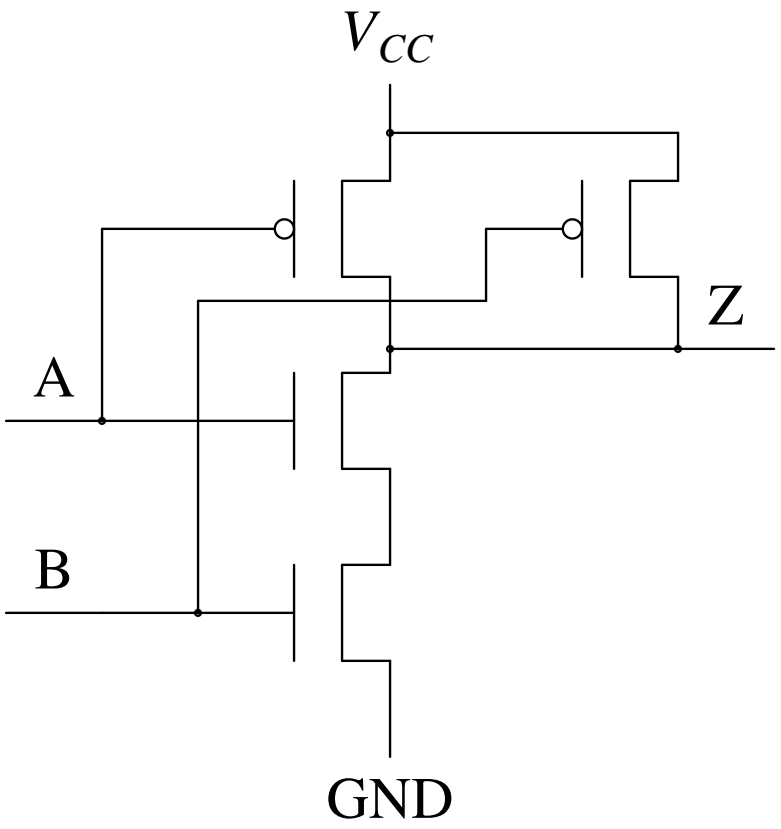
Chapter 14. Digital Circuits

Read:
Section 14.1; Review Lecture Notes 1.

14.1.5. Fan-In

The maximum number of inputs that a gate can have in a particular logic family is called the *fan – in* of the logic family.

We have seen CMOS gates with two inputs.
A 2-input CMOS NAND gate:

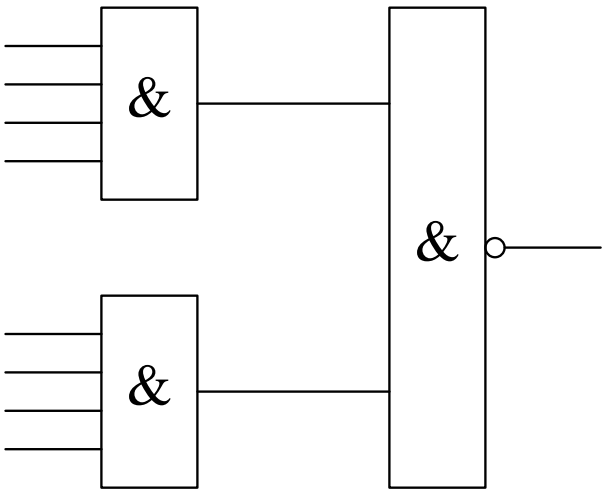


A CMOS gate with more than two inputs can be obtained by adding more transistors to the series and parallel connections.

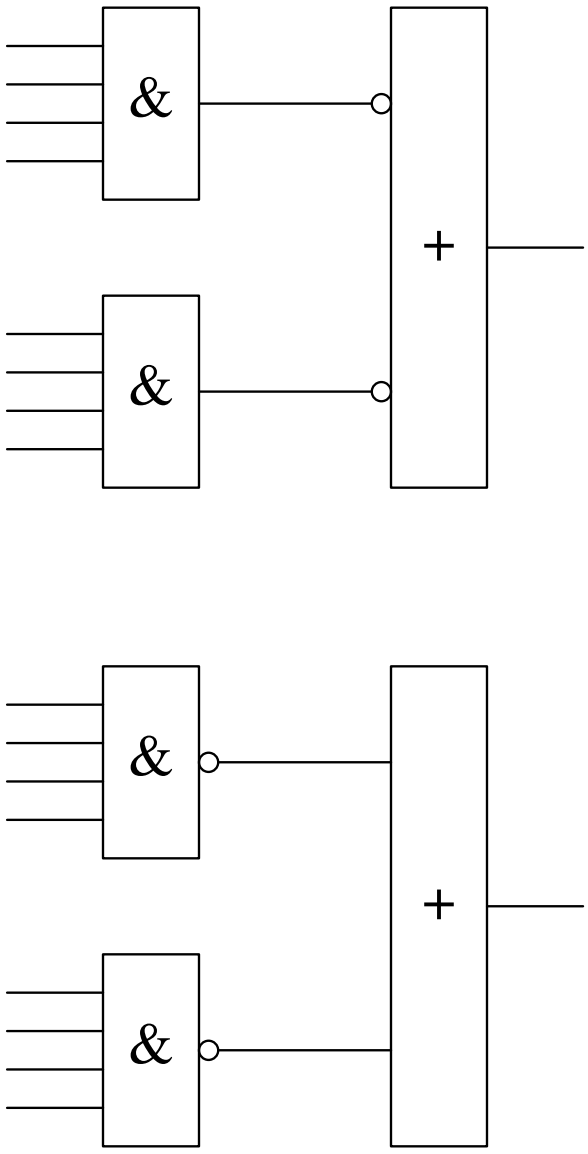
However, transistors have an "on" resistance that adds up when the transistors are connected in series.
This limits the fan-in, typically to four for NOR gates and six for NAND gates.

Transistors can be designed to reduce the resistance.
Beyond the family fan-in limit, gates with larger numbers of inputs are designed by connecting gates with fewer inputs.

Example: An 8-input NAND gate.

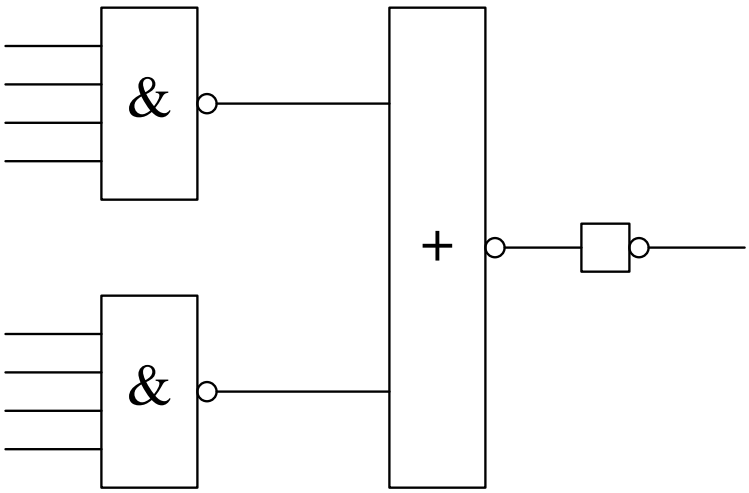


This design requires two inverters to implement AND gates using NAND gates.



This design requires one inverter to implement an OR gate using a NOR gate.

8-input NAND gate:



14.2. Electrical Behavior of CMOS Circuits

Understanding the electrical behavior of circuits is important for ensuring that the digital abstraction is valid, and that the circuits designed based on it will work correctly and reliably.

We need to consider:
Static behavior - situations where the inputs and outputs are not changing.
Dynamic behavior - situations where the inputs and outputs are changing.

The logical and electrical characteristics of a discrete device are given by the manufacturer in a *data sheet*.

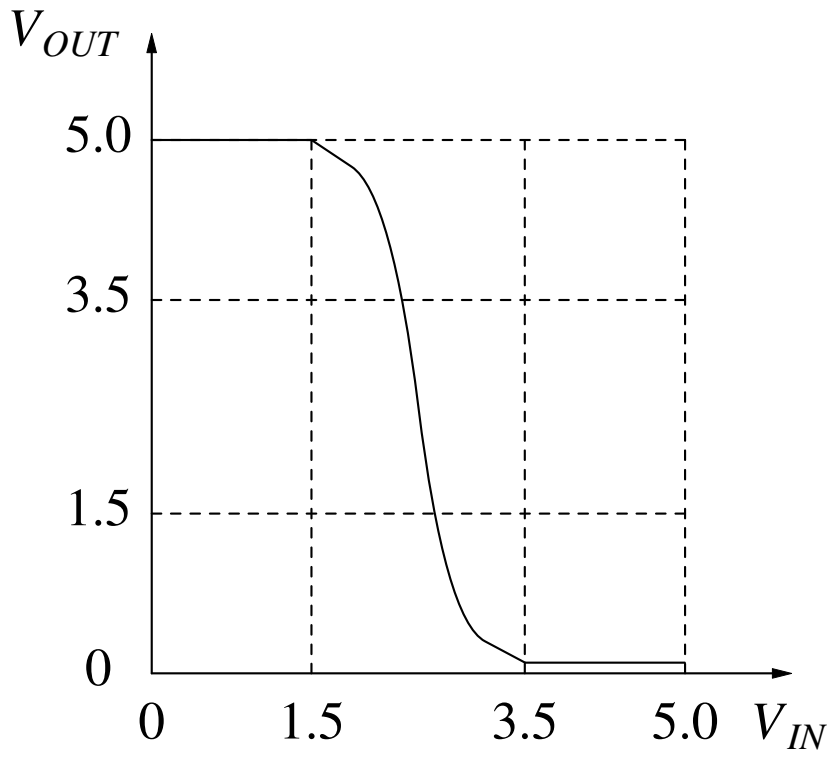
After we go through the important characteristics, the data sheet on page 749 of the textbook should make sense.

14.3. CMOS Static Electrical Behavior

Our earlier analysis of an inverter yielded the following results (assuming V_{CC} = 5V):

V_{IN}	V_{out}
0V	5V
5V	0V

The complete input-output transfer characteristic, called a *voltage transfer diagram*, has the following form:



The curve may change (be flatter, or be shifted) depending on:
power-supply voltage, temperature,
output loading, manufacturing variations.

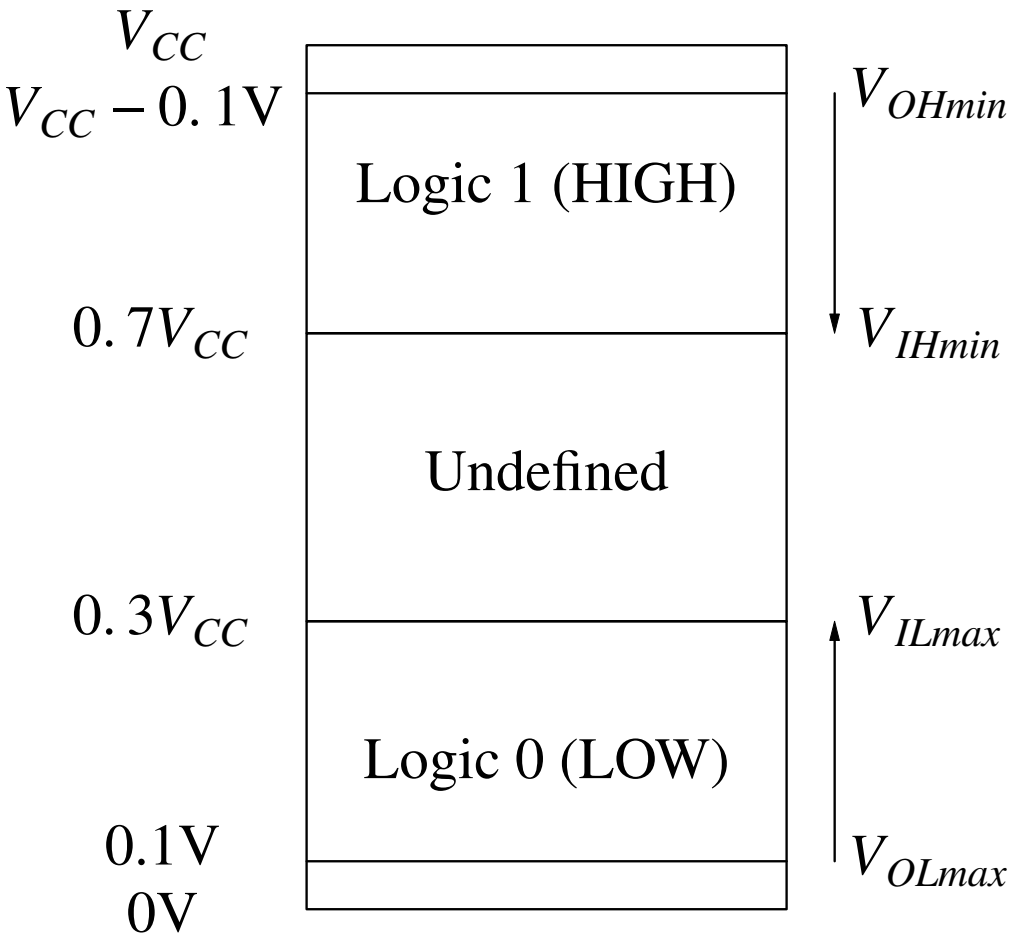
The manufacturer specifies the following parameters taking into account worst case situations:

V_{OHmin} - The minimum output voltage produced as a HIGH. Example: $V_{CC} - 0.1$V.

V_{IHmin} - The minimum input voltage guaranteed to be recognized as a HIGH.
Example: $0.7V_{CC}$.

V_{OLmax} - The maximum output voltage produced as a LOW. Example: GND + 0.1V.

V_{ILmax} - The maximum input voltage guaranteed to be recognized as a LOW. Example: $0.3V_{CC}$.


V_{CC}
$V_{CC} - 0.1\text{V}$
Logic 1 (HIGH)
V_{OHmin}
$0.7V_{CC}$
V_{IHmin}
Undefined
$0.3V_{CC}$
V_{ILmax}
Logic 0 (LOW)
0.1V
V_{OLmax}
0V

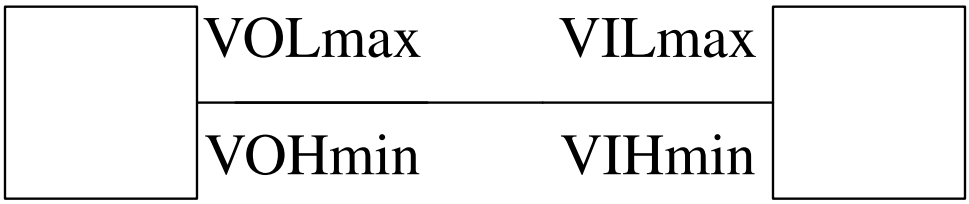
DC noise margin is a measure of the amount of noise it would take to corrupt a worst-case output voltage into a value that may not be recognized properly as an input.

For LOW voltages, the noise margin is

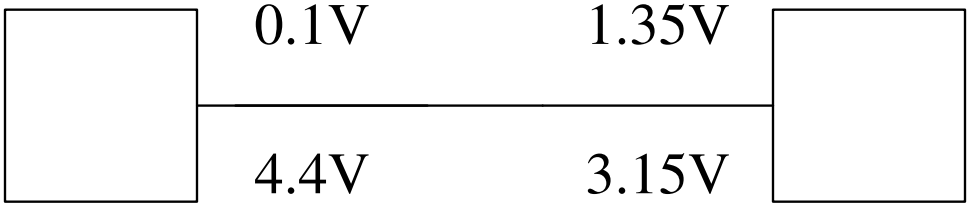
$$V_{ILmax} - V_{OLmax}.$$

For HIGH voltages, the noise margin is

$$V_{OHmin} - V_{IHmin}.$$



Using data from the data sheet on page 749:



$V_{ILmax} - V_{OLmax} = 1.25\text{V}.$
$V_{OHmin} - V_{IHmin} = 1.25\text{V}.$

Inputs of CMOS gates have very high resistance and they consume very little current, called leakage current.

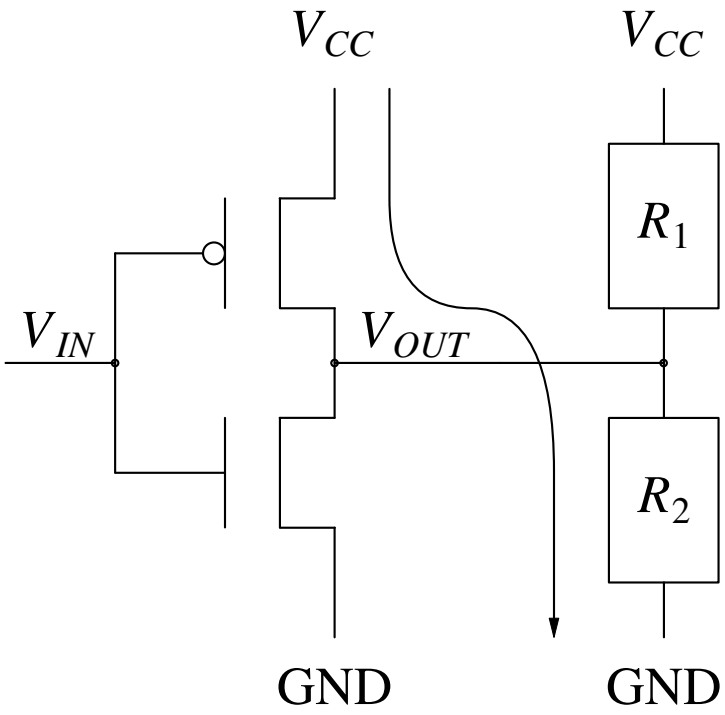
The maximum leakage current is specified by the device manufacturer as follows:

I_{IH} - the maximum current that flows into an input with a HIGH voltage.

I_{IL} - the maximum current that flows into an input with a LOW voltage.

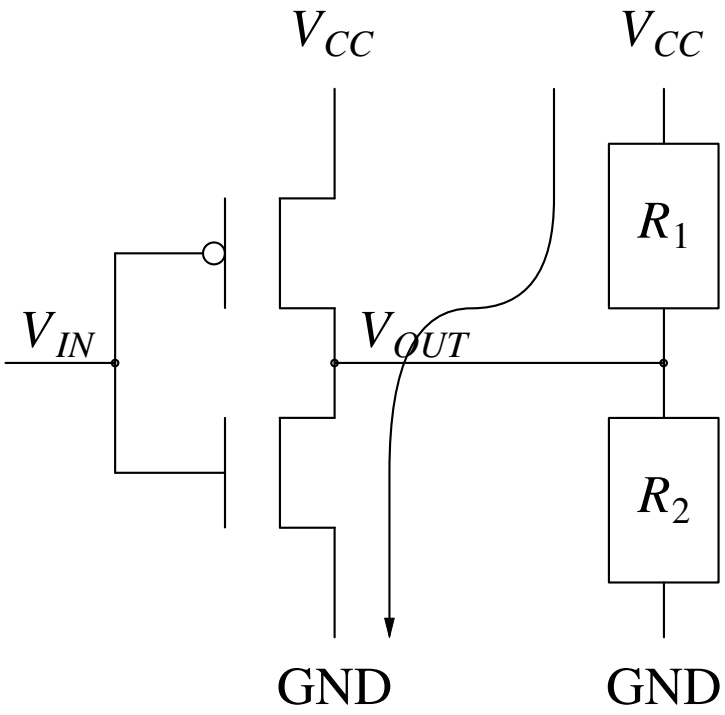
Other types of devices may have lower resistances and they may consume more current. When such a device is connected to the output of a CMOS gate, we call it a *resistive load* or a *DC load*.

A resistive load causes a voltage drop. As a result:
A LOW output voltage may be higher than a CMOS output LOW.
A HIGH output voltage may be lower than a CMOS output HIGH.



When $V_{IN} = 0$V:
The NMOS resistance is very high.
The PMOS resistance is very low.
Without the load, V_{OUT} is close to 5V.

With the load, there is non-trivial current flowing through the PMOS transistor and R_2.
This results in a voltage drop that reduces V_{OUT}.



When $V_{IN} = 5$V:
The PMOS resistance is very high.
The NMOS resistance is very low.
Without the load, V_{OUT} is close to 0V.

There is non-trivial current flowing through R_1 and the NMOS transistor.
This results in a voltage drop that increases V_{OUT}.

Manufacturers specify a maximum load for the output under HIGH and LOW voltages, and guarantee a worst-case output voltage for this load.

The load is specified in terms of current drawn:

I_{OLmax} - the maximum current that the output can sink when it is LOW while still maintaining an output voltage no higher than V_{OLmax}.

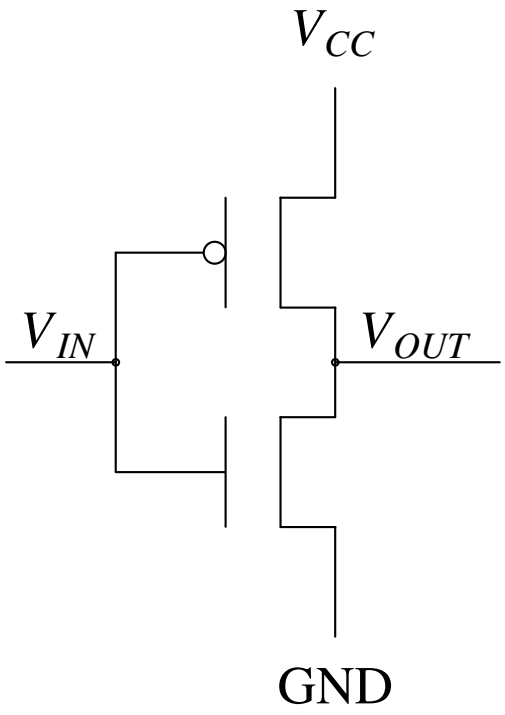
I_{OHmax} - the maximum current that the output can source when it is HIGH while still maintaining an output voltage no higher than V_{OHmin}.

Different values may be specified for CMOS and other loads.

Without a resistive load, the current flowing through the output of a CMOS circuit in steady-state is very low.
This is a result of the fact that one of the transistors is off, and has a very high resistance.
The power dissipation is very low.

The current flowing through a resistive load implies that power is dissipated even in steady-state, when inputs and outputs are not changing.

Non-trivial current may be obtained with non-ideal inputs even without resistive loads. A resistive load will make it worse.



When $V_{IN} = 3.5\text{V}$ (instead of 5V):
The PMOS resistance is high but not very high.
The NMOS resistance is low but not very low.
V_{OUT} is not as close to 0V as with an ideal input.
There is current $I_{nonideal}$ flowing through the transistors.
The gate dissipates power even in steady-state $P_{nonideal} = I_{nonideal} V_{CC}$.

Fanout

The *fanout* of a logic gate is the number of inputs that the gate can drive without exceeding its worst-case loading specifications.

The DC fanout considers the case where inputs and outputs are stable.

The AC fanout considers the case where inputs and outputs are changing.
In this case the gate needs to charge or discharge capacitances.
Its speed will be lower with a higher fanout.

Example of DC fanout:
With a LOW output voltage, the maximum output current of a CMOS gate driving another CMOS gate is $I_{OLmaxC} = 20\mu A$.
The maximum input current drawn by an input is $I_{IL} = 1\mu A$.
The gate can drive at most 20 inputs.

A HIGH-state fanout is computed in a similar way.

After computing a LOW-state fanout and a HIGH-state fanout, the overall fanout is the minimum of the HIGH-state and LOW-state fanouts.

Effects of Loading

• With a LOW output voltage, the output voltage V_{OL} may increase beyond V_{OLmax}.

• With a HIGH output voltage, the output voltage V_{OH} may decrease below V_{OHmin}.

• Propagation delay to the output may increase beyond its specifications.

• Output rise and fall times may increase beyond their specifications.

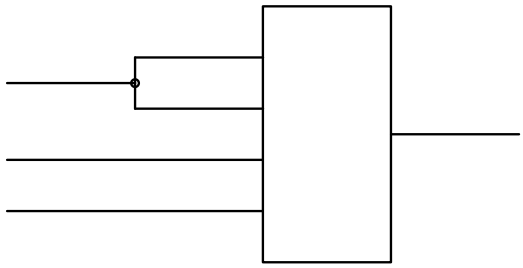
• The operating temperature of the device may increase, reducing its reliability and eventually causing failure.

Unused Inputs

Unused inputs may occur when designing with discrete components, an n-input gate is needed, but only m-input gates are available, for $m > n$.

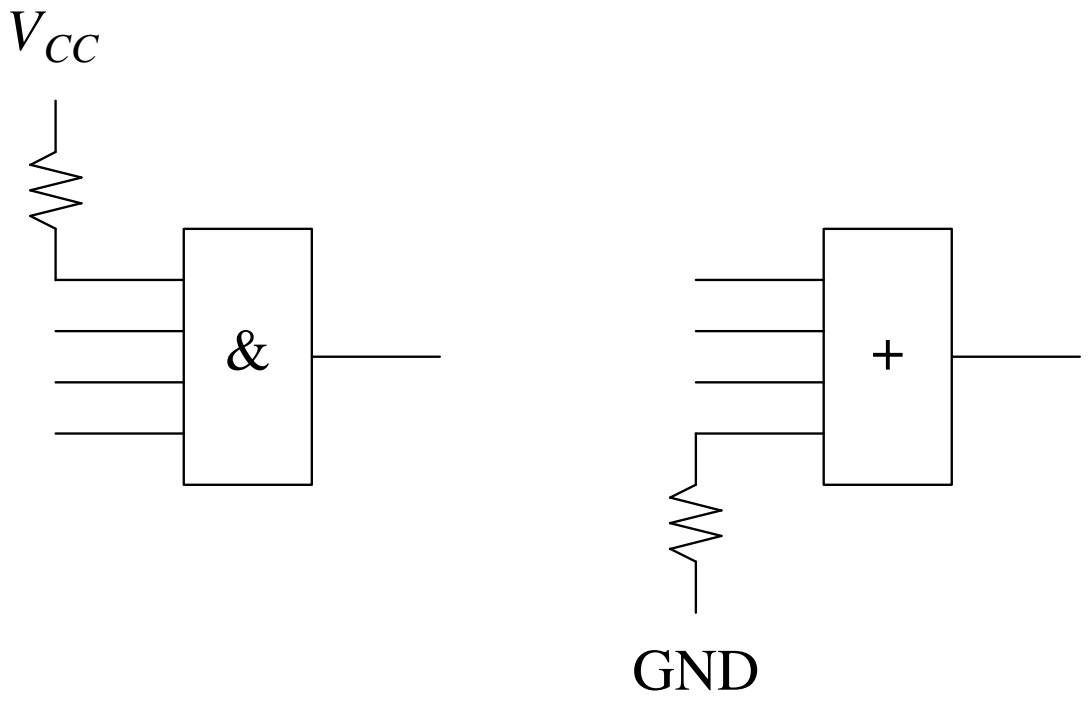
Such inputs cannot be left floating since a small amount of noise may make them appear to have a HIGH voltage.

Solution 1: Tie unused and used inputs together to reduce the number of used inputs.



This solution increases the capacitive load on the driving gate.

Solution 2: Tie unused inputs to constant values.
For NAND or AND gates the constant should be 1.
For NOR or OR gates the constant should be 0.
A small resistance is sometimes used for the connection.



14.4. CMOS Dynamic Electrical Behavior

The dynamic behavior determines the speed and power consumption of a device.

Speed depends on two characteristics, transition time and propagation delay.

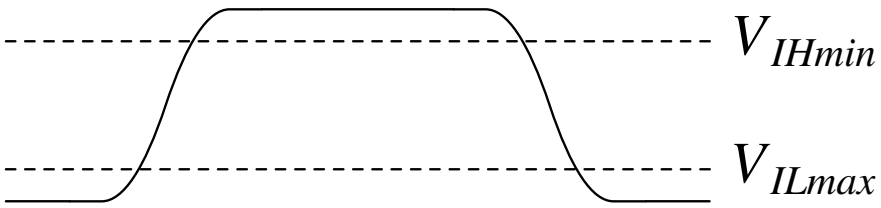
Transition Time

The *transition time* is the amount of time it takes for the output of a device to change from one voltage level to another.

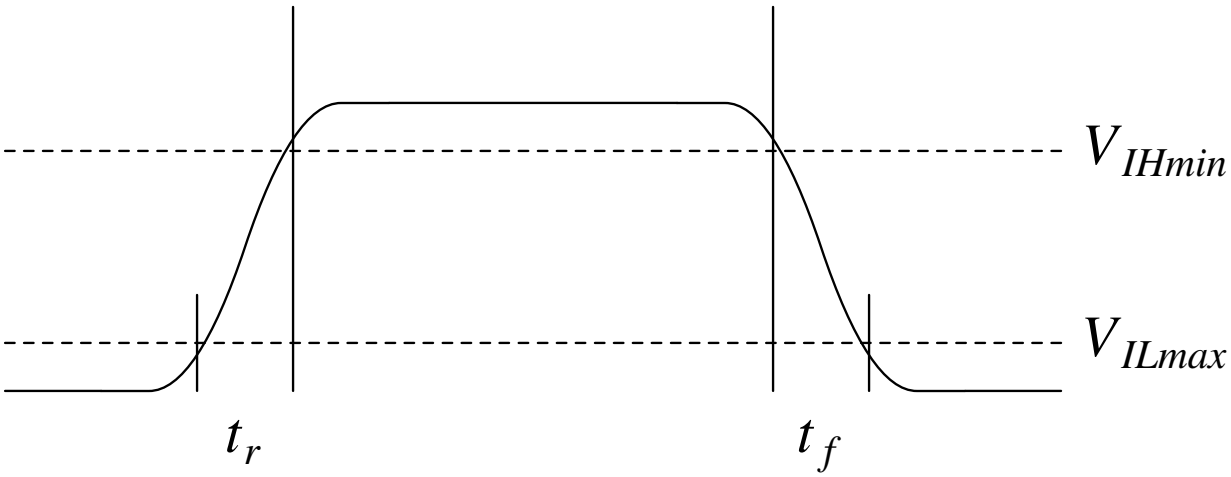
Zero delay transitions:

Due to wire and component capacitances, changes do not occur in zero time.
A more accurate model:

An even more accurate model allows only smooth changes:



The rise and fall times are the amounts of time it takes the output voltage to go through the undefined range between LOW and HIGH.



The rise and fall times depend on:
The on-resistances of the transistors.
The load capacitance.
A higher load capacitance means higher transition times.

Load capacitances come from three sources:

• Capacitances internal to the device.

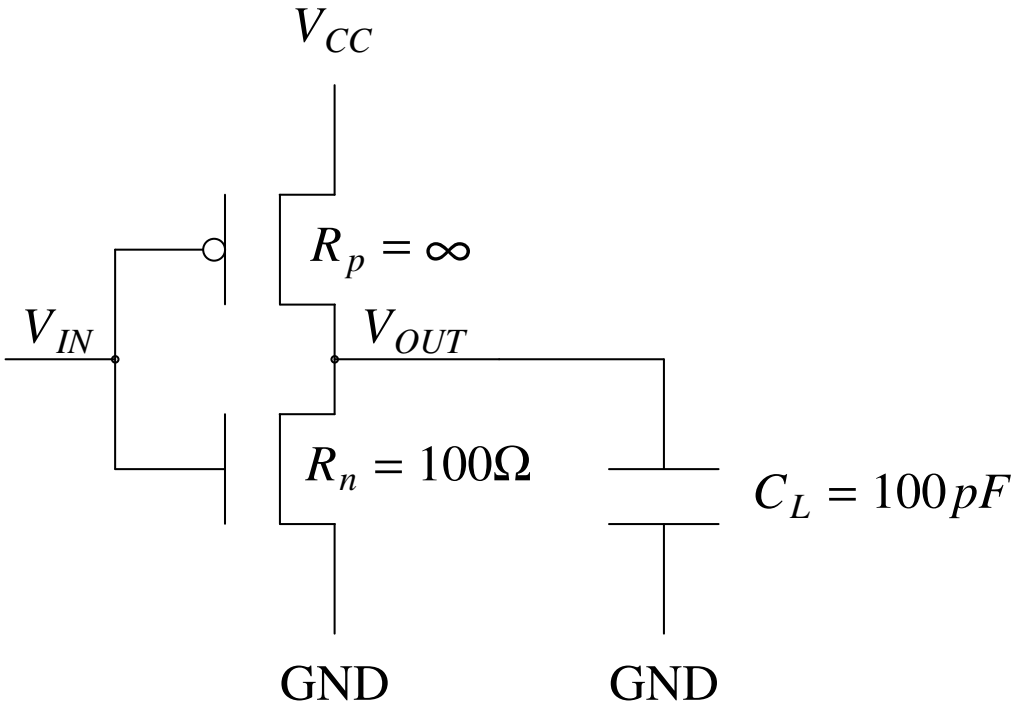
• The wires connecting the output to other devices.

• The inputs of other devices that the output drives.

Computing the fall time:

At time 0, V_{IN} changes from 0 to 5V, and $V_{OUT} = 5\text{V}$.

V_{OUT} is discharged through a circuit that very approximately resembles the following:



The equation describing V_{OUT} is

$$V_{OUT} = V_{CC} \cdot e^{-t/(R_n C_L)}$$

$$t = - R_n C_L \cdot \ln(V_{OUT}/V_{CC})$$

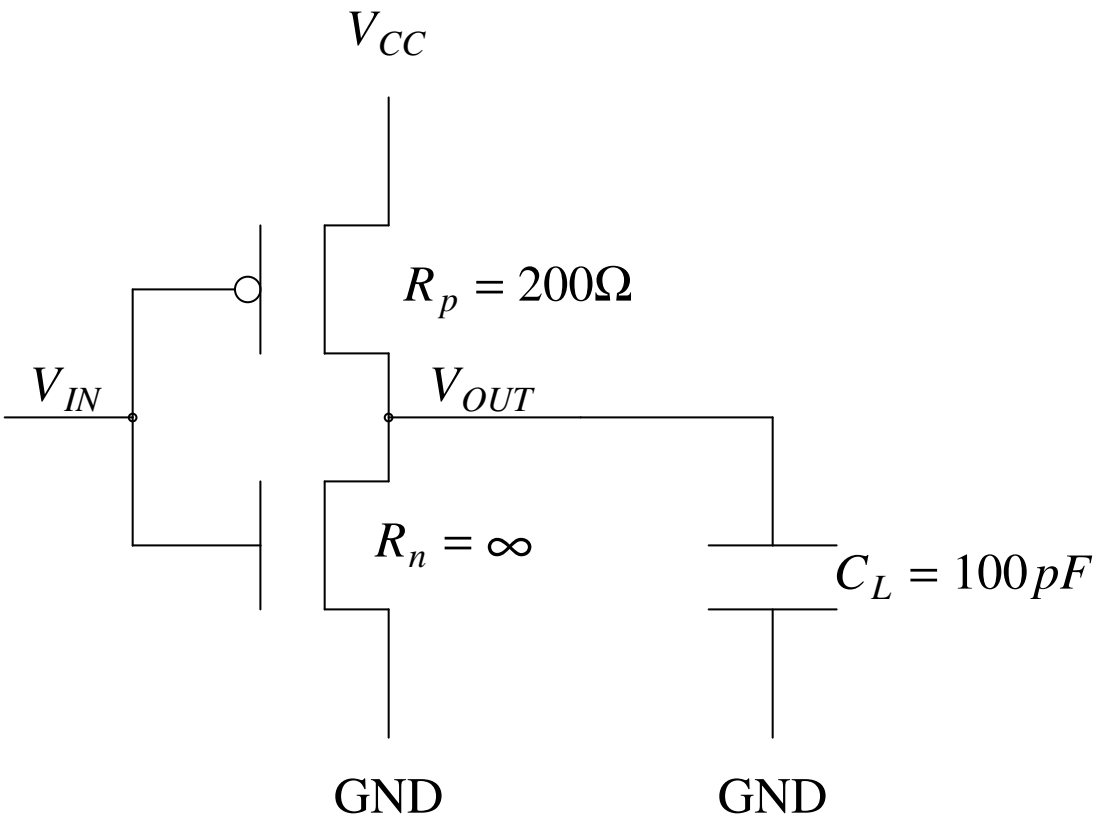
The fall time is

$$t(V_{OUT} = V_{IHmin}) - t(V_{OUT} = V_{ILmax}).$$

Computing the rise time:

At time 0, V_{IN} changes from 5V to 0, and $V_{OUT} = 0$.

V_{OUT} is charged through a circuit that very approximately resembles the following:



The equation describing V_{OUT} is

$$V_{OUT} = V_{CC} \cdot (1 - e^{-t/(R_p C_L)})$$

$$t = - R_p C_L \cdot \ln(1 - V_{OUT}/V_{CC})$$

The rise time is

$$t(V_{OUT} = V_{ILmax}) - t(V_{OUT} = V_{IHmin}).$$

Since R_p is typically higher than R_n, the rise time is typically higher than the fall time.

The rise and fall times increase with the load capacitance C_L.

Minimizing C_L can be done by:
Minimizing the number of inputs driven by a gate.
Careful physical layout of the circuit.

Propagation Delay

A *signal path* is an electrical path from an input signal to an output signal in a logic element.

The *propagation delay* t_p of a signal path is the amount of time it takes for a change in the input signal to produce a change in the output signal.

The propagation delay may depend on:
The specific signal path.
The direction of the input and output transitions.
The values of other inputs.

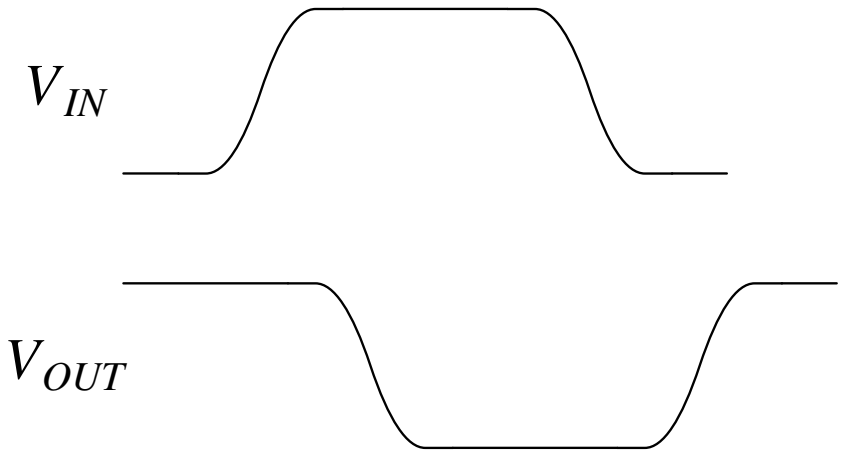
For an inverter:

t_{pHL} - the time between an input change and the corresponding output change when the output is changing from HIGH to LOW.

t_{pLH} - the time between an input change and the corresponding output change when the output is changing from LOW to HIGH.

Rise and fall times cause the transitions from HIGH to LOW and from LOW to HIGH to take non-zero time.

Propagation delays cause V_{OUT} to start changing later than V_{IN}.

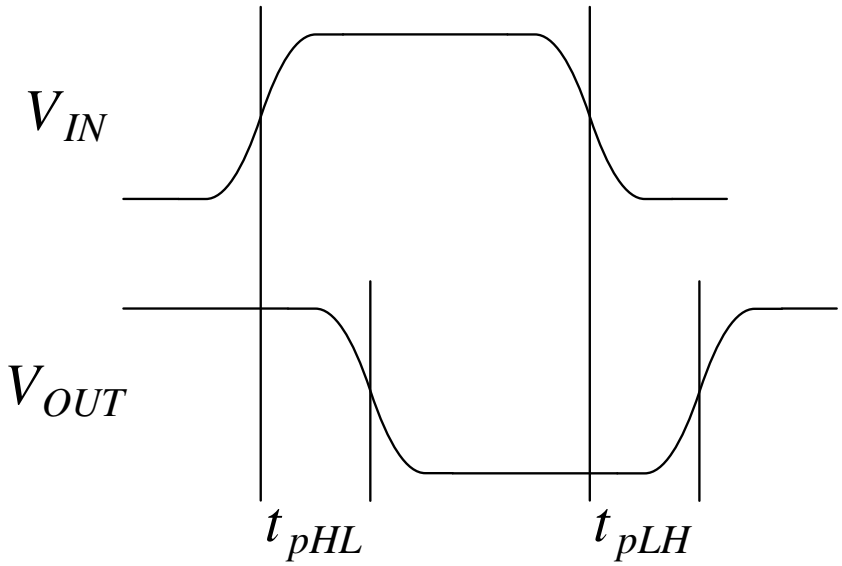


Nonzero propagation delays result from:

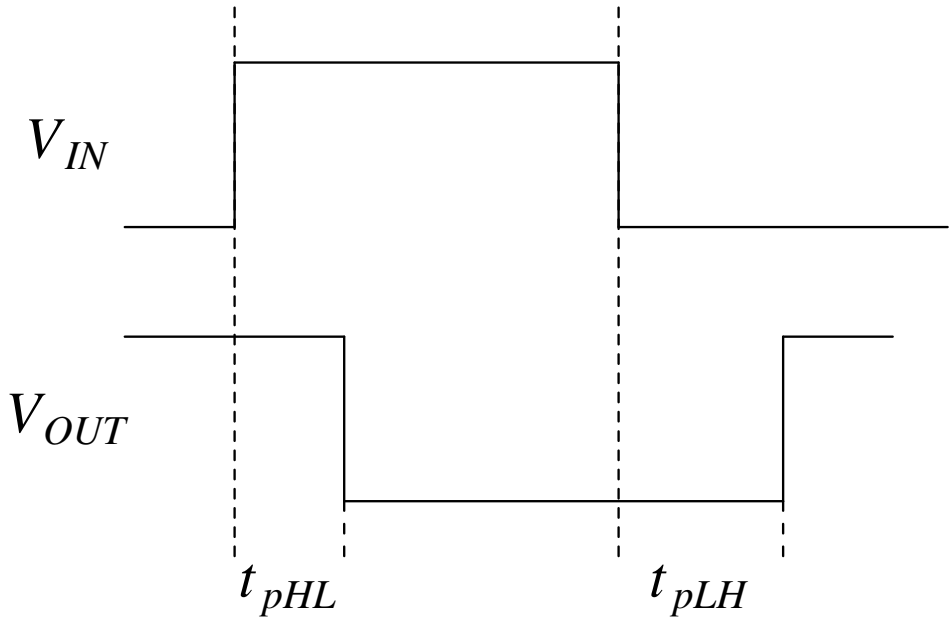
The physics of the device.

The circuit environment (input transition rate, input capacitances, output loading).

To remove the effects of rise and fall times, propagation delays are measured from the mid-points of transitions.



A simpler representation:



Power Consumption

Power dissipation in a device whose outputs are not changing is called static power dissipation or quiescent power dissipation.
CMOS circuits have very low static power dissipation.

Power dissipation during transitions is called dynamic power dissipation.

One source of dynamic power dissipation is the fact that both PMOS and NMOS transistors may be partially on when the input voltage is not close to 0V or V_{CC}.

In this case their total resistance can be low.

Current flows through both transistors from V_{CC} to ground.

The power dissipation P_T can be written as
$P_T = C_{PD} \cdot V_{CC}^2 \cdot f$, where:
f is the transition frequency and represents the speed by which transitions occur.
C_{PD} is a constant that represents physical effects that occur in the device.

The formula for P_T is valid only if the input transitions are fast enough.
This implies maximum rise and fall times.

Another source of dynamic power dissipation is the capacitive load C_L on the output.
The power dissipation P_L can be written as
$P_L = C_L \cdot V_{CC}^2 \cdot f$.

The total dynamic power dissipation is
$P_D = P_T + P_L = (C_{PD} + C_L) \cdot V_{CC}^2 \cdot f$.

Current Spikes and Decoupling Capacitors

When a CMOS output switches between LOW and HIGH, both the PMOS and NMOS transistors are partially on at the same time.
This results in *current spikes*.

Current spikes may result in noise on the power-supply and ground connections, especially when multiple outputs switch at the same time.

The solution is to place decoupling capacitors between V_{CC} and ground on a printed-circuit board.

Inductive Effects

Circuit wiring may have stray inductance.
The voltage across an inductance is proportionate to the rate of change in current.
When output transistors switch very fast, this may result in a voltage drop.
If it is high enough it may cause a HIGH voltage to be too low, or a LOW voltage to be too high.

A stray inductance may also exist in the connections to ground.

If several outputs need to switch simultaneously from HIGH to LOW, there will be significant current through the NMOS transistors and the inductance.

This may cause a voltage drop called *ground bounce*.

Ground bounce changes the internal ground voltage compared to the ground of a printed-circuit board.

It may cause LOW voltages to appear to be undefined or HIGH.

14.5. Other CMOS Input and Output Structures

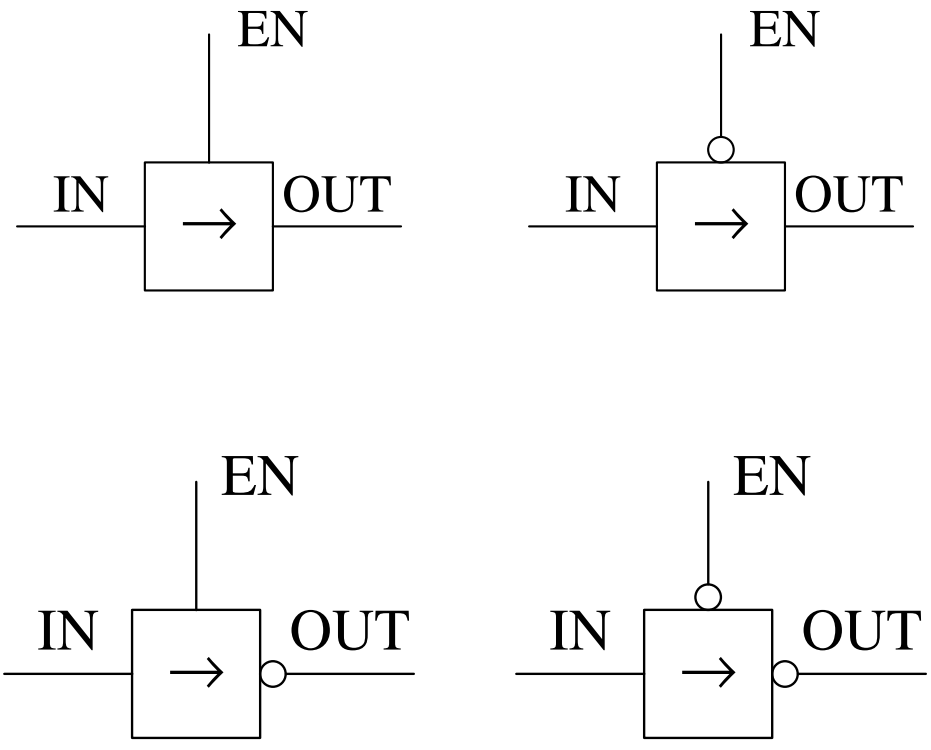
Read:
Sections 14.5.1 and 14.5.2;
Review Lecture Notes 1.

Three-State (Tri-State) Outputs

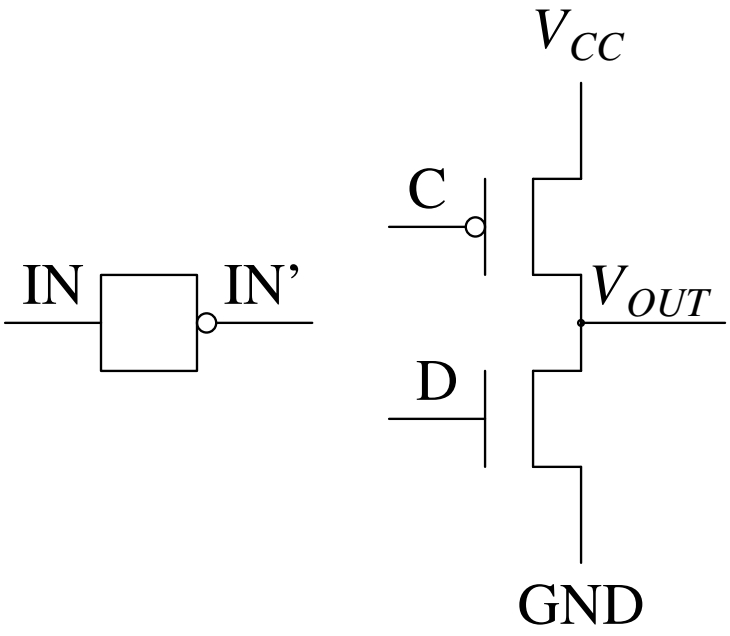
Some outputs have a third electrical state, in addition to LOW and HIGH.
It is called the high-impedance or floating or Hi-Z state.
In this state the output behaves as if it disconnected.
There is only a small leakage current that may flow into or out of the output.
An output with three possible states is called a three-state or tri-state output.

A three-state device has a special input, called output enable or output disable, for placing its output in the high-impedance state.
When the enable input is asserted the device behaves as a buffer (or inverter).
Otherwise the device output is in the high-impedance state.

Logic symbol:



The high-impedance state is created by turning off both the PMOS and NMOS transistors of an output.



EN	C	D
1	IN'	IN'
0	1	0

C = IN' + EN'

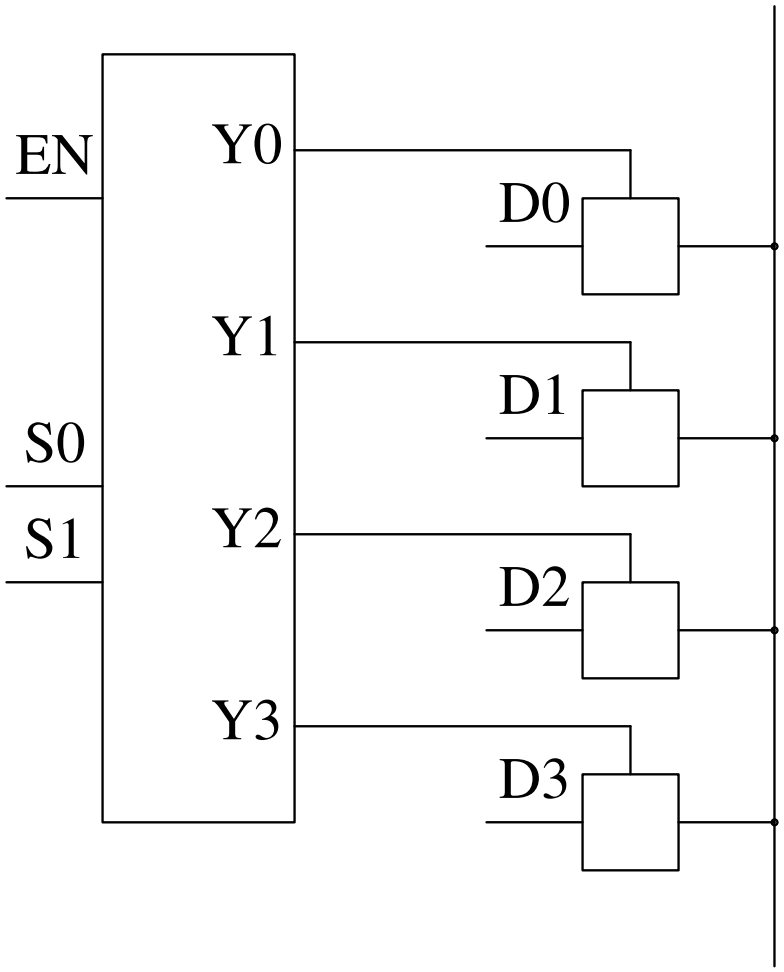
D = IN' · EN

When three-state buffers are placed on the outputs of devices, multiple devices can be connected to the same line (called a bus).

This works as long as only one device writes at any given time, and the other devices have their outputs at the hi-Z state.

A decoder (which we will see later) can be used to set the enable signals of tri-state buffers driving a bus.

Example: Four devices driving a bus.
Only their output buffers are shown.



Devices with three-state logic are typically designed so that the output enable delay (from Hi-Z to LOW or HIGH) is longer than the output disable delay (from LOW OR HIGH to Hi-Z).

When switching between two devices, this ensures that they are not both enabled at the same time.

However, this safety margin may disappear due to variations that cause one device to be faster than another.

A possible solution is to design the control logic such that there is enough time between disabling a device and enabling another.
A possible control sequence:

EN	S0	S1
0	x	x
1	0	0
0	x	x
1	1	0
0	x	x
1	1	1
0	x	x
1	1	0

Transceiver

A *bus transceiver* is a device used for connecting two buses, A and B.

It allows bus A to write to bus B, and bus B to write to bus A.

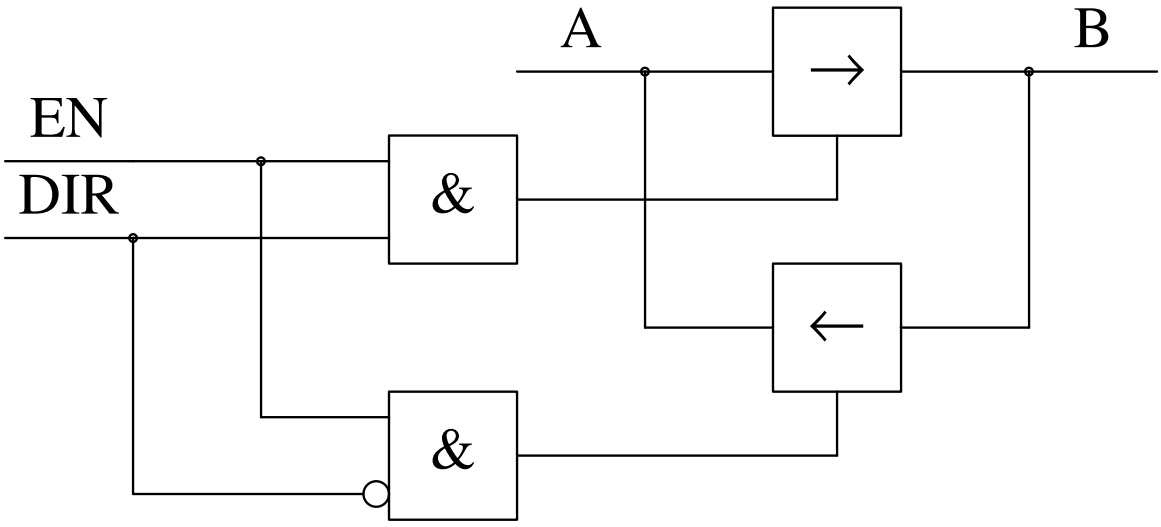
The pins on one side of the transceiver are connected to bus A, and the pins on the other side are connected to bus B.

The transceiver contains pairs of three-state buffers connected in opposite directions between each pair of pins.

This is also a way to create input/output pins that can transfer data in either direction.

Example:

EN	DIR	operation
1	1	data flows from A to B
1	0	data flows from B to A
0	x	data does not flow between A and B


A
B
EN
DIR
&
&

There is a leakage current associated with a CMOS three-state output in its Hi-Z state.
This current must be considered when calculating the maximum number of devices that can be placed on a three-state bus.

Read:
7.1. Three-State Devices
14.6. CMOS Logic Families
14.7. Low-Voltage CMOS Logic and Interfacing