ECE 270 (Spring 2022)

Homework 7

Due on 03/06/2022 (Sunday) by 11:59 pm sharp on BrightSpace.

Only legibly handwritten or typed submissions in PDF format are allowed.

1. What is the difference between blocking and non-blocking assignments? In what type of circuits do we use each type of the assignment? (5 points + 5 points)

2. Write the outputs for the below statements.

   (a) 6'b101010 << 3 (2.5 points)

   (b) 6'b111010 >> 4 (2.5 points)

   (c) 7'b1110011 >>> 2 (2.5 points) (Arithmetic Right Shift)

   (d) 5'b11011 <<< 4 (2.5 points) (Arithmetic Left Shift)

3. Consider a small Verilog code snippet as below:

```
wire [5:0] in; // line1

wire [5:0] out1 ; //line 2

wire [5:0] out2; //line3

out1 = {in[3:0], 2'b0}; //line4

out2 = {2'b0, in[5:3]}; //line5
```

   (a) Which operator is used in the lines 4,5 of the above code? (3 points)

   (b) What is the relation between the signals "in" and "out1" ? (3 points)

   (c) What is the relation between the signals "in" and "out2" ? (4 points)

4. If multiple values are assigned to the same signal in a verilog combinational always block, what is the signal's value when the always block completes execution: (10 points)

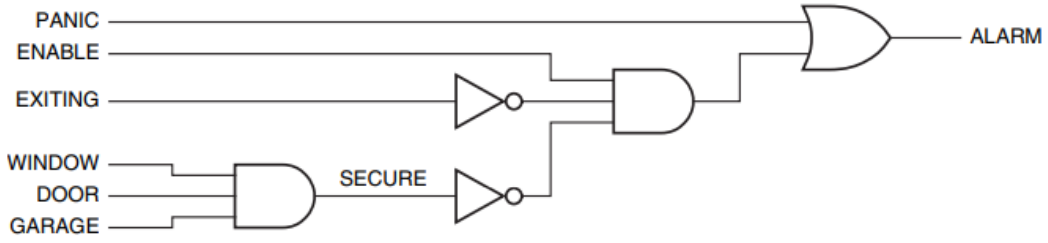
(a) the AND of all values assigned

(b) the OR of all values

(c) the last value assigned

(d) it depends

5. Consider the below circuit.



(a) Write a Verilog module to implement the above circuit in a behavioral model. (5 points)

(b) Write a Verilog module to implement the same circuit in the dataflow model. (5 points)

6. Write a Verilog module that implements a tri-state buffer using

(a) Dataflow Model (5 points)

(b) Behavioral Model (5 points)

7. Write the structural verilog code for the function C(A,B) = ∑ (0,3) considering that the verilog library contains only AND, OR and NOT gates (Hint: Get a Sum of Products expression from the function and write a structural code for it). (10 points)

8. Consider the below code snippet. (10 points)

```
always@(sel == 1'bx) begin
if (sel)
out = 1;
else
out = 0;
end
```

What do you think is the output of the code? Explain.

9. John has a four-digit lock to his apartment. Each digit in the lock can only take 0 or 1. The lock opens only when the first two digits equals the next two digits. Can you help John by finding a logic function that opens the lock? (10 points).

10. Write a small verilog module to implement the function in Question 9 (can be in any model). (10 points).