RAGHAV RASTOGI

498/C-1, Ground Floor, Palam Vihar, Gurugram – 122017
+91-9873915183
raghavrastogi08@yahoo.co.in

OBJECTIVE:

Seeking a position as an engineer which offers key participation, team oriented tasks and challenges that help in technical skill enhancement and also to become an asset to the organization by striving towards the attainment of its goals and hence valuably contribute to its success.

ACADEMIC DETAILS:

QUALIFICATION	SCHOOL/ COLLEGE	BOARD/ UNIVERSITY	CGPA/ PERCENTAGE	YEAR OF PASSING
B.Tech (ECE)	Manav Rachna University, Faridabad	Manav Rachna University, Faridabad	9.19 (Till 7th Semester.)	2019
AISSCE	DAV Public School, Gurgaon	CBSE	70.8%	2015
AISSE	DAV Public School, Gurgaon	CBSE	74.1%	2013

SKILLS & INTERESTS:

Language **:** Verilog, SystemVerilog (SV), VHDL, Python, TCL/TK, MATLAB, C, .Net
Software **:** ModelSim, Xilinx ISE, Tanner EDA, Cadence OrCAD, LabView, Proteus Design Suit.
Operating Systems **:**Windows 7/8/10, LINUX (Ubuntu 18.04).
Areas of Interest **:** Digital System Design, Design and Verification, VLSI, Microprocessors, Digital Electronics, Automation.

WORK EXPERIENCE:

Company : 3ST Technologies Pvt. Ltd.
Position : Intern.
Duration : Ongoing (January 2019 – Present)

Internship related to digital design and verification by using Verilog and SystemVerilog. Automating tasks via bash, Python and TCL scripting. Designing UI in TCL/TK and Python/TK.

Company : Microtek India Private Limited.
Position : Summer Intern.
Duration : 1 Month (June 2018 – July 2018)

Verification, repair and testing of E-rickshaw chargers, PCB tracing on OrCAD and introduction to PIC series microprocessors was done during the period of one month.

PROJECTS:

1. **RISC-V based microprocessor design and verification.**
   Duration : February 2018 – December 2018
   Technology : RISC-V RV32I and RV32M ISA, Verilog and SystemVerilog (SV).
   A 32 bit RISC-V ISA based Microprocessor with selected instructions from RV32I and RV32M is implemented. It is a 5 stage pipelined microprocessor with external memory. The design of the microprocessor is a combination of behavioural and structural implementation, coded in Verilog. The verification of the microprocessor is done using SystemVerilog.
2. **Review: Shortcoming of Bulk MOSFET and Advantages of FinFET**
   Duration : Under Review at FLAME 2018 (March 2016 - Present)
   Technology : Silvaco TCAD
   This is a Literature Review project in which a bulk MOSFET is compared against various types of FET's such as Multi Gate FET's (Omega – FET, Pi – FET, Gate All Around FET, Cylindrical Gate All Around FET) and SOI based technologies. This project discusses the disadvantages/problems faced by reducing the size of Bulk MOSFET as compared to other new technologies.
3. **Home Automation**
   Duration : 3 Months (June 2015 – August 2015)
   Technology : Arduino and Android (MiT Appinventor).
   Home automation system designed on Arduino using Bluetooth. The system contains a temperature sensor, relay modules and a LCD display. The system can automatically turn the heating and cooling device on or off depending on a pre-set temperature. A mobile device (Android) can also be used to switch on or off the light and fans. The LCD display is a small information panel which shows the current temperature and the status of all the connected devices.
4. **Autonomous Robot**
   Duration : 1 Month (May 2016 – June 2016)
   Technology : Arduino and Android (MiT Appinventor).
   A total autonomous robot was designed using Arduino and ultrasonic sensors. The ultrasonic sensor in the bot sensed the obstacles in front of it and used to program its way accordingly. The distance between the obstacles and bot were printed on a 16x2 LCD display and the values were also displayed on Android phone using an app developed on MITappinventor and communicated over by using a Bluetooth module.

CERTIFICATIONS:

1. Hardware Modelling using Verilog from IIT Kharagpur (NPTEL) on October 2018.
2. Innovations, Business Models and Entrepreneurship from IIT Roorkee (NPTEL) on October 2018.
3. Proficiency in English from Aspiring Minds on September 2018.
4. Sustainable Strategies from Purdue University on July 2016.

ACHIEVEMENTS:

1. Scholarship from Manav Rachna University.
2. Zonal Winner of BrainTech – 2017 on Networking and Cyber Security Championship organized by Azure Skynet.
3. 1st Runner up in Zenith – 2016, Hosted by Manav Rachna Educational Institution's CDC department.

TRAITS:

- Optimistic and Self-motivating.
- Quick Learner.
- Problem Solving.
- Ability to work with team under pressure.

PERSONAL INFORMATION

Father's name : Sandeep Rastogi
Date of Birth : 7th September 1997
Marital Status : Single
Religion : Hindu
Nationality : Indian
Communication Language : English and Hindi

HOBBIES:

- Multiplayer computer gaming (Favourite Titles: CSGO, Battlefield 4/3, PUBG and Tom Clancy's Universe).
- Listening To Music (Favourite Genre: Dubstep, Metal, Alternate, Pop).
- Badminton.