Memory Consistency Models

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  - One common approach is to apply synchronization.
  - But the degree of synchronization must be minimal.
  - Basically synchronization controls the order of read and write to shared memory locations.
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- The objective.
  - Less compromise on performance - With less degree of synchronization shall we get acceptable output ????
  - Arguing about the correctness of the program.

Memory Model

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- Essentially, a **Memory Model** defines the legitimate orderings of read and write to memory locations.
  - A strict memory model - Easy to argue about correctness, but restricts optimizations (both at compiler and hardware level).
  - A relaxed memory model - More opportunities for optimizations, but not easy to argue correctness.

Sequential Consistency (SC)

- Uniprocessor - A "read" returns the last "write" in program order.
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- **Sequential consistency** - An intuitive extension of uniprocessor model.
  - **Program order**: Each core executes statements in program order.
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Red Thread	Blue Thread
X = 1;	Y = 1;
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- Some possible interleavings.

Execution 1	Execution 2	Execution 3
X = 1;	Y = 1;	X = 1;
r1 = Y;	r2 = X;	Y = 1;
Y = 1;	X = 1;	r1 = Y;
r2 = X;	r1 = Y;	r2 = X;
//r1 == 0;	//r1 == 1;	//r1 == 1;
//r2 == 1;	//r2 == 0;	//r2 == 1;

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- Too much restriction for hardware and compiler optmizations
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  - Program order: (Refers to different memory locations)
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    - Read others' write early.
  - Write atomicity and program order.
    - Read own write early

Total Store Order (TSO)

Definition [2]:

1. A read can complete before an earlier write to a different address.
2. A read can not return the value of a write by another processor unless all processors have seen the write.
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- Some possible interleavings (in addition to that of SC).

Time	Execution 1
t_1	r1 = Y;
$t_2 = t_1 + \delta$	X = 1;
$t_2 = t_1 + \delta$	Y = 1;
$t_3 = t_2 + \delta$	r2 = X;
	//r1 == 0;
	//r2 == 1;

- Effect of 1: It is possible to reorder read to Y before write to X.
- Effect of 2: It is impossible to get value of r2 as 0, by reading 0 from X, because an earlier write to X by Red thread should have seen by the Blue thread.

Relaxed Consistency (RC)

- Same program may exhibit more executions on a relaxed model than SC [3].
- Let T_{Π}^{Y} be the set of executions on memory model Y. Then $T_{\Pi}^{Y} \subset T_{\Pi}^{SC}$ [3].
- To verify relaxed executions T_{Π}^{Y}, verify following two problems.
  - Use standard verification methodology for concurrent programs to show that the executions in T_{Π}^{SC} are correct.
  - Use specialized methodology for *memory model safety* verification showing that $T_{\Pi}^{Y} = T_{\Pi}^{SC}$.
  - The program is $Y - safe$ if $T_{\Pi}^{Y} = T_{\Pi}^{SC}$.

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Linearisability

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