

# Memory Consistency Models

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  - One common approach is to apply synchronization.
  - But the degree of synchronization must be minimal.
  - Basically synchronization controls the order of read and write to shared memory locations.
  - Without sychronization the order of read and writes may be altered either by compiler (optimizations) or by hardware for better performance.

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- The objective.
  - Less compromise on performance - With less degree of synchronization shall we get acceptable output ????
  - Arguing about the correctness of the program.



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- Eliminating gap between expected behaviour (by the programmer) and the actual behaviour.
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## Sequential Consistency (SC)

- Uniprocessor - A "read" returns the last "write" in program order.
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- **Sequential consistency** - An intuitive extension of uniprocessor model.
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- An Example [?]

Initially $X = Y = 0$	
Red Thread	Blue Thread
$X = 1;$	$Y = 1;$
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- Some possible interleavings.

Execution 1	Execution 2	Execution 3
$X = 1;$	$Y = 1;$	$X = 1;$
$r1 = Y;$	$r2 = X;$	$Y = 1;$
$Y = 1;$	$X = 1;$	$r1 = Y;$
$r2 = X;$	$r1 = Y;$	$r2 = X;$
// $r1 == 0;$	// $r1 == 1;$	// $r1 == 1;$
// $r2 == 1;$	// $r2 == 0;$	// $r2 == 1;$

## Relaxed Consistency (RC)

- SC is hard to realize.
- Too much restriction for hardware and compiler optimizations
- Even SC may not always be produce correct output.
- So we can live with **Relaxed Consistency Models**.
- Potential relaxations
  - Program order: (Refers to different memory locations)
    - Relax  $W \rightarrow R$  program order.
    - Relax  $W \rightarrow W$  program order.
    - Relax  $R \rightarrow R$  and  $R \rightarrow W$  program order.
  - Write atomicite: (Refers to same memory location)
    - Read others' write early.
  - Write atomicity and program order.
    - Read own write early



## Total Store Order (TSO)

Model	$W \rightarrow R$ order	$W \rightarrow W$ order	$R \rightarrow RW$ order	R Others' W Early	R Own W Early
TSO	✓				✓

## Relaxed Consistency (RC)

- Same program may exhibit more executions on a relaxed model than SC [?].
- Let  $T_{\Pi}^Y$  be the set of executions on memory model  $Y$ . Then  $T_{\Pi}^Y \subset T_{\Pi}^{SC}$  [?].
- To verify relaxed executions  $T_{\Pi}^Y$ , verify following two problems.
  - Use standard verification methodology for concurrent programs to show that the executions in  $T_{\Pi}^{SC}$  are correct.
  - Use specialized methodology for *memory model safety* verification showing that  $T_{\Pi}^Y = T_{\Pi}^{SC}$ .
  - The program is  $Y$  – safe if  $T_{\Pi}^Y = T_{\Pi}^{SC}$ .

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