Ultra-Low Power m-Sequence Code Generator using New XOR Gate for Body Sensor Node Applications

S.V.Raghu Sekhar Reddy, T.N.S.R.Revanth and Sarada Musala

***Abstract*—Body Sensor Nodes (BSNs) are devices which are used to improve and monitor human health by means of transmitting and receiving the data through transceivers wirelessly and are nowadays being used extensively in medical fields. The m-Sequence code generator is used in the transceiver in order to achieve spread spectrum transmission technique. In this paper an ultra-low power m-Sequence code generator is proposed in order to achieve low power consumption. The proposed m-Sequence code generator is designed using D-Flip-Flop based Linear Feedback Shift Register (LFSR) and new XOR gate. The proposed new XOR gate has low power dissipation, better PDP and high driving capability. The proposed designs are simulated using Cadence Virtuoso 90nm CMOS technology.**

***Index Terms*—LFSR, m-sequence code, Power consumption, Propagation delay, PDP.**

I. Introduction

BODY Sensor Nodes (BSNs) fall under wireless communication systems. In recent decades, development of wireless communication is growing exponentially and thus the usage of BSNs is also growing eventually. These sensors find their main application in medical field due to their feasibility to place on or inside the human body. They are used to improve and monitor health of the patient continuously and allow diagnosis in early stages.

The main problems that these sensor nodes face are their large power dissipation, limitations of their cell size and the power supply that they require to operate [1]. For such continuous monitoring of patient, sensor nodes must be provided with continuous power supply. To meet the requirement of node, usage of large batteries has to be adapted which will make nodes bulky and uncomfortable to wear. Alternatively, usage of small batteries requires time to time replacement which decreases patient's compliance. To overcome this problem, an alternative technique called Energy Harvesting process is adapted [2]. This process provides a continuous supply of energy by converting ambient energy into electrical energy. This technique can be accompanied by using energy harvesters.

The BSN consists of a sensor to sense the signals and a transceiver to transmit the data as shown in Fig. 1.

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Hence an ultra-low power wireless transceiver is to be designed. Basically, transceiver designs use Spread spectrum for establishing an effective communication link. In this technique, the transmission is done by multiplying user's data with Pseudo Noise (PN) code and spreading it to have a wider bandwidth [3]. In practice, transceivers that use this technique for communication will consume large power due to their complex circuitry. Thus, designing an ultra-low power PN code generator is essential.

Recent studies on techniques for reducing the power consumption made designers to work on various sectors. Among them, Scaling of supply voltage is one of the best successful approaches [4]. Adapting this approach will facilitate designer to design a circuit that consume less power[5-6]. Another approach is the designing of circuits at low power. Due to limitations of first approach the later technique is being used in this paper. Maximum length sequence (m-sequence) code is a type of PN code which is widely used in spread spectrum technique. Various digital circuits use m-sequence code for communication purposes due to its simple nature in designing and stableness in its generation.

In this paper, implementing an m-sequence code generator circuit is done. This circuit will be implemented at transistor level using 90nm CMOS technology. Necessary modifications are made to have ultra-low power consumption.

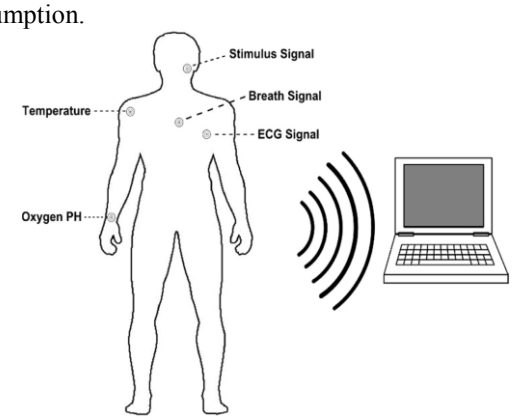

Fig. 1. Schematic of communication through BSNs

The remainder of the paper is structured as follows: Section II describes about design specifications and Section III presents the principles of m-sequence generation. In Section IV, the circuit design and its implementation are introduced. Section V deals with generation of m-sequence code. Power consumptions and comparisons are investigated in Section VI and finally the paper is concluded in Section VII.

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II. DESIGN SPECIFICATION

The m-sequence code is the heart of spread spectrum transmission technique [7]. The baseband signal at the transmitter is produced by multiplying the user data with PN code which will be further handled by modulator. At the receiver end, the same PN code has to be generated to de-spread the received spread signal. The pattern of m-sequence code has to be considered to have reduced power consumption. An important aspect that justifies whether the taken code is a power saving PN code [8] or not is toggle rate. Lesser the toggle rate, higher will be the power saving. Low toggle rate is basically preferred for low power applications which mean that transition activity is less which directly results in low power consumption. A toggle rate value which is not above 0.45 is basically recommended for spread spectrum transmission technique. In this paper, we are aiming to deal with a single user scenario which doesn't actually require a long length code as the interference of data between various users will not exist. Hence, m-sequence code is selected in such a way that it satisfies the above conditions and the code that is preferred in this paper is a 7-bit code '1001110' [9]. The toggle rate of the selected 7-bit m-sequence code is 3/7 = 0.428 which is less than recommend value of 0.45.

III. THE M-SEQUENCE PRINCIPLES

The m-sequence codes are cyclic and consist of 0's and 1's in a pseudo random manner [10]. Such kinds of codes are usually generated using linear feedback shift registers (LFSRs). D- Flip-flops will be connected in a linear format to have the design of a LFSR. Output of selected Flip-flops is connected to a feedback element whose output will be connected to first Flipflop. The feedback element used in this design is XOR gate and a generalized LFSR design is as shown in Fig. 2.

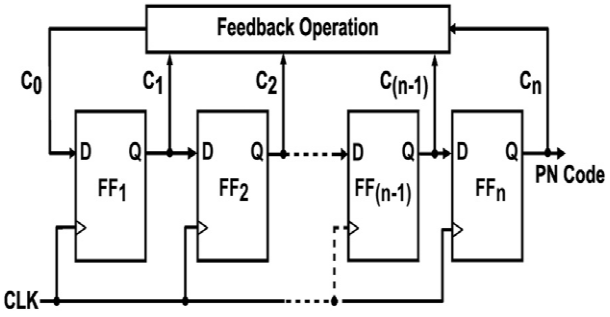

Fig. 2. Generalized schematic of m-sequence code generator.

Activation of FFs is done by using a clock pulse. The length of the code generated can be determined by knowing the number of FFs (N) used. The relation between maximum length of code (L) and number of FFs is given as $L = 2^N - 1$ [11]. A design in which the feedback element is placed in the feedback loop is preferred due to its low power consumption. First input given to the circuit is called as seed input. This input is what actually responsible for the total code sequence generation. A seed signal can be of any format except being an all zero combination as it eventually makes an all zero code sequence.

IV. CIRCUIT DESIGN AND IMPLEMENTATION

This section discusses about the circuit design of m-sequence code generator that generates a 7-bit code sequence of '1001110'. According to the relation between maximum length of code and number of FFs required, we need 3 FFs to design the circuit required. The feedback element used is XOR gate and the feedback taps are made at 1st and 3rd Flipflops as shown in Fig. 6.

A. Flip-flop CMOS design

Among various models of D-FFs, Transmission Gate based D-FF (TGFF) is selected in this circuit [9]. It is selected due to its best properties regarding good power delay product (PDP) values. A positive edge-triggered TGFF is utilized. The suggested FF consists of two latches that are connected in cascade whose schematic diagram is as shown in Fig. 3.

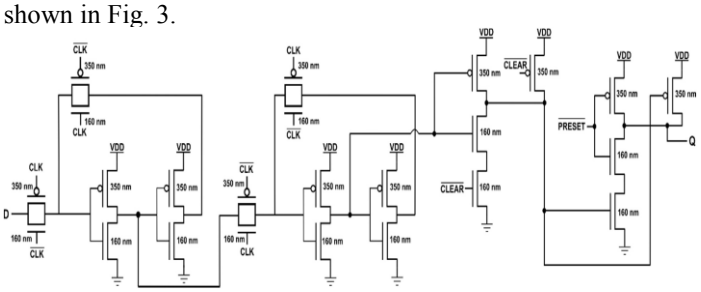

Fig. 3. Design of TG-based D Flip-flop

B. Exclusive-OR gate

The feedback element used in the design of this paper is selected to be a two input exclusive-OR gate (XOR). Various designs of XORs were proposed earlier which have their own pros and cons [12-17]. In this paper, different gates are compared with respect to their pros, cons and the best one is selected for code generator design. A pass transistor logic based XOR is shown in Fig. 4(a). It has very less power consumption at low supply voltages; but it produces poor outputs for some particular input combinations. Another design having an static inverter is shown in Fig. 4(b). Though this design has good driving capability, it shows poor output for input combinations of 01 and also has poor delay for input combination of 00. A design of TG based XOR is shown in Fig. 4(c). This design is better circuit when compared to all designs shown in Fig.4 in context of power consumption, propagation delay at all supply voltages. However, due to presence of static inverter, it occupies larger area. A design In Fig. 4(d), a design using 8 transistors is shown with a good output level at low voltages; however, the output deteriorates at high voltages and also it consumes more power when compared to other designs due to the availability of two static inverters[18]. To surpass this a design of 6 transistors was shown in Fig. 4(e) that has good output and driving capability, it has high power consumption and poor delay characteristics more specifically at low supply voltages. A design that has 4 transistors is shown in Fig. 4(f). Though it is efficient in terms of power consumption, it has poor delay characteristics. When compared, among all the six designs, TG-based XOR is chosen as the better design in terms of less power consumption and PDP values.

C. New XOR gate

In this paper, a new XOR gate design is proposed which can further surpass TG based XOR (Fig. 4(c)) in aspects of power consumption, propagation delay and PDP. The design of modified new XOR gate is shown in Fig. 5. The comparison results of TG XOR and proposed XOR gate are shown in Table [I-III].

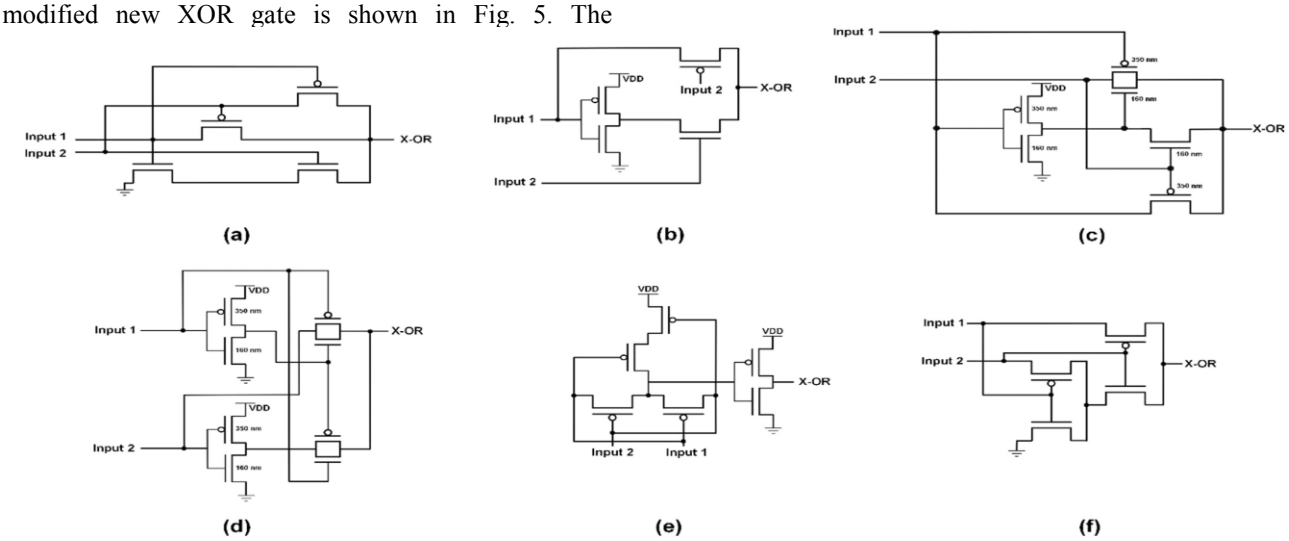

Fig. 4. Designs of various XOR gates

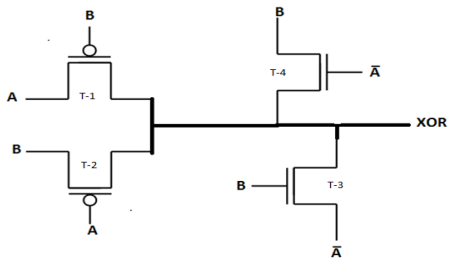

Fig. 5. Design of new XOR gate

It can so hereby be stated that the proposed XOR gate is better for having further more power saving in m-sequence code generator design when compared to TG based XOR.

V. ARCHITECTURE OF 7-BIT M-SEQUENCE CODE GENERATOR

The design of 7-bit m-sequence code generator is as shown in Fig. 6. Feedback XOR element is driven by two inputs coming from 1st and 3rd FFs outputs. The output of feedback XOR element is connected to input of 1st FF.

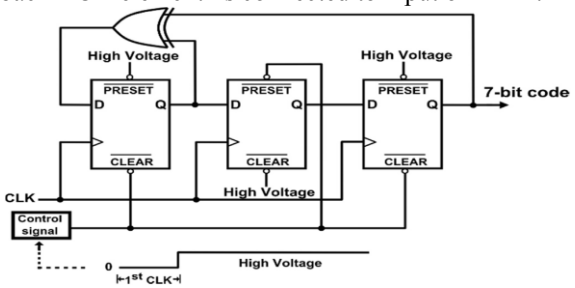

Fig. 6. (100110) 7-bit m-sequence code generator

Seed input signal which controls the code phase is given to CLEAR and PRESET inputs. These inputs are operated to either be activated or be deactivated by using control signal and high voltage.

Control signal is connected to CLEAR of first and third FFs and PRESET of second FF to have a seed input of 010. Control signal is made logic 0 to have its impact on design and is made to logic 1 to have no impact of it on design. Accordingly, control signal is made logic 0 for first clock cycle so that FFs are loaded with 010 at their outputs and then this control signal is made logic 1 to disable its effect on design such that a 7-bit cyclic sequence of 100110 is obtained.

VI. SIMULATION AND RESULTS

The outputs of TG based XOR and new XOR gate discussed in this paper are as shown in the Fig. [7-8]. Both these designs are investigated at same supply voltage of 0.5V to have no bias in characteristics of transient analysis.

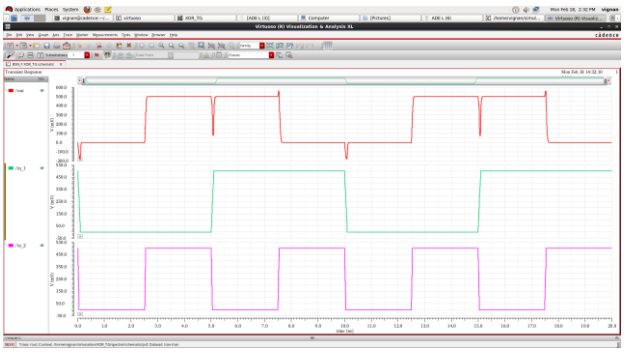

Fig. 7. Transient response of TG based XOR

From the above observed transient response it is clear that both TG based XOR and new XOR gates has full swing. Fig. 11 shows the Layout diagram of new XOR gate. It takes an area of 13.2136µm^2. TGFF is also implemented for its transient response to show the impact of CLEAR and PRESET inputs on output of FF. The

transient response is implemented at clock frequency of 200MHz and a supply voltage of 0.5V.

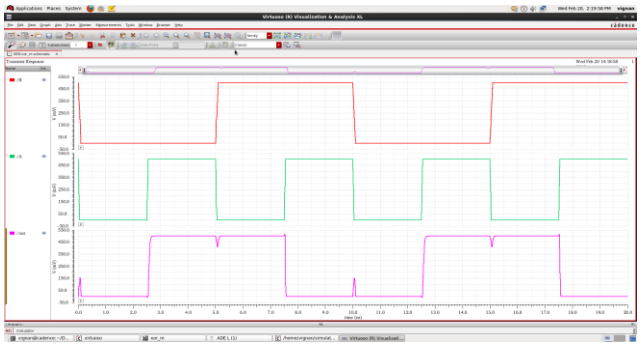

Fig. 8. Transient response of new XOR gate

Its transient response is obtained as shown in Fig. 9. From response it is clear that output of TGFF also has full swing.

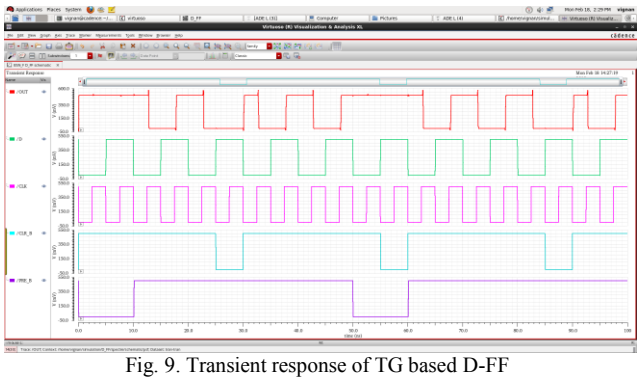

Fig. 9. Transient response of TG based D-FF

Power consumption comparison is shown in Table I. Propagation delay comparison is shown in Table I. PDP comparison is shown in Table II. From the comparison observations it is clear that new XOR gate is best gates than TG based XOR in context of power consumption, propagation delay and PDP values.

TABLE I
PROPAGATION DELAY OF TG BASED XOR AND MODIFIED NEW XOR GATE

Supply voltage (V)	TG based XOR		New XOR	
	Delay (ns)	Power (nW)	Delay (ns)	Power (nW)
0.3	0.355	28.3	0.305	7.38
0.4	0.102	51.25	0.08	13.78
0.5	0.0552	77.2	0.0419	21.31
0.6	0.0398	105	0.0352	29.86
0.7	0.0309	138.5	0.0240	39.42
0.8	0.0258	185	0.0199	50.81
0.9	0.0220	188.4	0.0172	64.91
1.0	0.0195	345	0.0155	82.97
1.1	0.0175	349	0.0139	106.6
1.2	0.0159	643.3	0.0128	138
1.3	0.0150	646.8	0.0121	179.8

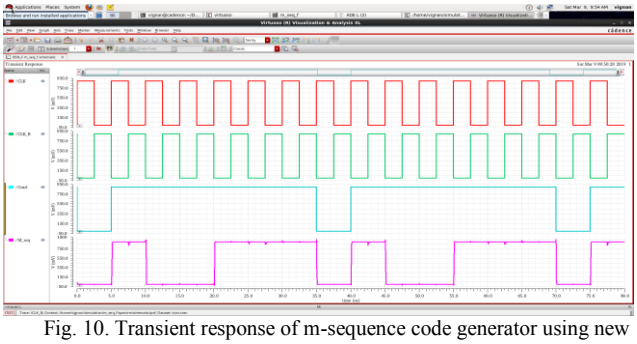

Fig. 10. Transient response of m-sequence code generator using new XOR gate

TABLE II
POWER DELAY PRODUCT OF TG BASED XOR AND MODIFIED NEW XOR

Supply Voltage (V)	TG based XOR XOR (10^{-18}J)	Modified new (10^{-18}J)
0.3	10.04	2.2509
0.4	5.2275	1.1024
0.5	4.0298	0.8928
0.6	4.179	1.0510
0.7	4.2796	0.9460
0.8	4.773	1.011
0.9	4.1448	101216
1.0	6.7275	1.2860
1.1	6.1075	1.4776
1.2	10.2284	1.7813
1.3	9.702	2.170

m-sequence code generator circuit is designed as shown in Fig. 6. By using new XOR gate, TGFF and is simulated in Cadence Virtuoso 90nm CMOS technology. Transient response of this generator is as shown in Fig. 10.

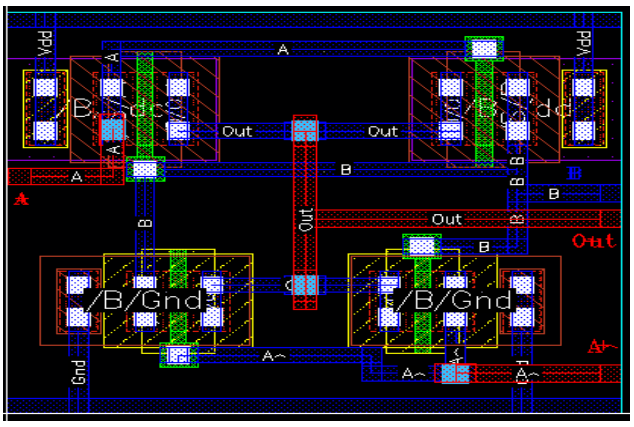

Fig. 11. Layout diagram of new XOR gate

TABLE III
POWER DISSIPATION OF M-SEQUENCE CODE GENERATOR

Supply voltage (V)	TG based XOR (nW)	New XOR gate (nW)
0.3	144.6	130.5
0.4	478.6	448.7
0.5	753.1	719.2
0.6	1108.2	1059.1
0.7	1540.4	1480.9
0.8	2060.7	1980.8
0.9	3730.9	2586.3
1.0	3440.8	3310.1
1.1	4320.5	4170.8
1.2	5384.4	5204.5
1.3	6638.9	6425.4

It is clear that the required code sequence of 1001110 is generated with full swing characteristics. This circuit is implemented with both TG based XOR and new XOR gate as feedback elements separately and their power consumption's are compared and the comparison results are as shown in Table III. Therefore by observing these values it can be concluded that the power consumption of overall m-sequence code generator is reduced by replacing a conventional XOR with new XOR gate.

VII. CONCLUSION

So as to have low power consumption m-sequence code generator, in this paper a new XOR gate was proposed which is operated at different voltage levels and compared it with the TG-based XOR gate in terms of power consumption delay, and PDP. The simulation results concludes that the code generator design that uses new XOR gate has low power consumption when compared to the design that uses TG based XOR. The circuit of the code generator was simulated by Cadence and implemented using 90 nm CMOS technology.

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