BHASKAR MONI

M.S., NTU Singapore

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Career Objective

Well versed in layout of semiconductor chip. Seeking an opportunity to work as a Physical Design Engineer in a dynamic and competitive environment.

Work Experience

Physical Design Trainee **VLSI Guru Institute, Bangalore** **Sep'18-Present**

- Owning Two Block level design
- Working on 28 nm technology node with 40 macros, 240 IO pins and more than 50k std. cells
- Complete floorplan to timing closure using Synopsys ICC tool
- CTS, Parasitic Extraction, STA and Verification done using Synopsys tools

Faculty Member **Math Vision Pvt. Ltd., Singapore** **Aug'15– Feb'16**

- Acted as the Assistant Faculty Head of Physics Department.
- Taught Physics to international students of Grades 9th to 12th (High School) for IB and IGCSE boards

Research Associate **Nanyang Technological University, Singapore** **Jun'15– Aug'15**

- Studied cancer cell ablation using High Intensity focused ultrasound (HIFU) on porcine kidneys.
- Performed experimental setup and gathered PCD signal.
- Signal analysis was done using Matlab including signal dosage and Fast Fourier Transforms (FFT).
- Used LabView to drive instruments including LeCroy Oscilloscope and gather data.
- Project funded by Ministry of Health (MOH), Singapore.

Assistant Systems Engineer **Tata Consultancy Services Ltd., India** **Sep'11– Jun'13**

- Worked on block level design with multiple power domains with gate count over 8 million on 45 nm process.
- Worked on floor plan and PnR of the design using Synopsys ICC tool.
- Parasitic extraction was performed using Synopsys StarRC
- Handled sign off checks for the design like IR drop analysis.
- Improved power distribution for the design based on the IR drop feedback.
- Handled congestion analysis and routing experiments for the design as the design density was high.
- Did signal integrity checks (DRV) and repairs for the design using Cadence Encounter.
- Did STA trials for the design using Synopsys PrimeTime
- Implemented ECOs on the design.
- Did timing closure for the design.

Academic Projects

Standard Cell Design: 6 Transistor SRAM Cell layout

- Schematic Capture was done using Cadence Virtuoso in TSMC 65 nm library manually.
- Created full custom layout including floorplan, power-plan using Cadence Virtuoso.
- Performed DRC, LVS and PEX was performed using Cadence Assura.
- Performed pre-layout and post-layout simulations for verification of its functionality

Verilog Simulation and Synthesis: Full Adder based 8:2 compressor

- Verilog was used to code the design the test bench.
- Functional verification was performed using Cadence NC Verilog.
- Synthesis was done in Cadence Encounter RTL Compiler.
- Pre-layout and Post-layout simulations was performed
- Estimated delays introduced by gates based on TSMC 65 nm library
- Performed Power simulations

Dissertation & Internships

Low Power performance analysis of CMOS arithmetic units **Mar'14 – Dec'14**
(M.Sc. dissertation NTU, Singapore)

- The dissertation aimed at comparing eight different power reduction architectures by implementing one bit full adder cells and the simulations were carried out on transistor level simulation in Cadence virtuoso on TSMC's 65nm process.
- Schematic Capture and full custom layout was done using Cadence Virtuoso.
- Floorplanning and Placement of the final 8:2 lossy compressor was performed using Cadence Encounter
- DRC, LVS and PEX was carried out in Cadence Assura.
- Design and Layout was implemented using Low power techniques such as Sub-Threshold operation, Multiple Threshold Voltage, Dynamic Voltage and Frequency Scaling and Logic Reduction Techniques
- Performed Corner Testing on all the corners including FF, TT, SF, FS, SS.
- Comparison is made on the basis of average power consumed, delay and power delay product.

Vehicle Security System using Image Processing **Jan'11 – May'11**
(B. Tech. project SRM University, India)

- The project aimed at vehicle security using the image and the fingerprints of the driver and matching them to a pre-stored database.
- Image analysis was achieved using PCA algorithm and for fingerprints using minutia matching algorithm.
- Was responsible for the interfacing the face recognition system, fingerprint recognition system, GPS module, GSM module and the control platform on the system level.
- Programming of the hardware was achieved using C and Matlab

Technical Skills

- **Languages:** Verilog, C, C++, Tcl, Shell Scripting, Matlab
- **EDA Tools:** Synopsys IC Compiler (ICC), Synopsys StarRC, Synopsys IC Validator (ICV), Synopsys Formality, Synopsys Design Vision, Cadence Virtuoso, Cadence Encounter, Synopsys VCS, Synopsys Design Compiler, Synopsys Power Compiler, Quartus Prime, KiCAD
- **Others:** MS Office, Visual Basic 2011, Unix/ Linux

Academic Qualifications

M.S. (Electronics)	**Nanyang Technological University, Singapore**	**Aug'2013 - May'2015**
B. Tech (E.E.E.)	**S.R.M. University, India**	**Aug'2007 - May'2011**

Co-curricular Activities

- Achieved 1st position for the paper titled "Real time control of power in Smart Rooms" in Energy Wise Contest, Aaruush'10 national level technical fest of SRM University.
- Guided 2 URECA (Undergraduate Research Experience on Campus) research students of IC Design during my Masters at NTU
- Worked as Organizer and Trainer of multiple robotics event.
- Poster presentation of "Vehicle Security System using Image Processing" in IET-SEISCON 2011, Chennai.
- Volunteered for Singapore Semiconductor Industry Association (SSIA) conference in 2013