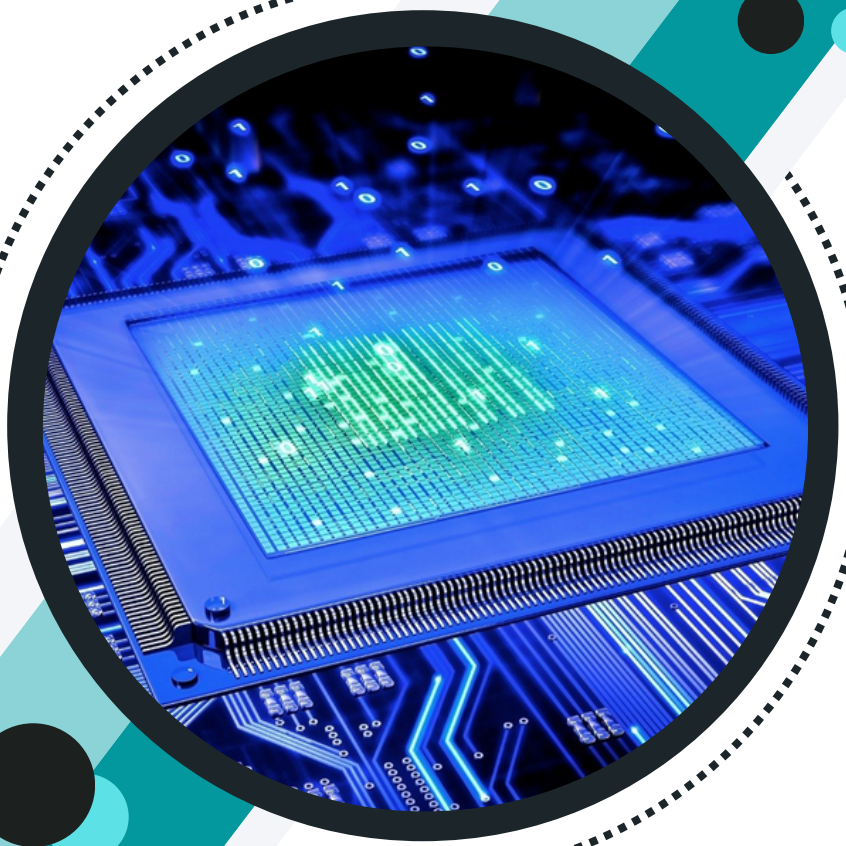
FINAL PROJECT REPORT

14TH JULY, 2023

DESIGN AND IMPLEMENTATION 8 - BIT ARITHMETIC LOGIC UNIT USING CMOS

USING CADENCE VIRTUOSO



Prepared By:

21BEC1662 - RAGHUL G
21BEC1692 - OVISHREE S
21BEC1655 - NIRANJANA D
21BEC1625 - RAGUL D

This project contain an Arithmetic & Logic Unit (ALU) using logic gates.

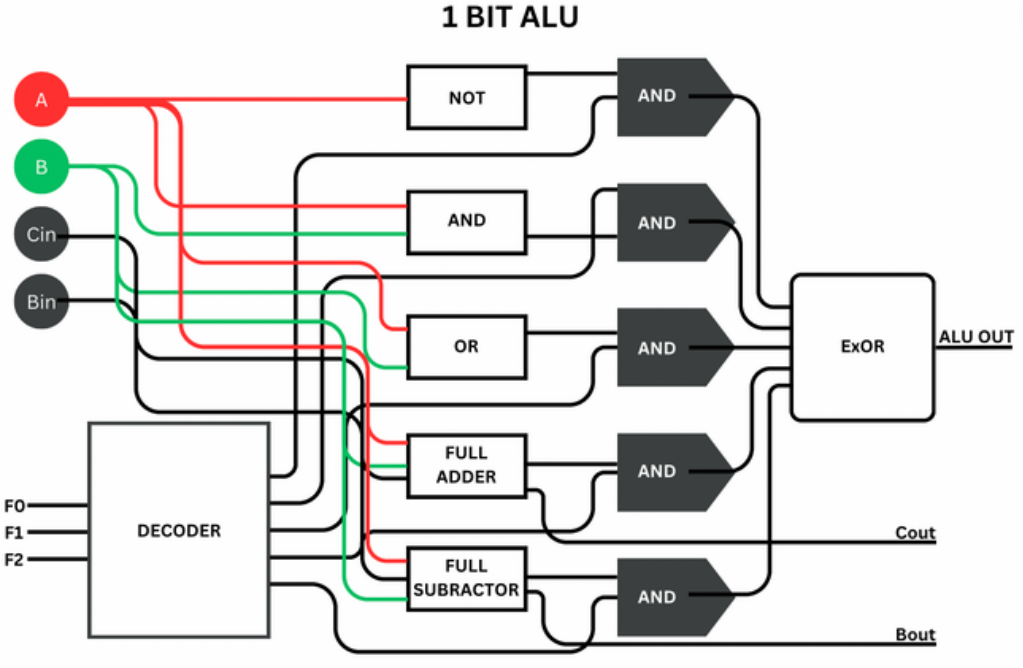
This ALU will perform 5 different operations:

- **LOGIC NOT**
- **LOGIC AND**
- **LOGIC OR**
- **ARITHMETIC ADDITION**
- **ARITHMETIC SUBTRACTION**

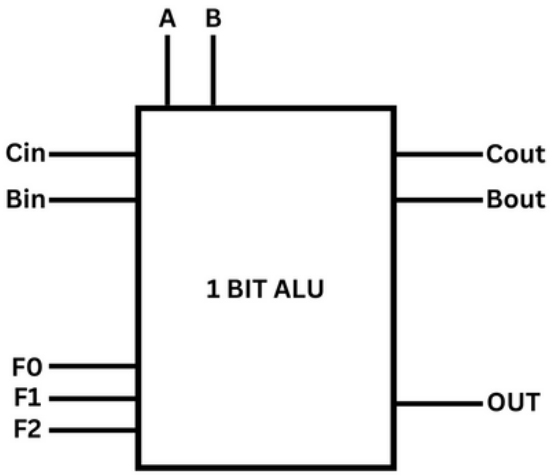
INSTRUCTION TABLE OF ALU

FO	F1	F2	OPERATIONS
0	0	0	NOT
0	0	1	AND
0	1	0	OR
0	1	1	FULL ADDER
1	0	0	FULL SUBTRACTOR

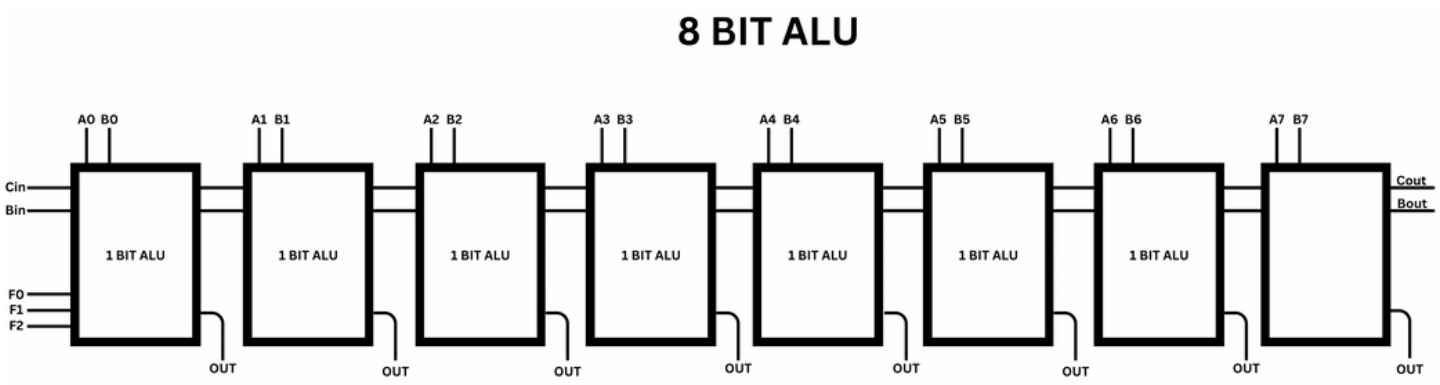
1 BIT ALU CIRCUIT



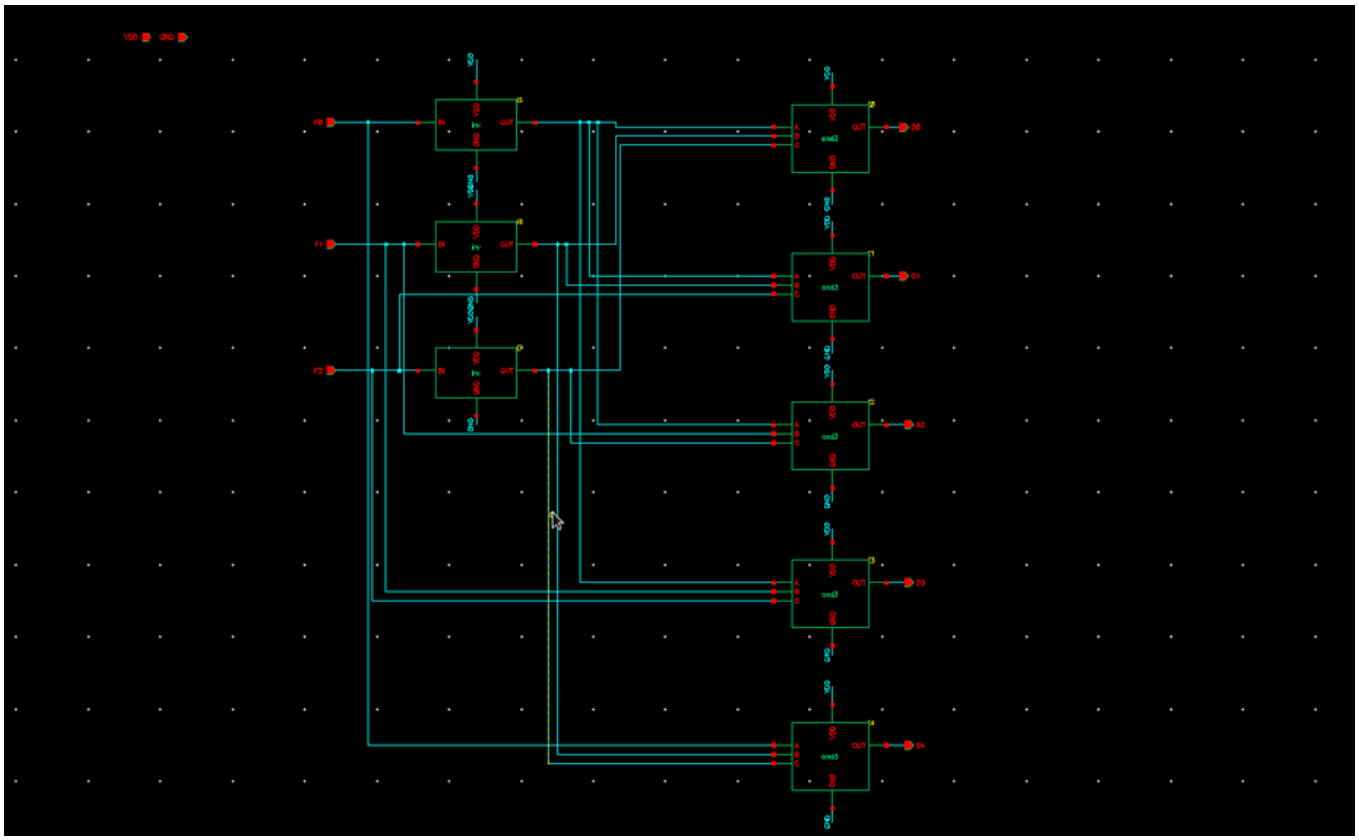
1 BIT ALU SYMBOL



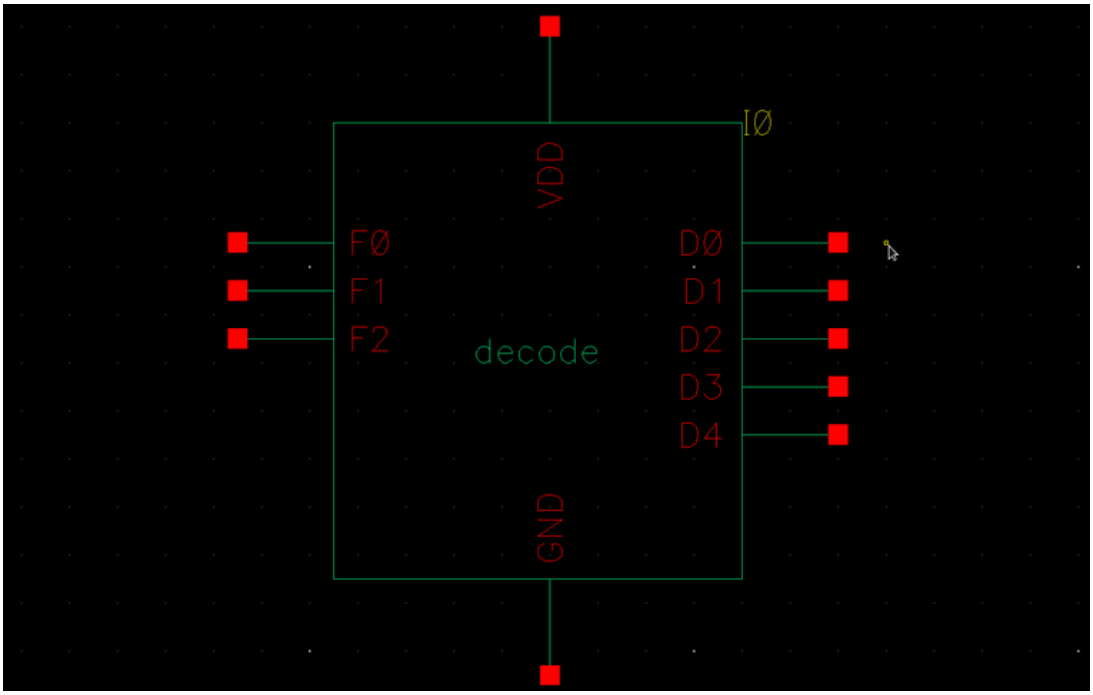
8 BIT ALU SYMBOL



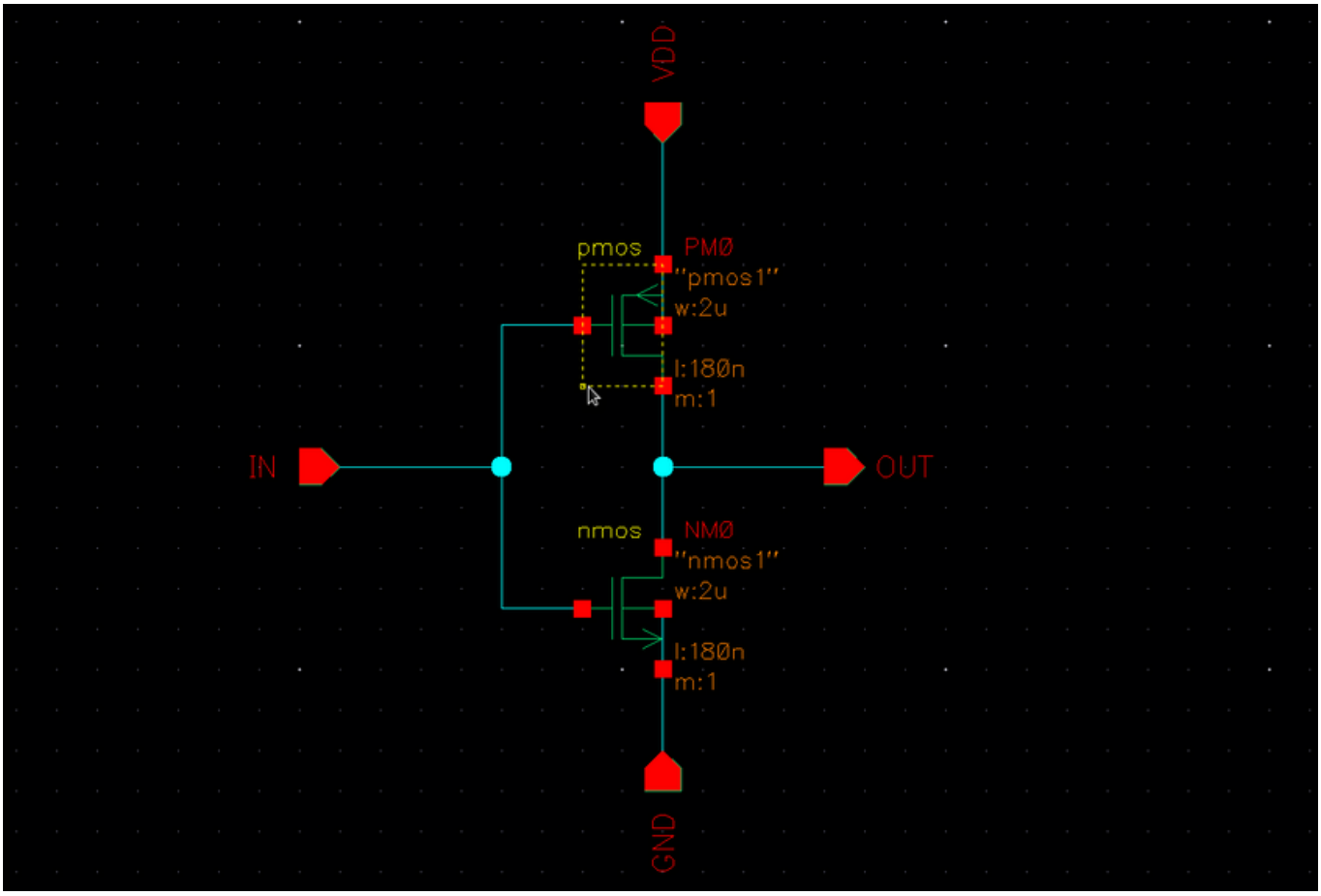
DECODER CIRCUIT



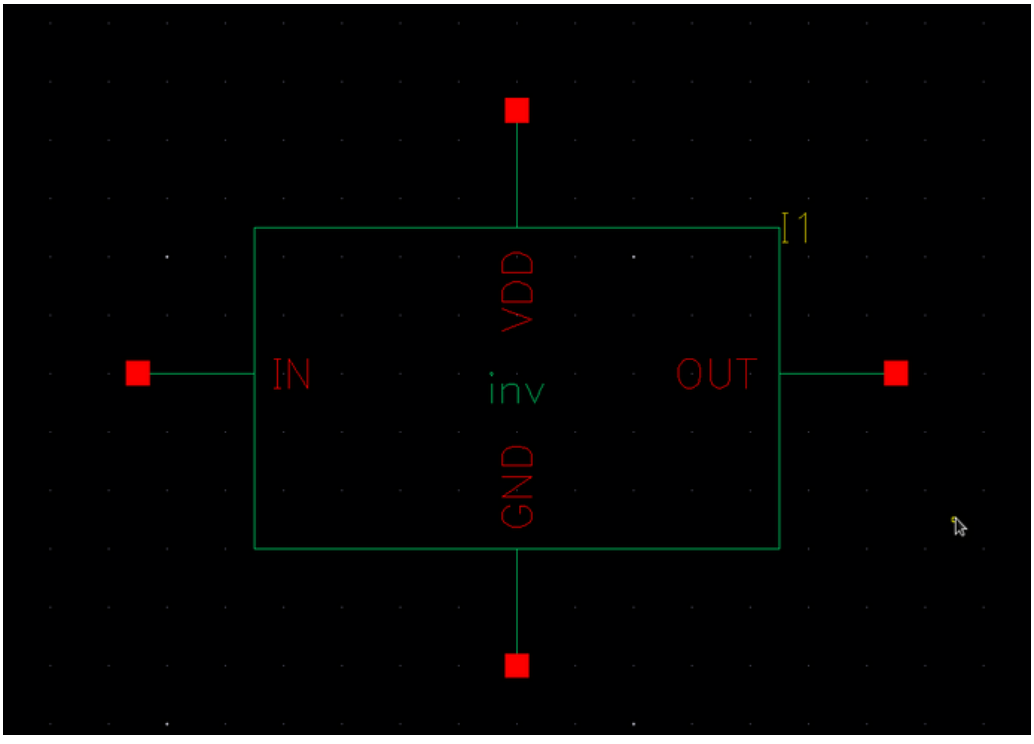
DECODER SYMBOL



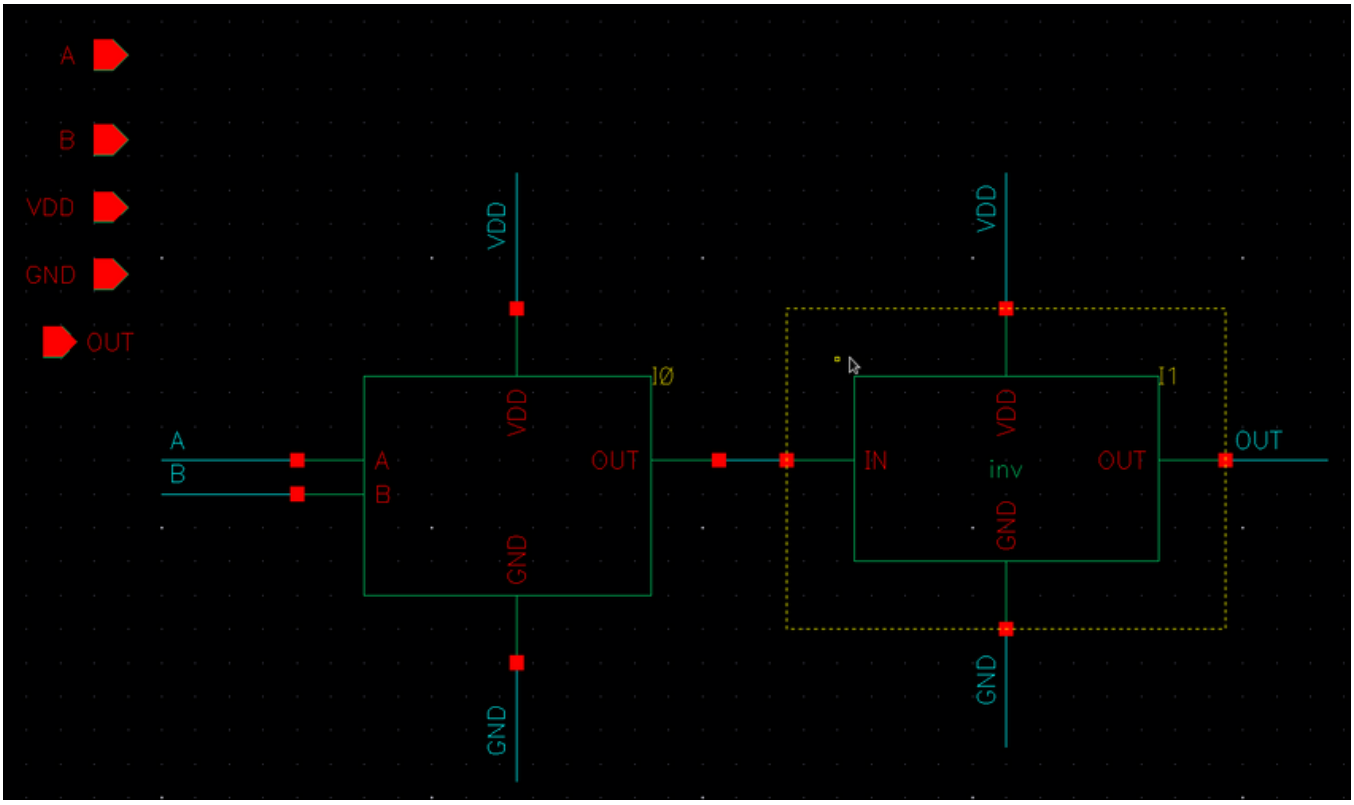
NOT GATE CIRCUIT



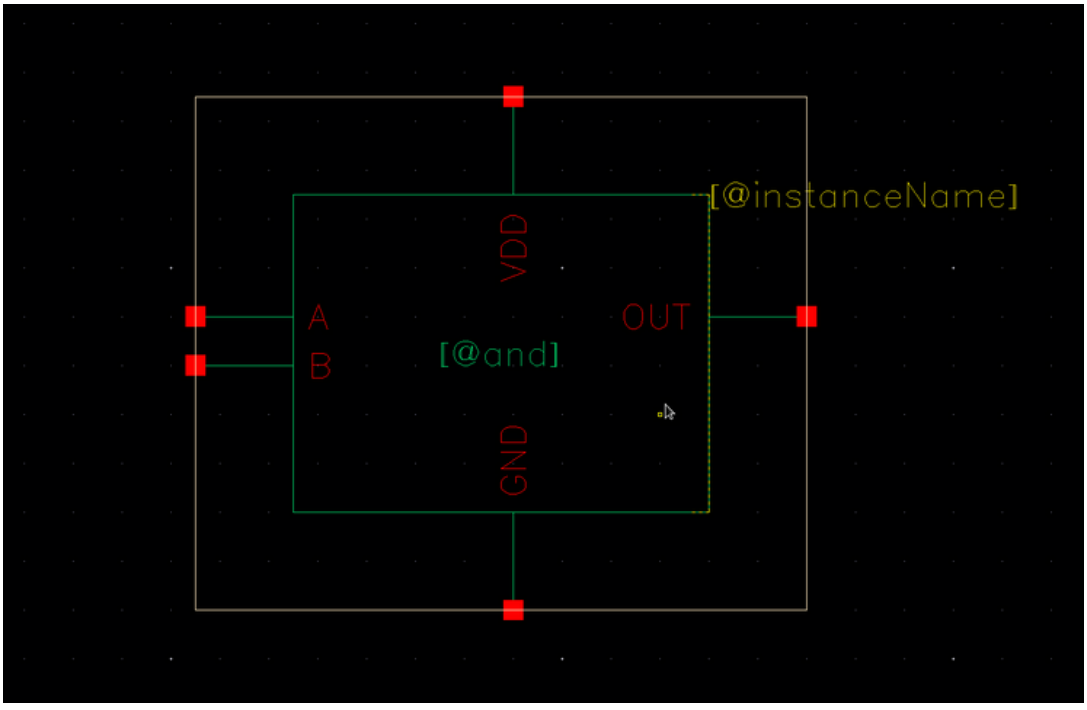
NOT GATE SYMBOL



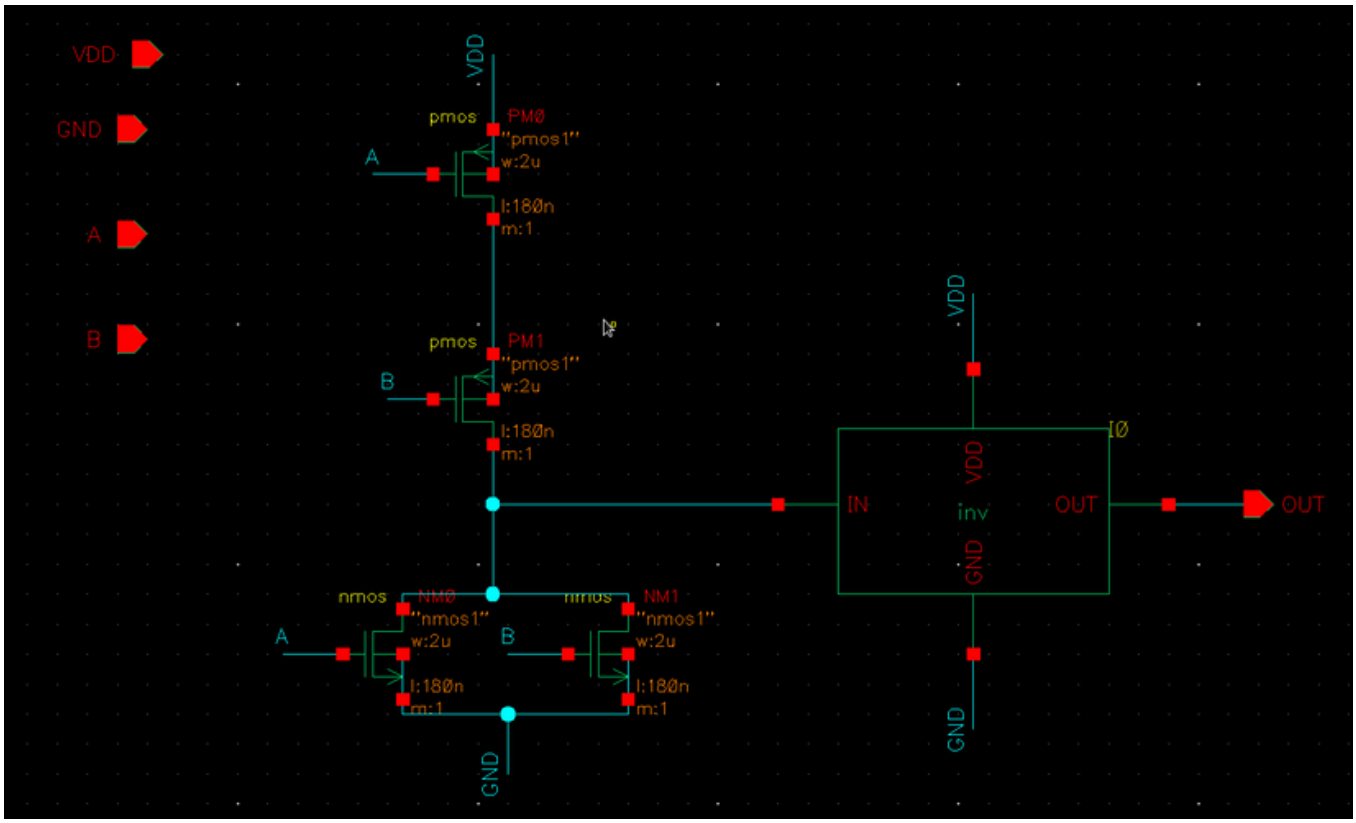
AND GATE CIRCUIT



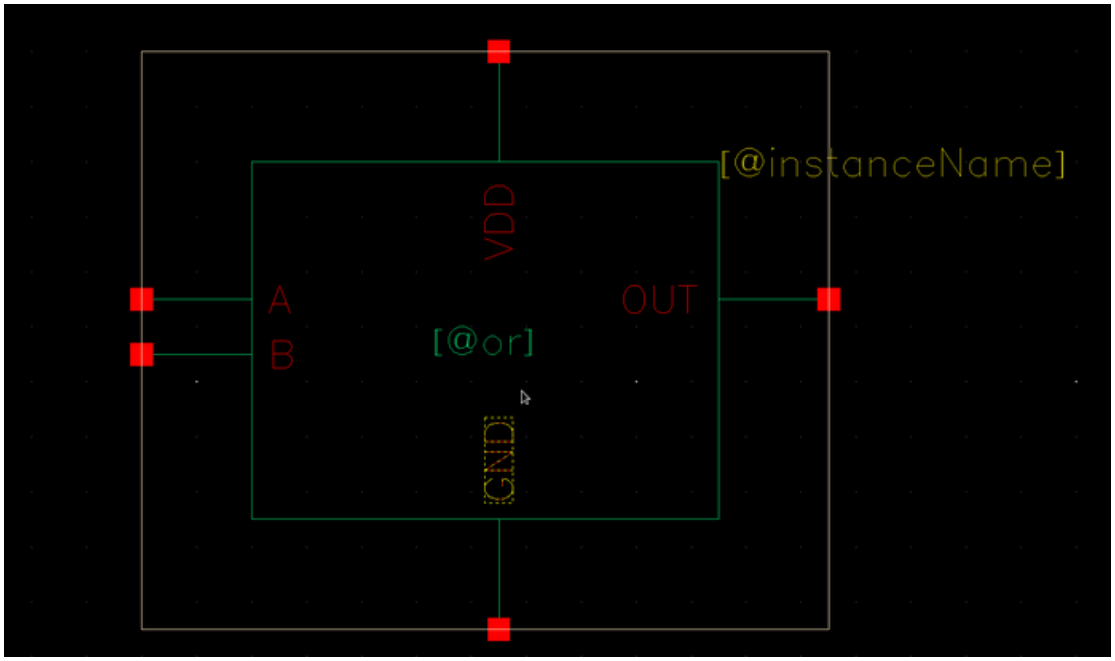
AND GATE SYMBOL



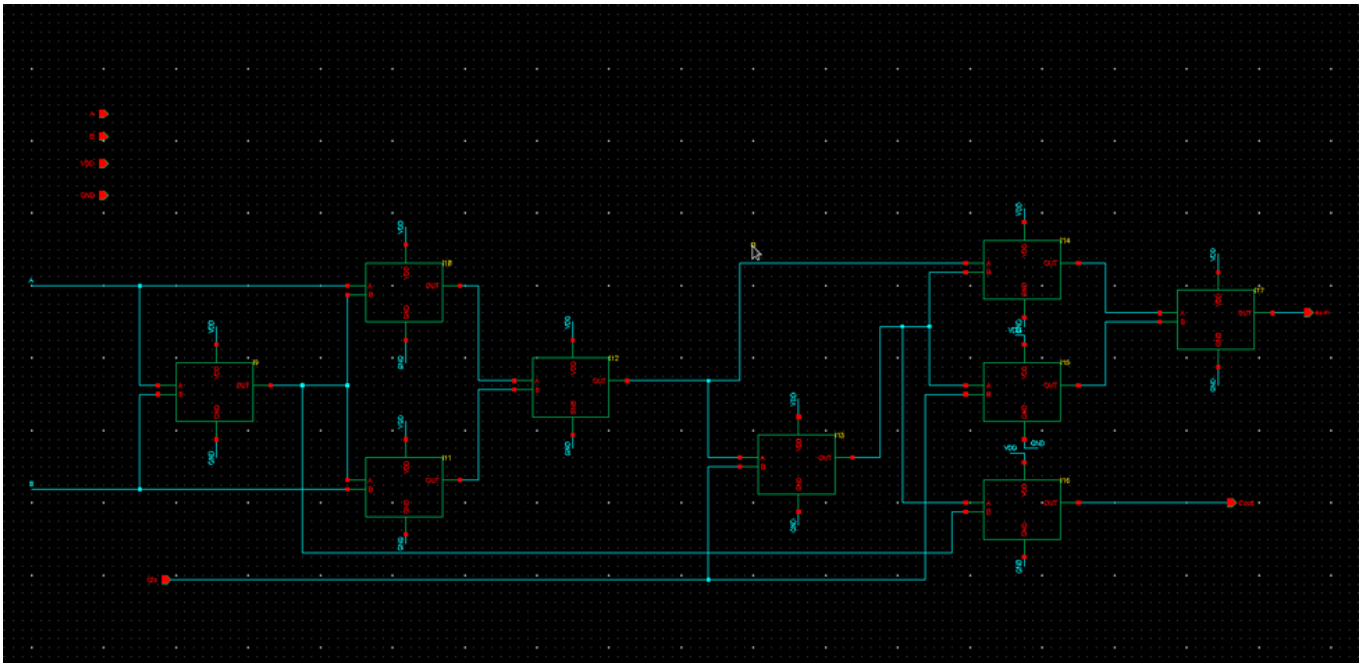
OR GATE CIRCUIT



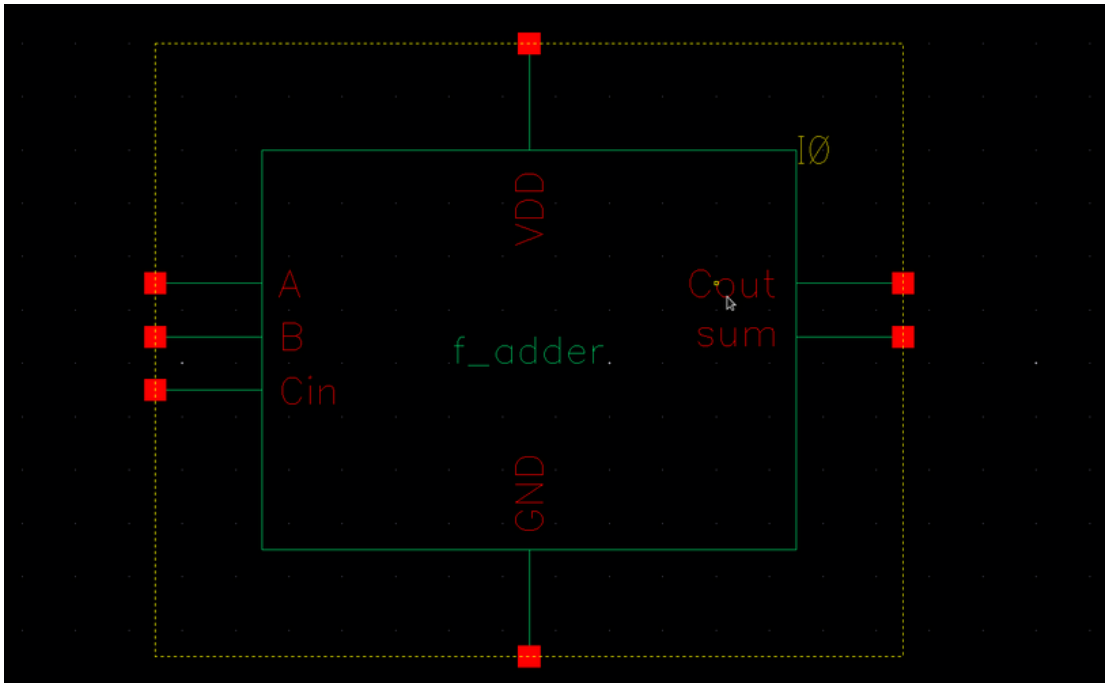
OR GATE SYMBOL



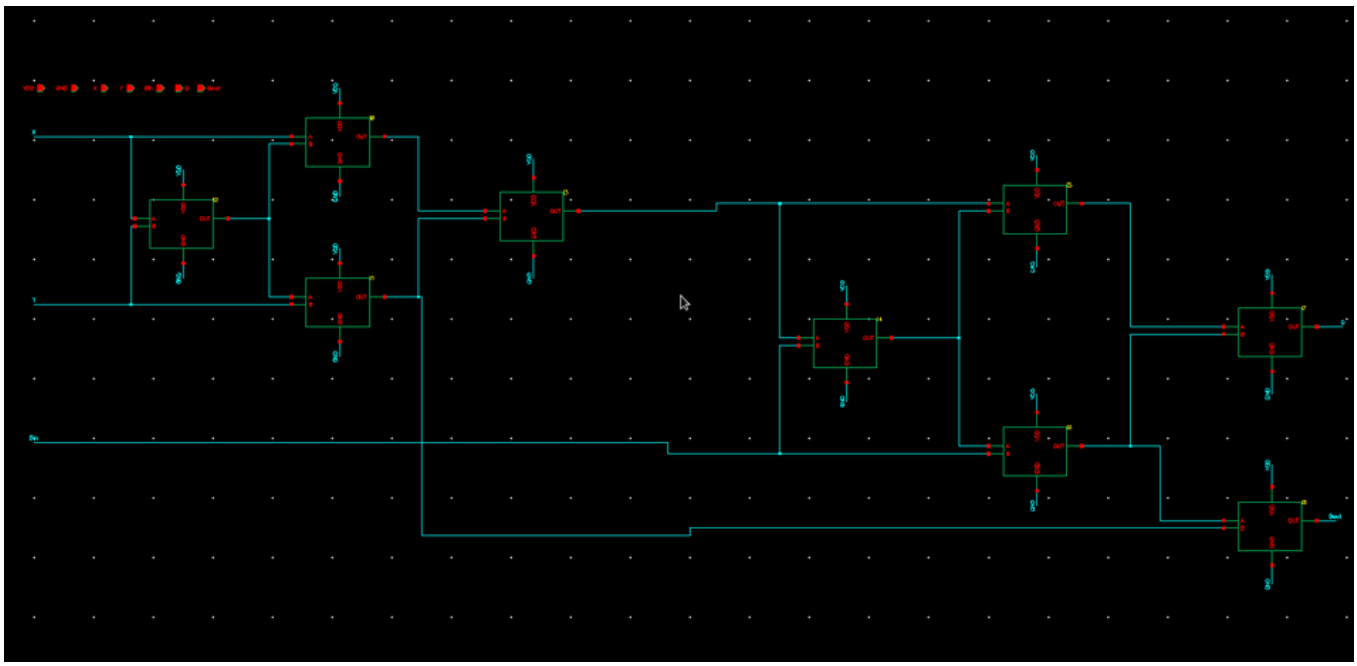
FULL ADDER CIRCUIT



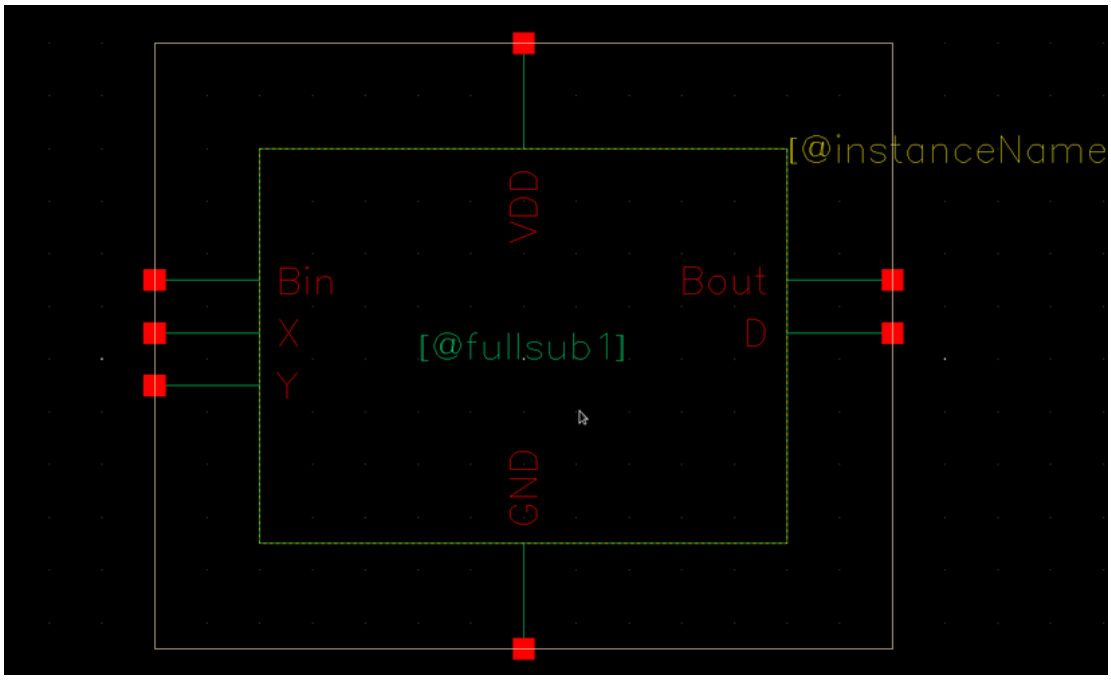
FULL ADDER SYMBOL



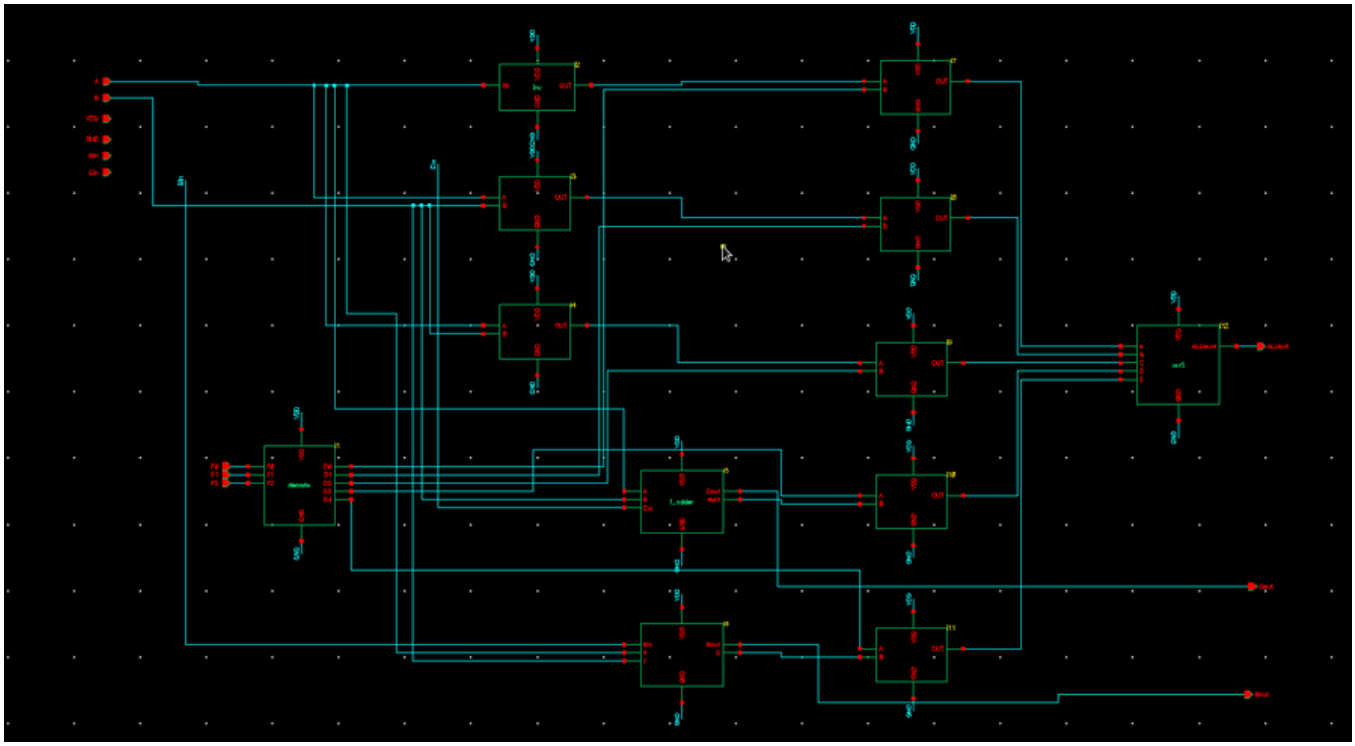
FULL SUBTRACTOR CIRCUIT



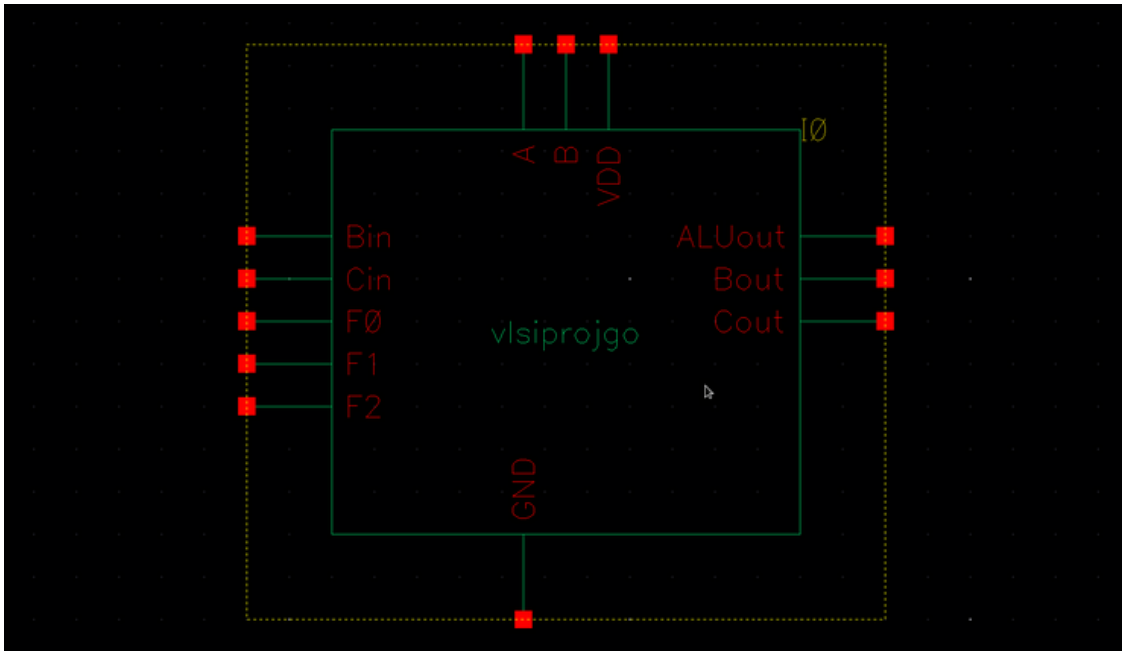
FULL SUBTRACTOR SYMBOL



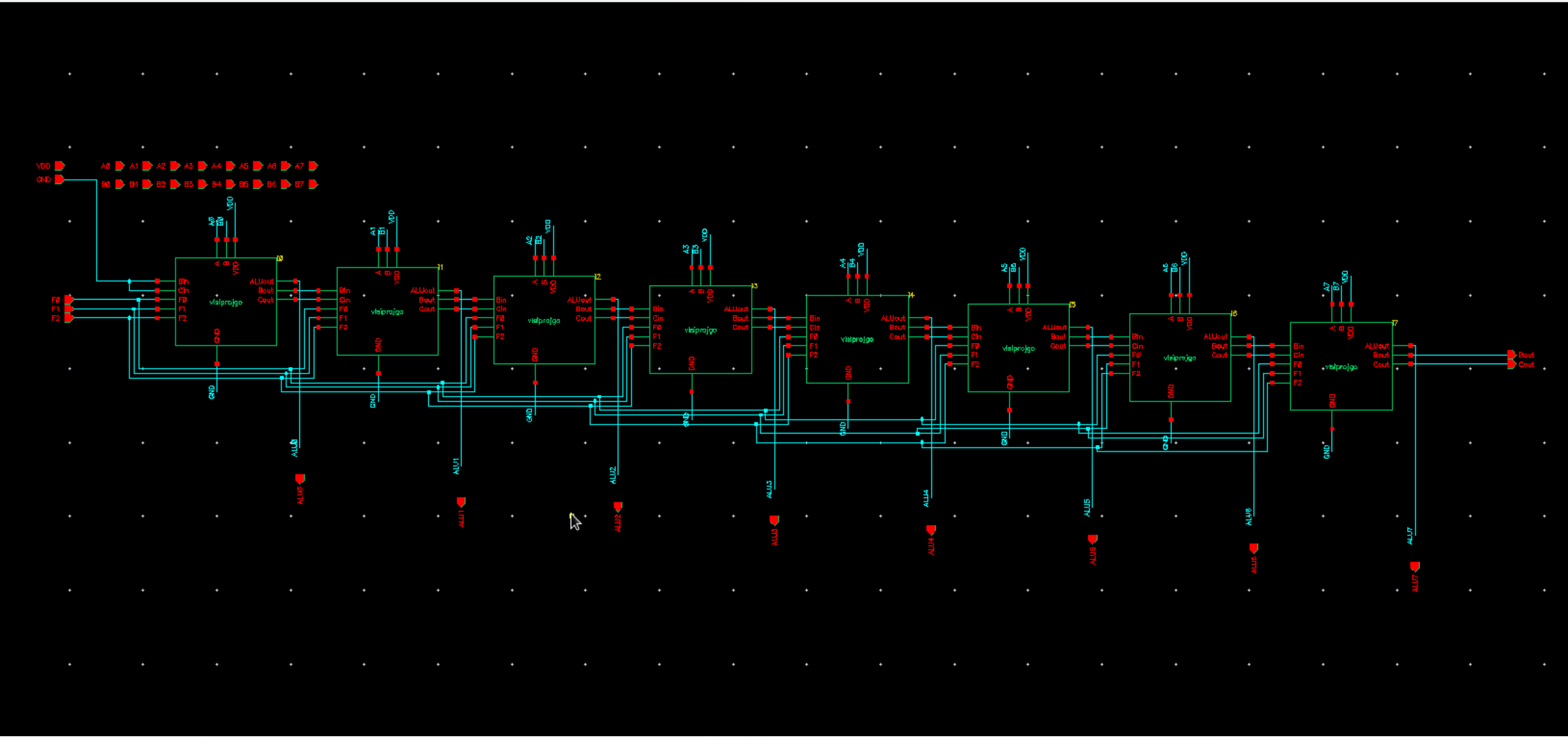
1 BIT ALU CIRCUIT



1 BIT ALU SYMBOL



8 - BIT ALU


VDD
GND
A0 A1 A2 A3 A4 A5 A6 A7
B0 B1 B2 B3 B4 B5 B6 B7
F0
F1
F2
Bin
Cin
F0
F1
F2
ALUout
Bout
Cout
vlsiprojgo
GND
ALU0
ALU1
ALU2
ALU3
ALU4
ALU5
ALU6
ALU7
Bout
Cout

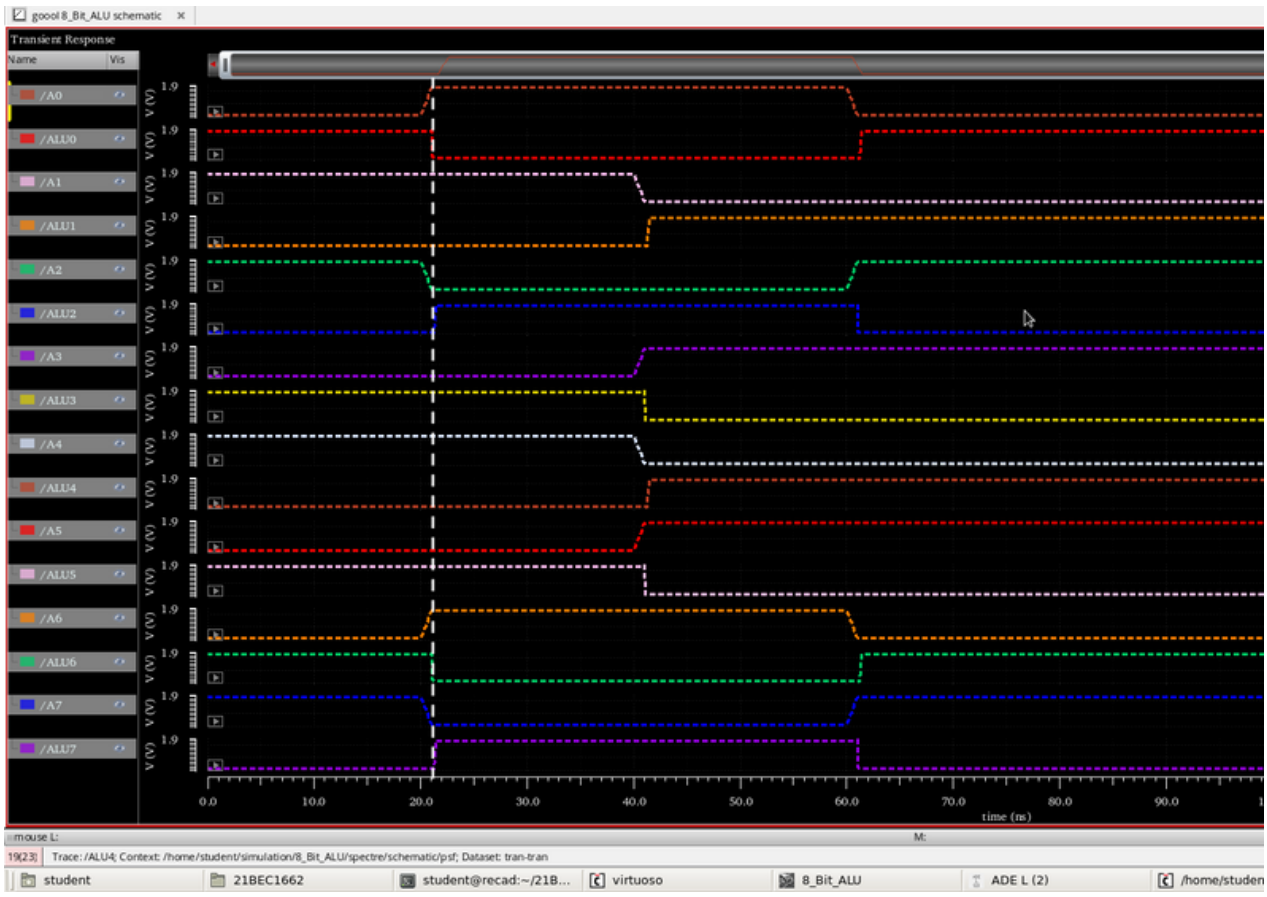
R E S U L T

COMBINATION 1

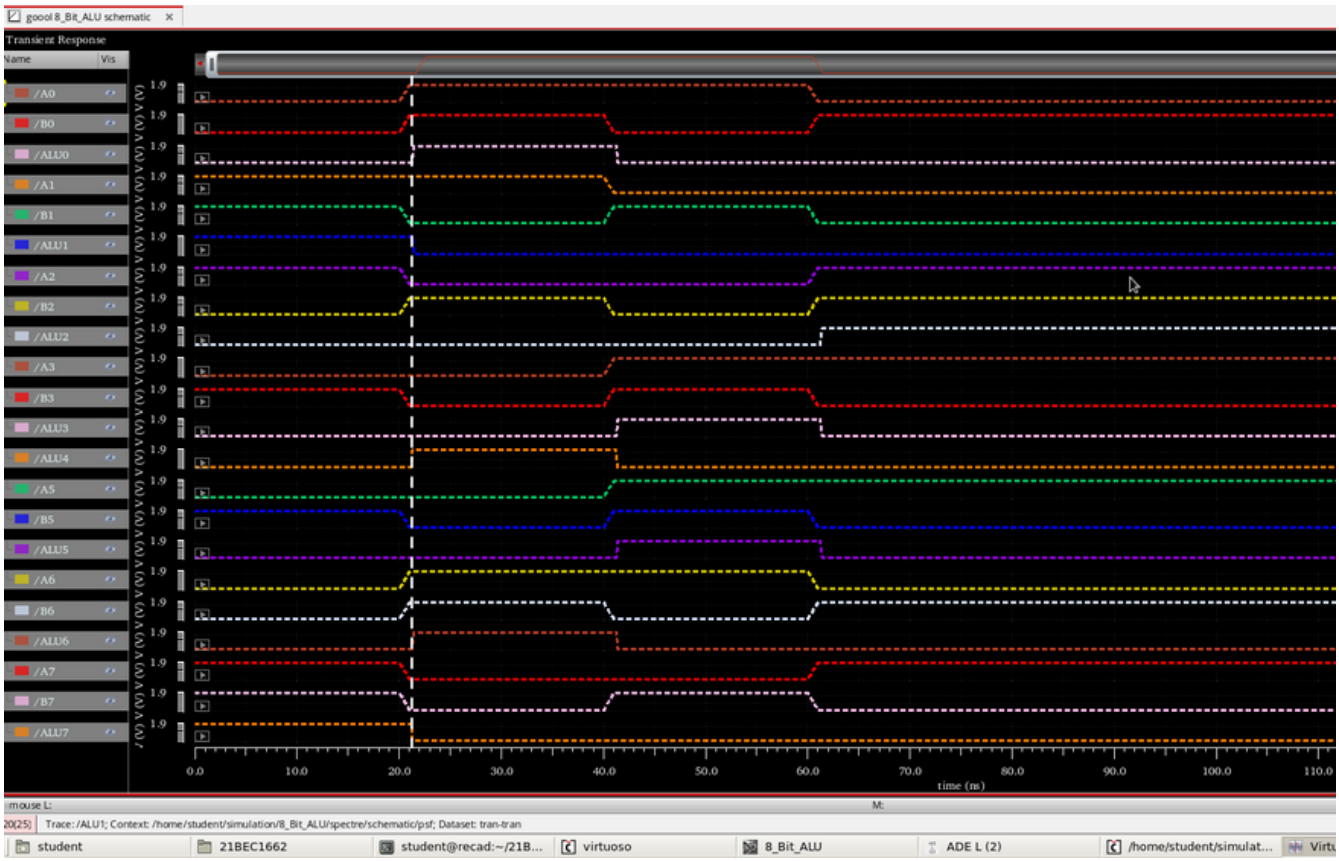
INPUTS		ALU OPERATIONS				
AO	BO	NOT	AND	OR	F A	F S
0	0	1	0	0	0	0
1	1	0	1	1	0	0
1	0	0	0	1	0	1
0	1	1	0	1	0	1
1	0	0	0	1	0	0
0	1	1	0	1	0	1
0	0	1	0	0	1	1
1	1	0	1	1	0	1

Cout = 1
Bout = 1

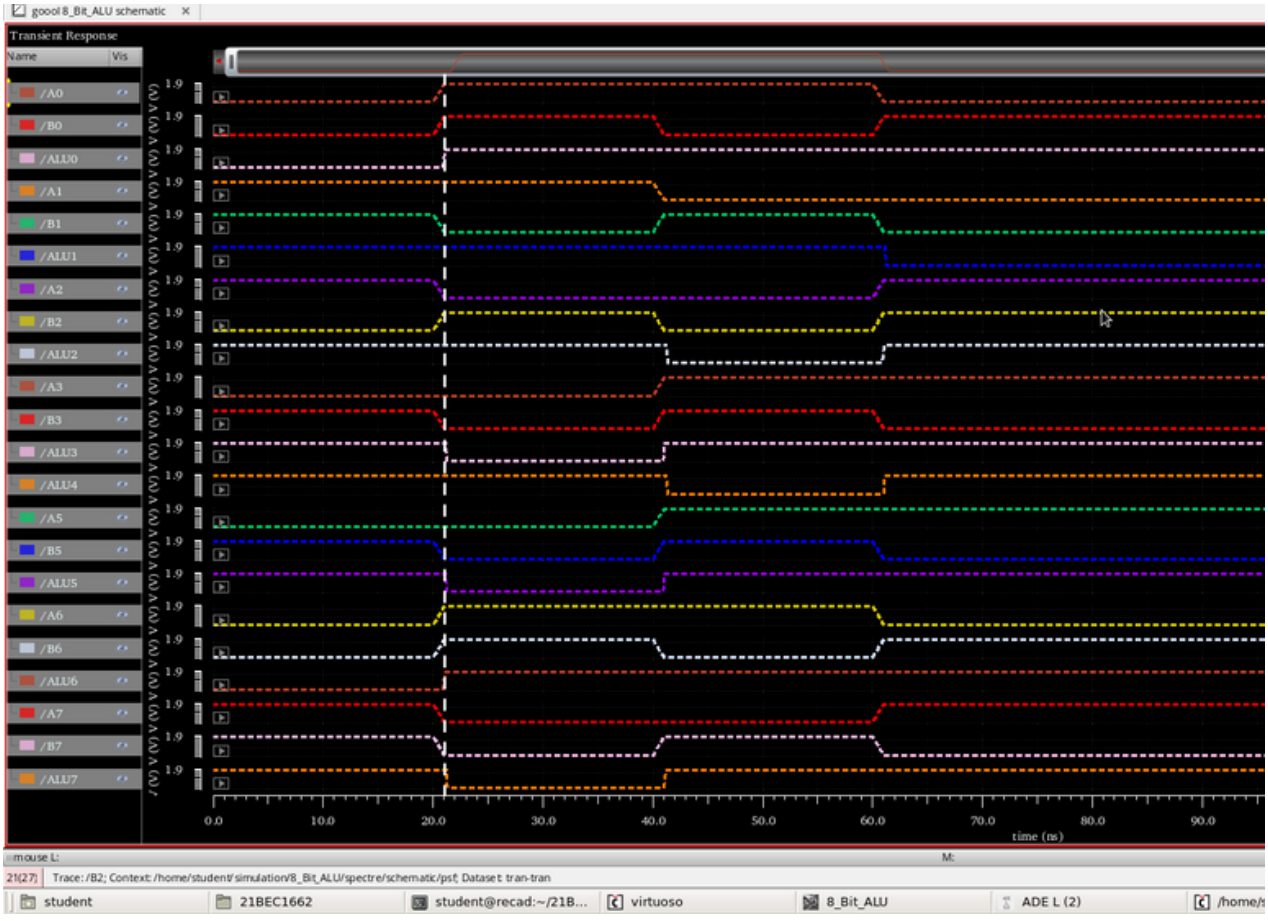
NOT



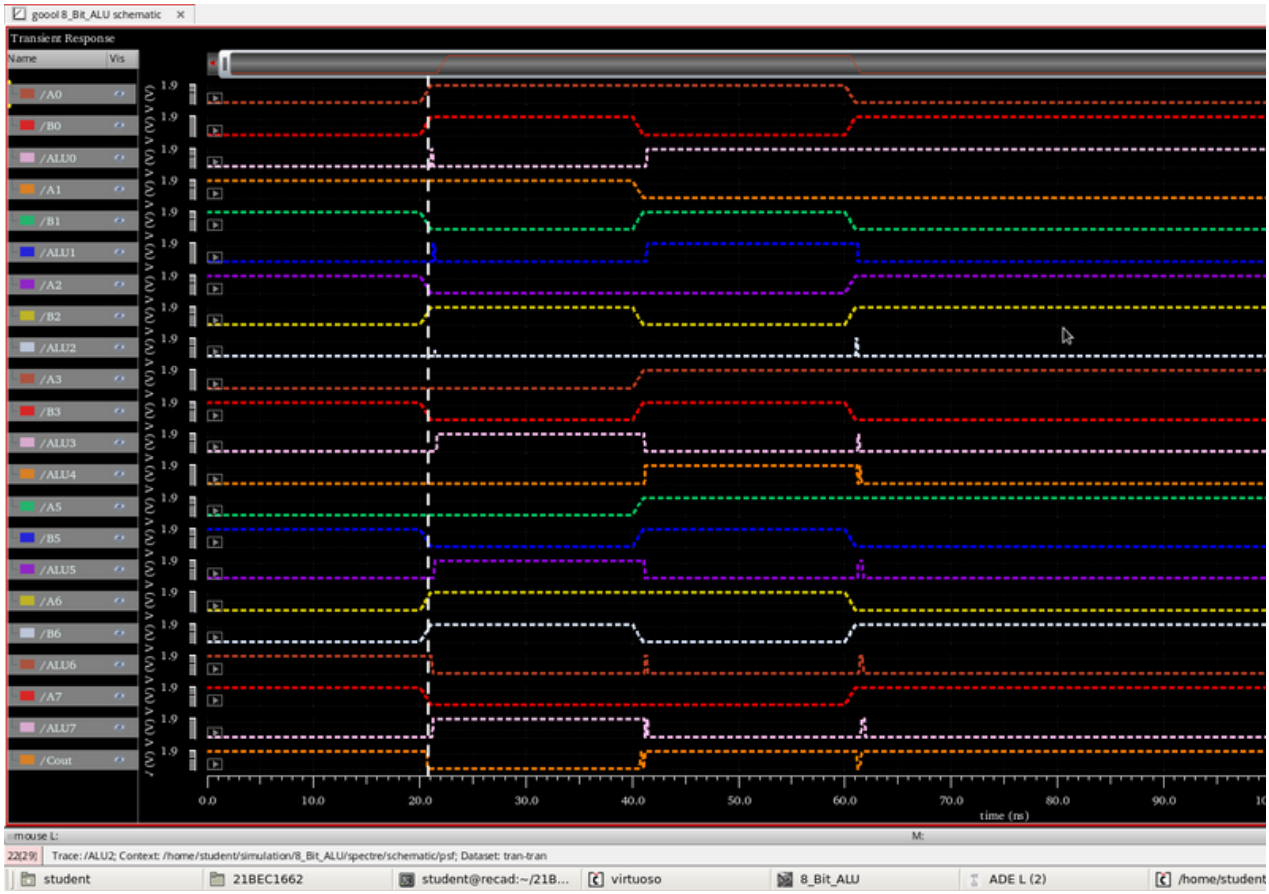
AND


goool 8_Bit_ALU schematic
Transient Response
Name
Vis
/A0
/B0
/ALU0
/A1
/B1
/ALU1
/A2
/B2
/ALU2
/A3
/B3
/ALU3
/ALU4
/A5
/B5
/ALU5
/A6
/B6
/ALU6
/A7
/B7
/ALU7
1.9
0.0
10.0
20.0
30.0
40.0
50.0
60.0
70.0
80.0
90.0
100.0
110.0
time (ns)
mouse L:
M:
Trace: /ALU1; Context: /home/student/simulation/8_Bit_ALU/spectre/schematic/psf; Dataset: tran-tran
student
21BEC1662
student@recad:~/21B...
virtuoso
8_Bit_ALU
ADE L (2)
/home/student/simulat...

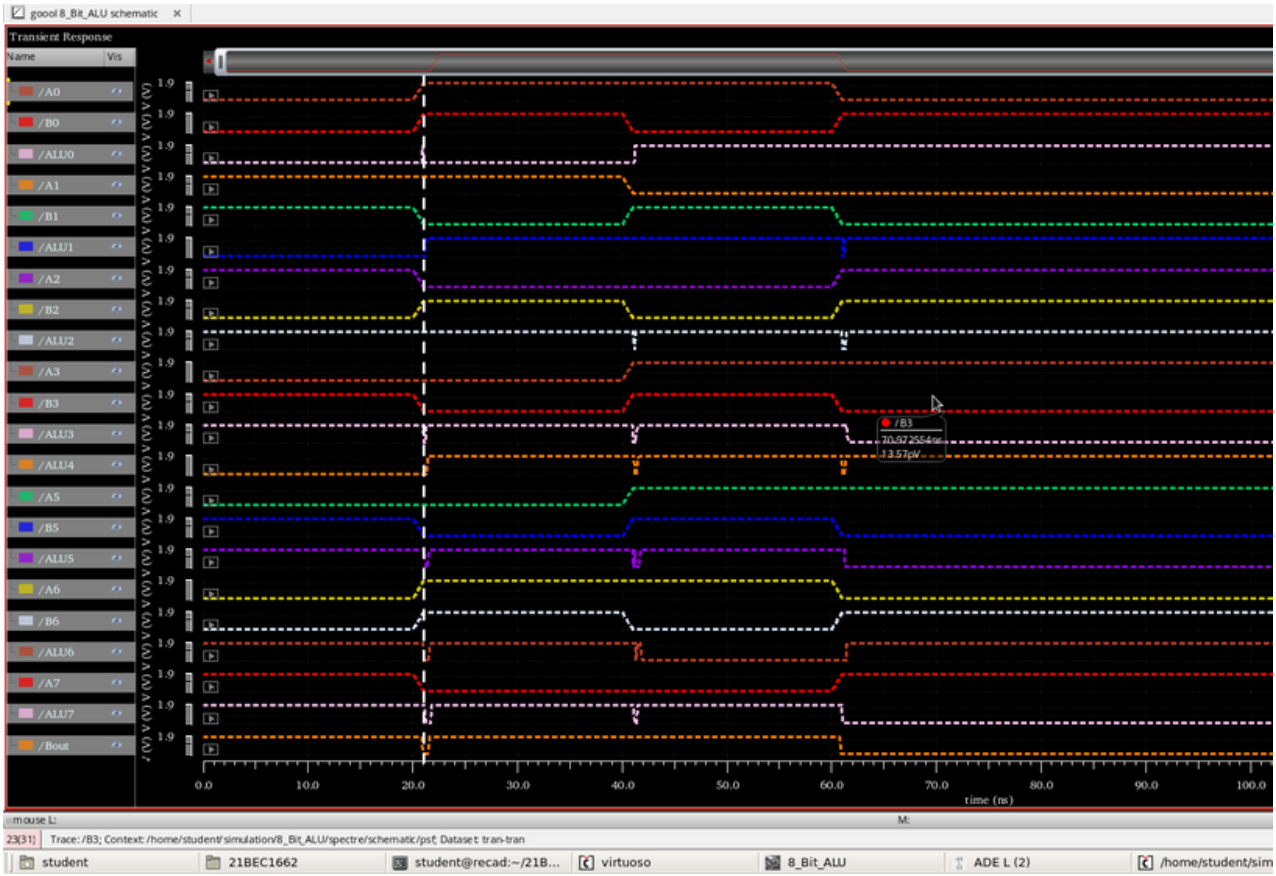
OR


goool 8_Bit_ALU schematic
Transient Response
Name
Vis
/A0
/B0
/ALU0
/A1
/B1
/ALU1
/A2
/B2
/ALU2
/A3
/B3
/ALU3
/ALU4
/A5
/B5
/ALU5
/A6
/B6
/ALU6
/A7
/B7
/ALU7
1.9
0.0
10.0
20.0
30.0
40.0
50.0
60.0
70.0
80.0
90.0
time (ns)
mouse L:
M:
Trace: /B2; Context: /home/student/simulation/8_Bit_ALU/spectre/schematic/psf; Dataset: tran-tran
student
21BEC1662
student@recad:~/21B...
virtuoso
8_Bit_ALU
ADE L (2)

FULL ADDER



FULL SUBTRACTOR

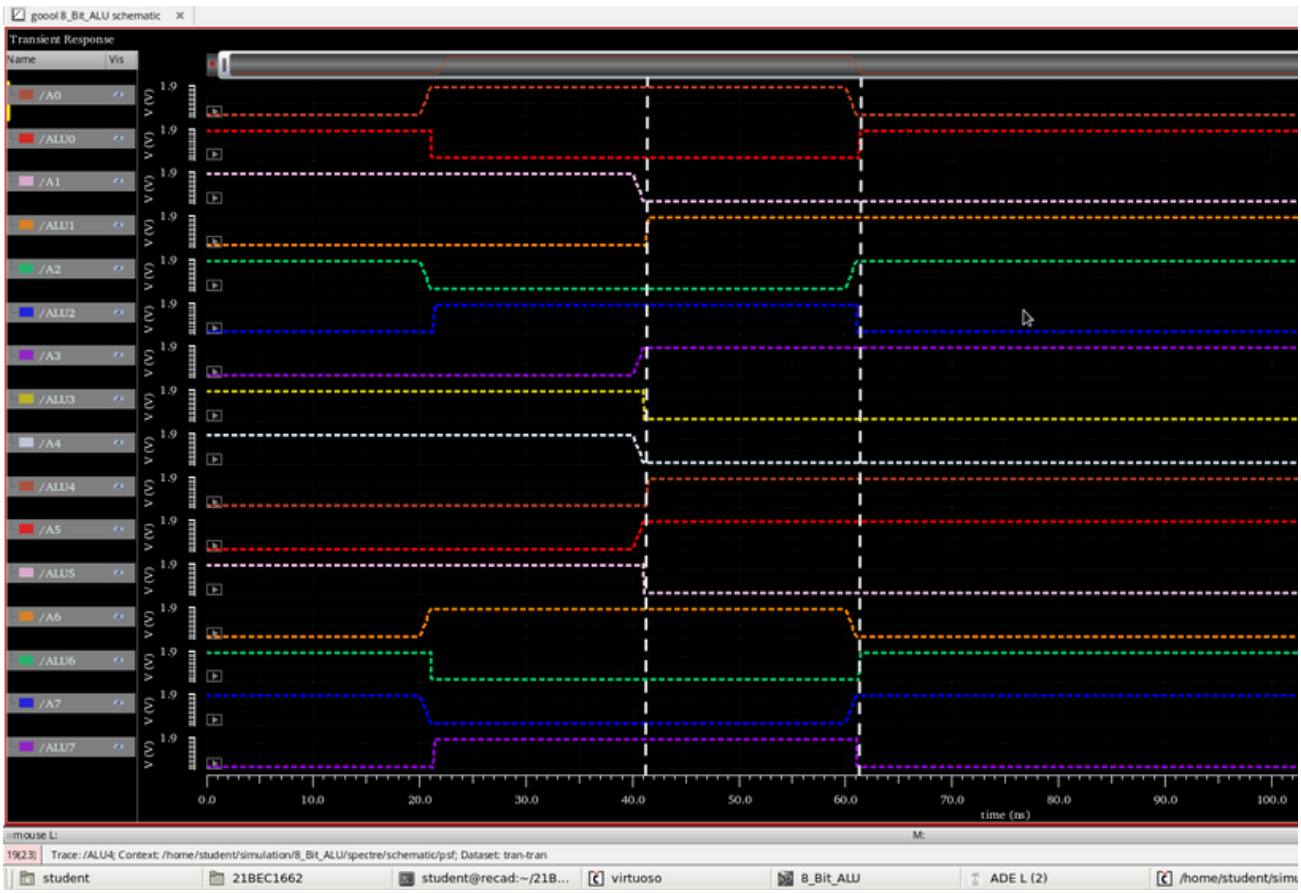


COMBINATION 2

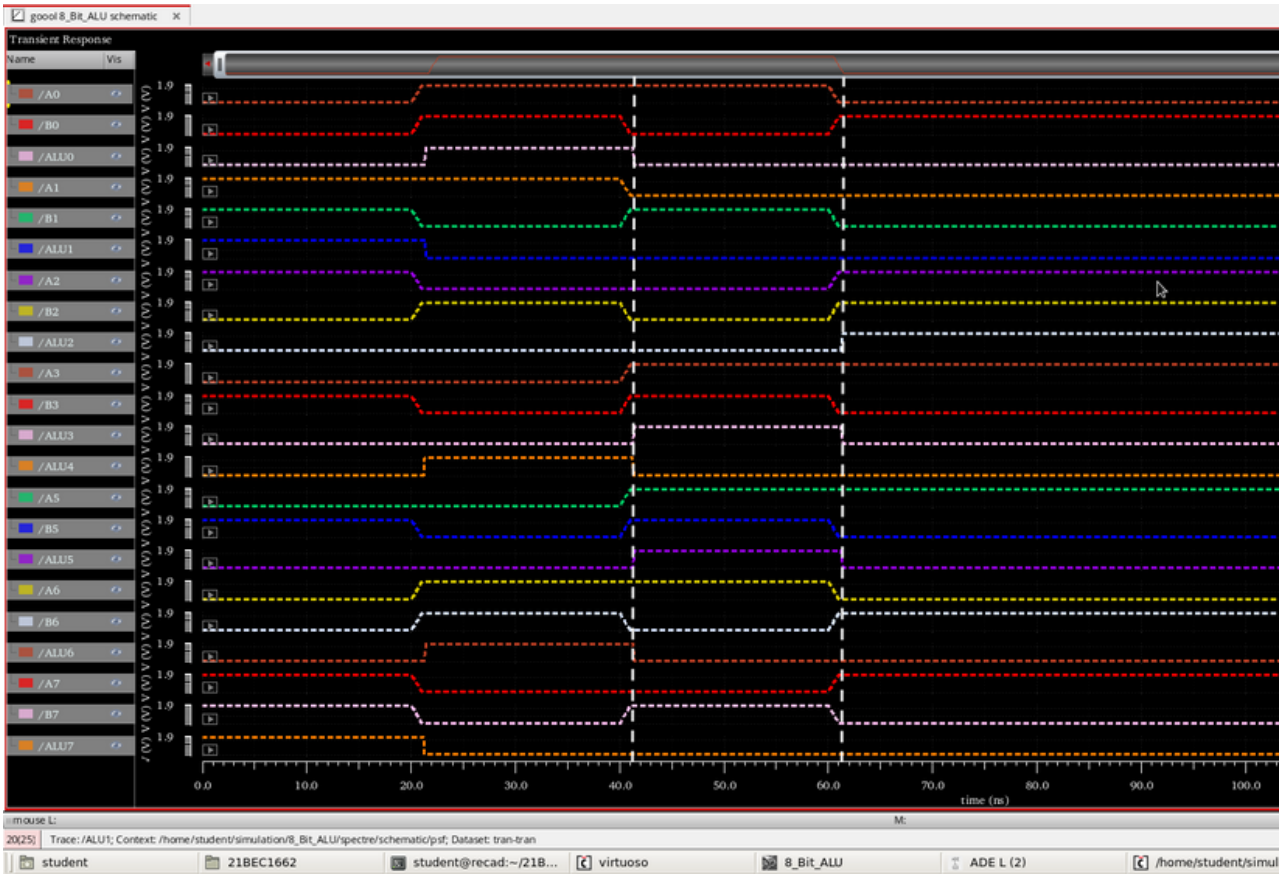
INPUTS		ALU OPERATIONS				
AO	BO	NOT	AND	OR	F A	F S
1	0	0	0	1	1	1
0	1	1	0	1	1	1
0	0	1	0	0	0	1
1	1	0	1	1	0	1
0	0	1	0	0	1	1
1	1	0	1	1	0	1
1	0	0	0	1	0	0
0	1	1	0	1	0	1

Cout = 1
Bout = 1

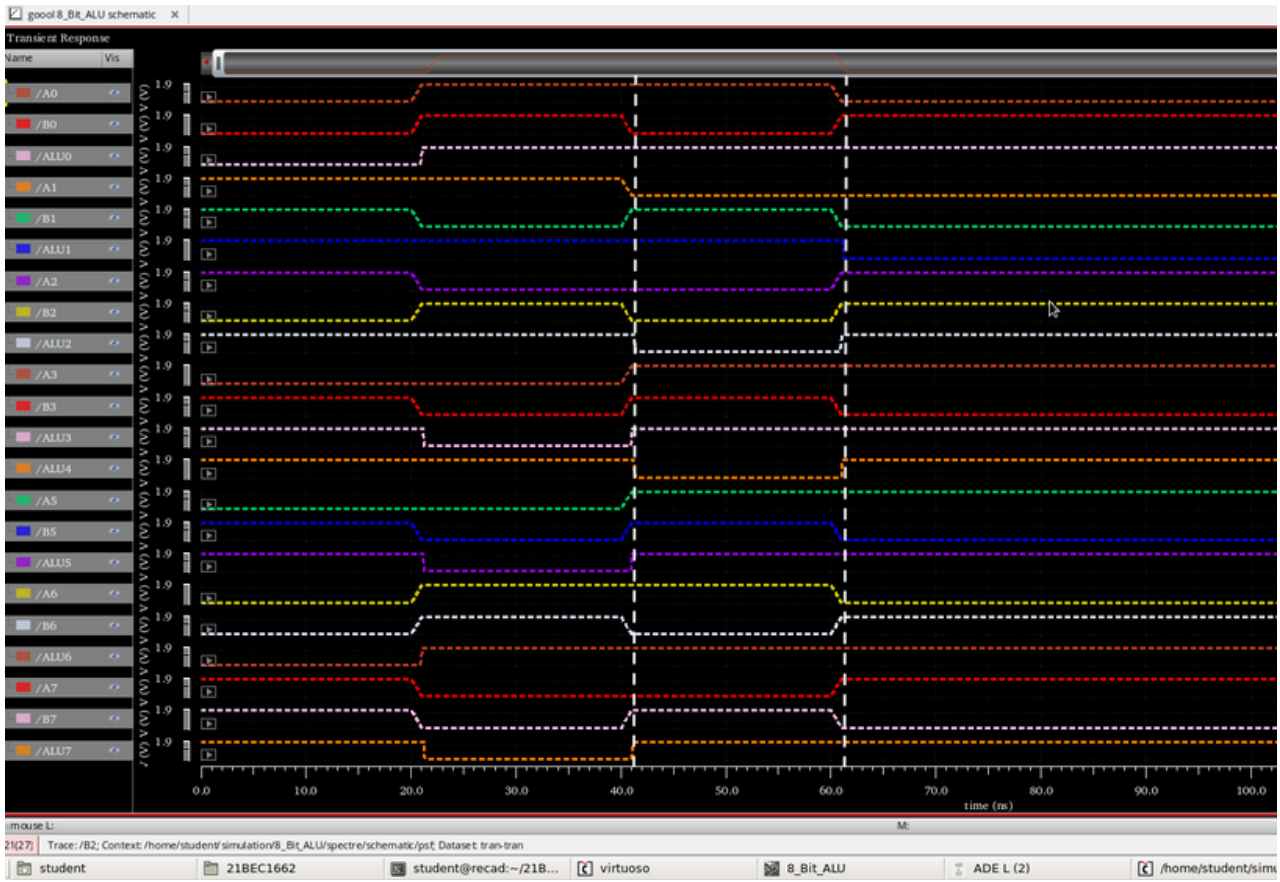
NOT



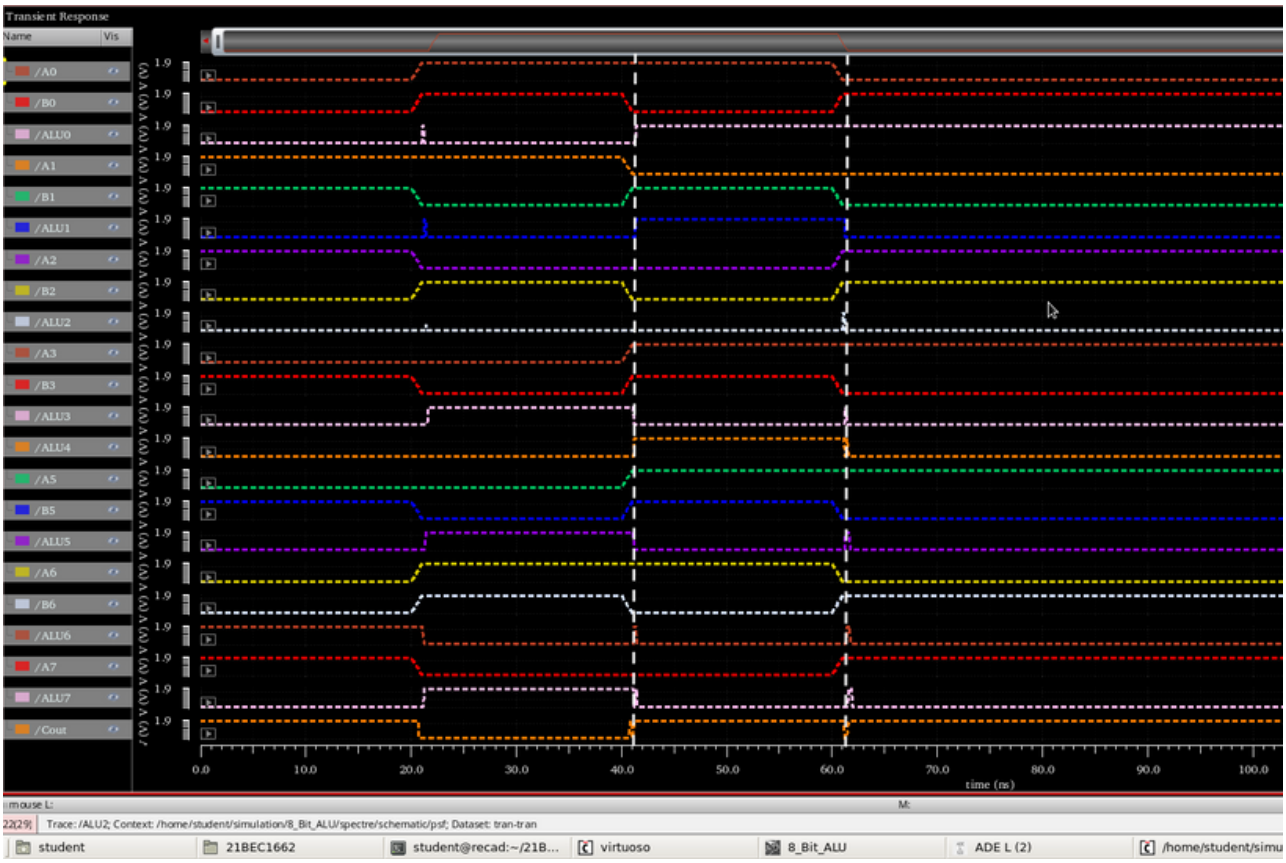
AND


goool 8_Bit_ALU schematic
Transient Response
Name
Vis
/A0
/B0
/ALU0
/A1
/B1
/ALU1
/A2
/B2
/ALU2
/A3
/B3
/ALU3
/ALU4
/A5
/B5
/ALU5
/A6
/B6
/ALU6
/A7
/B7
/ALU7
0.0
10.0
20.0
30.0
40.0
50.0
60.0
70.0
80.0
90.0
100.0
time (ns)
mouse L:
M:
Trace: /ALU1; Context: /home/student/simulation/8_Bit_ALU/spectre/schematic/psf; Dataset: tran-tran
student
21BEC1662
student@recad:~/21B...
virtuoso
8_Bit_ALU
ADE L (2)

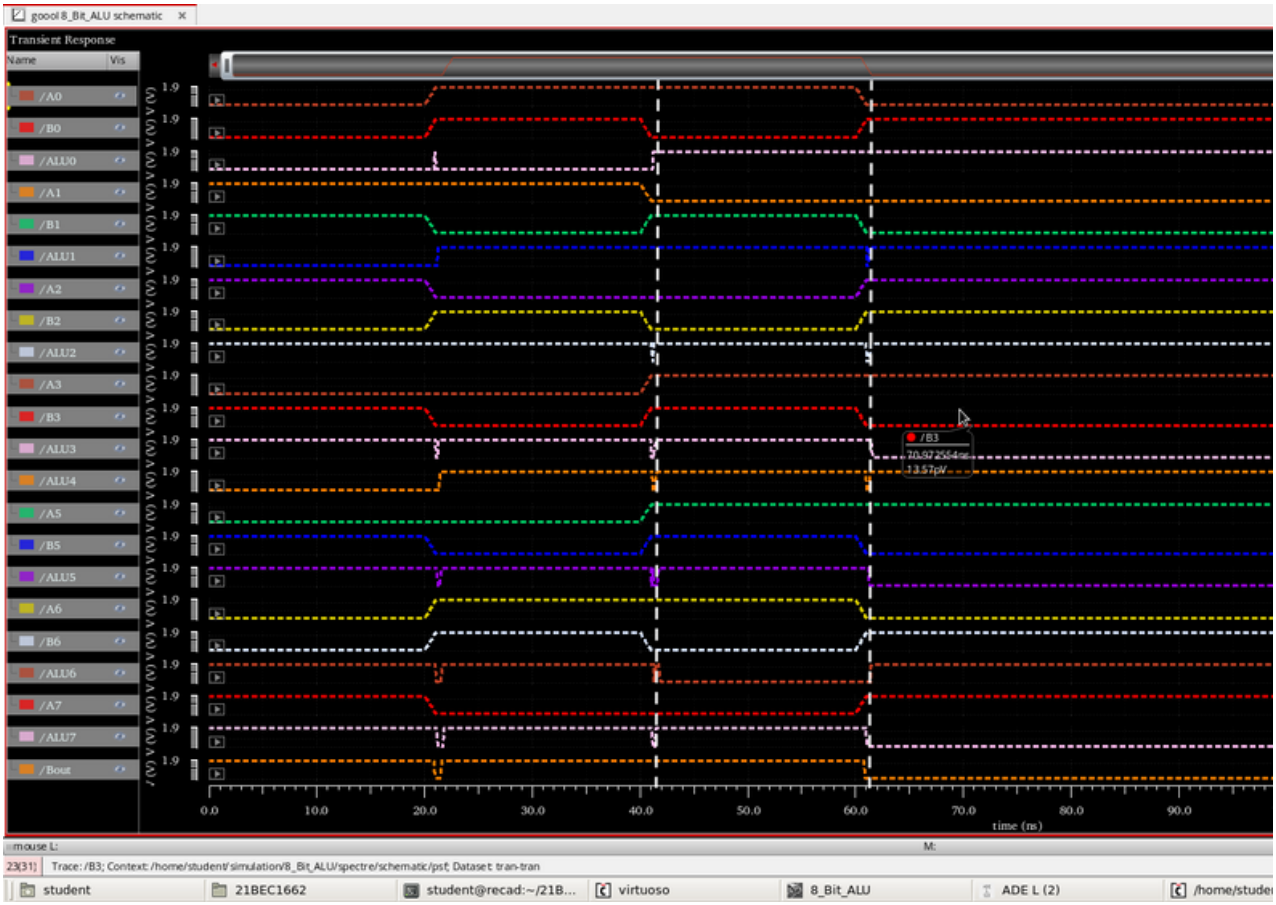
OR


goool 8_Bit_ALU schematic
Transient Response
Name
Vis
/A0
/B0
/ALU0
/A1
/B1
/ALU1
/A2
/B2
/ALU2
/A3
/B3
/ALU3
/ALU4
/A5
/B5
/ALU5
/A6
/B6
/ALU6
/A7
/B7
/ALU7
0.0
10.0
20.0
30.0
40.0
50.0
60.0
70.0
80.0
90.0
100.0
time (ns)
mouse L:
M:
Trace: /B2; Context: /home/student/simulation/8_Bit_ALU/spectre/schematic/psf; Dataset: tran-tran
student
21BEC1662
student@recad:~/21B...
virtuoso
8_Bit_ALU
ADE L (2)

FULL ADDER



FULL SUBTRACTOR



RESULT:

We have implemented 8 Bit ALU which contains logical NOT, AND, OR and Arithmetic ADDER and SUBTRACTOR using cadence.

We can infer that both Theoretical and Graphical values are same.

THANK YOU