Digital Design LA1 (10 Marks)

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* Required

MCQ Questions

Each Carries 1 marks

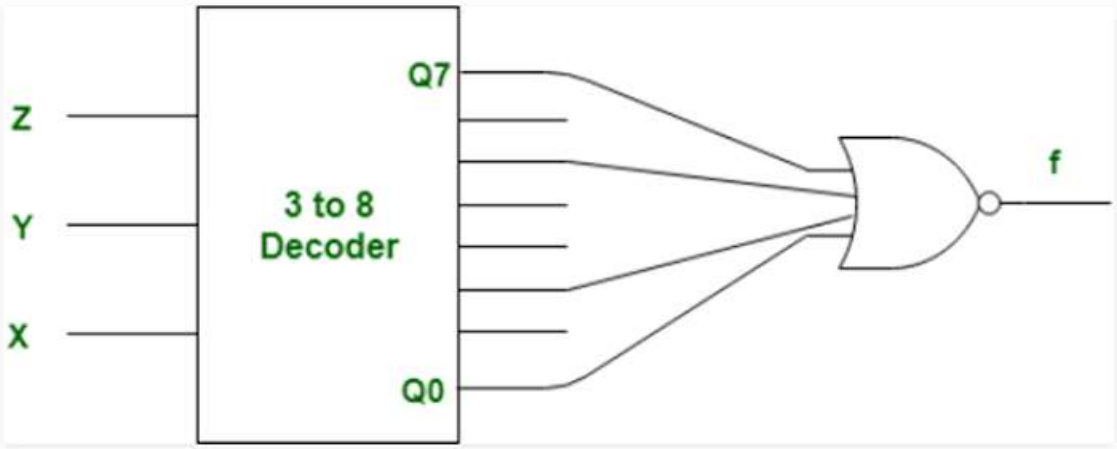
*

A circuit outputs a digit in the form of 4 bits. 0 is represented by 0000, 1 by 0001, ..., 9 by 1001. A combinational circuit is to be designed which takes these 4 bits as input and outputs 1 if the digit ≥ 5, and 0 otherwise. If only AND, OR and NOT gates may be used, what is the minimum number of gates required?

- (●) 3
- ( ) 5
- ( ) 2
- ( ) 4

*

What Boolean function does the circuit below realize ?



- B) xz'+x'z
- xz+x'z'
- x'y'+yz
- xy+y'z'

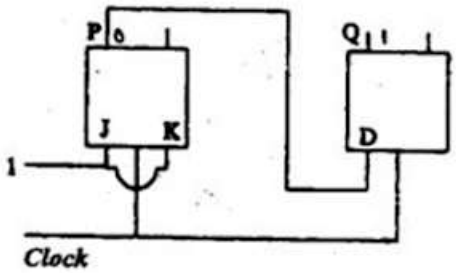
*

How many pulses are needed to change the contents of a 8-bit up counter from 10101100 to 00100111 (rightmost bit is the LSB)?

- 133
- 123
- 134
- 124

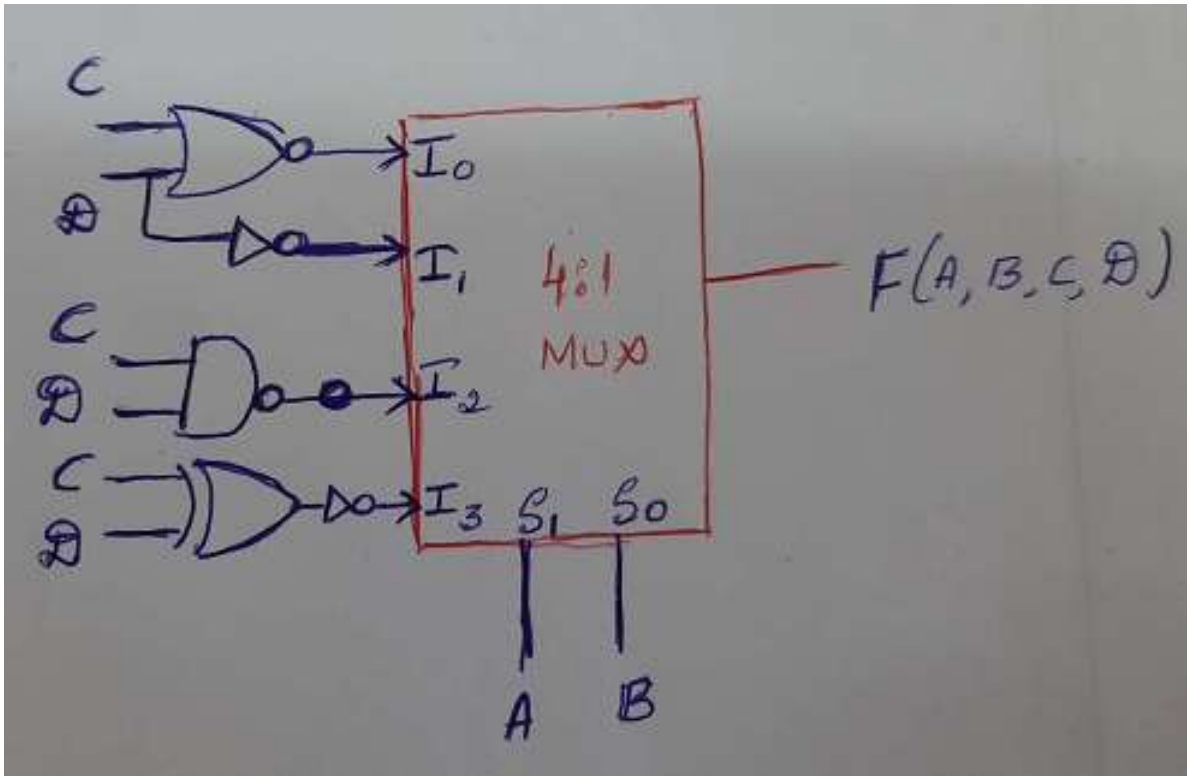
*

The following arrangement of master-slave flip flops has the initial state of P, Q as 0, 1 (respectively). After three clock cycles the output state P, Q is (respectively),



- (●) 1, 0
- ( ) 0, 0
- ( ) 0, 1
- ( ) B) 1, 1

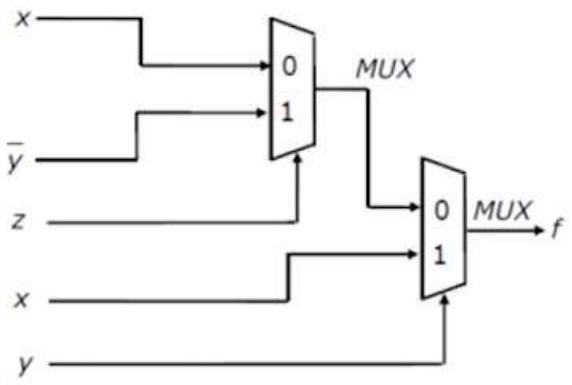
The Boolean function realized by the logic circuit shown is *



- F = Σm (0,4,6,11,12,13)
- F = Σm (0,4,6,9,11,12)
- F = Σm (0,4,6,10,11,12)
- F = Σm (0,4,6,11,12,15)

*

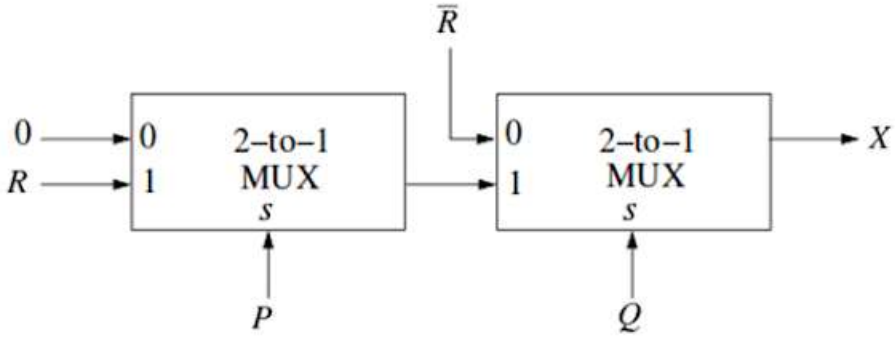
Consider the circuit above.Which one of the following options correctly represents f(x,y,z)?



- xz + xy' + y'z
- xy' + xy + y'z
- xz + xy + (yz)'
- xz' + xy + (yz)'

*

Consider the two cascaded 2-to-1 multiplexers as shown in the figure.



The minimal sum of products form of the output X is

(A) $\bar{P}\bar{Q}+PQR$

(B) $\bar{P}Q+QR$

(C) $PQ+\bar{P}\bar{Q}R$

(D) $\bar{Q}\bar{R}+PQR$

- [ ] C
- [x] D
- [ ] B
- [ ] A

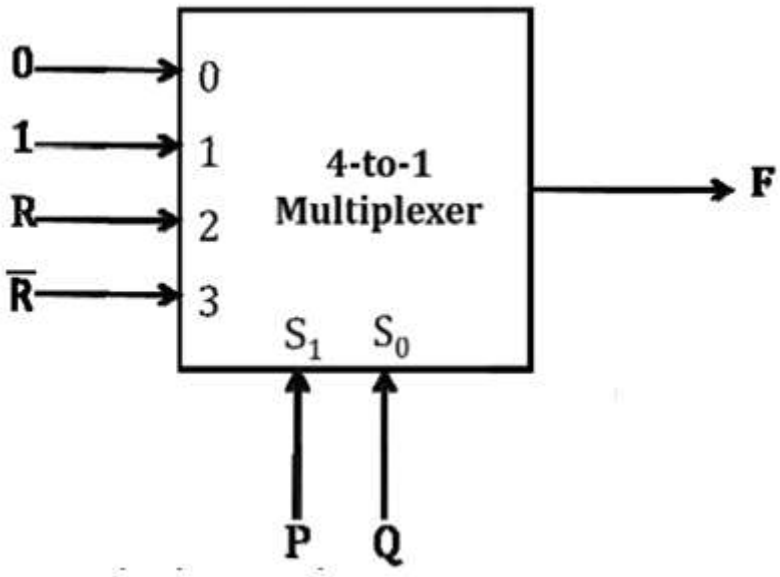
An Asynchronous Counter is a *

- [ ] None of the above
- [ ] Parallel Counter
- [ ] Fast Counter
- [x] Ripple Counter

Which of the following is a sequential circuit? *

- ○ Decoder
- ○ Full adder
- ◉ Counter
- ○ Multiplexer

The Boolean expression for the output F of the multiplexer shown below is *



- ○ D) PQR'
- ○ C) P'QR + P'QR' + QR' + PQ'R
- ○ P'Q + P'QR' + PQR' + PQ'R
- ◉ P'Q + QR' + PQ'R

In Boolean algebra, rule (X+Y)(X+Z) = *

- ○ XZ+Y
- ○ XY+Z
- ○ Y+XZ
- ◉ X+YZ

A combinational logic circuit which generates a particular binary word or number is *

- ○ Decoder
- ○ Encoder
- ○ Demultiplexer
- ◉ Multiplexer

*

In a positive-edge-triggered JK flip-flop, if J and K both are high then the output will be _____ on the rising edge of the clock.

- ○ Reset
- ○ No change
- ◉ Toggle
- ○ Set

*

What is the minimum number of NAND gates required to implement a 2-input EXCLUSIVE-OR function without using any other logic gate?

- (●) 4
- ( ) 5
- ( ) 3
- ( ) 6

*

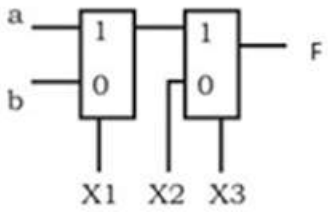
The Boolean function with the Karnaugh map is:

CD \ AB	00	01	11	10
00	0	1	1	0
01	0	1	1	1
11	1	1	1	1
10	0	1	1	0

- (●) (A+C).D+B
- ( ) (A+D).C+B
- ( ) (A+C).B+D
- ( ) (A+B).C+D

*

The following circuit implements a two-input AND gate using two 2-1 multiplexers. What are the values of X_1, X_2, X_3?



- ○ X1=a, X2=0, X3=b
- ◉ X1=b, X2=0, X3=a
- ○ X1=a, X2=b, X3=1
- ○ X1=b, X2=1, X3=b

Evaluate (X xor Y) xor Y? *

- ○ All 1's
- ◉ X
- ○ All 0's
- ○ Y

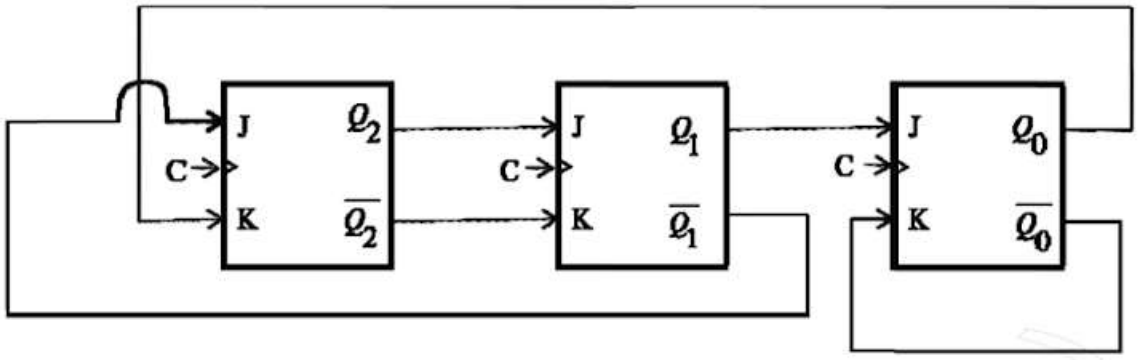
*

Which of the following binary number is the same as its 2's complement?

- 0101
- 1001
- 1000
- 1010

*

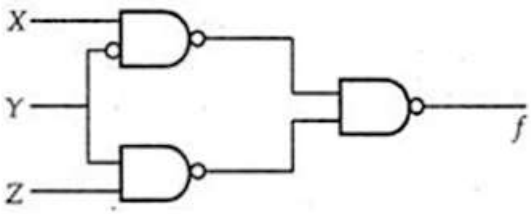
The below sequential circuit is built using JK flip-flops is initialized with Q2Q1Q0 = 000. The state sequence for this circuit for the next 3 clock cycle is



- 100, 110, 111
- 100, 011, 001
- 111, 110, 101
- 001, 010, 011

*

Consider the following circuit. Which one of the following is TRUE?



- ○ f is independent of Y
- ◉ None of X, Y, Z is redundant
- ○ f is independent of X
- ○ f is independent of Z

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