CompSOC: Virtual execution platforms for mixed-criticality systems

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- Cyber-physical, embedded real-time systems usually contain multiple concurrent applications that have different characteristics and requirements, and are often designed by different parties. As a result, a single system contains applications designed using different models of computation (MOC), and with different criticalities (e.g. real time, safety critical, adaptive, or not). By offering an independent execution virtual platform to each application, the CompSOC platform enables independent design, verification, and execution of applications with different criticalities and models of computation. We present the underlying concepts, architecture, and formalism of the CompSOC platform. More information can be found on www.compsoc.eu.

the current CompSOC team

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- Eindhoven university of technology
  - Kees Goossens (team leader)
  - Gabriela Breaban
  - Valeriu Codreanu
  - Sven Goossens
  - Manil Dev Gomony
  - Martijn Koedam
  - Reinier van Kampenhout
  - Rachana Kumar
  - Yonghui Li
  - Andrew Nelson
  - Shubhendu Sinha
  - Rasool Tavakoli
  - Juan Valencia
- Prague University
  - Benny Akesson
- close collaboration with the dataflow research (SDF3) at TU/e
  - Marc Geilen
  - Sander Stuijk
  - Dip Goswami
  - Majid Nabi
- and many others

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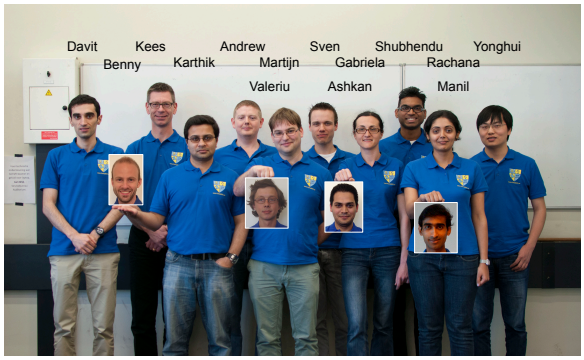
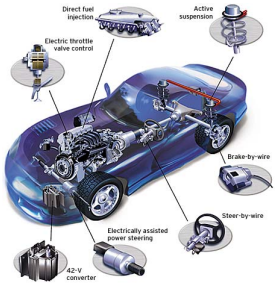


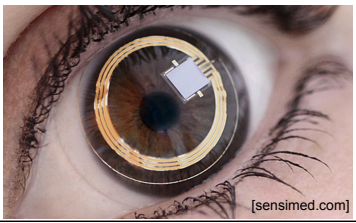
trend: embedded systems

3

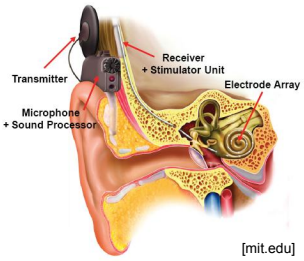
- phones, game consoles, cars, refrigerators, buildings, ...
- interaction with physical world ➔ real-time requirements



[wikipedia.org]



[sensimed.com]



[mit.edu]

trend: embedded systems

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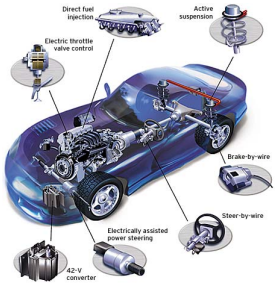

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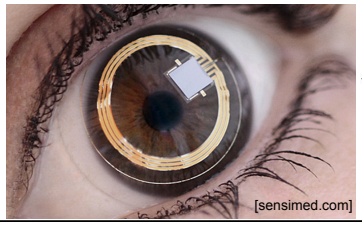
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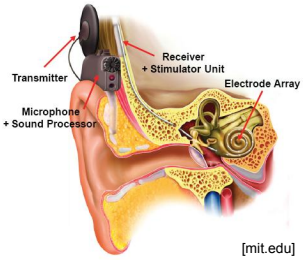

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trend: multiple applications on one embedded device

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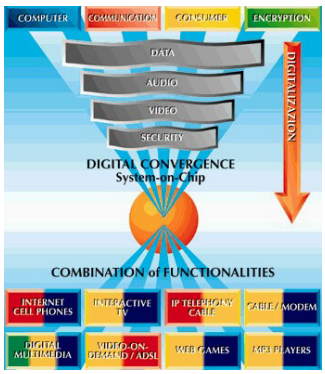
- different application domains
  - infotainment (streaming → video analysis), games
  - real-time control, (wireless) networking stacks



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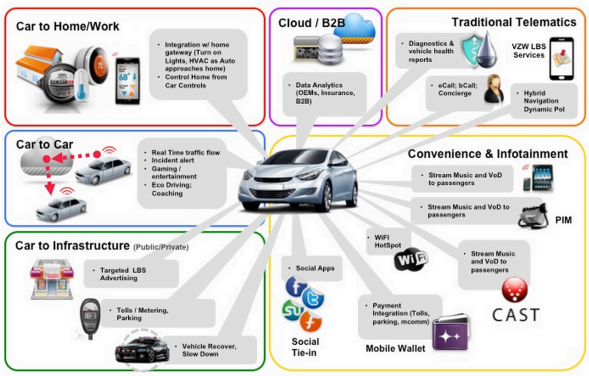

[carvoyant.com]

trend: multiple applications on one embedded connected device

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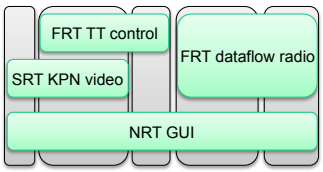
- different application domains
  - infotainment (streaming → video analysis), games
  - real-time control, (wireless) networking stacks
- use cases
- sharing resources



observation: different applications

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- have different characteristics and requirements
  - FRT, SRT, NRT, adaptive, ...
- are designed by different parties
- use different models of computation (MOC) & verification approaches
  - FRT → worst case & formal verification
  - NRT → average case & simulation
  - adaptive SRT → actual case & simulation
- use different resource-management policies
  - data / event / time, schedulers, power management

problem: design time

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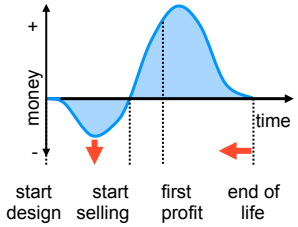
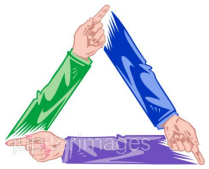
- systems are complex
- time is short

- it takes too long
- getting worse



- monolithic verification after integration
  - hardware, multiple applications

- circular verification
  - who to blame for errors?



goal & approach

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- reduce SOC design & verification effort

- independent design, verification, and deployment per application
  - application as the unit of verification

- two complexity-reducing techniques
  - composability
  - predictability

- applied to multi-processor system with distributed shared memory

composability

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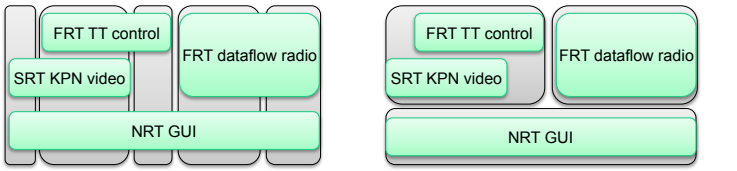
- virtual execution platform per application
  - defined by its space, time, energy budgets
- design, verify, deploy in a virtual platform
- no interference
  - when integrating, executing, or switching use cases



N! combinations & interleavings	➔	N virtual platforms
inter-dependent state $2^S \times 2^S \times 2^S \times 2^S$	➔	independent states $2^S + 2^S + 2^S + 2^S$

composability

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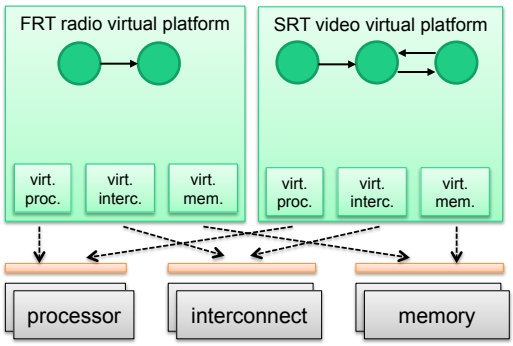
- time-division-multiplex virtual execution platforms
  - space, time, energy budgets
  - no interference



inter-application scheduling
µkernel

composability & predictability

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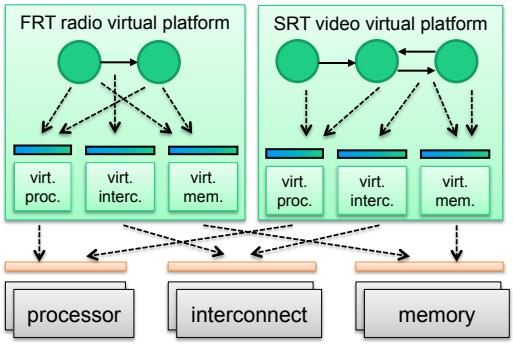
- each application can have its own
  - programming model, scheduling, power management
  - (CS)DF, KPN, TT, DSM
- for RT use predictable schedulers, and associated real-time formalism



intra-application scheduling & power management

inter-application scheduling

CompSOC

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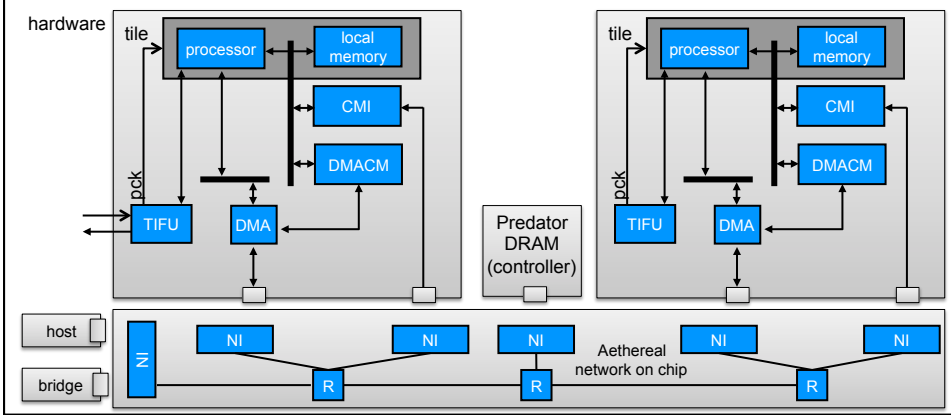

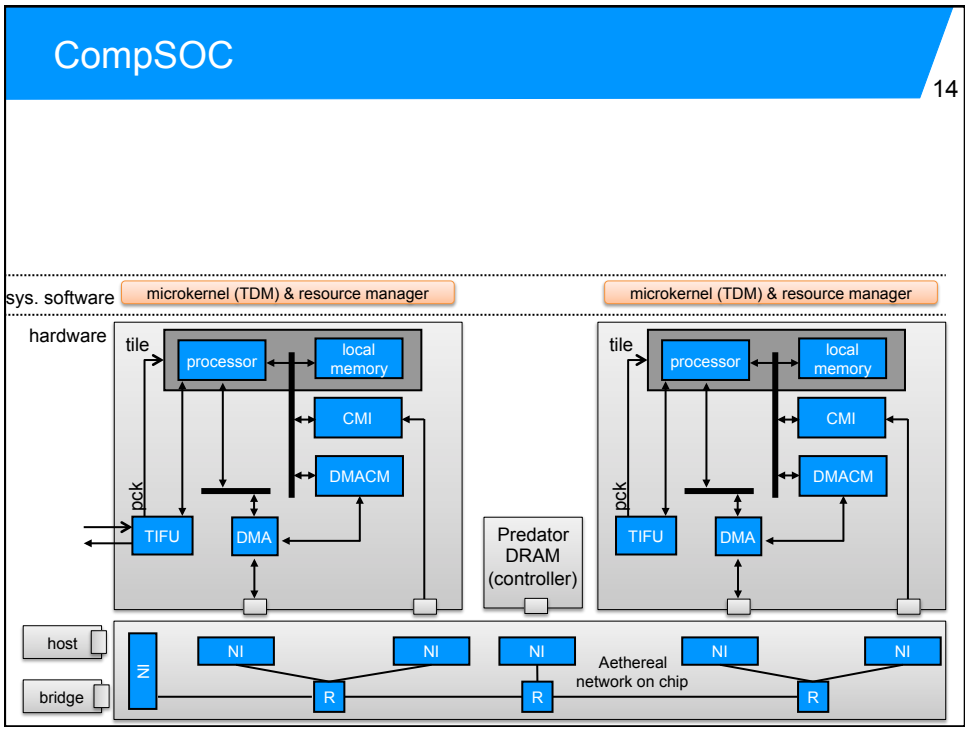
CompSOC
14
sys. software
microkernel (TDM) & resource manager
microkernel (TDM) & resource manager
hardware
tile
processor
local memory
CMI
DMACM
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TIFU
DMA
Predator DRAM (controller)
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Aethereal network on chip
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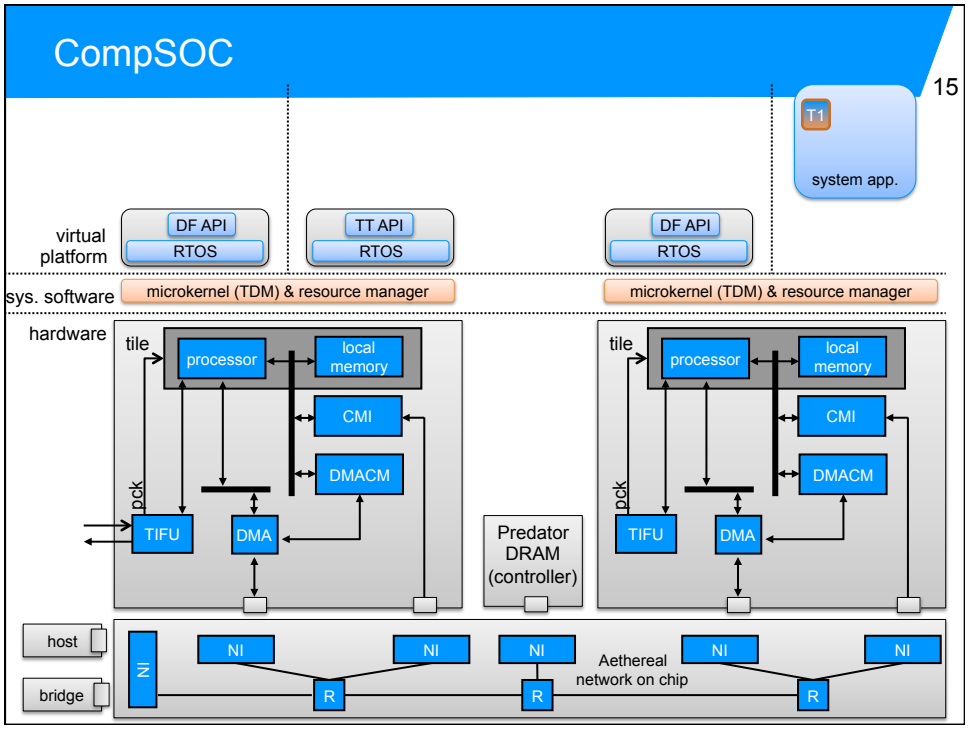
CompSOC
15
T1
system app.
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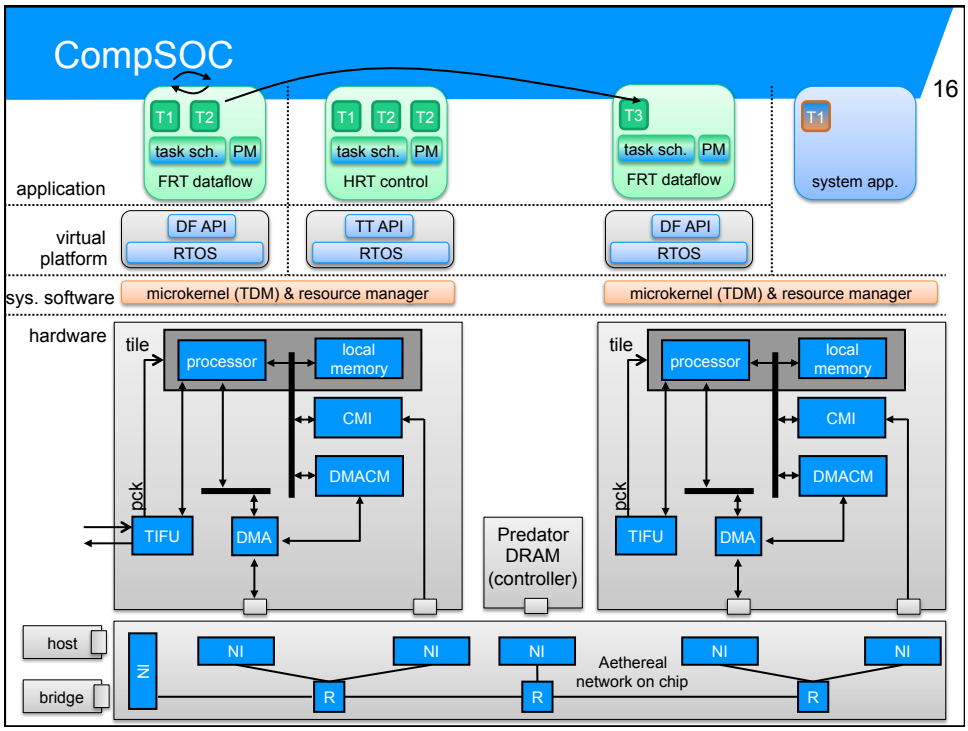
CompSOC
16
application
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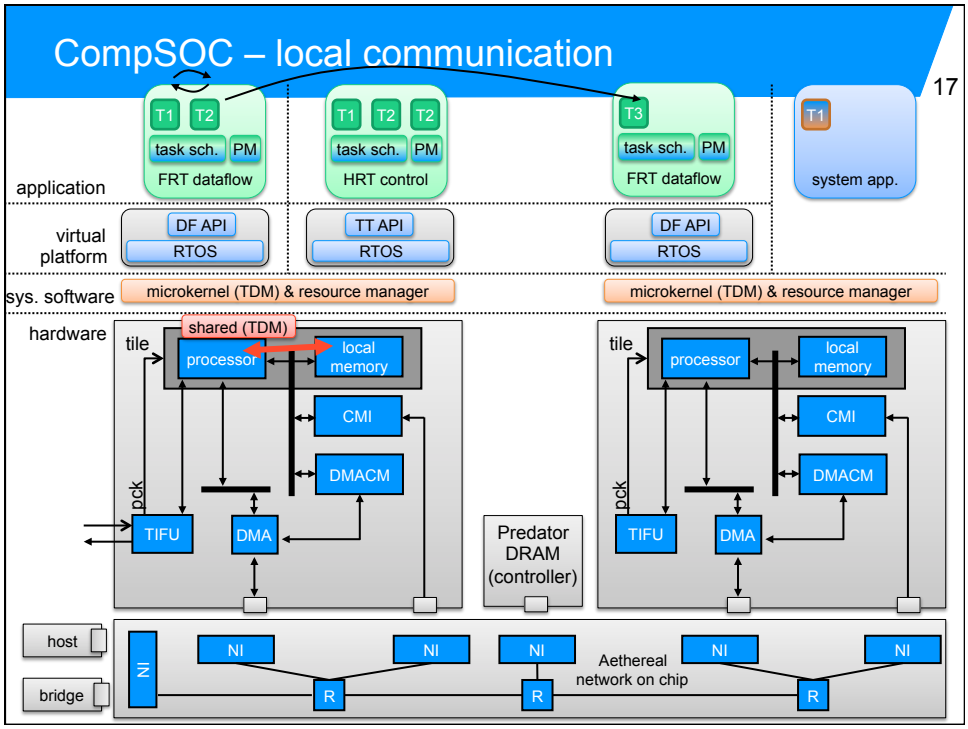
CompSOC – local communication
17
application
virtual platform
sys. software
hardware
shared (TDM)
T1
T2
task sch.
PM
FRT dataflow
HRT control
T3
system app.
DF API
TT API
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microkernel (TDM) & resource manager
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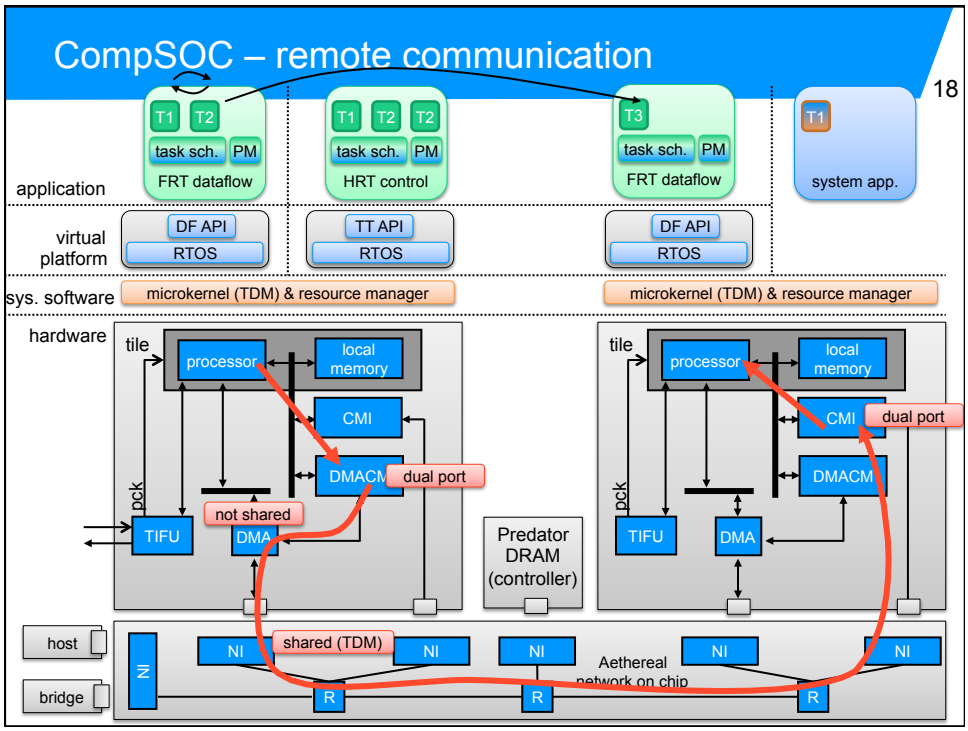
Aethereal network on chip


CompSOC – remote communication
18
application
virtual platform
sys. software
hardware
T1
T2
task sch.
PM
FRT dataflow
HRT control
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system app.
DF API
TT API
RTOS
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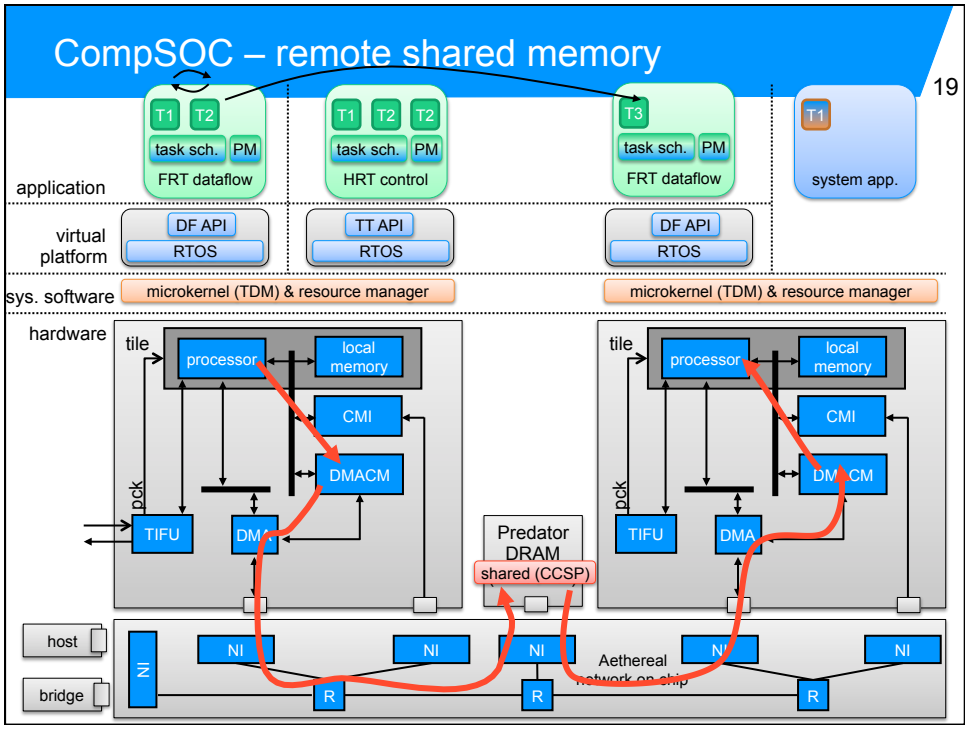
Aethereal network on chip


CompSOC – remote shared memory
19
application
virtual platform
sys. software
hardware
T1
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task sch.
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HRT control
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CompSOC software architecture

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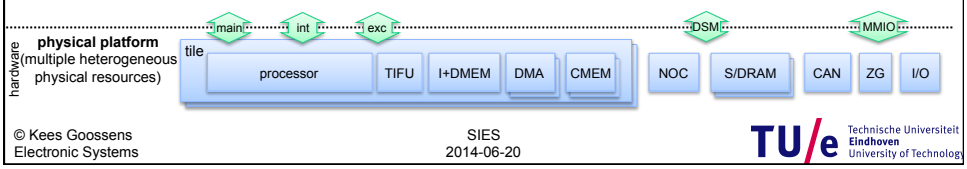

CompSOC software architecture

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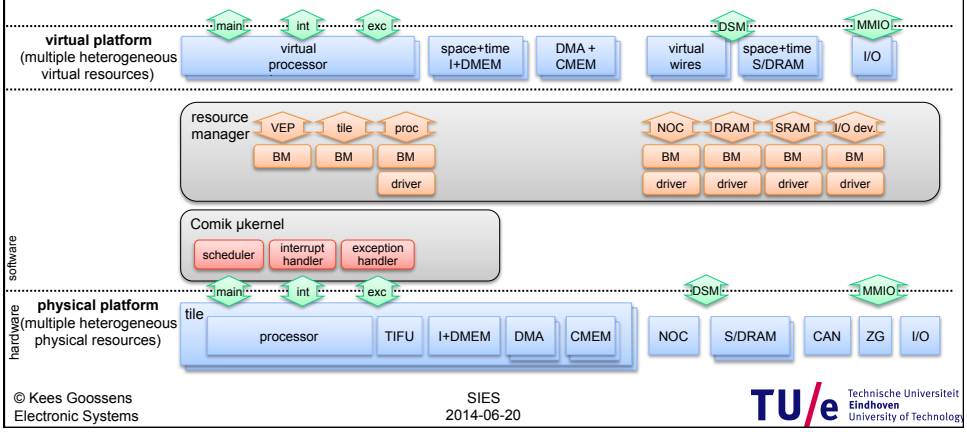

CompSOC software architecture

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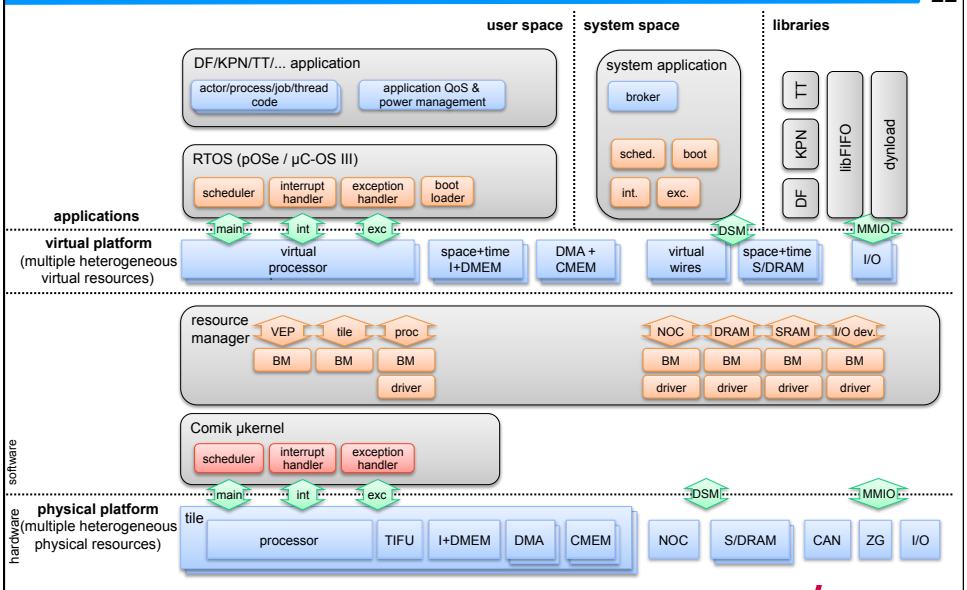

composability

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- applications can use any programming model
  - cyclo-static dataflow
  - variable-rate dataflow
  - KPN
  - time-triggered
  - distributed-shared memory, with restrictions (see later)
- mixed-criticality platform

demo: 4-battery-run-short.avi [DATE'12]

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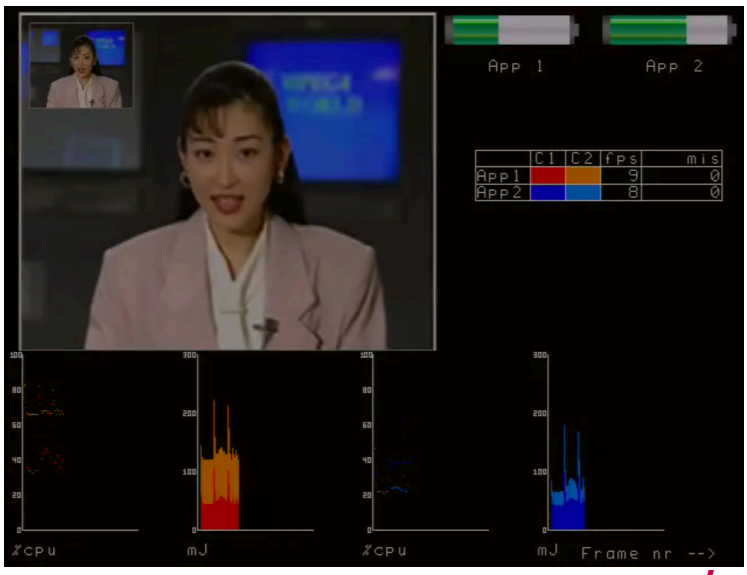
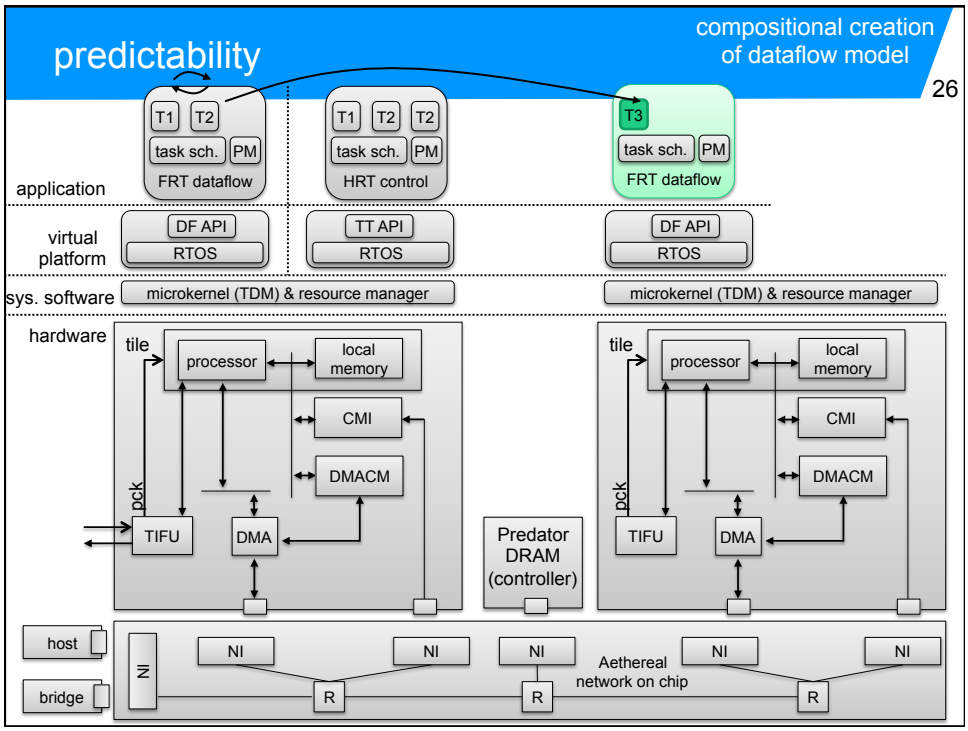


predictability

25

- cyclo-static dataflow (CSDF) is
  - the programming model
  - used to describe the binding of application to platform
    - unshared resources
    - shared resources
- extending to scenario/mode-aware dataflow (Stuijk, Moreira)


predictability
compositional creation of dataflow model
26
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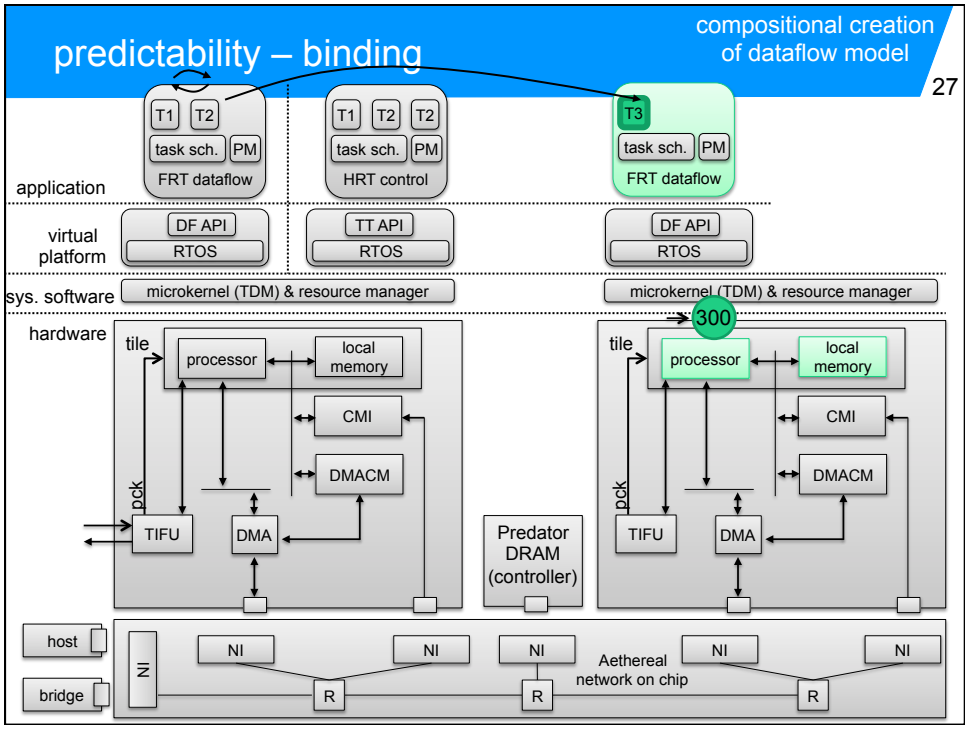
predictability – binding
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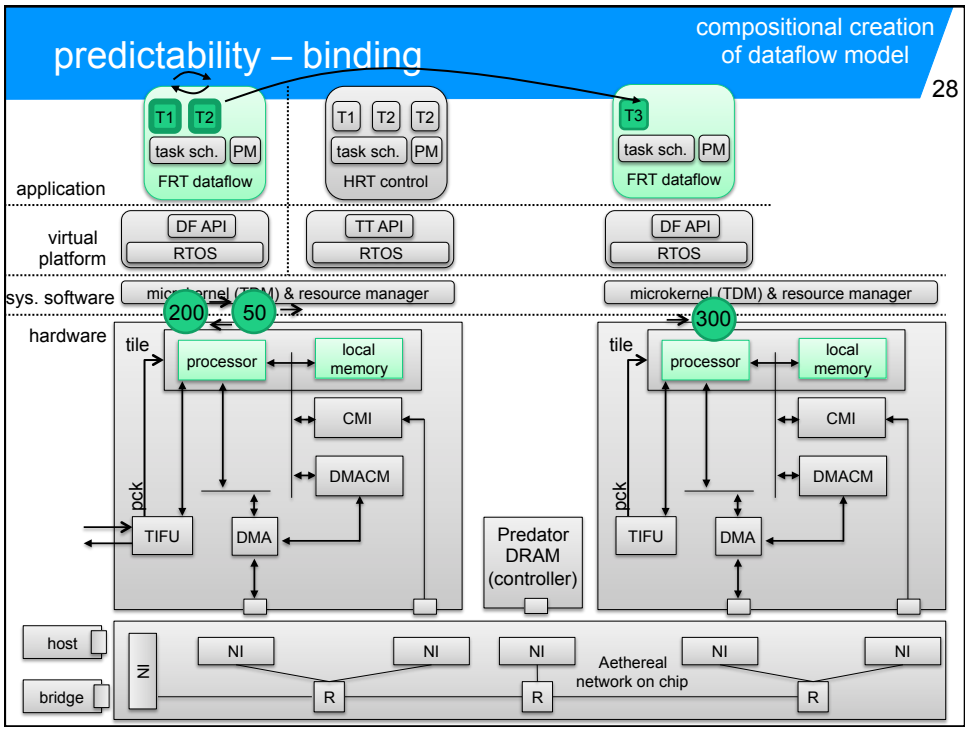
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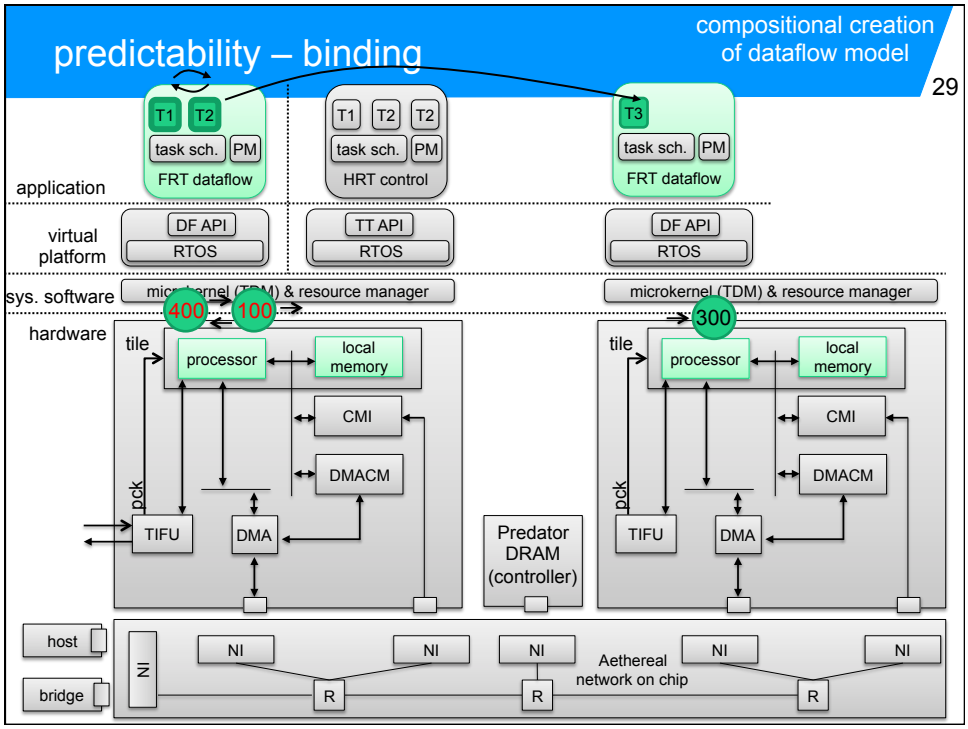
predictability – binding
compositional creation of dataflow model
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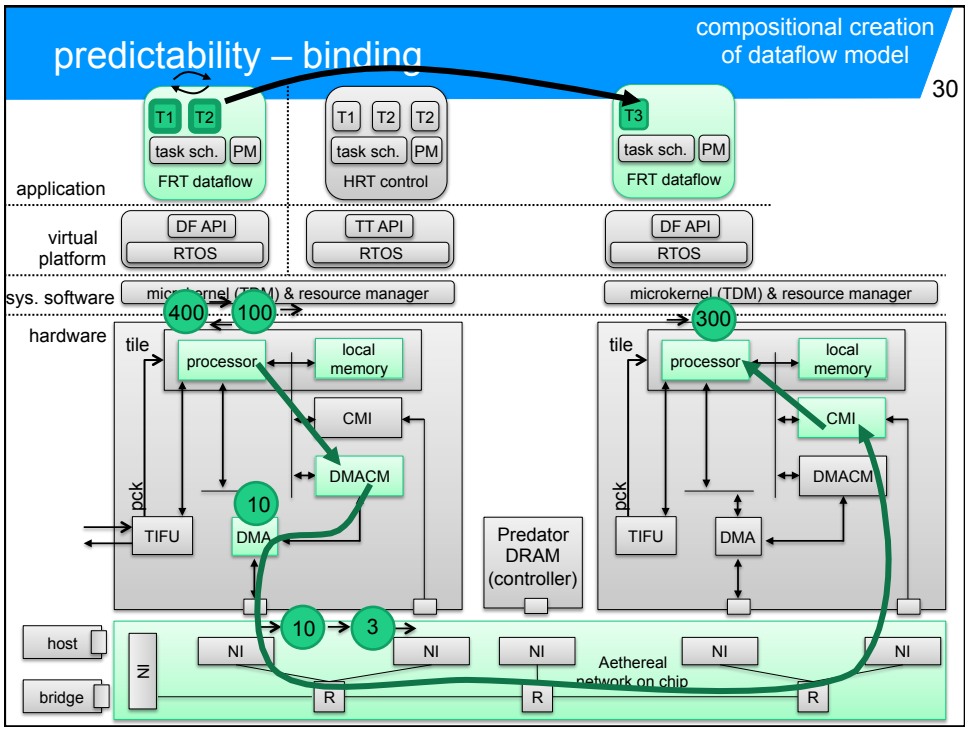

predictability with CSDF

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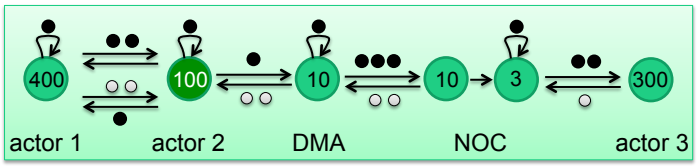

- CSDF graph captures
  - application functionality & data dependencies
  - mapping of application on unshared resources (WCET)
  - resource sharing (SO, TDM, RR, LR, ...)
  - finite buffer sizes, flow control / backpressure
- compositional method
  - CSDF graph is constructed of independent smaller subgraphs
  - budgets within application, and between applications

predictability with CSDF

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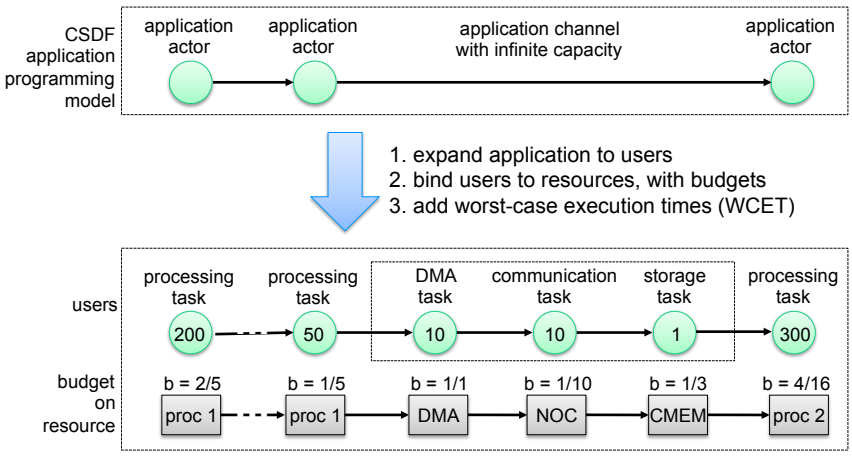

predictability with CSDF

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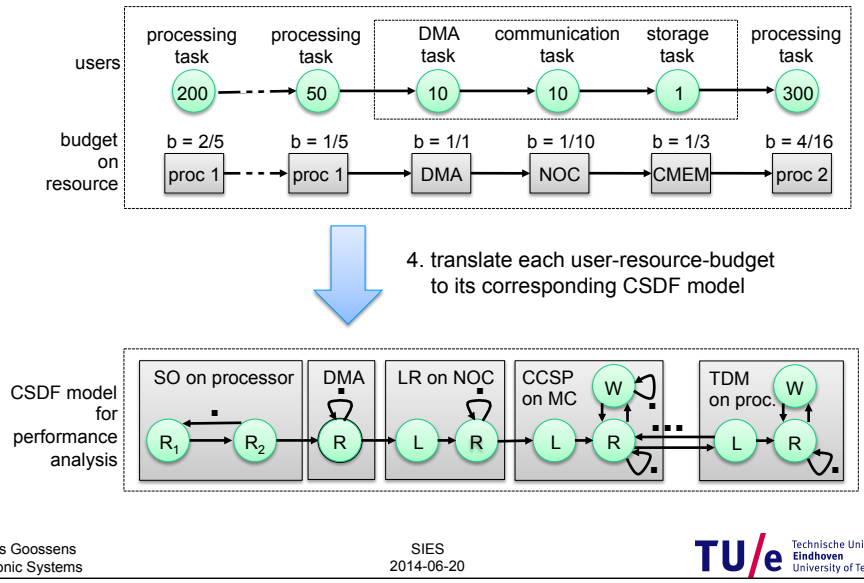
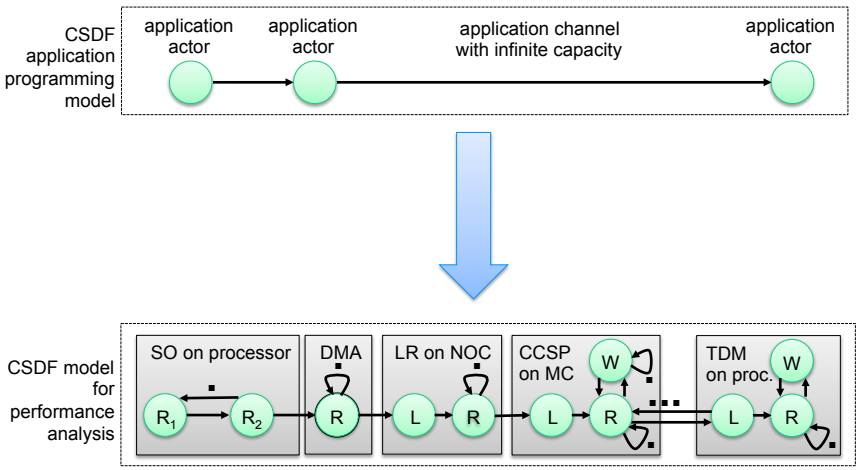


predictability with CSDF

34



design flow

35

- the CompSOC & SDF3 dataflow framework
- automatic generation of
  - hardware: processor tiles, NOC, memory controllers
  - software: RTOS, resource management, drivers, MOC libraries
- for applications
  - application bundles
    - ELFs
    - virtual platform specification (actor-resource binding, buffer sizes, RTOS scheduling interval, scheduler settings (SO schedule, TDM slots, CCSP priorities, etc.))
    - dynamically loaded on the hardware at run time
- for CSDF applications
  - end-to-end application throughput and latency analysis
- FPGA prototype

CompSOC & SDF³ design flow

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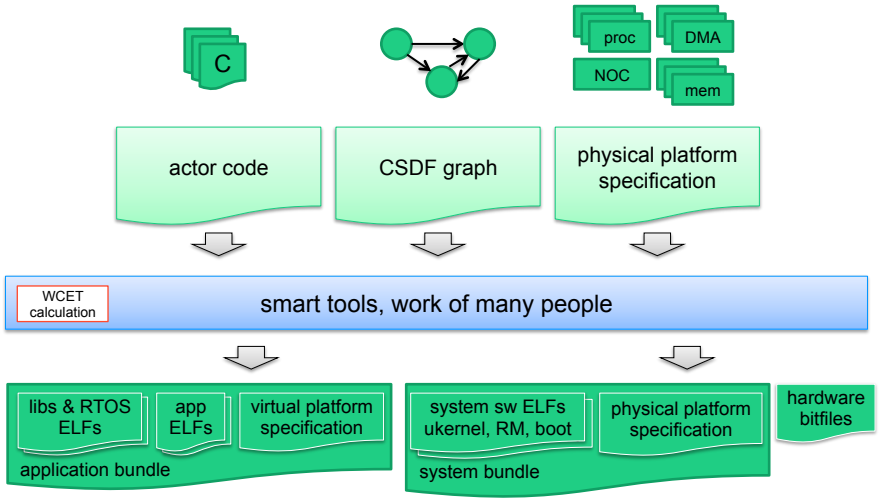

CompSOC design flow

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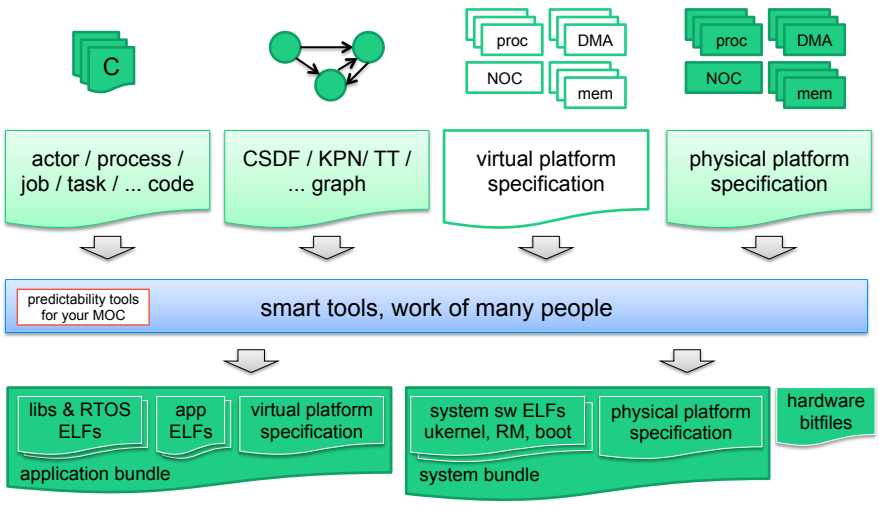
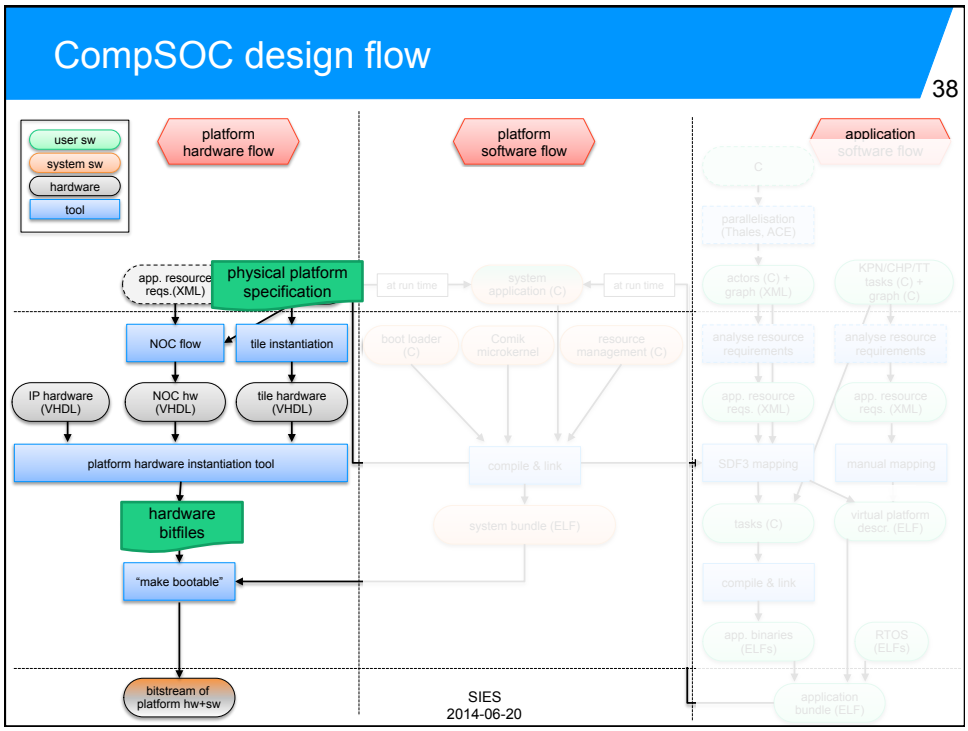
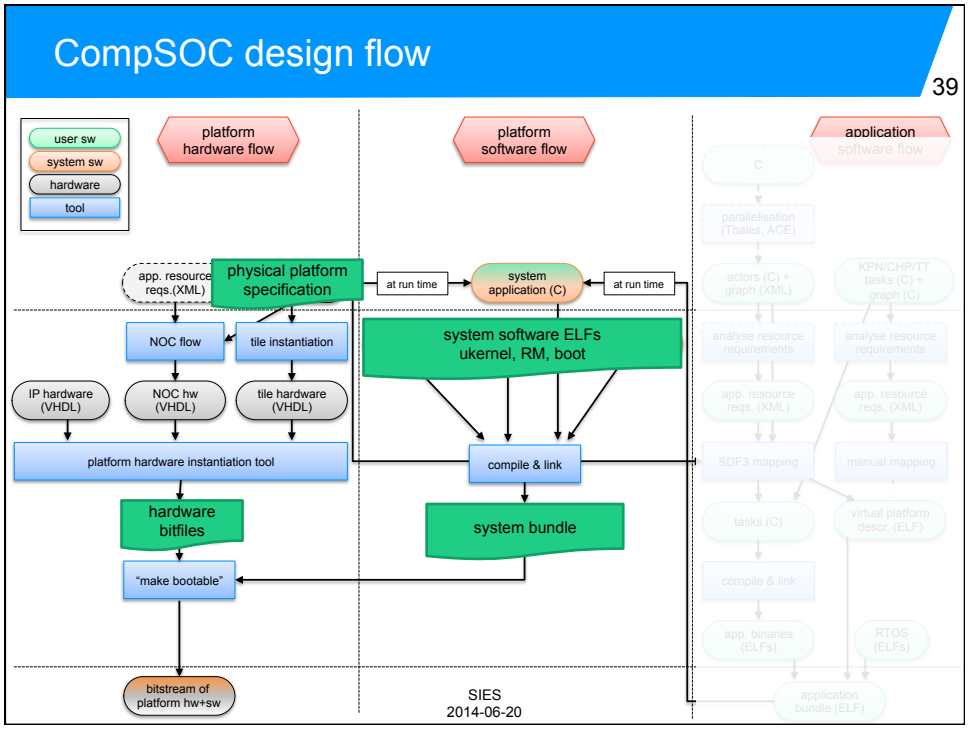



CompSOC design flow
38
user sw
system sw
hardware
tool
platform hardware flow
platform software flow
application software flow
app. resource reqs.(XML)
physical platform specification
at run time
system application (C)
at run time
NOC flow
tile instantiation
boot loader (C)
Comik microkernel
resource management (C)
IP hardware (VHDL)
NOC hw (VHDL)
tile hardware (VHDL)
platform hardware instantiation tool
compile & link
hardware bitfiles
system bundle (ELF)
"make bootable"
bitstream of platform hw+sw
SIES
2014-06-20
C
parallelisation (Thales, ACE)
actors (C) + graph (XML)
KPN/CHP/TT tasks (C) + graph (C)
analyse resource requirements
app. resource reqs. (XML)
SDF3 mapping
manual mapping
tasks (C)
virtual platform descr. (ELF)
compile & link
app. binaries (ELFs)
RTOS (ELFs)
application bundle (ELF)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39
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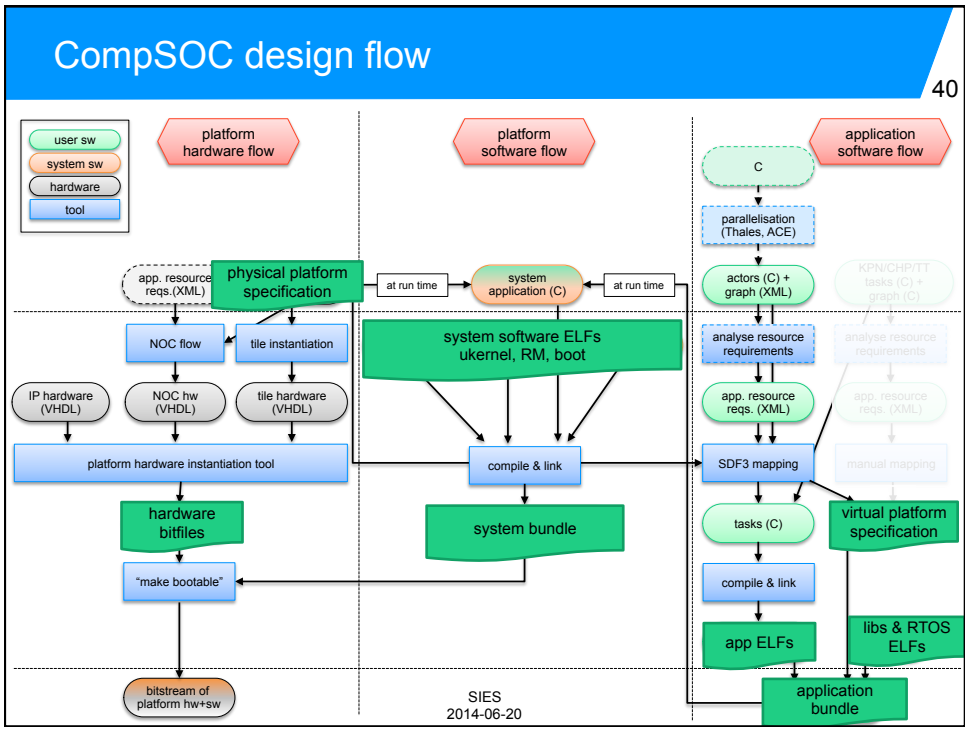
CompSOC design flow
40
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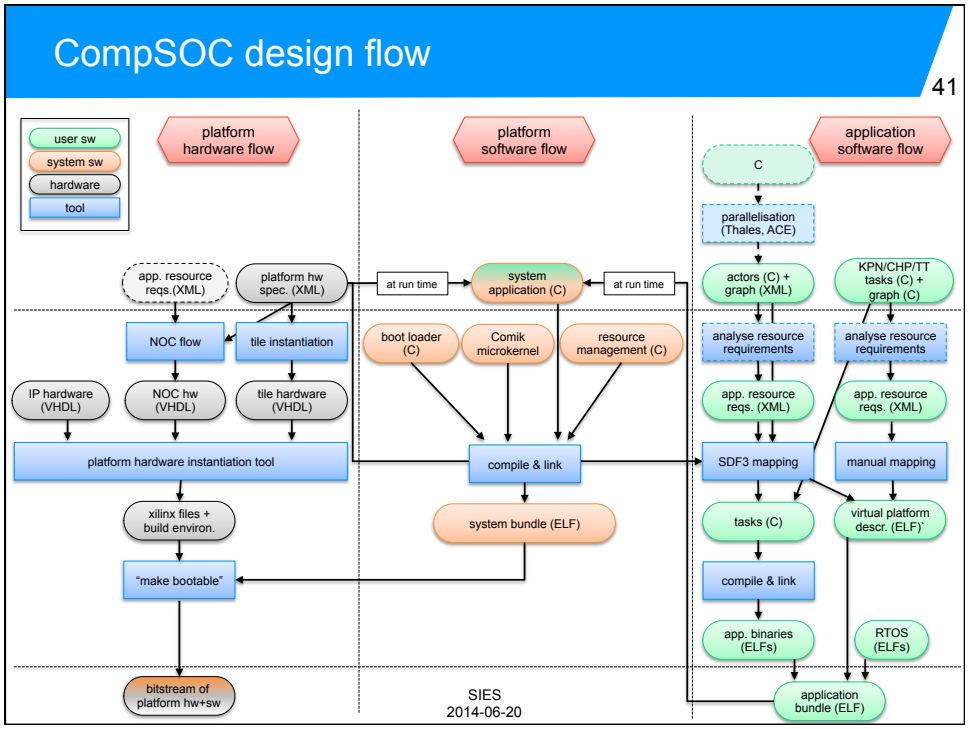
compile & link
app ELFs
libs & RTOS ELFs
bitstream of platform hw+sw
SIES
2014-06-20
application bundle


CompSOC design flow
41
user sw
system sw
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tool
platform hardware flow
platform software flow
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C
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SIES
2014-06-20
application bundle (ELF)

CompSOC – run-time loading

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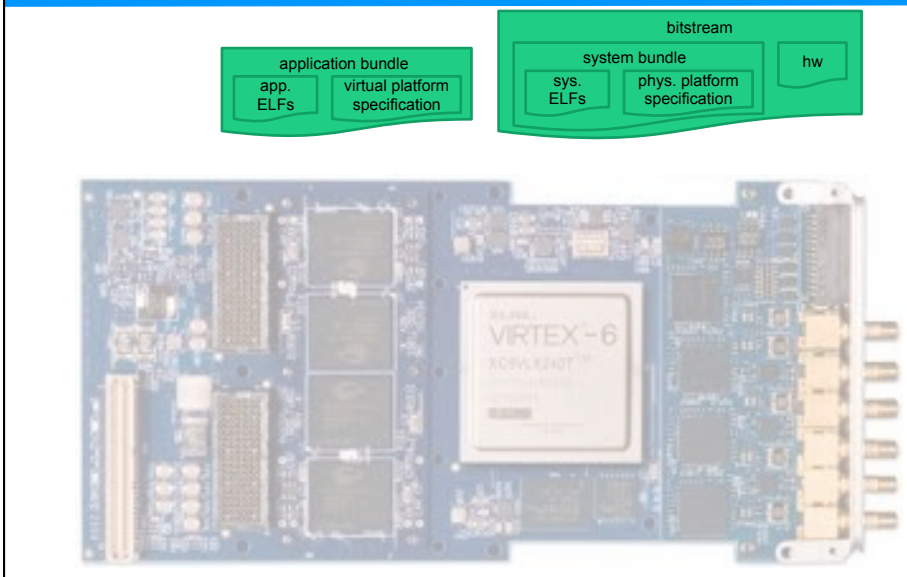
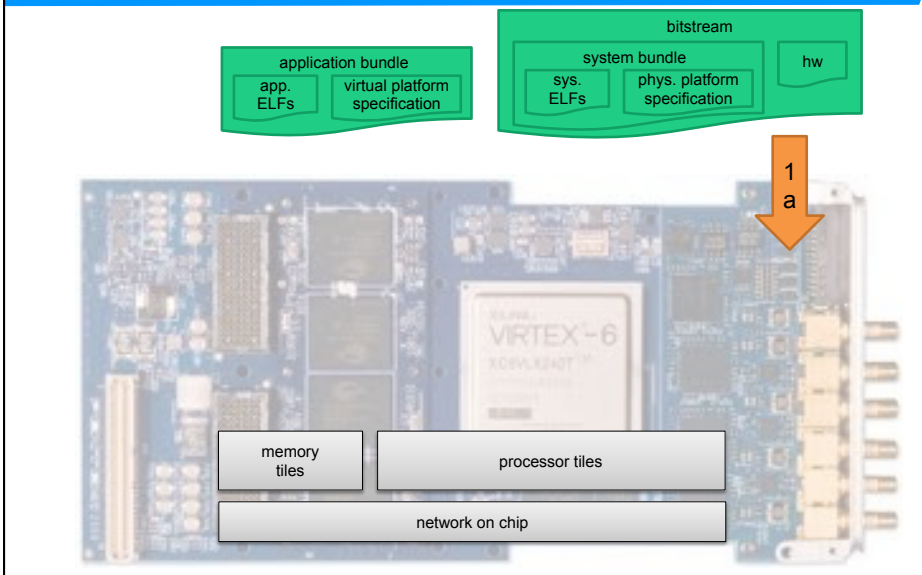


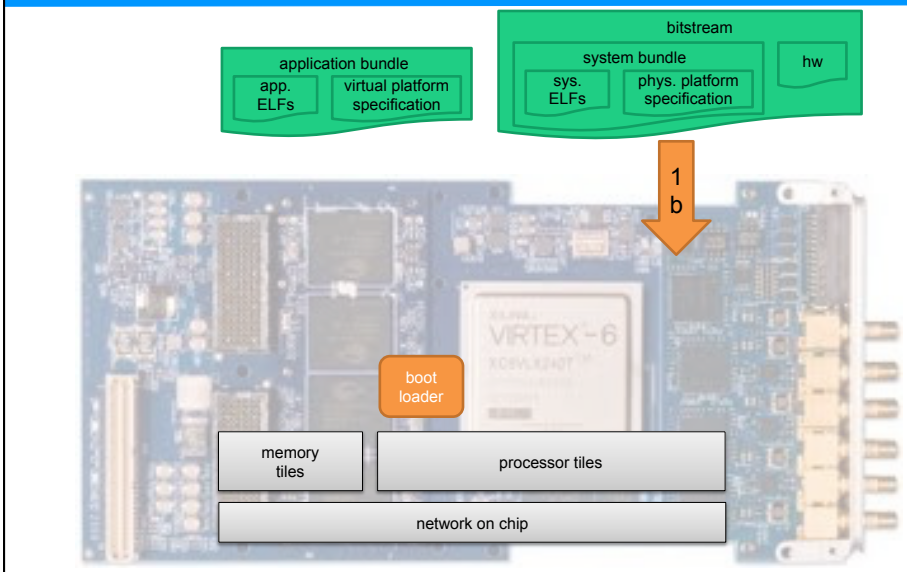
CompSOC – run-time loading

43



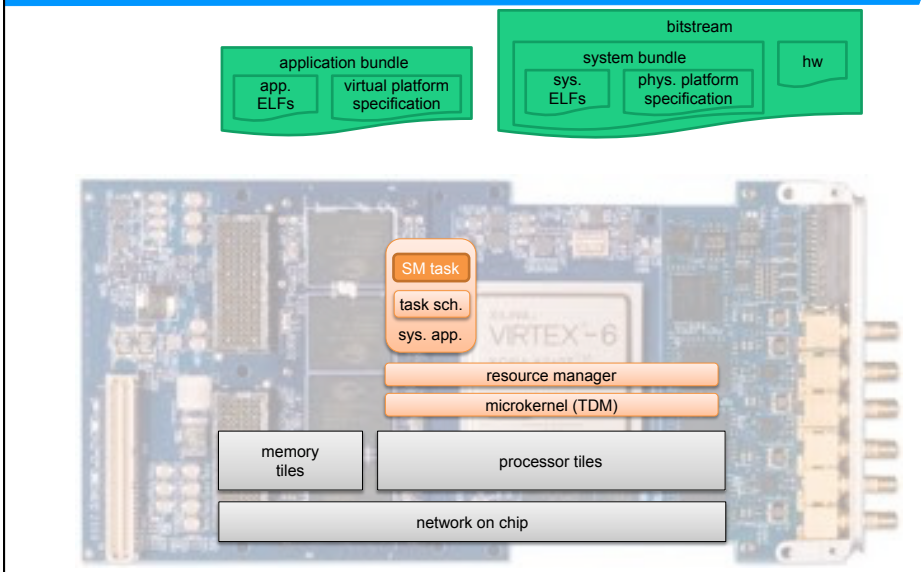
CompSOC – run-time loading

44



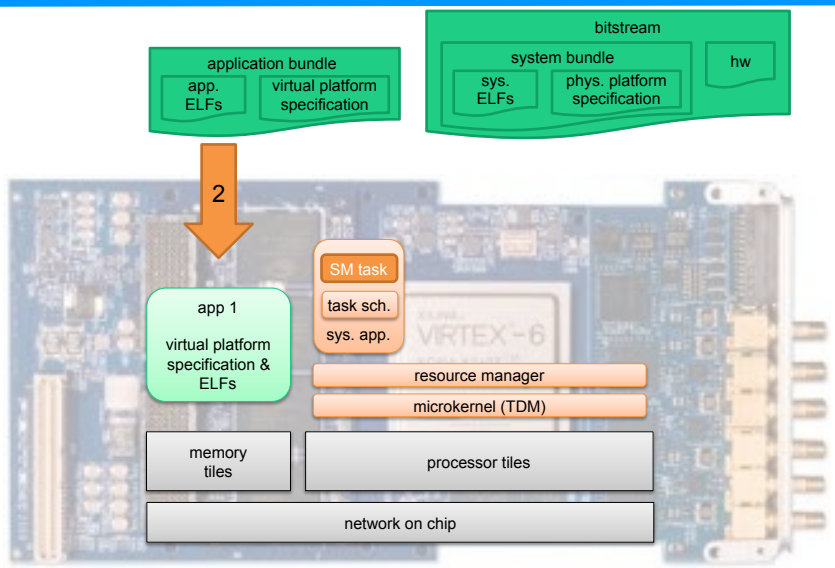
CompSOC – run-time loading

45



CompSOC – run-time loading

46



CompSOC – run-time loading

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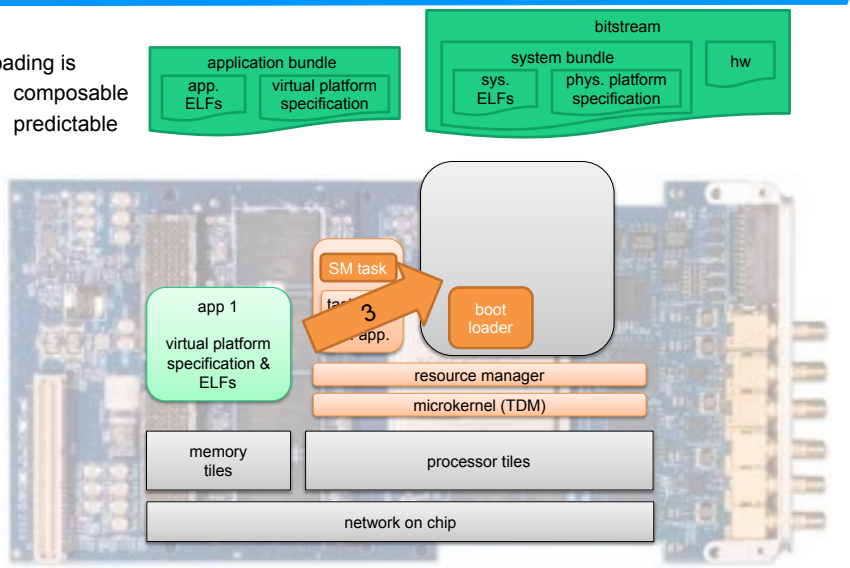
- loading is
  - composable
  - predictable



CompSOC – run-time loading

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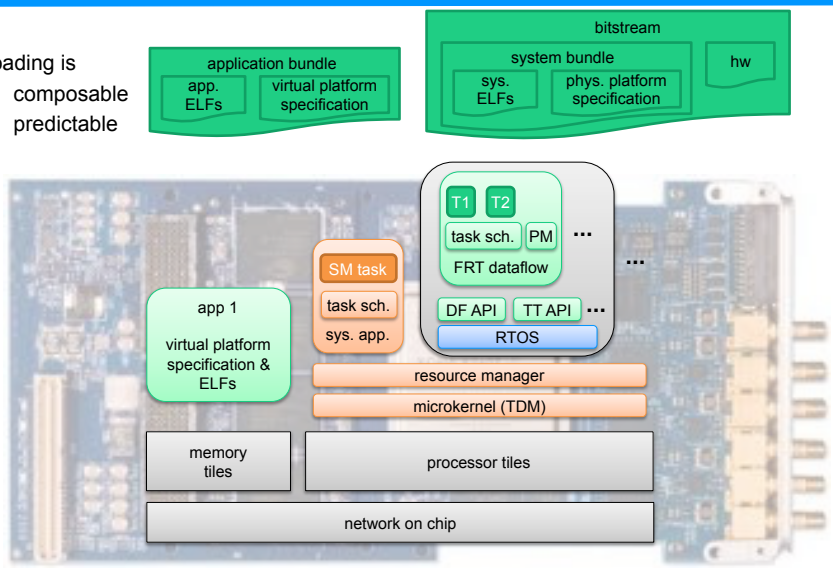
- loading is
  - composable
  - predictable



(current) restrictions

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- data and code must fit in local tile memories
  - no caches, or else flush on preemption
- no I/O virtualisation
- DVFS is simulated on FPGA
- external interrupts – supported
- preemptive intra-application scheduling – supported
- memory protection – supported

- limited support for multiple use cases in the design flow
- currently supported programming models
  - cyclo-static dataflow (actors)
  - Kahn process networks (processes)
  - time-triggered (jobs) – limited

demo: playback-dynamic-load.mp4 [DATE'14]

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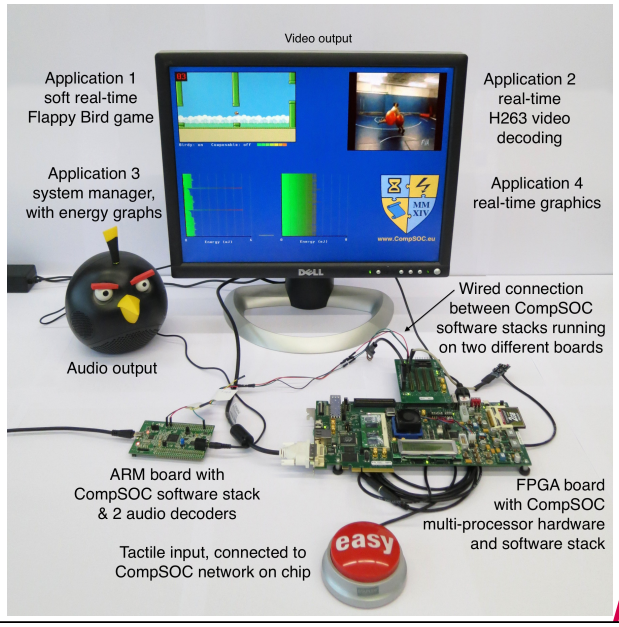

demo: playback-dynamic-load.mp4 [DATE'14]

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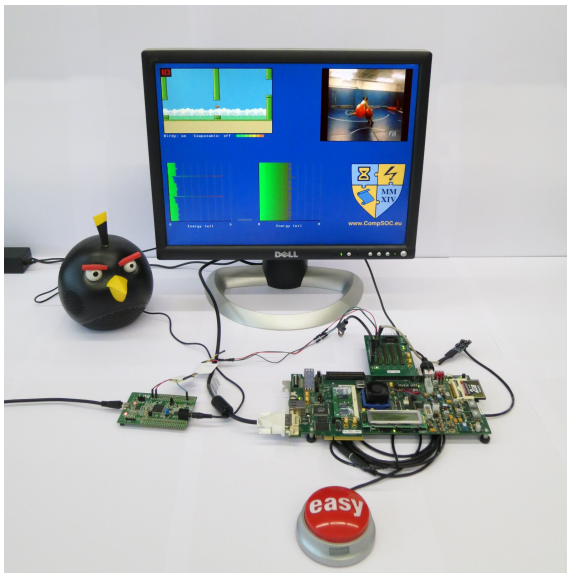
- applications
  - SRT flappy bird
  - RT adaptive H263 decoder
  - RT graphics
  - system application
  - 2x audio decoding
- FPGA board
  - MPSOC
  - for button input
  - for video output
- ARM board
  - for audio mixing & output
- linked with serial I/O



demo: playback-dynamic-load.mp4 [DATE'14]

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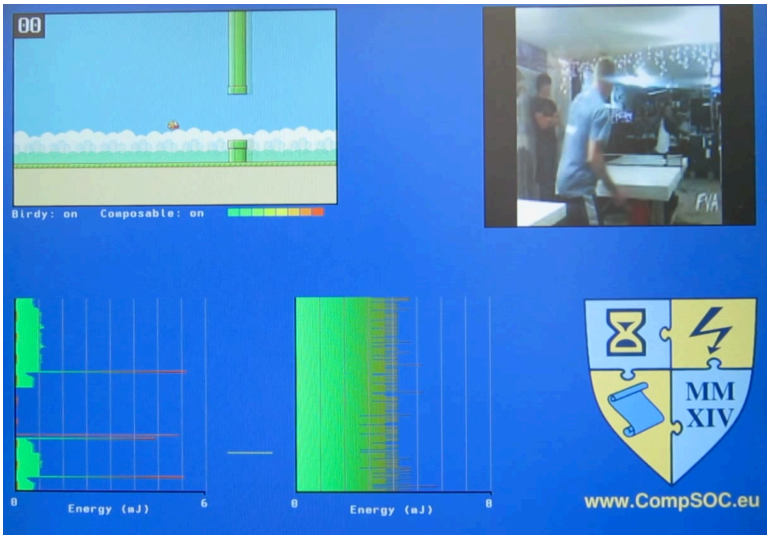

conclusions

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- reduce SOC design effort
- independent design, verification, and execution per application
- composability
- predictability
- virtual execution platforms with
  application-specific MOC, scheduling, power management
  – any mix of NRT, SRT, FRT
- design flow
- FPGA prototype
- used in teaching MSc embedded systems lab

more information: www.compsoc.eu

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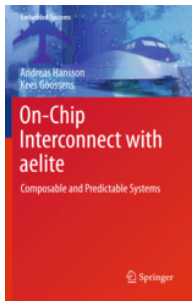
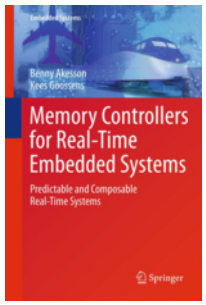
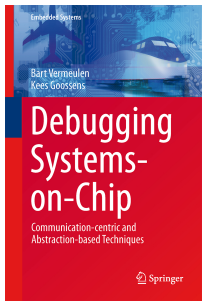
- CompSOC overview in SIGBED'13 and in Multiprocessor System-on-Chip. Huebner (ed), Springer, 2010
- Aethereal real-time NOC, DAC'10
- Real-time DRAM memory controller, DATE'13, ECRTS'14
- CompOSe RTOS, MICPRO'11
- CoMiK microkernel, DATE'14
- Composable power management, SAMOS'11
- Design flow, FPGA World'13
- SDF3, DAC'06 http://www.es.ele.tue.nl/sdf3/







acknowledgements

55

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  - Kees Goossens (team leader)
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  - Sven Goossens
  - Martijn Koedam
  - Reinier van Kampenhout
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  - Marc Geilen
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end

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for further information

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