SWITCHED CAPACITOR BASED MULTI-LEVEL BOOST INVERTER

A MINI PROJECT - II REPORT

submitted by

RAGHURAM S (119005096)

towards partial fulfillment of the requirements for the award of the degree

of

Bachelor of Technology
in
Electrical & Electronics Engineering

School of Electrical and Electronics Engineering

SASTRA DEEMED TO BE UNIVERSITY
(A University established under section 3 of the UGC Act, 1956)
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BONAFIDE CERTIFICATE

This is to certify that the project work entitled "**SWITCHED CAPACITOR BASED MULTI-LEVEL BOOST INVERTER"** is a bonafide record of the work carried out by

RAGHURAM S (119005096)

student of fourth year B.Tech., Electrical and Electronics Engineering, in partial fulfillment of the requirements for the award of the degree of B.Tech in Electrical & Electronics Engineering of the **SASTRA DEEMED TO BE UNIVERSITY, Thirumalaisamudram, Thanjavur - 613401,** during the year 2015-2019.

Mr. Girish Ganesan. R (AP - II/EEE/SEEE)

SIGNATURE

Project Viva-Voce held on _____

Examiner -I **Examiner-II**

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ABSTRACT

KEY WORDS: Switched capacitor, Multilevel Inverter, Self-charge balancing, HPWM, Series-Parallel Connection

Currently, reduced number of circuit components and voltage sources are considered as one of the most important features in Multi-Level Inverters (MLIs). Thus, in this project, a switched capacitor multilevel inverter is proposed which has inherent boosting property and self-charge balancing of capacitors without the use of voltage sensors or auxiliary balancing circuits. It also employs reduced number of components, thus decreasing complexity and costs. The structure proposed is capable of producing 9 level output waveform using two capacitors in tandem with a single voltage source. The voltage levels are obtained through series parallel switching and use of redundant switching states. The inverter is modulated using Hybrid PWM technique, which enables significant switching loss reduction by making use of low switching frequency modulation. Hence, a high quality output waveform, with close resemblance to a sine wave is therefore obtained.

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ABBREVIATIONS

DC	Direct Current
AC	Alternating Current
PWM	Pulse-Width Modulation
THD	Total Harmonic Distortion
MLI	Multilevel inverter
FACTS	Flexible AC Transmission Systems
FFT	Fast Fourier Transform
HPWM	Hybrid Pulse-Width Modulation
RLC	Resistive-Capacitive-Inductive
SC	Switched-Capacitor
SCMLI	Switched Capacitor Multilevel Inverter
CM	Commander Coefficient

NOTATIONS

V_{ref}	Reference voltage value
A_r	Amplitude of reference voltage
A_c	Amplitude of carrier
Sgn	Signum function

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CHAPTER 1

INTRODUCTION

1.1 Classical Inverters

In recent years, industries have begun to demand higher power equipment, even reaching the megawatt level. Power Electronic devices are nowadays the most important component in converting and controlling of electric power, principally in extracting power from renewable sources.

Inverters play a crucial role in variable frequency drives, air conditioning, uninterruptible power supplies, induction heating, high voltage DC power transmission, electric vehicle drives, static var compensators, active filters, flexible AC transmission systems. They are also used for converting the DC power commonly obtained from storage elements to AC power required for common electrical loads.

Based on the nature of the output waveform, inverters can be classified as: square wave inverters, quasi-square wave inverters, two-level PWM inverters and multilevel inverters [1] (Fig. 1.1.1).

1.2 Motivation

THD is a measure of the harmonics that are present in a waveform. These harmonics are integral multiples of the fundamental frequency. Harmonics mitigation is crucial as they distort the output waveform and produce losses in the system.

In order to reduce these harmonics, passive filters have been widely available. However, the main issue with these filters is that the size of the inductor and capacitor is too large to be

feasible and efficient for lower order harmonics at a fundamental frequency of 50 Hz.

The principle aim of a multilevel inverter is to produce a waveform that resembles a pure sine wave as much as possible. Reduction in overall part count as compared to the classical topologies has been an important objective in the recently introduced multilevel topologies.

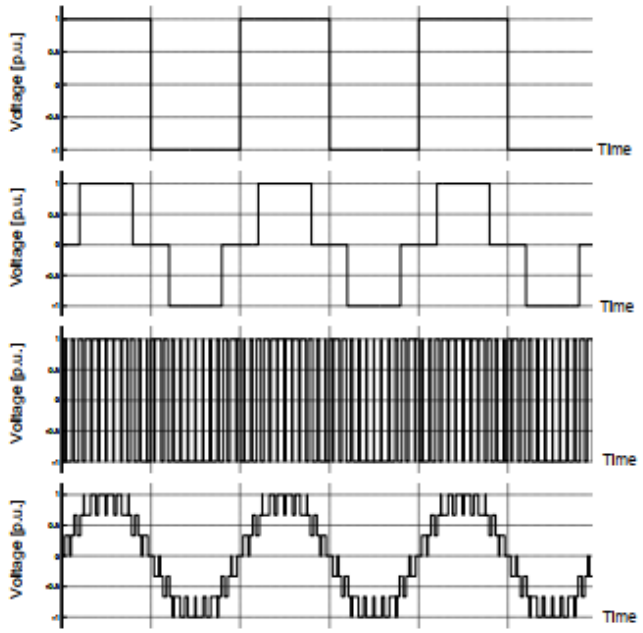


Fig 1.1.1 Output waveforms of popular inverter topologies: (a) Square wave (b) Quasi-square wave (c) Two-level PWM waveform and (d) Multilevel PWM waveform

1.3 Multilevel Inverters

The need for highly efficient and good power quality has spawned a breed of inverters called multilevel inverters. They include an array of power semiconductors and capacitor voltage sources, the output of which generate voltages with stepped waveforms.

These inverters have benefits like low stress on switches, low harmonic distortion and can be used in high voltage and high-power applications.

MLIs are used in low and high-power applications such as Uninterruptible Power Supply

(UPS), Induction Motor Drives, and FACTS.

Different multilevel inverter topologies, modulation techniques, and control strategies. Also, other properties such as fault tolerant operation, efficiency improvement, optimized control strategies, and new applications are gaining importance. These converters also feature a high modularity degree because each inverter can be seen as a module with similar circuit topology, control structure, and modulation, enabling easy replacement of these modules in the case of a fault.

CHAPTER 2

LITERATURE REVIEW

A preliminary study of various topologies and working of multilevel inverters was done. General considerations, important topologies such as cascaded H-Bridge inverters, diode clamped inverters and switched-capacitor inverters were studied. Relevant control methods such as Phase disposition PWM, Phase opposition disposition PWM were considered.

MATLAB Simulink was used for simulation of the power circuit. The Simscape Power Systems toolbox enables simulation of complex PWM modulation techniques with relative ease. FFT analysis can be done on the output waveform to compute the Total Harmonic Distortion (THD).

A literature study was done on Multilevel inverters. The different topologies were studied for their component count, number of output levels, switching losses and conduction losses. An in-depth study was done on switched-capacitor multilevel inverters. Self-charge balancing of capacitors was one of the main factors considered to remove the need for auxiliary circuits.

2.1 Multilevel Boost Converters

Rosas-Caro et.al [1] presented a DC-DC boost converter which utilizes switched capacitors as the storage element unlike inductors in conventional boost converters. It also has self-balanced voltage of capacitors and is modular. The boost factor depends on the number of capacitors used.

Reza et.al [2] proposed a novel switched capacitor-based inverter with reduced number of circuit devices along with detailed analysis of cascaded topologies.

2.2 Cascaded Inverters

Novel multilevel inverters consisting of cascade of one or more units is done in [3], [4] and [5].

2.3 Novel Inverterx

A novel topology is presented by Babaei et.al in [6] wherein cost and size were considered. A topology suggested by Chen-Han Hsieh et.al [7] requires additional circuitry to facilitate charge balancing of capacitors.

In [8], a topology consisting of modified H-bridge is proposed by Kamaldeep et.al.

2.4 PWM Techniques

A study of different PWM techniques employed in inverters is presented in [9] by Deepa et.al.

Kishor et.al has presented a study in [10] where performance improvement by implementing different PWM techniques.

CHAPTER 3

SCOPE OF THE PRESENT WORK

The project aims to present a switched-capacitor based inverter which has voltage boost capability, reduced number of switches and self-charge balancing of capacitors. A configuration is presented wherein a 9 level voltage waveform is obtained using a single DC voltage source and 2 capacitors with 9 power switches. The relevant switches are modulated on a hybrid PWM technique which ensures minimum switching losses. Reduced number of power diodes and complexity are also features of the proposed inverter. The circuit is also verified under different types of loading conditions using MATLAB Simulink.

CHAPTER 4

SWITCHED CAPACITOR BASED MULTI-LEVEL BOOST INVERTER

4.1 Circuit Configuration

The proposed circuit is shown in Fig. 4.1.1. The inverter is capable of producing 9 levels of output voltage while operating at a low switching frequency [1]. The main features of this circuit are:

1. Boosting capability of the output voltage.

2. Requiring only 2 electrolytic capacitors and 1 voltage source to produce high number of voltage levels.

3. Use of only 9 power switches and gate drivers working at low switching frequency.

4. Lessening of total switching loss by employing HPWM technique.

5. Self-charge-balancing capability, removing the need for auxiliary charge balancing circuits.

Switched capacitor inverters offer many features such as high reliability, reduction in cost, easy swapping of components and reduction in number of DC sources required. However, the main disadvantage is that they require delicate voltage or charge balancing to be done. This can be done in open loop by natural charge balancing every cycle by providing suitable switching and current flow paths. It can also be done closed loop or by using a RLC filter tuned at the switching frequency in parallel with the load. However, this increases the cost and depreciates the dynamic response of the circuit.

The PSPWM technique is considered the best method to be employed for a capacitor based MLI as it offers self-balancing property when applied to an ideal and symmetrical circuit.

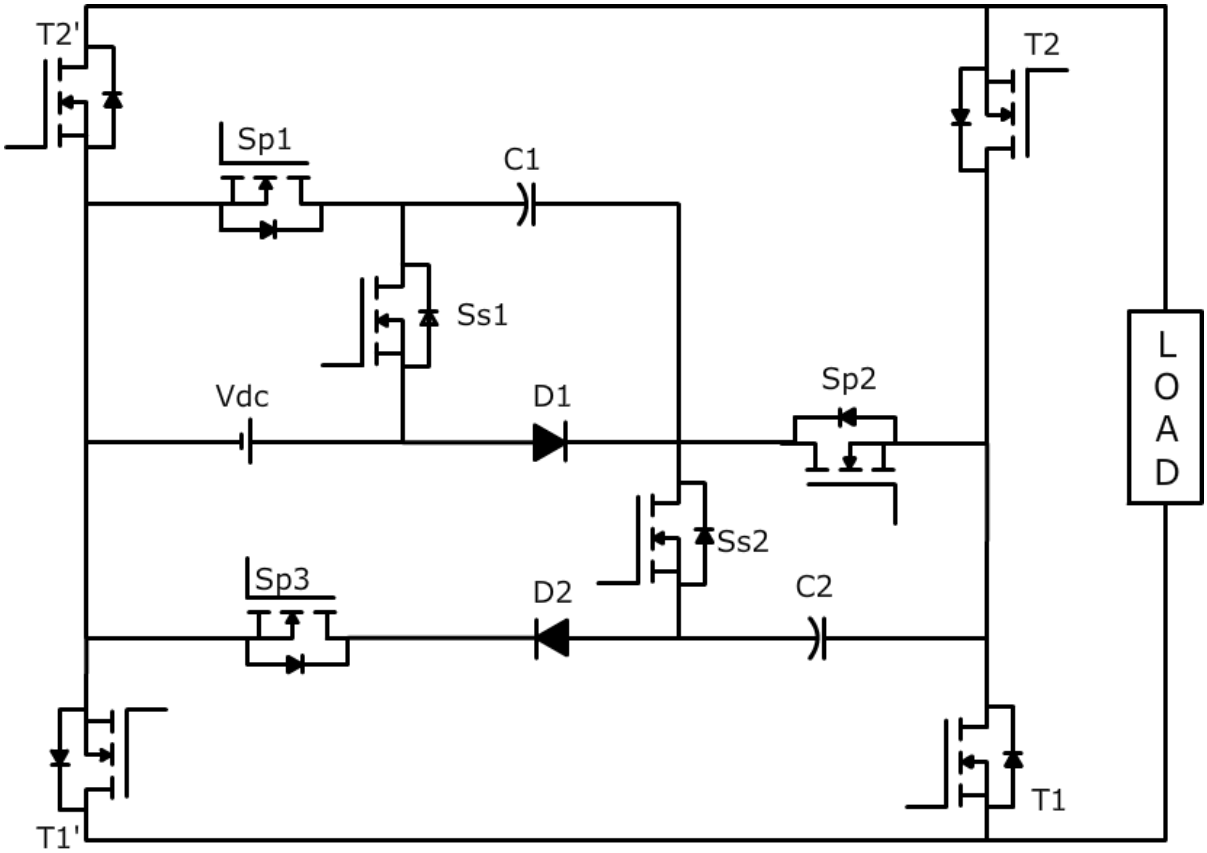


Fig. 4.1.1 Proposed circuit

The SC cell unit is capable of producing 9 levels (4 positive, 4 negative and one zero level) using two integrated capacitors, two passive diodes and nine power switches. Using series-parallel conversion of the capacitors along with the DC source of magnitude Vdc, the circuit produces the positive levels 0, Vdc, 2Vdc, 3Vdc and 4Vdc and the corresponding negative levels. The voltage across the capacitors C1 and C2 is fixed at Vdc and 2Vdc respectively, without the need for voltage sensors or auxiliary charge balancing circuits.

The diodes are used to counteract the effect of the parasitic body diode present in the power switches and enable the reverse flow of load current.

4.2 Power circuit operation

Fig.4.2.1 (a) – (i) indicates the various current flow paths of the SCMLI.,

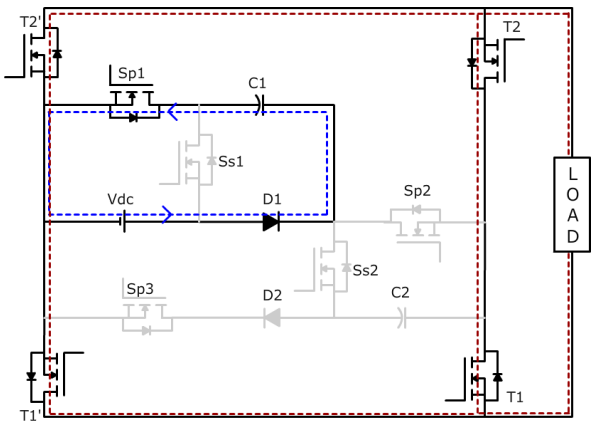
Zero voltage level can be achieved using either of the redundant states by turning ON the switches T1 and T2 or T1′ and T2’. Also, Sp1 is turned ON to charge the capacitor C1 to Vdc.

The first positive and negative output voltage levels (±Vdc) attained by using only the DC source Vdc without any of the capacitors in the load path. Also, Sp1 is kept ON to facilitate charging of the capacitor C1, while C2 remains disconnected.

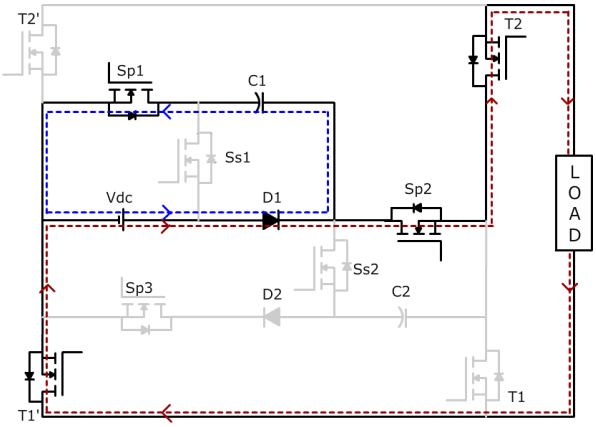
For the second positive and negative output voltage levels (±2Vdc), the voltage across of the DC source is added to the voltage of C1 that has been previously charged to Vdc. By turning OFF Sp1 and turning ON Ss1, C1 is now discharging. The net voltage across the load is now the addition of DC source Vdc and voltage Vdc accumulated in C1, i.e., 2Vdc. Also, in this interval, by turning ON Sp3, power diode D2 becomes forward biased and C2 now gets charged to 2Vdc.

The third positive and negative output voltage levels (±3Vdc) are created by series connection of the stored voltage in C2 and the DC voltage source value through the series switch Ss2. This is achieved by turning ON the switch Ss2. Also, Sp1 is turned ON to charge C1 again to Vdc.

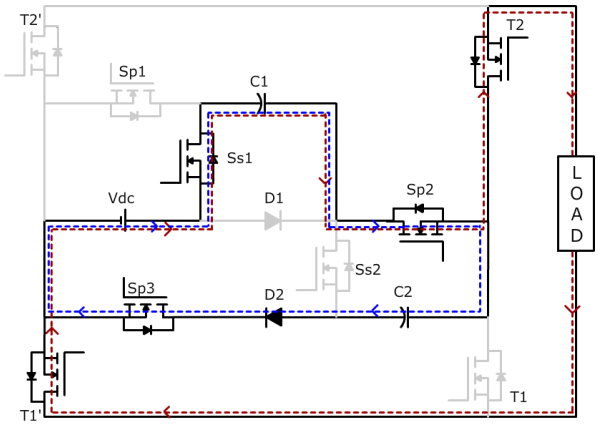
Finally, in the fourth positive and negative output voltage levels (±4Vdc), both the capacitors must be series with power supply through Ss1 and Ss2. This is realized by turning ON the switches Ss1 and Ss2, discharging both the capacitors and the required voltage level is attained.


T2'
T2
Sp1
C1
Ss1
Vdc
D1
Sp2
LOAD
Ss2
Sp3
D2
C2
T1'
T1

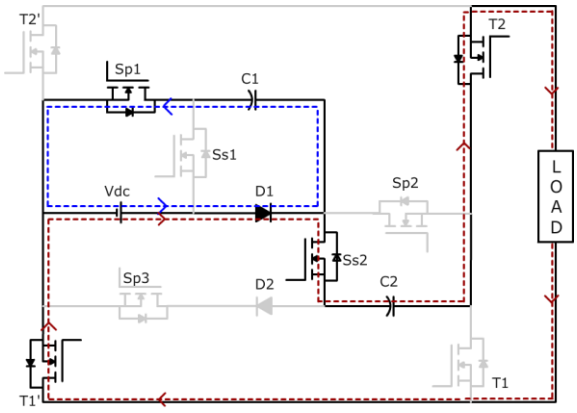
(a)


T2'
T2
Sp1
C1
Ss1
Vdc
D1
Sp2
LOAD
Ss2
Sp3
D2
C2
T1'
T1

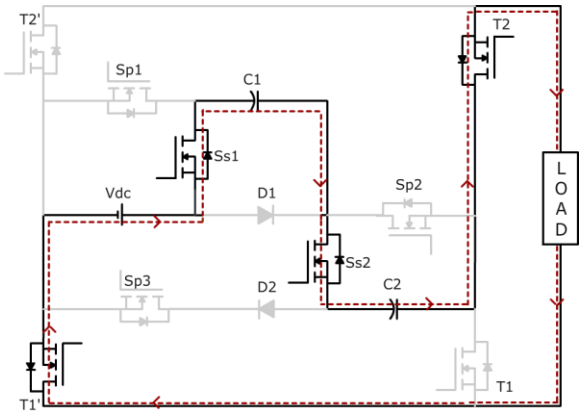
(b)


T2'
T2
Sp1
C1
Ss1
Vdc
D1
Sp2
LOAD
Ss2
Sp3
D2
C2
T1'
T1

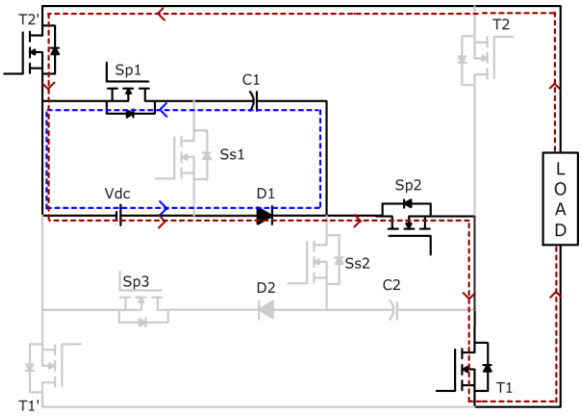
(c)


T2'
T2
Sp1
C1
Ss1
Vdc
D1
Sp2
LOAD
Ss2
Sp3
D2
C2
T1'
T1

(d)


T2'
T2
Sp1
C1
Ss1
Vdc
D1
Sp2
LOAD
Ss2
Sp3
D2
C2
T1'
T1

(e)


T2'
T2
Sp1
C1
Ss1
Vdc
D1
Sp2
LOAD
Ss2
Sp3
D2
C2
T1'
T1

(f)

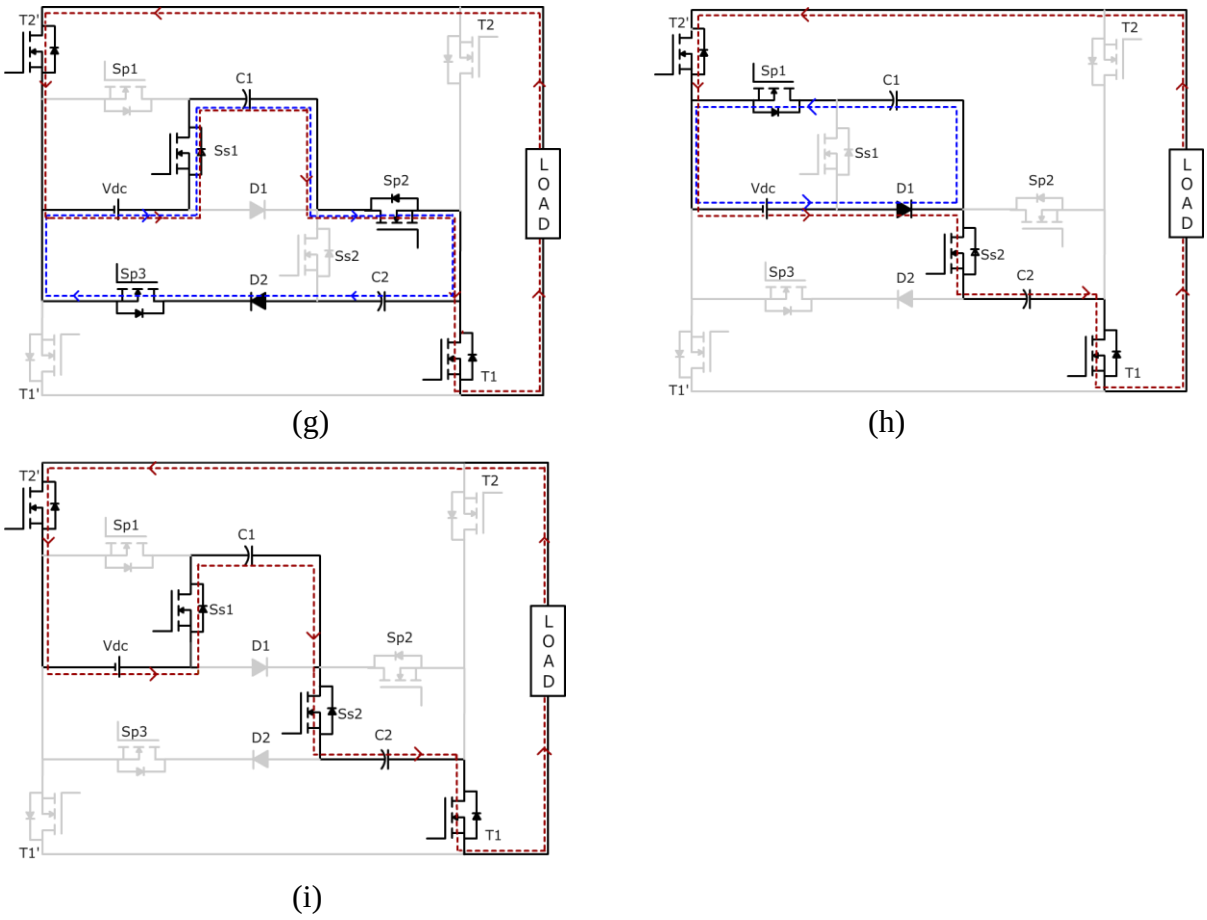


Fig. 4.2.1 Switching states (a) Zeroth level (b) First positive level (c) Second positive level (d) Third positive level (e) Fourth positive level (f) First negative level (g) Second negative level (h) Third negative level (i) Fourth negative level

Table 4.2.1 presents the various switching states of the switches present in the circuit during each voltage level.

4.3 Proposed PWM strategy

The switching pulses for the switches are obtained by comparison of reference sine waveform which resembles the desired output voltage with carriers. The technique used here is called Phase Disposition PWM (PDPWM), wherein, the absolute function of a reference sine waveform is compared to 9 level shifted triangle carrier waveforms. The sine wave is chosen

to have an amplitude of 450 and each of the triangle carrier waves have an amplitude of 50 each. The reference sine wave is defined as

$$Vref = Arsinwt$$

The modulation index is calculated using the following equation:

$$m = \frac{Ar}{9\text{Ac}}$$

Where A_c is the amplitude of each carrier wave and A_r is the amplitude of the reference wave. A_r is chosen as 450 and A_c is chosen as 50. Thus, the modulation index is calculated as 1. Also, a commander coefficient (CM) is defined to be used to select the positive half or negative half of the reference wave over a single cycle.

$$CM = \frac{1 + \text{sgn}(\text{Vref})}{2}$$

Where Vref is the reference sine wave.

Ss1	Ss2	Sp1	Sp2	Sp3	T1	T2	T1'	T2'	Voltage
0	0	1	0	0	1	1	1	1	0Vdc
0	0	1	1	0	0	1	1	0	1Vdc
1	0	0	1	1	0	1	1	0	2Vdc
0	1	1	0	0	0	1	1	0	3Vdc
1	1	0	0	0	0	1	1	0	4Vdc
0	1	1	0	0	0	1	1	0	3Vdc
1	0	0	1	1	0	1	1	0	2Vdc
0	0	1	1	0	0	1	1	0	1Vdc
0	0	1	0	0	1	1	1	1	0Vdc
0	0	1	1	0	1	0	0	1	-1Vdc
1	0	0	1	1	1	0	0	1	-2Vdc
0	1	1	0	0	1	0	0	1	-3Vdc
1	1	0	0	0	1	0	0	1	-4Vdc
0	1	1	0	0	1	0	0	1	-3Vdc
1	0	0	1	1	1	0	0	1	-2Vdc
0	0	1	1	0	1	0	0	1	-1Vdc
0	0	1	0	0	1	1	1	1	0Vdc

Table 4.2.1 List of switching states of inverter

CHAPTER 5

RESULTS AND DISCUSSION

5.1 Simulation in MATLAB Simulink

The proposed 9 level SCMLI was simulated using MATLAB Simulink r2018a. The Simscape PowerSystems toolbox was used for simulation. The Tustin/Backward Euler solver was utilized.

The objective of this project is to minimize THD for a 200 ohm purely resistive load. The FFT Analyser was used to calculate the THD of the output current and voltage waveforms.

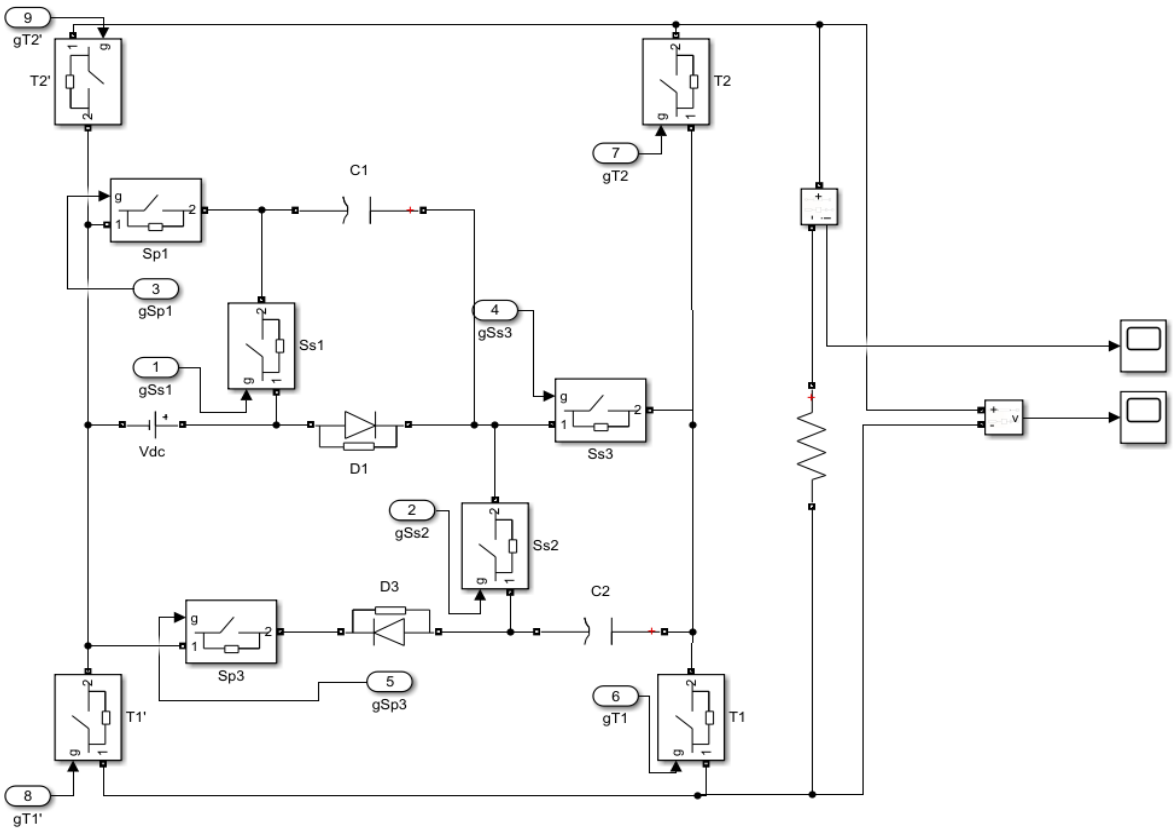


Fig. 5.1.1 Circuit simulated in Simulink

5.2 Design of circuit

The design parameters and THD characteristics of the inverter are shown in Table 5.1.1 and Table 5.2.2.

Input Voltage	100V
Input Current	8A
Load	200 ohm
Output Voltage	392.34V
Output Current	1.968A
Input Power	800W
Output Power	772.12W
Total Loss	27.8W
Efficiency	96.51%
Frequency	50 Hz
Power Factor	1

Table 5.2.1 Characteristics of the inverter

Frequency (Hz)	Order	%
0	DC	0.00
50	Fnd	100.00
100	h2	0.00
150	h3	0.53
200	h4	0.00
250	h5	6.30
300	h6	0.00
350	h7	0.95
400	h8	0.00
450	h9	2.40
500	h10	0.00
550	h11	1.37
600	h12	0.00
650	h13	1.51
700	h14	0.00
750	h15	1.13
800	h16	0.00
850	h17	3.52
900	h18	0.00
950	h19	0.54
1000	h20	0.00

Table 5.2.2 Output THD characteristics

The value of capacitors C1 and C2 are chosen as 1000 uF and 1550 uF respectively.

5.3 PWM Generator circuits

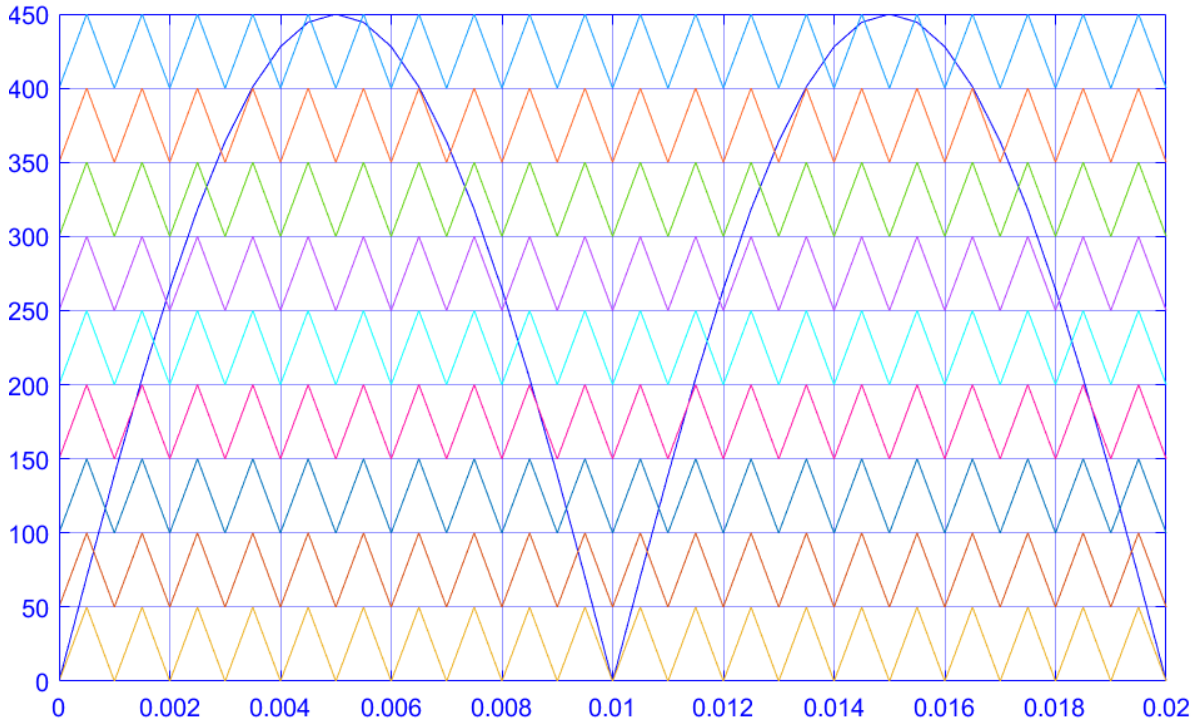
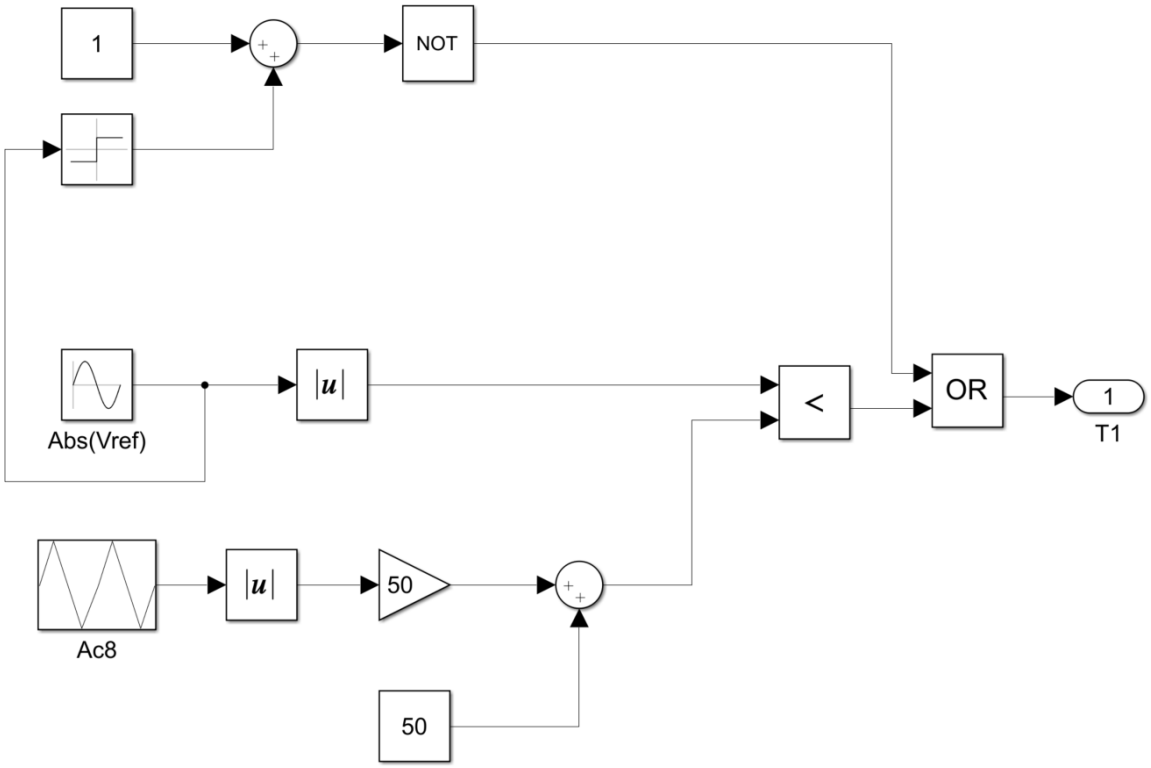
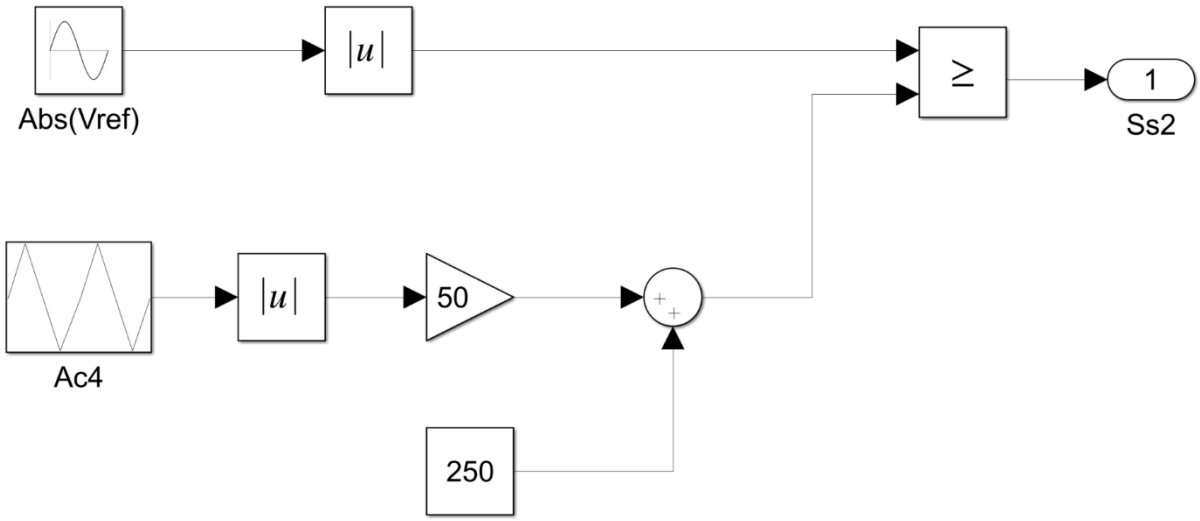


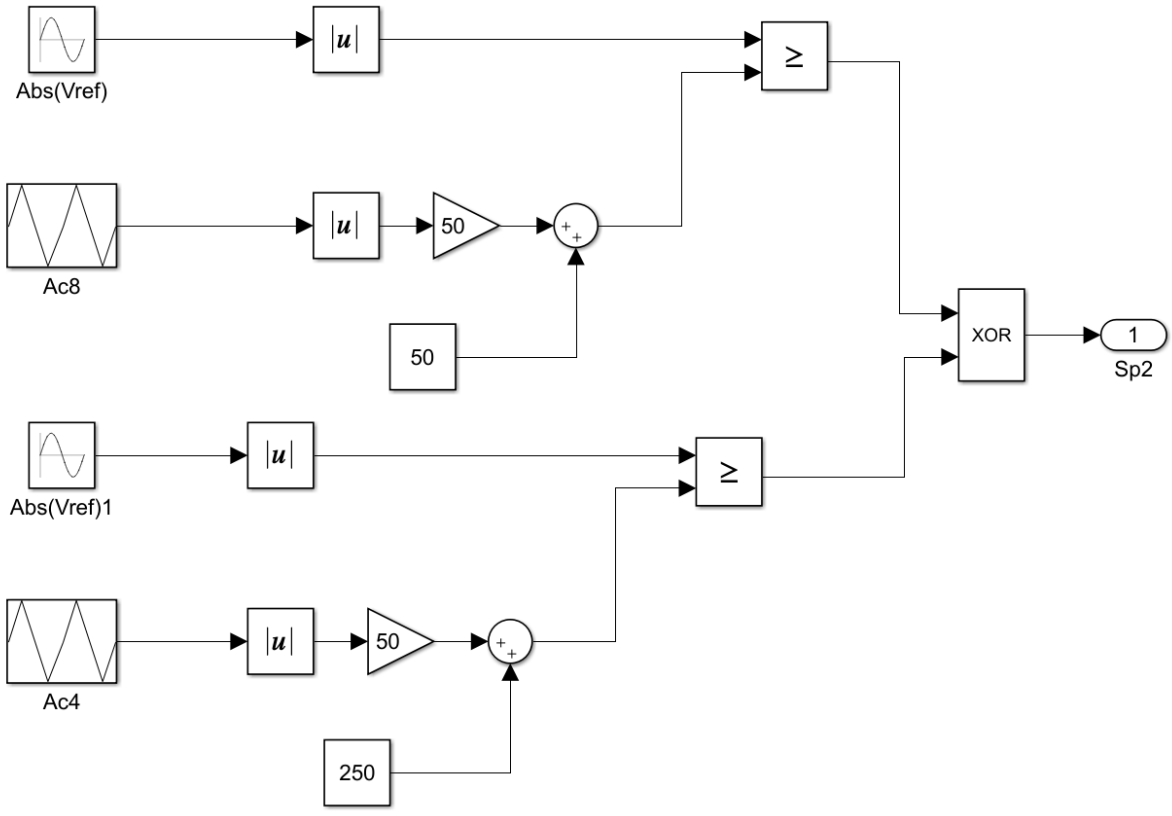
Fig. 5.3.1 PDPWM scheme



(a) T1



(b) Ss2



(c) Sp2

Fig. 5.3.2 Pulse generator circuits for various switches

5.4 Output Waveforms

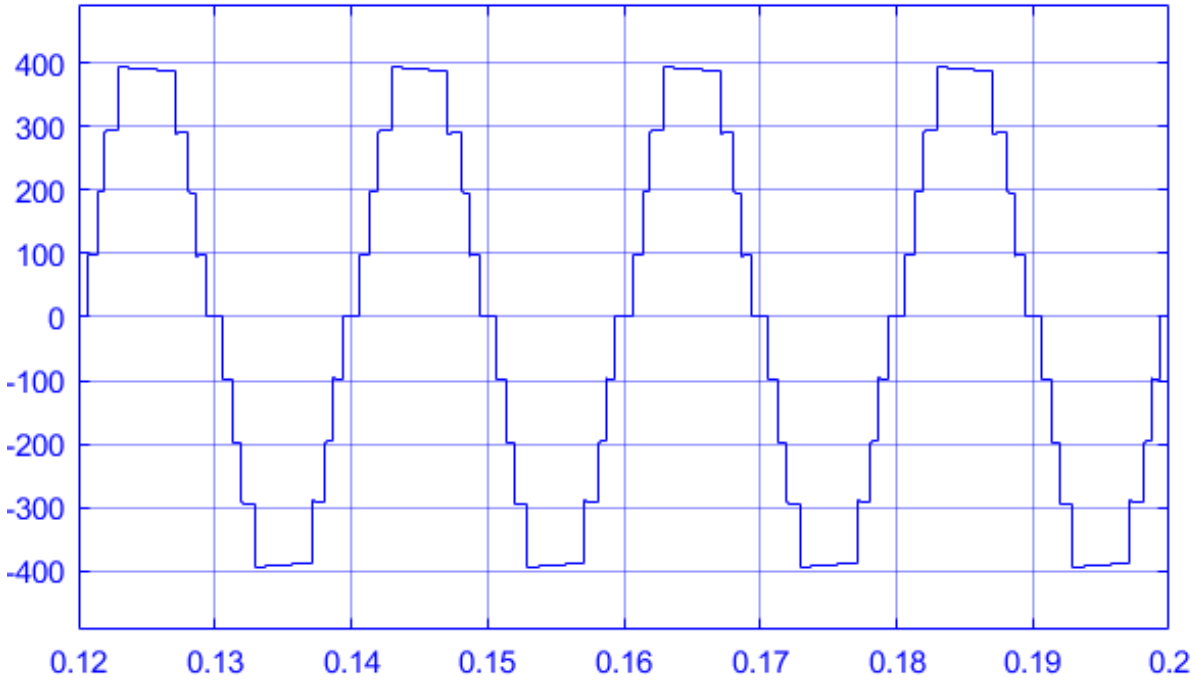


Fig. 5.4.1 Voltage waveform

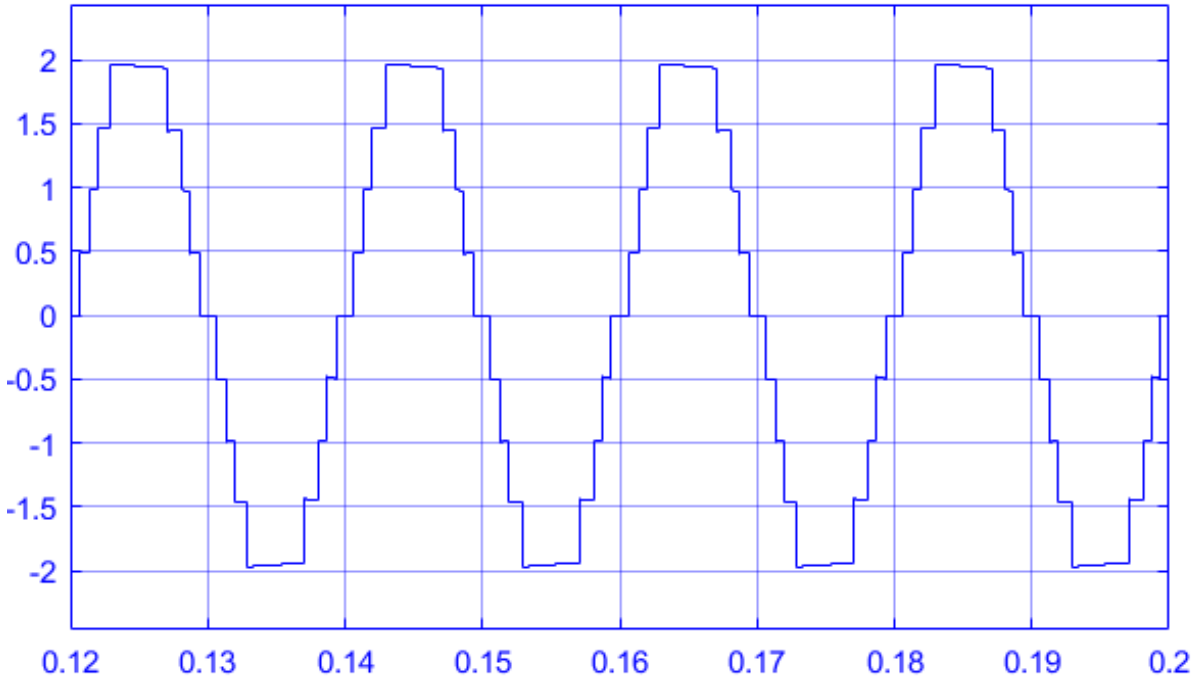


Fig. 5.4.2 Current Waveform

5.5 THD Analysis

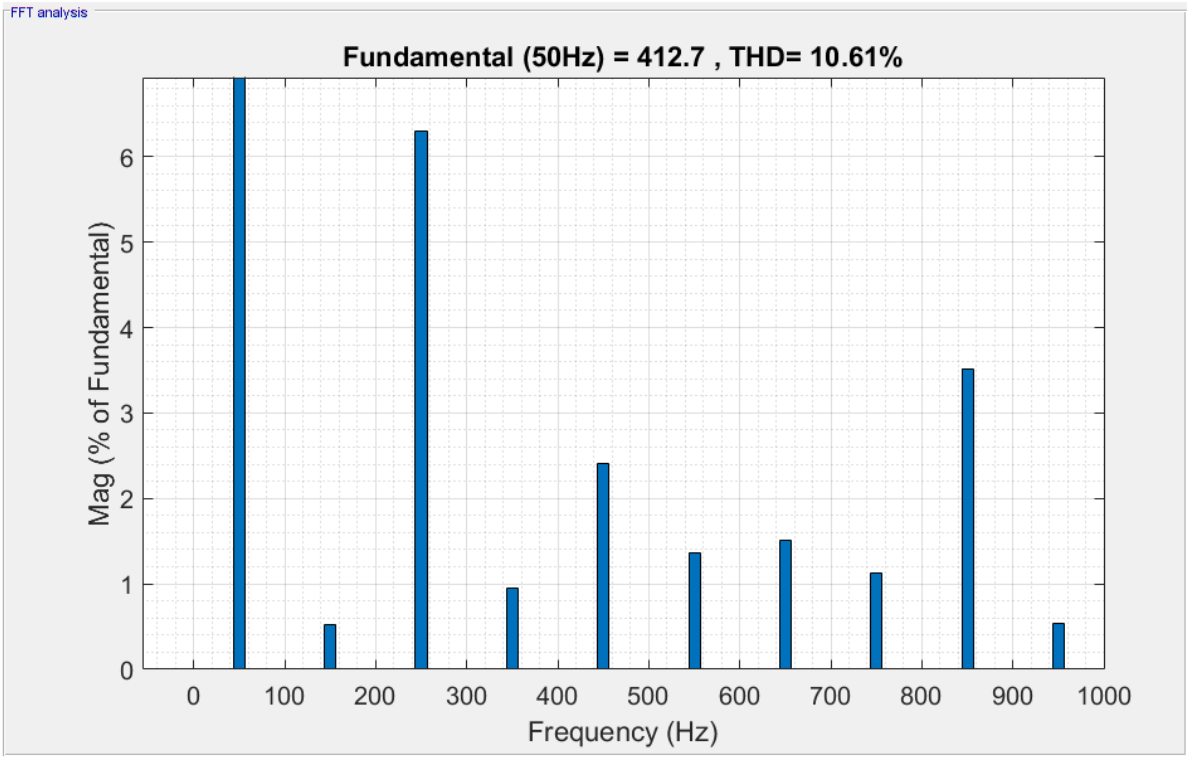


Fig. 5.5.1 THD analysis of output voltage

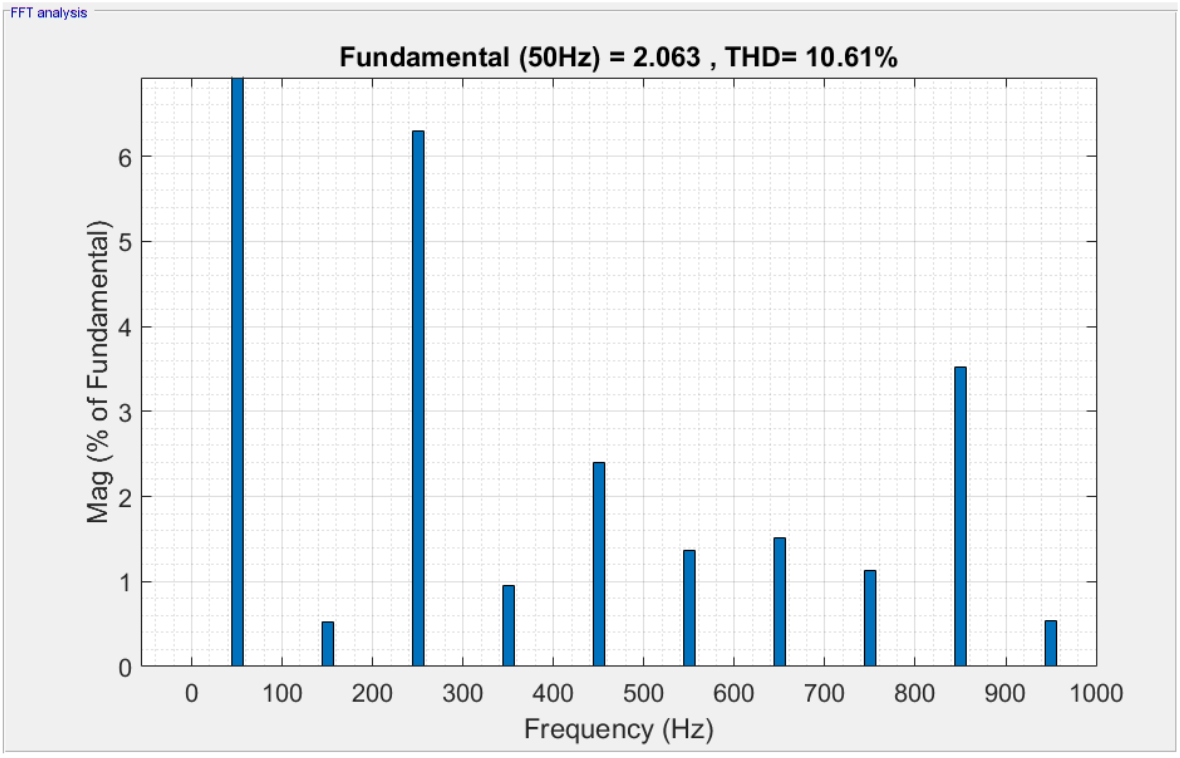


Fig. 5.5.2 THD analysis of output current

CHAPTER 6

CONCLUSION

In this project, a switched capacitor based single phase multi-level inverter with reduced number of devices was proposed. A literature survey of the different topologies of multi-level inverters and new PWM techniques was presented. The carrier based PDPWM technique was used for generating switching pulses. The output waveforms for voltage and current were recorded for a resistive load. Simulation was done in MATLAB Simulink environment using the Simscape PowerSystems toolbox. FFT analysis for output voltage and current was done and the THD was noted.

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