SWITCHED CAPACITOR BASED MULTI-LEVEL BOOST INVERTER FOR SMART GRID APPLICATIONS

A PROJECT REPORT

submitted by

RAGHURAM S (119005096)

towards partial fulfillment of the requirements for the award of the degree

of

Bachelor of Technology
in
Electrical & Electronics Engineering

School of Electrical and Electronics Engineering

SASTRA DEEMED TO BE UNIVERSITY
(A University established under section 3 of the UGC Act, 1956)
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BONAFIDE CERTIFICATE

This is to certify that the project work entitled "**SWITCHED CAPACITOR BASED MULTI-LEVEL BOOST INVERTER FOR SMART GRID APPLICATIONS"** is a bonafide record of the work carried out by

RAGHURAM S (119005096)

student of fourth year B.Tech., Electrical and Electronics Engineering, in partial fulfillment of the requirements for the award of the degree of B.Tech in Electrical & Electronics Engineering of the **SASTRA DEEMED TO BE UNIVERSITY, Thirumalaisamudram, Thanjavur - 613401,** during the year 2015-2019.

Mr. Girish Ganesan. R (AP - II/EEE/SEEE)

SIGNATURE

Project Viva-Voce held on _____

Examiner -I **Examiner-II**

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ABSTRACT

SWITCHED CAPACITOR BASED MULTILEVEL BOOST INVERTER FOR SMART GRID APPLICATIONS

RAGHURAM S (119005096)

KEY WORDS: Switched Capacitor, Multilevel Inverter, Smart Grid

Inverters are power electronic converters essential for linking sources of DC power to the AC grid. Conventional inverters often use transformers and harmonic filters which are bulky, expensive and lossy. Multilevel inverters are a viable alternative to classical inverters, offering reduced THD, inductor-less design and increased range of control. They produce a stepped waveform, with close resemblance to a sine wave. Smart grids may have several distributed sources and when these sources have minimal THD, there is a reduced stress for filtering them at the point of common coupling. In this paper, two switched capacitor based multilevel inverters offering boost capability and low THD are proposed. The inverters have inherent charge balancing capability, removing the need for voltage sensors and auxiliary circuits. The switches in the inverters are modulated using PODPWM technique, which facilitates voltage balancing and reduced switching losses. The designs are validated by simulation and the output waveforms and parameters are presented.

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ABBREVIATIONS

DC	Direct Current
AC	Alternating Current
PWM	Pulse-Width Modulation
THD	Total Harmonic Distortion
MLI	Multilevel inverter
FACTS	Flexible AC Transmission Systems
FFT	Fast Fourier Transform
HPWM	Hybrid Pulse-Width Modulation
RLC	Resistive-Capacitive-Inductive
SC	Switched-Capacitor
SCMLI	Switched Capacitor Multilevel Inverter
CM	Commander Coefficient
NT1	Novel Topology 1
NT2	Novel Topology 2

NOTATIONS

V_{ref}	Reference voltage value
A_r	Amplitude of reference voltage
A_c	Amplitude of carrier
Sgn	Signum function

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CHAPTER 1

INTRODUCTION

1.1 Power Electronic Devices

In recent years, industries have begun to demand higher power equipment, even reaching the megawatt level. Power Electronics is the application of solid-state electronics for control and conversion of electric power. These devices are nowadays the most important component in extracting power from renewable sources. During conversion of AC to DC or vice versa, efficiency plays an important role in high powered applications. Power Electronics enables highly efficient conversion of power, reducing losses expended as heat and in turn, size of the devices.

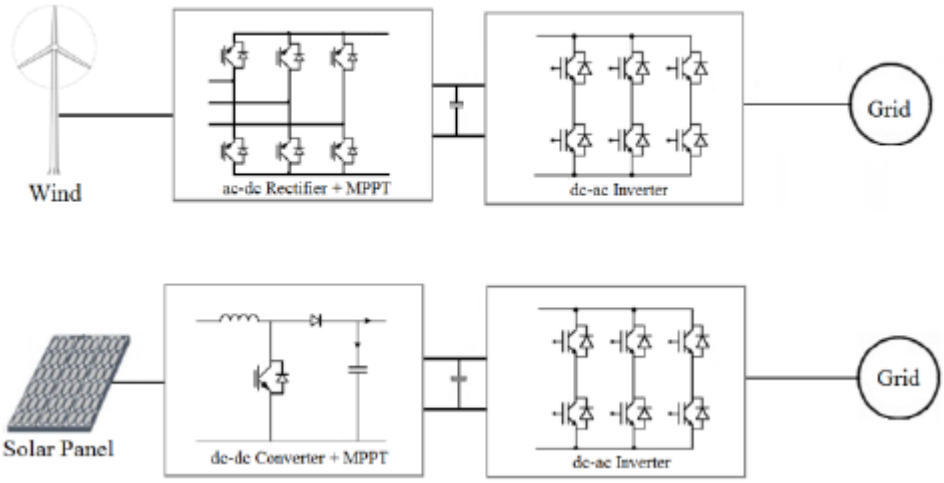


Fig 1.1.1 Application of Power Electronics in the power grid

Inverters are power electronic modules that are used to convert DC voltages to AC waveform. The output frequency maybe constant or variable depending on the application. A waveform that closely resembles a sinewave has the least harmonic content and it increases with increase in deviation of the output voltage waveform from the sine wave. In certain applications, these

harmonics cause increased losses and produce pulsating torques when applied to an AC Motor [1, 2].

These devices play a crucial role in variable frequency drives, air conditioning, uninterruptible power supplies, induction heating, high voltage DC power transmission, electric vehicle drives, static var compensators, active filters, flexible AC transmission systems. They are also used for converting the DC power commonly obtained from storage elements to AC power required for common electrical loads.

Based on the nature of the output waveform, inverters can be classified as: square wave inverters, quasi-square wave inverters, two-level PWM inverters and multilevel inverters [3] (Fig. 1.1.2).

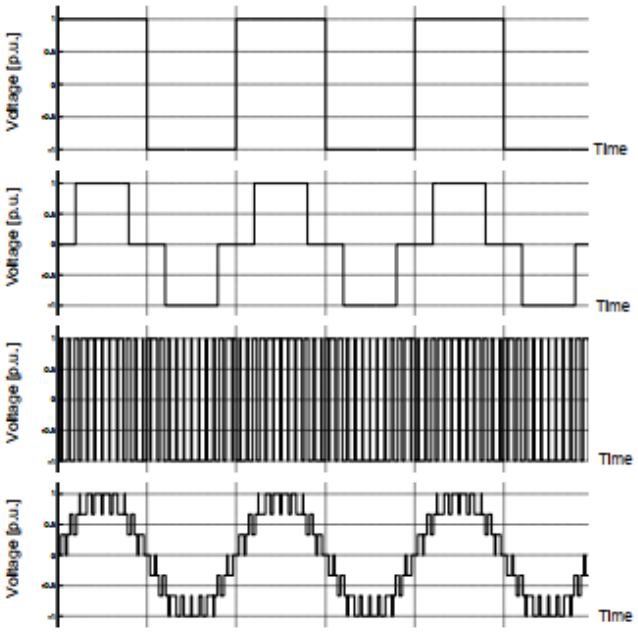


Fig 1.1.2 Output waveforms of popular inverter topologies [3]: (a) Square wave (b) Quasi-square wave (c) Two-level PWM waveform and (d) Multilevel PWM waveform

1.2 Motivation

THD is a measure of the harmonics that are present in a waveform. These harmonics are integral multiples of the fundamental frequency. Harmonics mitigation is crucial as they distort the output waveform and produce losses in the system.

Due to the presence of several distributed sources in smart grid, handling the harmonics at the point of common coupling (PCC) becomes an issue. MLIs are lucrative power conversion alternative as they are simple to control and are useful for low harmonics power injection.

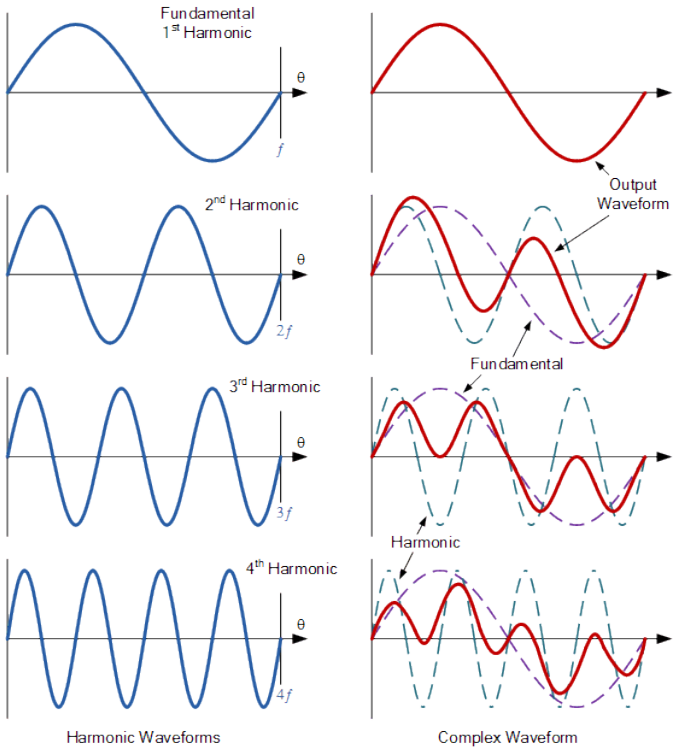


Fig 1.2.1 Fundamental and addition of harmonics

In order to reduce these harmonics, passive filters have been widely available. However, the main issue with these filters is that the size of the inductor and capacitor is too large to be feasible and efficient for lower order harmonics at a fundamental frequency of 50 Hz.

Power electronics provide the means to convert electric power generated into that required by the load. They are a crucial component in the power system which forms the power grid of a country. Their advantages include:

1. Reduce energy use by reducing losses
2. Enhance the functionality of the power system
3. Enable the integration of renewables
4. Facilitate the creation of a low-carbon energy future

The losses in transmission can also be minimized in the power grid by using HVDC Transmission systems wherein inverters and converters are used for efficient power conversion.

1.3 Multilevel Inverters

The need for highly efficient and good power quality has spawned a breed of inverters called multilevel inverters. They include an array of power semiconductors and capacitor voltage sources, the output of which generate voltages with stepped waveforms.

Multilevel inverters are a breed of inverters that produce a stepped waveform resembling a sine wave. They are more popular as they don't require inductors and transformers, for the power conversion. The desired stepped waveform is achieved by using one of the many available Pulse-Width Modulation techniques.

The principle aim of a multilevel inverter is to produce a waveform that resembles a pure sine wave as much as possible. Reduction in overall part count as compared to the classical topologies has been an important objective in the recently introduced multilevel topologies.

There are three classical multilevel inverter topologies: neutral point clamped (NPC), cascaded H-bridge (CHB), and flying capacitors (FCs). The cascaded multilevel inverters offer reliable performance and can reach higher voltage levels [4]. These inverters offer high power quality associated with reduced number of power switches [5]. Traditional multilevel inverters suffer from requiring many auxiliary circuit devices for charge balancing of capacitors for desired operation [6, 7]. These inverters do not have a boost function as the magnitude of the output voltage cannot be higher than the scalar superimposition of the DC link voltages [8]. Current trends in multilevel inverters are alternative topologies for CHBs with reduced number of switches for the same power rating and improved THD reduction.

One of the major issues faced in the rapidly growing photovoltaic renewable energy system is the small magnitude of available DC source voltage. Since most loads operate at higher voltage than the panel output voltage, a boost converter, which steps up DC voltages from low values to high values without the use of a transformer is often employed before converting it into AC using an inverter. Switched capacitor-based designs offer a suitable alternative due to inherent voltage boosting capability and reduction in number of voltage sources needed to produce high magnitude output waveform.

Multi-level inverters are a viable and more efficient alternative to classical inverters in Motor Drives [9, 10], FACTS [11] and Static VAR Generators [12, 13]. These inverters have benefits like low stress on switches, low harmonic distortion and can be used in high voltage and high-power applications.

MLIs are used in low and high-power applications such as Uninterruptible Power Supply (UPS), Induction Motor Drives, and FACTS.

Different multilevel inverter topologies, modulation techniques, and control strategies. Also, other properties such as fault tolerant operation, efficiency improvement, optimized control strategies, and new applications are gaining importance. These converters also feature a high modularity degree because each inverter can be seen as a module with similar circuit topology, control structure, and modulation, enabling easy replacement of these modules in the case of a fault.

In this project, two improved configurations of switched capacitor-based step-up Multilevel inverters are proposed. Quantitative and qualitative aspects of the MLI are improved, along with analysis of THD of the output voltage under different modulation index and control strategies. Quantitative improvement is done by reducing the number of semiconductor switches and diodes. Qualitative improvement is done by reducing THD by increased number of levels and improved PWM strategy.

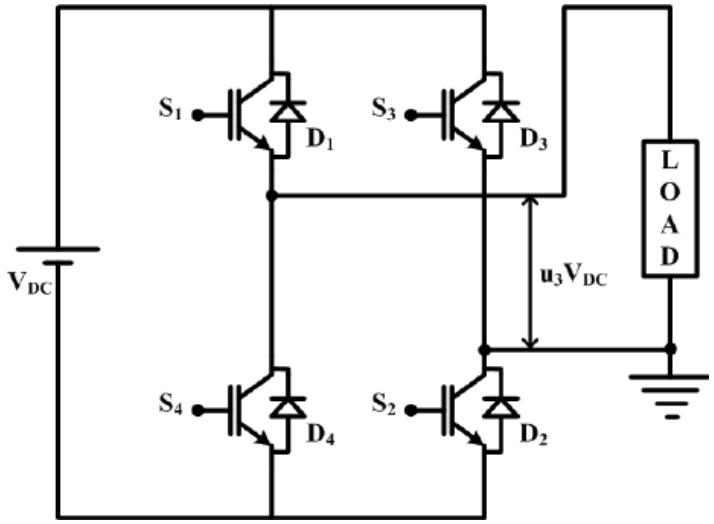


Fig. 1.3.1 H-Bridge Inverter

1.4 Applications in Smart Grids

A smart grid is an electrical grid which includes a variety of operation and energy measures including smart meters, smart appliances, renewable energy resources, and energy efficient resources. Electronic power conditioning and control of the production and distribution of electricity are important aspects of the smart grid. The revival of the electric vehicle, particularly the plug-in Hybrid Vehicle has been the most impacting on the power grid [14]. Thus, some techniques such as load forecasting have been developed to cope up with the increase in demand of electric power. Targeting PHEV powertrains optimization, a plethora of energy management strategies (EMSs) have been proposed [15]. Varying in complexity and accuracy, these algorithms offer different solutions according to the need of the given system.

Fig 1.4.1 Smart Grids

The Internet of Things (IoT) plays an important role in enabling smart grid powered countries. IoT is the extension of Internet connectivity into physical devices and everyday objects. Embedded with electronics, Internet connectivity, and other forms of hardware (such as sensors), these devices can communicate and interact with others over the Internet, and they

can be remotely monitored and controlled.

By integrating with IoT, a large number of smart meters can be deployed in houses and buildings connected in smart grid communication networks [16]. This enables constant monitoring of the power drawn by loads, allowing us to create a power profile which allows us to predict and reroute power to where it is needed in the grid.

CHAPTER 2

LITERATURE REVIEW

A preliminary study of various topologies and working of multilevel inverters was done. General considerations, important topologies such as cascaded H-Bridge inverters, diode clamped inverters and switched-capacitor inverters were studied. Relevant control methods such as Phase disposition PWM, Phase opposition disposition PWM were considered.

MATLAB Simulink was used for simulation of the power circuit. The Simscape Power Systems toolbox enables simulation of complex PWM modulation techniques with relative ease. FFT analysis can be done on the output waveform to compute the Total Harmonic Distortion (THD).

A literature study was done on Multilevel inverters. The different topologies were studied for their component count, number of output levels, switching losses and conduction losses. An in-depth study was done on switched-capacitor multilevel inverters. Self-charge balancing of capacitors was one of the main factors considered to remove the need for auxiliary circuits.

2.1 Multilevel Boost Converters

Rosas-Caro et.al [17] presented a DC-DC boost converter which utilizes switched capacitors as the storage element unlike inductors in conventional boost converters. It also has self-balanced voltage of capacitors and is modular. The DC–DC multilevel boost converter (MBC) is a pulse-width modulation (PWM) based DC–DC converter, which combines the boost converter and the switched capacitor function to provide different output voltages and a self-balanced voltage using only one driven switch, one inductor, 2N-1 diodes and 2N-1 capacitors

for a N_x MBC.

Reza et.al [18] proposed a novel switched capacitor-based inverter with reduced number of circuit devices along with detailed analysis of cascaded topologies. It has several advantages over the classical topologies such as: An appropriate boosting property, higher efficiency, lower number of required dc voltage sources and other accompanying components with less complexity and lower cost. The basic structure of the proposed converter is capable of making nine-level output voltage by using the same two capacitors paralleled to a DC voltage source under different kinds of loading conditions.

2.2 Cascaded Inverters

Novel multilevel inverters consisting of cascade of one or more units is done in [19], [20] and [21]. In [19], Reza et.al presented a new family of cascaded multilevel inverters (CMLIs) which can generate a considerable number of output voltage levels with minimum number of required accompanying switching devices. In addition, to reach different number of output voltage levels, four different algorithms pertaining to the symmetrical, binary asymmetrical, trinary asymmetrical and also hybrid patterns for determining the magnitude of isolated dc voltage sources are presented.

Mohammed et.al [20] proposed a new power inverter topology that creates fifteen voltage levels by considering four DC-links and eight power switches. Different values of DC-links are also proposed in this paper and a comparison is done among proposed magnitudes to investigate their advantages and disadvantages.

In [21], Kaustubh et.al presented a cascaded asymmetric multilevel inverter is proposed which contains minimum number of switches and can be employed in AC applications using solar

energy. The proposed topology consists of 25 output levels using 10 switches with near sinusoidal output, thereby reducing gate driver circuitry and optimizing circuit layout.

2.3 Novel Inverters

A novel topology is presented by Babaei et.al in [22] wherein cost and size were considered. A new basic 15-level inverter was proposed. By developing the proposed basic unit, a 71-level inverter and generally an m-level inverter were proposed. Then, the proposed multilevel inverter was compared with several conventional multilevel inverters in design of minimum 15 levels and 71 levels at the output. By comparing these inverters, it was obtained that the proposed inverter is able to generate higher number of output levels by using lower number of DC voltage sources and power electronic devices.

A topology suggested by Chen-Han Hsieh et.al [23] requires additional circuitry to facilitate charge balancing of capacitors. The novel design generates seven-level ac output voltage with the appropriate gate signals' design. Also, the low-pass filter is used to reduce the total harmonic distortion of the sinusoidal output voltage.

In [24], a topology consisting of modified H-bridge is proposed by Kamaldeep et.al. In the proposed topology, eight switches are required for generation of 15-level single phase output voltage. The proposed topology is simple and can be extended easily to get a greater number of levels in the output voltage. Therefore, there is a significant reduction in size, cost and complexity for higher number of levels in output voltage.

2.4 PWM Techniques

A study of different PWM techniques employed in inverters for medium and high power applications is presented in [25] by Ilhami et.al. This paper and review results constitute a

useful basis for matching of inverter topology and the best control scheme according to various application areas.

Kishore et.al has presented a study in [26] where performance improvement by implementing different PWM techniques. The PWM strategies include Phase Disposition PWM (PDPWM), Phase Disposition Opposition PWM (PODPWM) and Alternate Phase Opposition Disposition PWM (APODPWM).

CHAPTER 3

SCOPE OF THE PRESENT WORK

The project aims to present two novel designs of switched-capacitor based inverters which have voltage boost capability, reduced number of switches and self-charge balancing of capacitors. Firstly. the configuration proposed in the base paper is simulated and the expected output waveform and characteristics are verified.

Then, a novel configuration is presented wherein the same 19-level voltage waveform is obtained using 2 DC voltage sources and 4 capacitors with only 10 power switches. The relevant switches are modulated on a new PDPWM technique which reduces switching losses considerably. Reduced complexity is also a feature of the proposed inverter. A second novel configuration based on the above design is presented, wherein a 17-level voltage waveform is obtained using 2 DC voltage sources and 2 capacitors with 9 power switches and also uses a similar PDPWM technique.

The first novel module focuses on producing the same performance and output characteristics as the base model, while reducing the number of components and power losses. The second novel module aims at producing nearly the same output, but also drastically reducing the number of components, thereby decreasing the cost of the inverter. It also thus increases its reliability. The circuits are verified under resistive loading conditions using MATLAB Simulink.

CHAPTER 4

SWITCHED CAPACITOR BASED MULTI-LEVEL BOOST INVERTER FOR SMART GRID APPLICATIONS

4.1 Base circuit configuration and working

Multilevel inverters with novel switched capacitor-based designs have been proposed by various authors [27,28]. These designs focus on reliability while reducing the costs of the components and power losses. A switched capacitor based 19-level inverter has been presented in the [29] and has been analyzed and simulated first.

The circuit proposed in the base paper is shown in Fig. 4.1.1. The inverter is capable of producing 19 levels of output voltage while operating at a low switching frequency [29]. The main features of switched capacitor based circuits are:

1. Boosting capability of the output voltage.

2. Requiring only 4 electrolytic capacitors and 2 voltage sources to produce high number of voltage levels.

3. Use of only 12 power switches and 10 gate drivers working at low switching frequency.

4. Lessening of total switching loss by employing HPWM technique.

5. Self-charge-balancing capability, removing the need for auxiliary charge balancing circuits.

Switched capacitor inverters offer many features such as high reliability, reduction in cost, easy swapping of components and reduction in number of DC sources required. However, the main disadvantage is that they require delicate voltage or charge balancing to be done. This

can be done in open loop by natural charge balancing every cycle by providing suitable switching and current flow paths. It can also be done closed loop or by using a RLC filter tuned at the switching frequency in parallel with the load. However, this increases the cost and depreciates the dynamic response of the circuit. The PDPWM technique is considered the best method to be employed for a capacitor based MLI as it offers self-balancing property when applied to an ideal and symmetrical circuit.

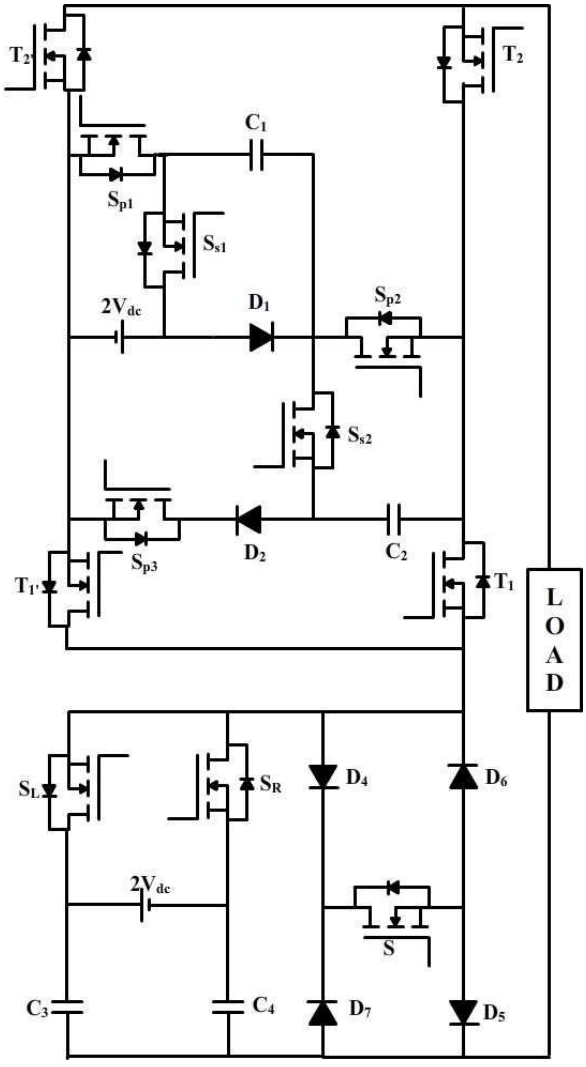


Fig. 4.1.1 Circuit proposed in the base paper [29]

4.2 Operation of base circuit

The SC cell unit is capable of producing 9 levels (4 positive, 4 negative and one zero level) using two integrated capacitors, two passive diodes and nine power switches. Using series-parallel conversion of the capacitors along with the DC source of magnitude $2V_{dc}$, the circuit produces the positive levels 0, $2V_{dc}$, $4V_{dc}$, $6V_{dc}$ and $8V_{dc}$ and the corresponding negative levels. The voltage across the capacitors C_1 and C_2 is fixed at $2V_{dc}$ and $4V_{dc}$ respectively, without the need for voltage sensors or auxiliary charge balancing circuits. The diodes are used to counteract the effect of the parasitic body diode present in the power switches and enable the reverse flow of load current.

The FCB cell unit produces 3 levels (1 positive, 1 negative and one zero level) using two capacitors, four diodes and 3 power switches. Similar to the series-parallel switching in the SC cell, the FCB cell also produces levels 0, V_{dc} and $-V_{dc}$. The four power diodes are essential to undertake the backward load current that causes by characteristic of inductive loads and leads to a unidirectional voltage blocking capability.

The modulation index was chosen as 0.95 by the authors. Since 19-level output voltage is to be generated by the proposed hybridised structure, use of 18 carrier waveforms may increase the complexity of the system. Since HPWM technique involves the fundamental and high switching frequencies in the hybridised MLVSIs, it can effectively reduce the value of switching loss. The circuit has been simulated in MATLAB and the output voltage waveform has been presented in Fig. 4.2.1.

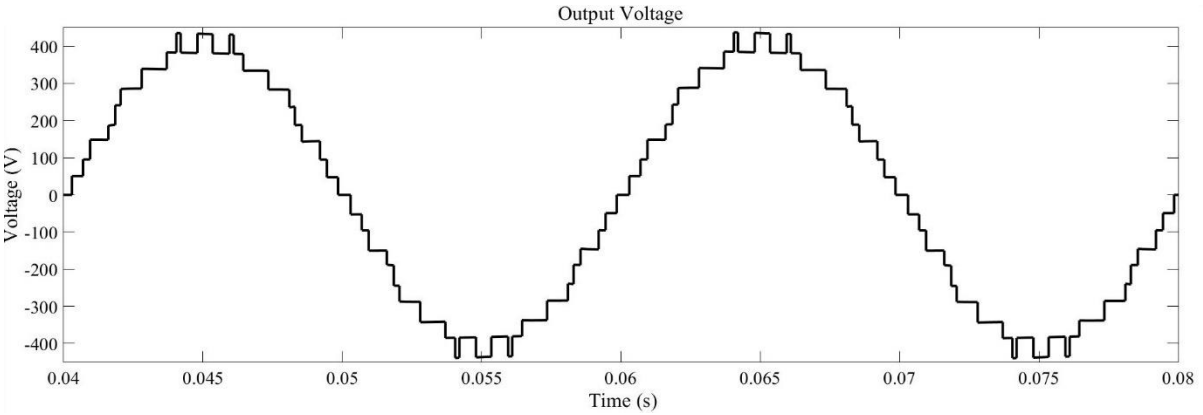


Fig. 4.2.1 Overall output voltage of design proposed in base paper

The circuit uses series-parallel switching of capacitors using power semiconductor switches and diodes to produce multilevel stepped waveform.

Zero voltage level can be achieved using either of the redundant states by turning ON the switches T_1, S and T_2 or T_1', S and T_2'. Also, S_{p1} is turned ON to charge the capacitor C_1 to $2V_{dc}$. The working of the SC cell is described as follows:

The first positive and negative output voltage levels ($\pm 2V_{dc}$) attained by using only the DC source $2V_{dc}$ without any of the capacitors in the load path. Also, S_{p1} is kept ON to facilitate charging of the capacitor C_1, while C_2 remains disconnected.

For the second positive and negative output voltage levels ($\pm 4V_{dc}$), the voltage across of the DC source is added to the voltage of C_1 that has been previously charged to V_{dc}. By turning OFF S_{p1} and turning ON S_{s1}, C_1 is now discharging. The net voltage across the load is now the addition of DC source V_{dc} and voltage $2V_{dc}$ accumulated in C_1, i.e., $4V_{dc}$. Also, in this interval, by turning ON S_{p3}, power diode D_2 becomes forward biased and C_2 now gets charged to $4V_{dc}$.

The third positive and negative output voltage levels ($\pm 6V_{dc}$) are created by series connection of the stored voltage in C_2 and the DC voltage source value through the series switch S_{s2}. This is achieved by turning ON the switch S_{s2}. Also, S_{p1} is turned ON to charge C_1 again to $2V_{dc}$.

Finally, in the fourth positive and negative output voltage levels ($\pm 8V_{dc}$), both the capacitors must be series with power supply through S_{s1} and S_{s2}. This is realized by turning ON the switches S_{s1} and S_{s2}, discharging both the capacitors and the required voltage level is attained.

The FCB cell produces 3 level waveform of amplitude V_{dc}, which when superimposed with the output of the SC cell output waveform using suitable modulation technique, a 19-level waveform is finally obtained.

4.3 Novel Topology 1

The power circuit of the proposed topology, shown in Figure 4.3.1, consists of two distinct switched capacitor-based cells, Switched Capacitor (SC) cell and Floating Capacitor (FC) cell, which work in tandem to produce the desired 19-level output waveform. Each cell employs a single DC voltage source and 2 capacitors, which are then switched suitably to produce distinct 9-level and 3-level waveforms.

SC cell operates at low switching frequency, while the FC cell operates at higher switching frequency. The SC cell produces a nine-level waveform consisting of four positive levels, four negative levels and a zero level. FC cell produces a three-level waveform consisting of one positive level, one negative level and a zero level. A series connection of SC and FC cells allow the inverter to produce a stepped sine wave with a peak amplitude of nine times the DC voltage source. This is achieved using ten MOSFET switches, four capacitors and three diodes. The capacitor and diodes form the switched capacitor network, providing the voltage boosting capability.

Voltage balancing of capacitors is achieved by series-parallel switching of the capacitor network through the semiconductor switches which gives uniform charging and discharging cycles. The Phase Disposition PWM (PDPWM) technique is used and this allows the circuit to operate with reduced switching losses and minimized switching frequency.

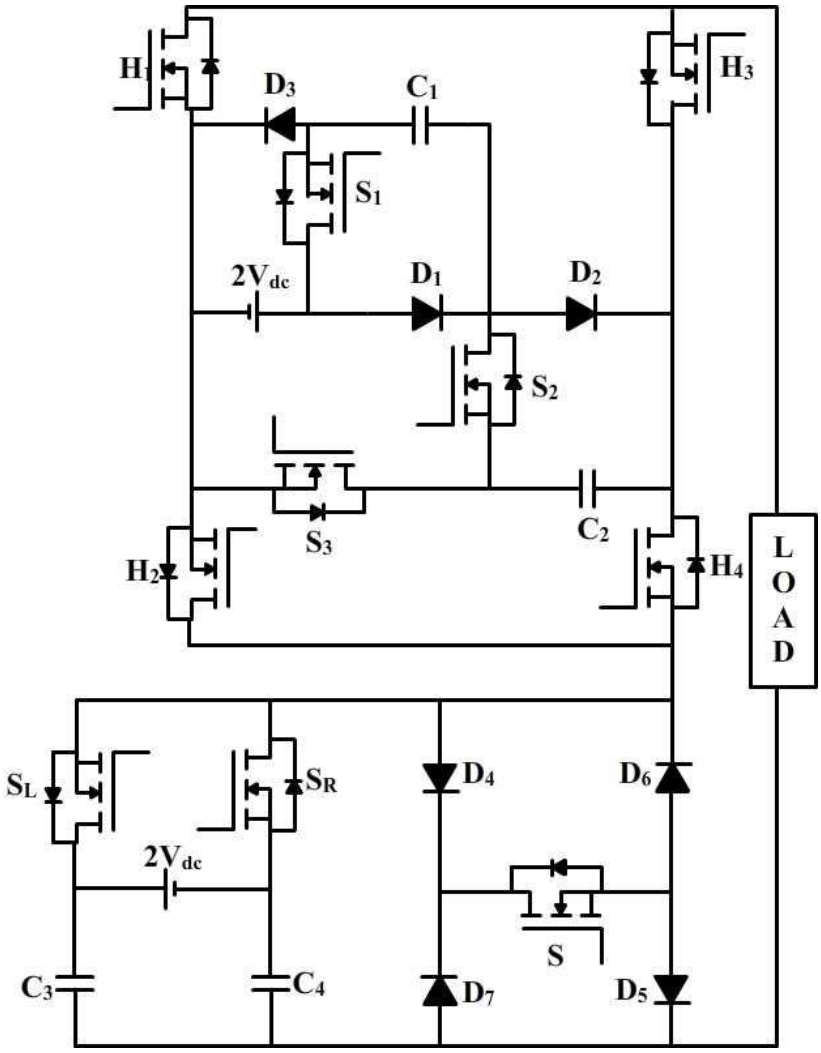


Fig 4.3.1 Proposed Novel Topology 1

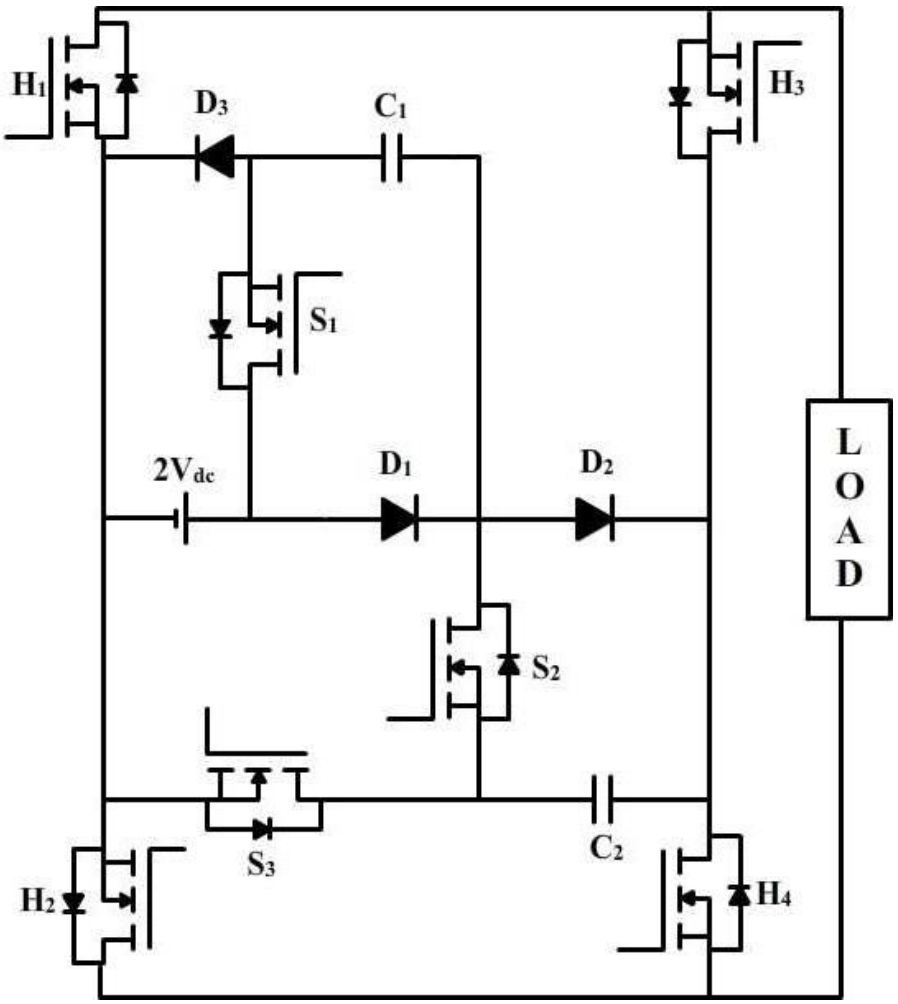


Fig. 4.3.2 SC cell of NT1

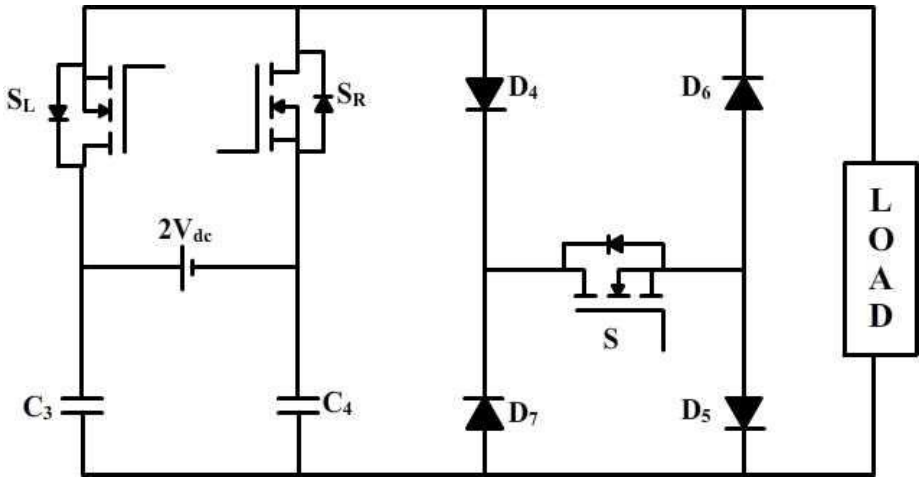


Fig. 4.3.3 FC cell of NT1

4.4 Operation of Novel Topology 1

A schematic of the SC circuit is shown in Fig. 4.3.2. Zero voltage level is achieved by turning ON the switches H_1 and H_2 or H_3 and H_4. Also, power diode D_1 becomes forward biased, charging capacitor C_1 to $2V_{dc}$. The first positive and negative voltage levels ($\pm 2V_{dc}$) is obtained by using only the DC source $2V_{dc}$ without any of the capacitors in the load path. Capacitor C_1 maintains its voltage at $2V_{dc}$ by being connected to the voltage source.

When S_1 is ON, the source voltage added with the voltage of the capacitor C_1 gives the second positive and negative voltage levels ($\pm 4V_{dc}$). When S_3 turns ON, power diode D_3 becomes forward biased and C_2 charges to $4V_{dc}$. When S_2 is ON, the source voltage added with the voltage of the capacitor C_2 gives the third positive and negative voltage levels ($\pm 6V_{dc}$). C_1 charges to $2V_{dc}$ as the diode D_1 becomes forward biased.

When S_1 and S_2 are both turned ON, the source voltage added with the voltages of the capacitors C_1 and C_2 gives the fourth positive and negative voltage levels ($\pm 8V_{dc}$).

Figure 4.3.3 shows the Floating Capacitor circuit. Switch S, with diodes D_4, D_5, D_6 and D_7, facilitate bidirectional flow of current. Capacitors C_3 and C_4 have been strategically placed to facilitate their charging to voltage V_{dc} simultaneously, with opposing polarity. When either of the switches S_L or S_R are closed, the capacitors get discharged to the load, contributing to the output waveform. When switch S is ON, the capacitors do not add to the upper cell. Thus, the voltage source is never directly connected to the load and is used only to charge the two capacitors.

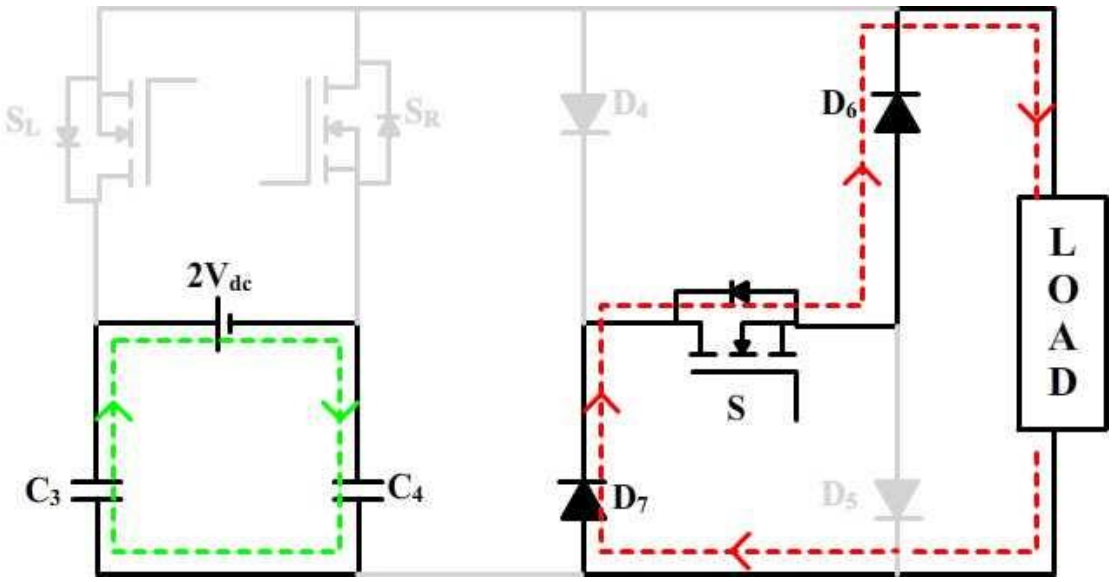
During the positive half cycle, only capacitor C_3 is used and during the negative cycle, only capacitor C_4 is used. By using switches S_L and S_R in tandem with S, voltage balancing of

capacitors is achieved without any external circuitry.

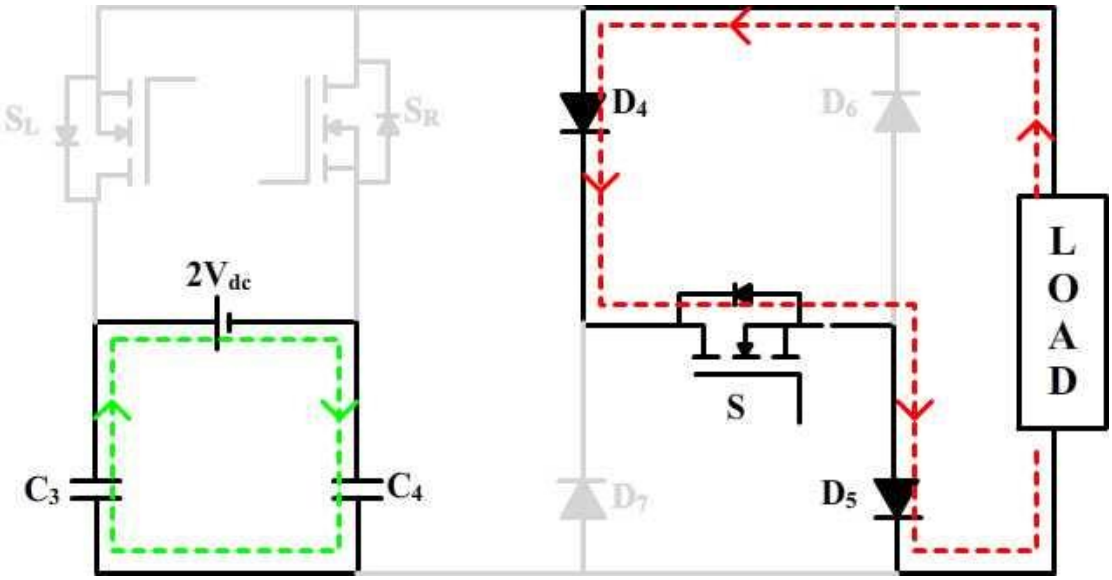
The 19-level stepped waveform is obtained by switching ON and OFF switches in the following pattern:

- Zero level is produced by turning ON H_1, H_2, H_3, H_4 and S.
- First positive level V_{dc} is produced by turning ON H_2, H_3 and S_L.
- Second positive level $2V_{dc}$ is produced by turning ON H_2, H_3 and S.
- Third positive level $3V_{dc}$ is produced by turning ON H_2, H_3 and S_L.
- Fourth positive level $4V_{dc}$ is produced by turning ON H_2, H_3, S_1, S_3 and S.
- Fifth positive level $5V_{dc}$ is produced by turning ON H_2, H_3, S_1, S_3 and S_L.
- Sixth positive level $6V_{dc}$ is produced by turning ON H_2, H_3, S_2 and S.
- Seventh positive level $7V_{dc}$ is produced by turning ON H_2, H_3, S_2 and S_L.
- Eighth positive level $8V_{dc}$ is produced by turning ON H_2, H_3, S_1, S_2 and S.
- Ninth positive level $9V_{dc}$ is produced by turning ON H_2, H_3, S_1, S_2 and S_L.
- First negative level $-V_{dc}$ is produced by turning ON H_1, H_4, H_2, H_4 and S_R.
- Second negative level $-2V_{dc}$ is produced by turning ON H_1, H_4 and S.
- Third negative level $-3V_{dc}$ is produced by turning ON H_1, H_4 and S_R.
- Fourth negative level $-4V_{dc}$ is produced by turning ON H_1, H_4, S_1, S_3 and S.
- Fifth negative level $-5V_{dc}$ is produced by turning ON H_1, H_4, S_1, S_3 and S_R.
- Sixth negative level $-6V_{dc}$ is produced by turning ON H_1, H_4, S_2 and S.
- Seventh negative level $-7V_{dc}$ is produced by turning ON H_1, H_4, S_2 and S_R.
- Eighth negative level $-8V_{dc}$ is produced by turning ON H_1, H_4, S_1, S_2 and S.
- Ninth positive level $-9V_{dc}$ is produced by turning ON H_1, H_4, S_1, S_2 and S_L.

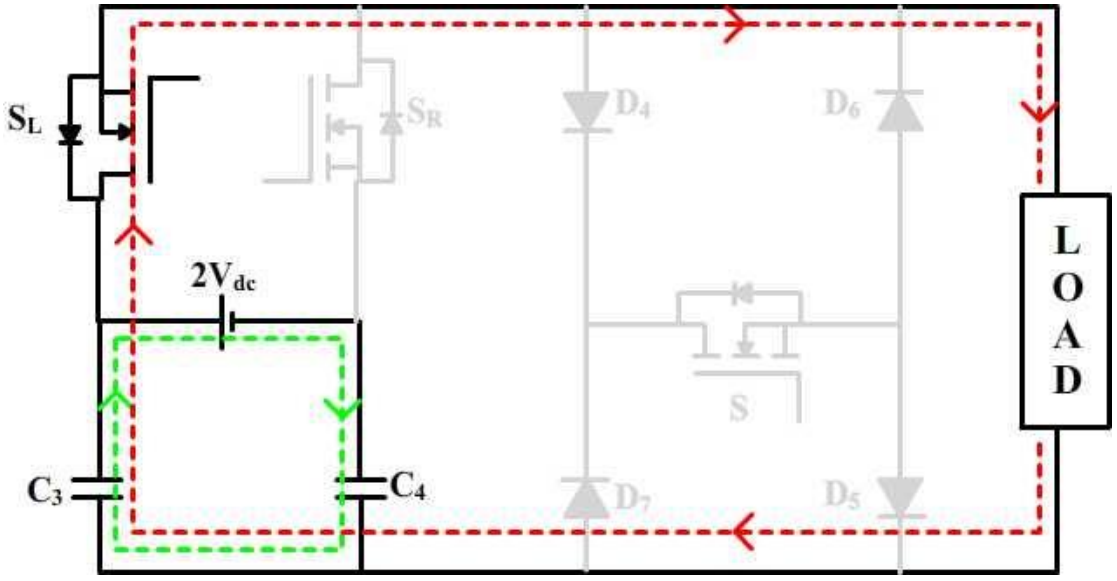
The operational stages are also presented with path of flow of current in Fig. 4.4.1.



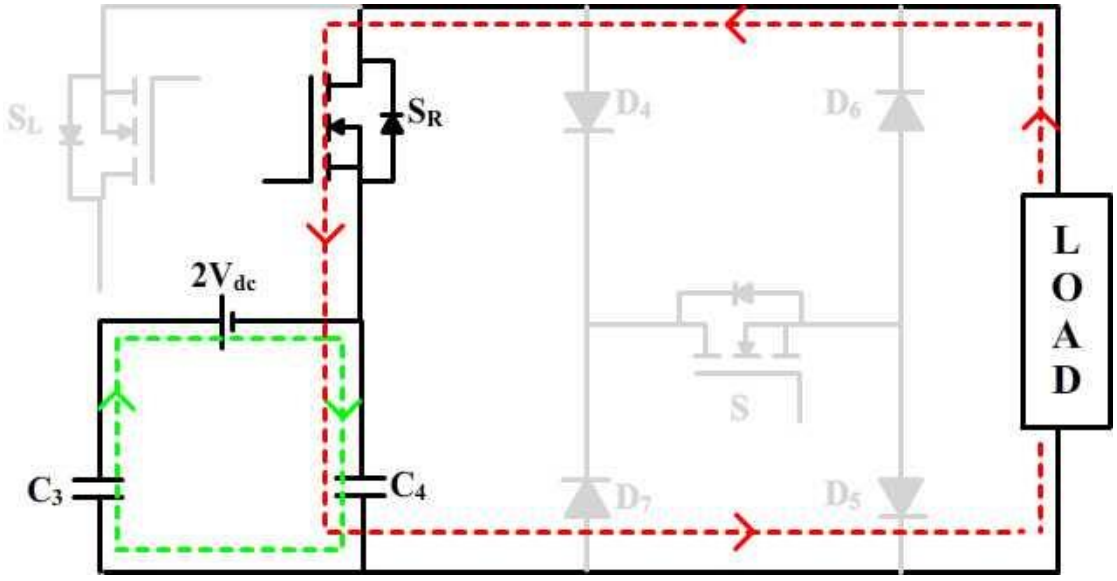
(a)



(b)



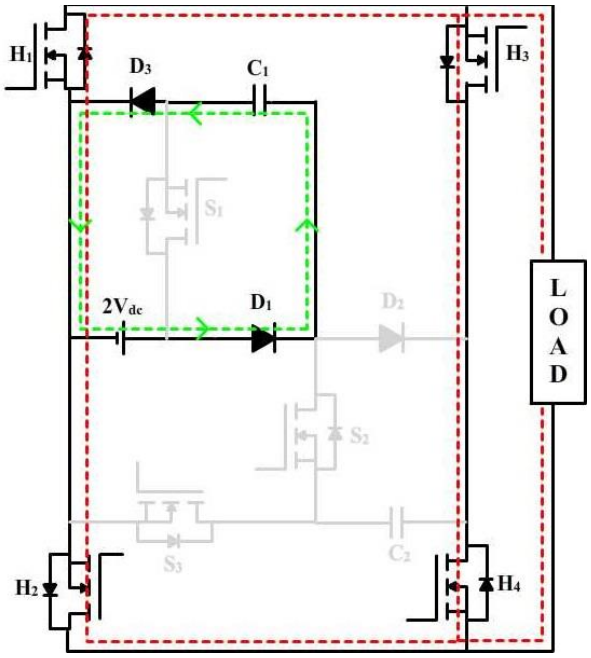
(c)



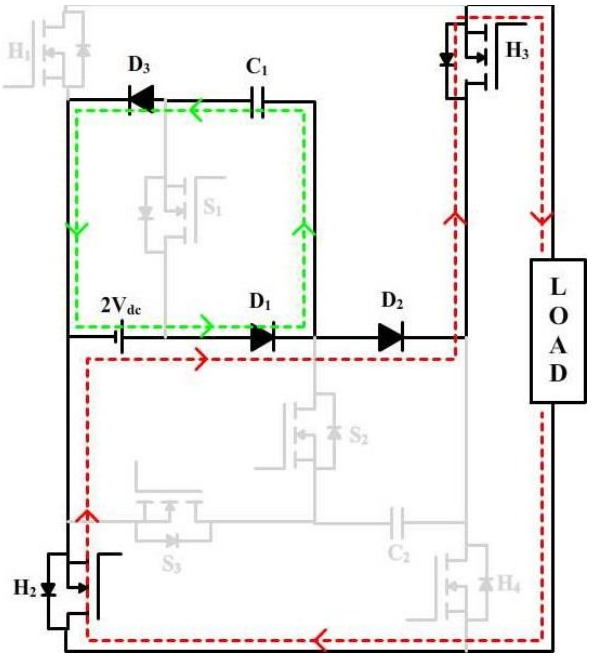
(d)

Fig. 4.4.1 FC cell operating stages (a) Zero level A (b) Zero level B (c) $+V_{dc}$ Level

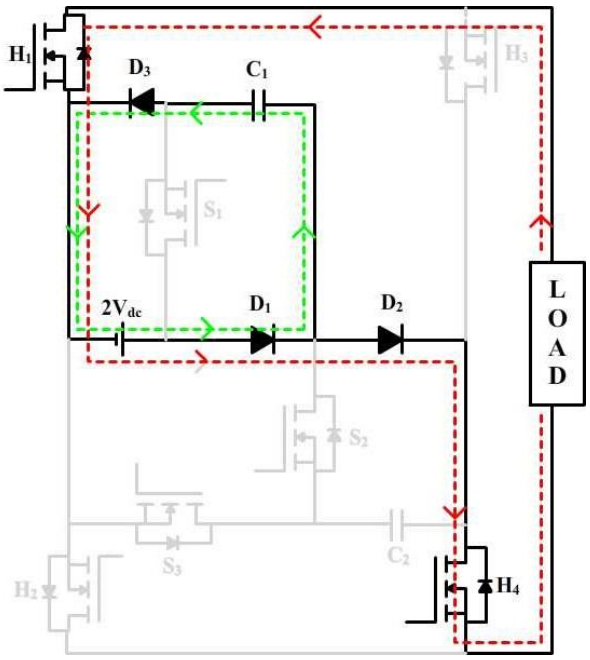
(d) $-V_{dc}$ Level


H1
D3
C1
H3
S1
2Vdc
D1
D2
LOAD
S2
S3
C2
H2
H4

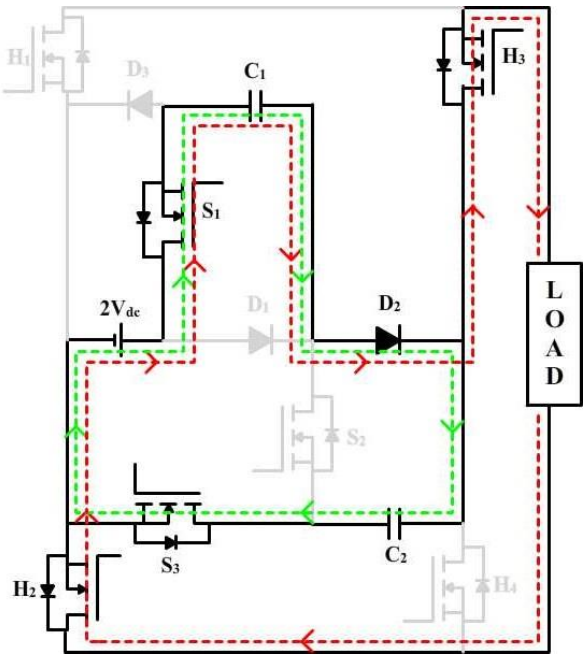
(a)


H1
D3
C1
H3
S1
2Vdc
D1
D2
LOAD
S2
S3
C2
H2
H4

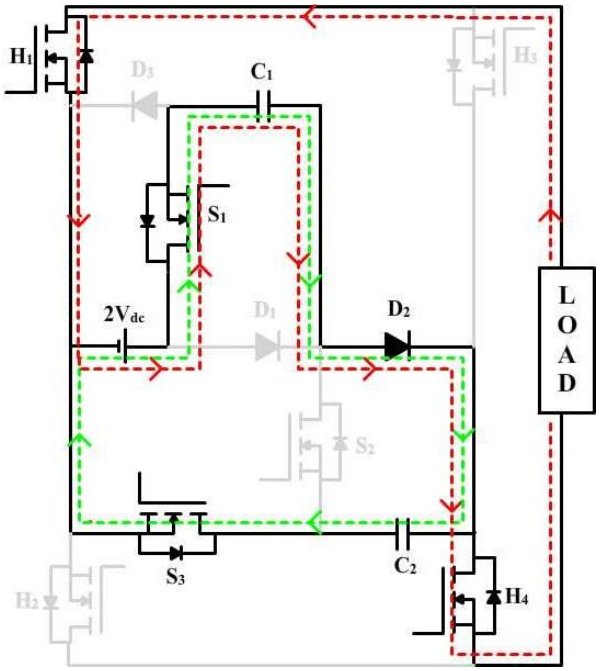
(b)


H1
D3
C1
H3
S1
2Vdc
D1
D2
LOAD
S2
S3
C2
H2
H4

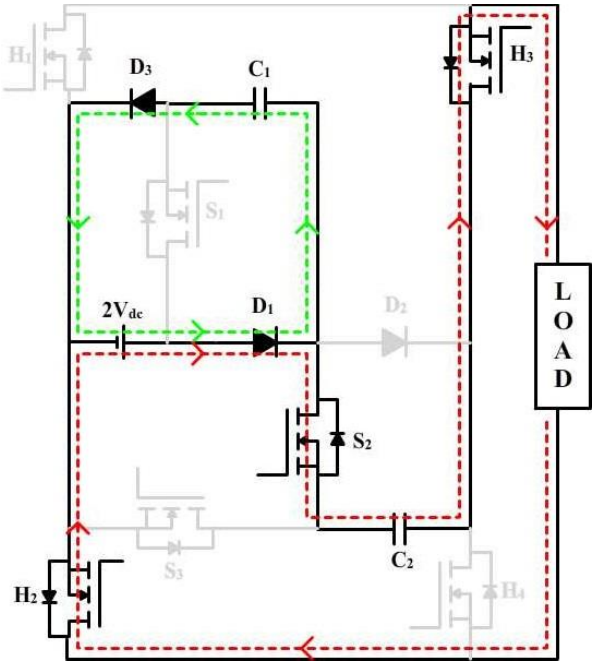
(c)


H1
D3
C1
H3
S1
2Vdc
D1
D2
LOAD
S2
S3
C2
H2
H4

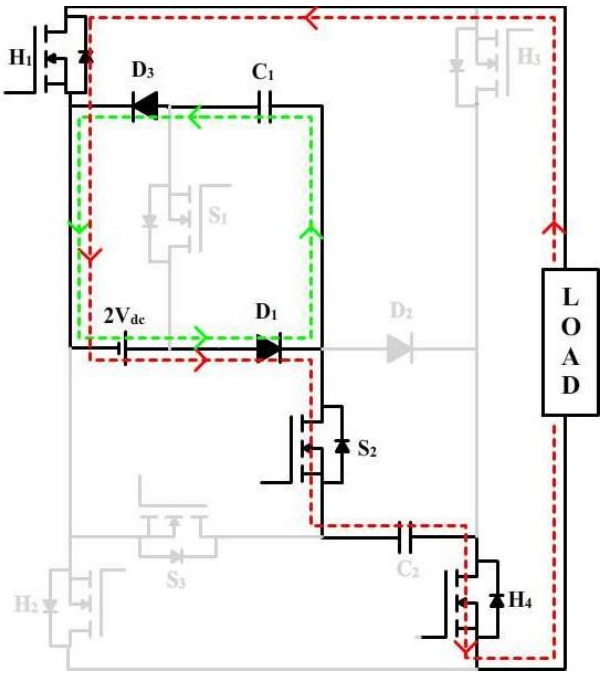
(d)


H1
D3
C1
H3
S1
2Vdc
D1
D2
LOAD
S2
S3
C2
H2
H4

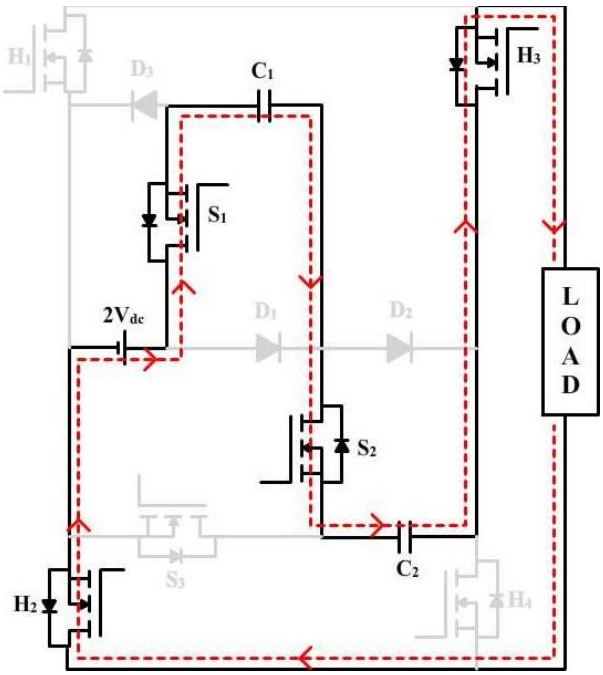
(e)


H1
D3
C1
H3
S1
2Vdc
D1
D2
LOAD
S2
S3
C2
H2
H4

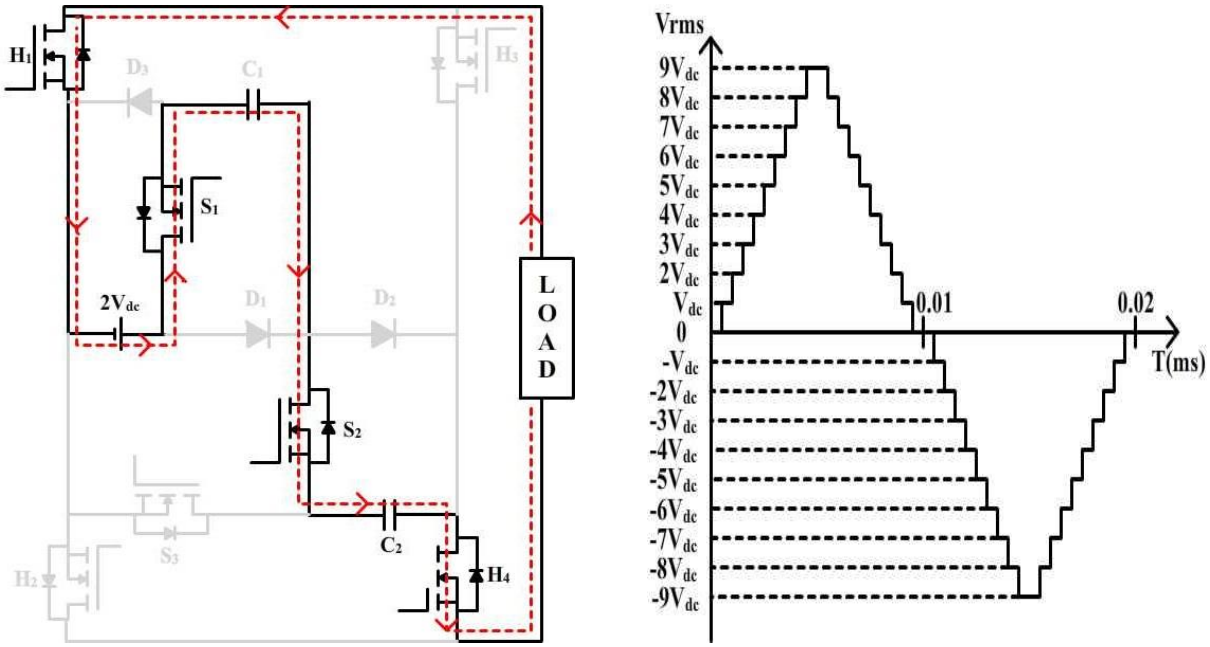
(f)


H1
D3
C1
H3
S1
2Vdc
D1
D2
LOAD
S2
S3
C2
H2
H4

(g)


H1
D3
C1
H3
S1
2Vdc
D1
D2
LOAD
S2
S3
C2
H2
H4

(h)



(i) (j)

Fig. 4.4.2 SC cell operational Stages (a) Zero level (b) +2 V_{dc} level (c) -2V_{dc} level

(d) +4V_{dc} level (e) -4 V_{dc} level (f) +6V_{dc} level (g) -6V_{dc} level (h) +8V_{dc} level

(i) -8V_{dc} level (j) Overall theoretical waveform

4.5 Novel Topology 2

The converter circuit consists of 9 switches, 3 diodes, 2 capacitors and 2 DC voltage sources. This project discusses a symmetric configuration, where both voltage sources have the same magnitude of voltages. The 2 capacitors act as storage elements and are charged and discharged multiple times within the same cycle. Each switch is switched ON and OFF to yield different output voltage at each stage, producing multilevel voltage waveform. This multilevel waveform, when fed to an H-Bridge produces multilevel AC voltage of reduced THD. Each charging stage of the capacitors can be divided into 2 modes:

1. Switch S_4 is ON and Switch S_5 is OFF

2. Switch S_5 is ON and Switch S_4 is OFF.

In mode 1, only voltage source is present in the charging circuit. In mode 2, both the voltage sources are present in the charging circuit. It is assumed that each voltage source is of magnitude 100V. Hence, capacitor C_1 gets charged to a voltage of 100V and 200V, while capacitor C_2 gets charged to voltage of 200V and 400V during the operation of the circuit. Thus, at each stage, different output voltages are obtained by series-parallel switching of the voltage sources with the capacitors facilitated by the power semiconductor diodes and switches. Fig. 4.5.1 shows a schematic of the proposed power circuit.

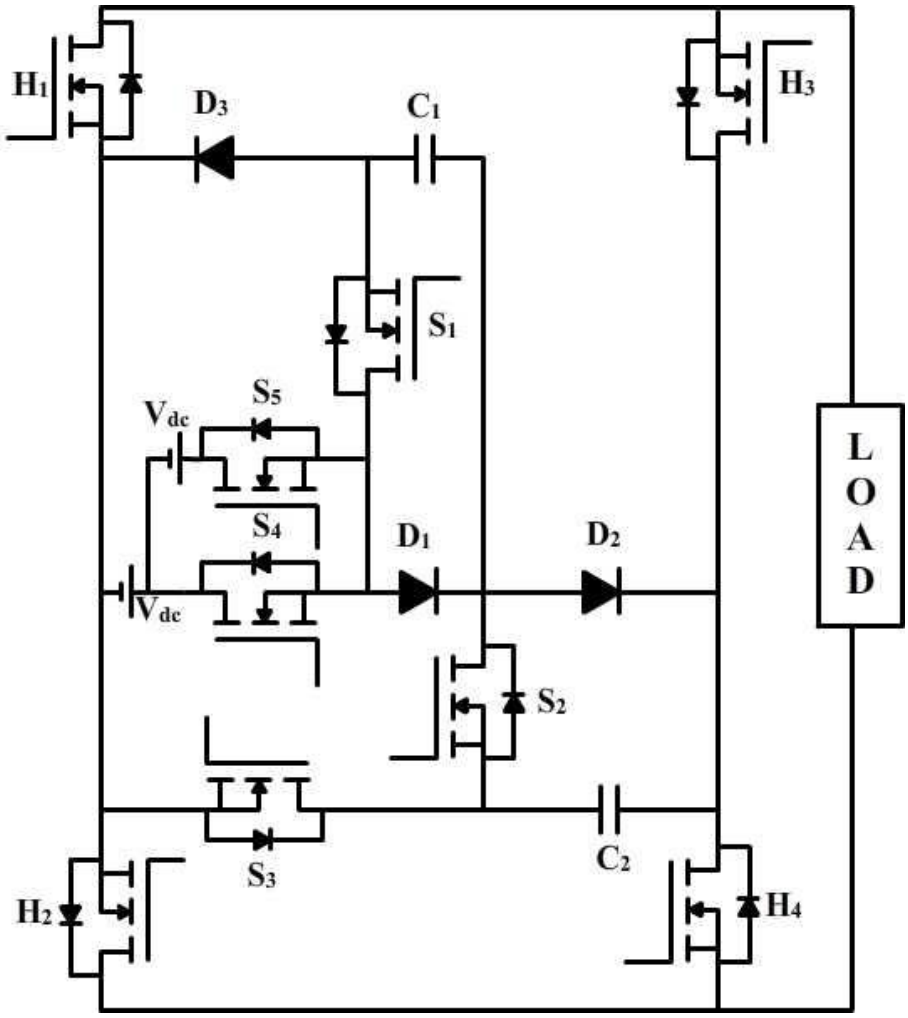


Fig. 4.5.1 Proposed Novel Topology 2

Both capacitors are self-charge balanced during each cycle without the need for external circuits to discharge the charges during each cycle. This is achieved by series-parallel switching of capacitor network realized using Phase Disposition Pulse Width Modulation (PDPWM). This facilitates complex gate signals which can switch ON and OFF the switches multiple times during a cycle, giving rise to charging and discharging paths and redundancies.

4.6 Operation of Novel Topology 2

A schematic of the SC circuit is shown in Fig. 4.5.1. The circuit works by alternatively switching ON and OFF switches S_4 and S_5 complementary to each other. Zero voltage level is achieved by turning ON the switches H_1 and H_2 or H_3 and H_4. Also, power diode D_1 becomes forward biased, charging capacitor C_1 to V_{dc}.

The first positive and negative voltage levels ($\pm V_{dc}$) is obtained by using only one DC source V_{dc} without any of the capacitors in the load path. This is achieved by switching ON S_4. Then, by turning ON S_5 and turning OFF S_4, diode D_3 gets forward biased and capacitor C_1 gets charged to $2V_{dc}$ by being connected to the voltage sources in series to each other and the second positive and negative voltages ($\pm 2V_{dc}$) are obtained.

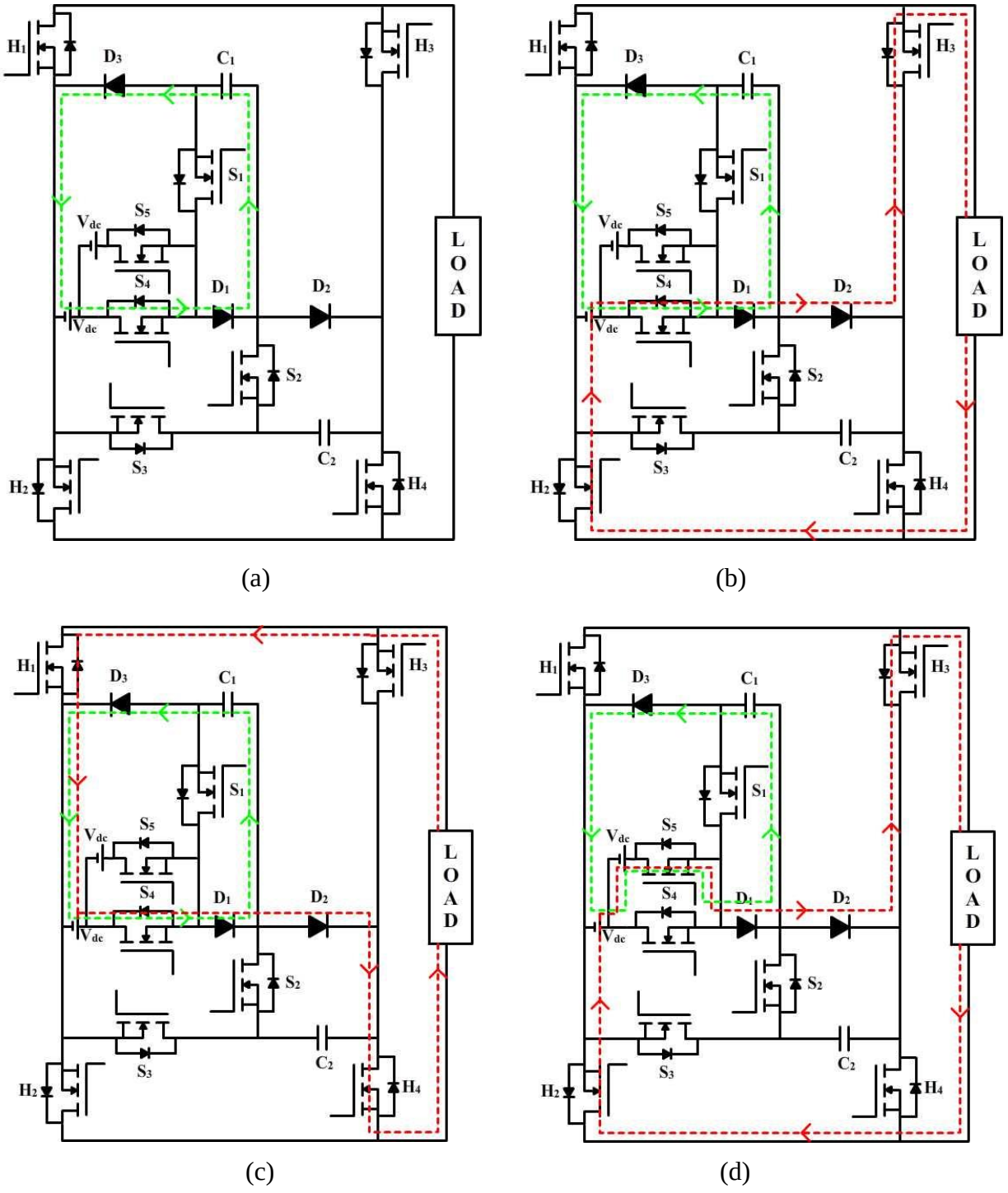
When S_1 is ON, the source voltage added with the voltage of the capacitor C_1 gives the third positive and negative voltage levels ($\pm 3V_{dc}$). The fourth positive and negative levels ($\pm 4V_{dc}$) are obtained by switching ON S_5 and adding the second voltage source. When S_3 turns ON, power diode D_2 becomes forward biased and C_2 charges to $2V_{dc}$. Now, when S_2 is ON, the source voltages added with the voltage of the capacitor C_2 gives the fifth and sixth positive and negative voltage levels ($\pm 5V_{dc}$) and ($\pm 6V_{dc}$). C_1 charges to V_{dc} as the diode D_1 becomes forward biased and C_2 maintains voltage of $2V_{dc}$.

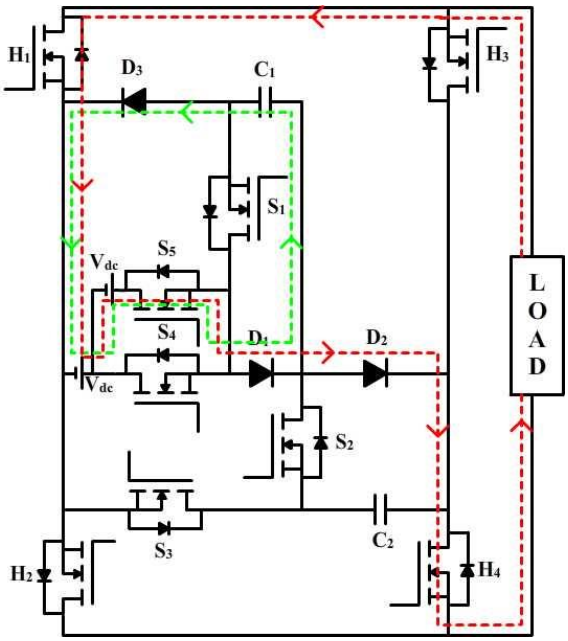
When S_1 and S_2 are both turned ON, the source voltages, added to the voltages of the capacitors C_1 and C_2 gives the seventh and eighth positive and negative voltage levels ($\pm 7V_{dc}$) and ($\pm 8V_{dc}$).

The 17-level stepped waveform is obtained by switching ON and OFF switches in the following pattern:

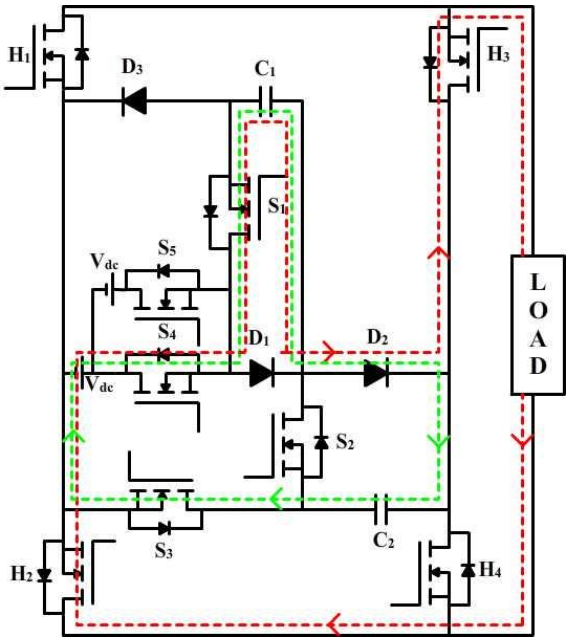
- Zero level is produced by turning ON H_1, H_2, H_3, H_4 and S_4.
- First positive level V_{dc} is produced by turning ON H_2, H_3 and S_4.
- Second positive level $2V_{dc}$ is produced by turning ON H_2, H_3 and S_5.
- Third positive level 3Vdc is produced by turning ON H_2, H_3, S_4, S_1 and S_3.
- Fourth positive level $4V_{dc}$ is produced by turning ON H_2, H_3, S_5, S_1 and S_3.
- Fifth positive level $5V_{dc}$ is produced by turning ON H_2, H_3, S_4 and S_2.
- Sixth positive level $6V_{dc}$ is produced by turning ON H_2, H_3, S_5 and S_2.
- Seventh positive level $7V_{dc}$ is produced by turning ON H_2, H_3, S_4, S_1 and S_2.
- Eighth positive level $8V_{dc}$ is produced by turning ON H_2, H_3, S_5, S_1 and S_2.
- First negative level $-V_{dc}$ is produced by turning ON H_1, H_4 and S_4.
- Second negative level $-2V_{dc}$ is produced by turning ON H_1, H_4 and S_5.
- Third negative level $-3V_{dc}$ is produced by turning ON H_1, H_4, S_4, S_1 and S_3.
- Fourth negative level $-4V_{dc}$ is produced by turning ON H_1, H_4, S_5, S_1 and S_3.
- Fifth negative level $-5V_{dc}$ is produced by turning ON H_1, H_4, S_4 and S_2.
- Sixth negative level $-6V_{dc}$ is produced by turning ON H_1, H_4, S_5 and S_2.
- Seventh negative level $-7V_{dc}$ is produced by turning ON H_1, H_4, S_4, S_1 and S_2.
- Eighth negative level $-8V_{dc}$ is produced by turning ON H_1, H_4, S_5, S_1 and S_2.

The operational stages are also presented with path of flow of current in Fig. 4.6.1.

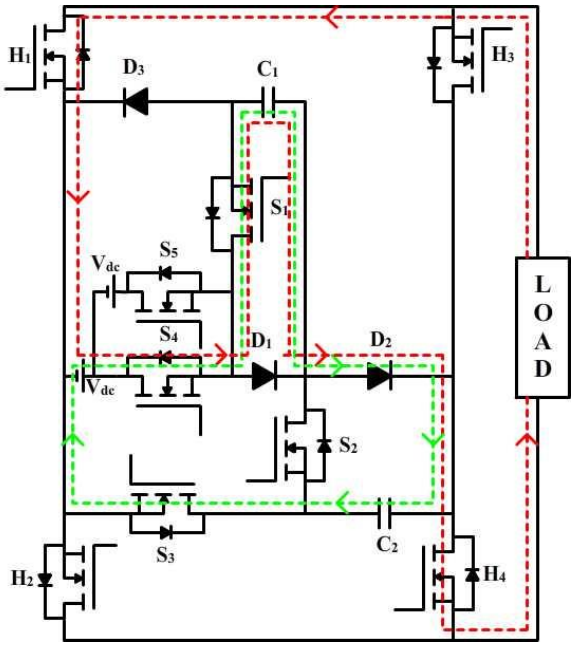



H1
D3
C1
H3
S1
Vdc
S5
S4
D1
D2
Vdc
S2
S3
C2
H2
H4
LOAD

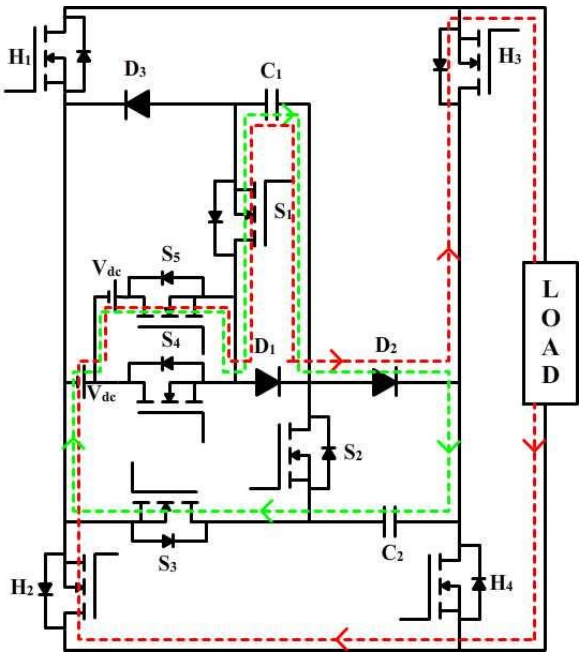
(e)


H1
D3
C1
H3
S1
Vdc
S5
S4
D1
D2
Vdc
S2
S3
C2
H2
H4
LOAD

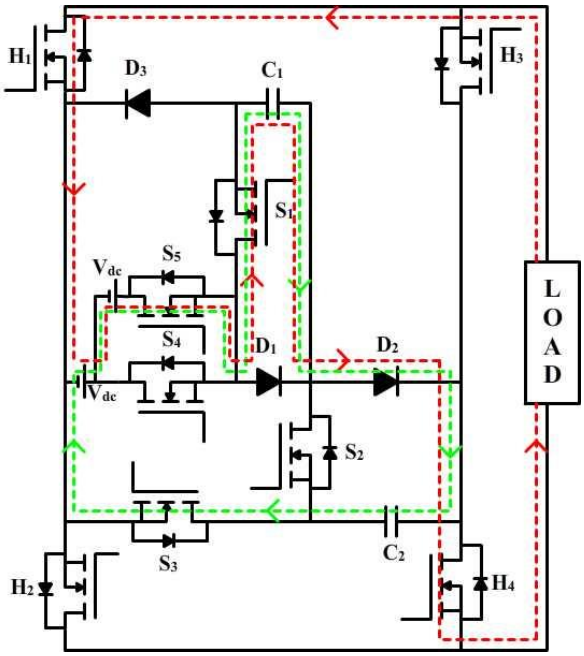
(f)


H1
D3
C1
H3
S1
Vdc
S5
S4
D1
D2
Vdc
S2
S3
C2
H2
H4
LOAD

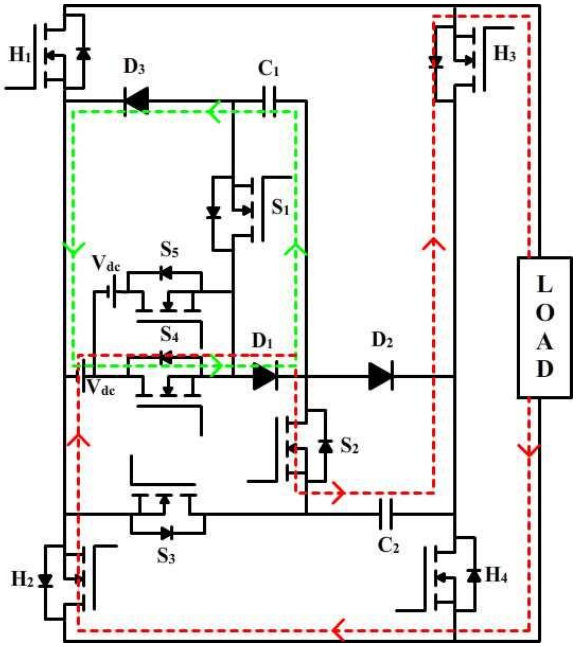
(g)


H1
D3
C1
H3
S1
Vdc
S5
S4
D1
D2
Vdc
S2
S3
C2
H2
H4
LOAD

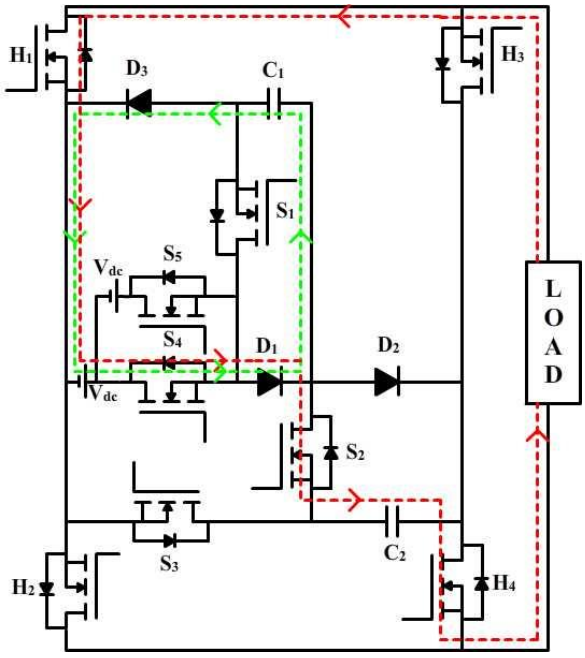
(h)


H1
D3
C1
H3
S1
Vdc
S5
S4
D1
D2
Vdc
S2
S3
C2
H2
H4
LOAD

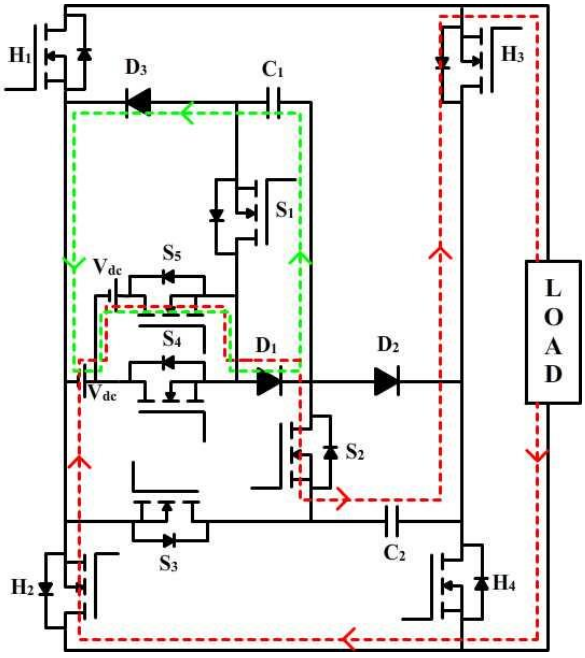
(i)


H1
D3
C1
H3
S1
Vdc
S5
S4
D1
D2
Vdc
S2
S3
C2
H2
H4
LOAD

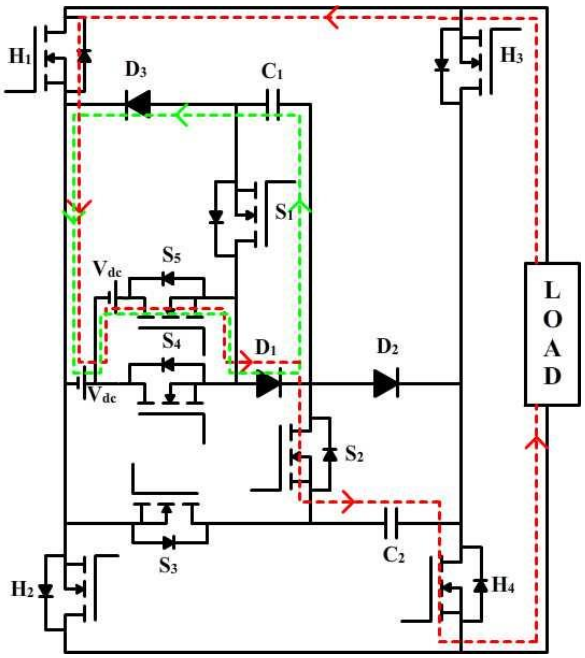
(j)


H1
D3
C1
H3
S1
Vdc
S5
S4
D1
D2
Vdc
S2
S3
C2
H2
H4
LOAD

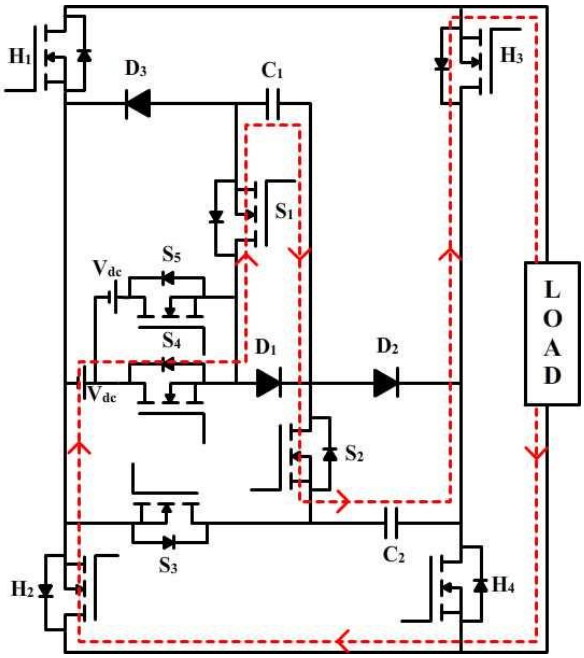
(k)


H1
D3
C1
H3
S1
Vdc
S5
S4
D1
D2
Vdc
S2
S3
C2
H2
H4
LOAD

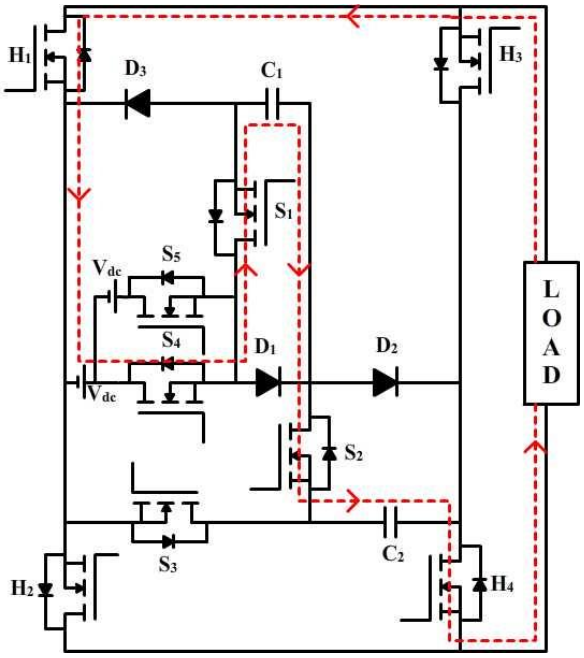
(l)


H1
D3
C1
H3
S1
Vdc
S5
S4
D1
D2
Vdc
S2
S3
C2
H2
H4
LOAD

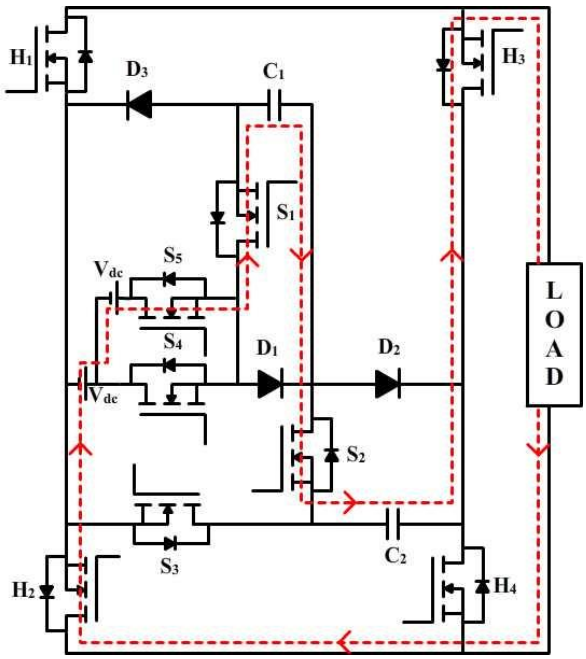
(m)


H1
D3
C1
H3
S1
Vdc
S5
S4
D1
D2
Vdc
S2
S3
C2
H2
H4
LOAD

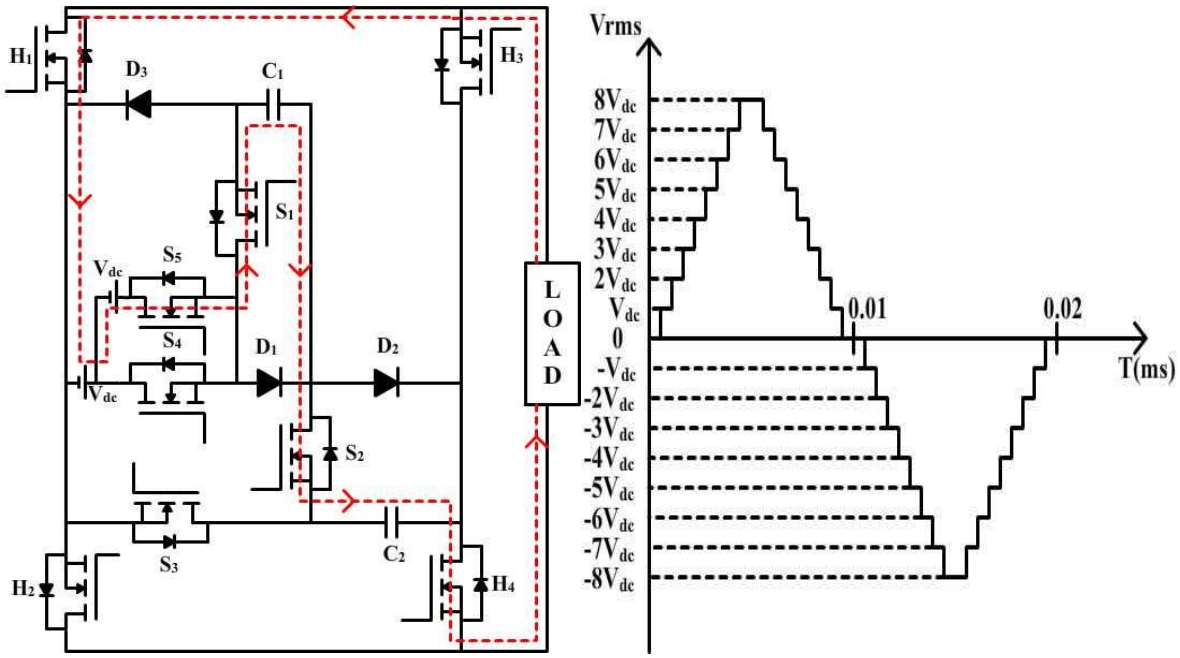
(n)


H1
D3
C1
H3
S1
Vdc
S5
S4
D1
D2
Vdc
S2
S3
C2
H2
H4
LOAD

(o)


H1
D3
C1
H3
S1
Vdc
S5
S4
D1
D2
Vdc
S2
S3
C2
H2
H4
LOAD

(p)



(q) (r)

Fig. 4.6.1 NT2 circuit operational stages (a) Zero level (b) + V_{dc} level (c) -V_{dc} level

(d) +2V_{dc} level (e) -2 V_{dc} level (f) +3V_{dc} level (g) -3V_{dc} level (h) +4V_{dc} level

(i) -4V_{dc} level (j) 5V_{dc} level (k) -5V_{dc} level (l) +6V_{dc} level (m) -6V_{dc} level

(n) +7V_{dc} level (o) -7V_{dc} level (p) +8V_{dc} level (q) -8V_{dc} level

(r) Overall theoretical waveform

4.7 Proposed PWM strategy

The switching pulses for the switches in both of the above proposed topologies are obtained by comparison of reference sine waveform which resembles the desired output voltage with carriers. The technique used here is called Phase Disposition PWM (PDPWM), wherein, the absolute function of a reference sine waveform is compared to 9 level shifted triangle carrier

waveforms in the first novel topology and 8 level shifted triangular carrier waveforms in the second novel topology. The reference sine wave is chosen to have an amplitude of 9 or 8 and each of the triangle carrier waves have an amplitude of 1 each. The reference sine wave is defined as

$$Vref = Arsinwt$$

The modulation index is calculated using the following equation:

$$m = \frac{Ar}{\mathrm{n} * \mathrm{Ac}}$$

Where A_c is the amplitude of each carrier wave, n is the number of triangular carrier waves and A_r is the amplitude of the reference sine wave. A_r is chosen as 9 and 8 in the first topology and second topology respectively and A_c is chosen as 1. Thus, the modulation index is calculated as 1. This allows the maximum number of levels to be obtained and the THD to be minimized in this particular case. Also, a commander coefficient (CM) is defined to be used to select the positive half or negative half of the reference wave over a single cycle.

$$CM = \frac{1 + \mathrm{sgn}(\mathrm{Vref})}{2}$$

Where,

$$Vref = Arsin(wt).$$

Here, by selecting CM = 1, the comparison between V_{ref} and each carrier waveform will be done in the first half-cycle of the reference waveform; therefore the positive output voltage levels are made, whereas by setting CM on zero, the second half-cycle of the reference waveform is involved in the comparative process and as a result the negative steps of the output

voltage are built.

From the working of the base circuit, it can be seen that all the switches of the proposed SC cell sub-unit are commutating under the low switching frequency, whereas three power switches located at the FCB side are modulating with a high switching frequency that its value is attributed to the frequency of the carrier triangular waveforms.

In the novel topology 1, the number of switches in the SC cell have been reduced and the switching mechanism in the FCB cell has been changed such that only two of the switches operate at high frequency at a given time, hence reducing conduction losses and switching losses significantly.

In the novel topology 2, the FC cell has been removed and two new switches have been added to the SC cell to enable selection of either of the two voltage sources. These selecting switches work at high frequency complementary to each other while the other switches operate at low switching frequency.

CHAPTER 5

RESULTS AND DISCUSSION

5.1 Simulation of Novel Topology 1

The proposed 19-level SCMLI was simulated using MATLAB Simulink r2018a. The Simscape PowerSystems toolbox was used for simulation. The Tustin/Backward Euler solver was utilized.

The objective of this project is to minimize THD for a 200 ohm purely resistive load foe both the topologies. The FFT Analyser was used to calculate the THD of the output current and voltage waveforms.

5.2 Design and Output parameters of Novel Topology 1

The output parameters, THD characteristics and circuit design parameters of the inverter are shown in Table 5.1.1, Table 5.2.2 and Table 5.2.3.

Parameter	Value
V_{rms}	302.9V
I_{rms}	1.59A
Output Power	481.6W

Table 5.2.1 Output parameters of NT1

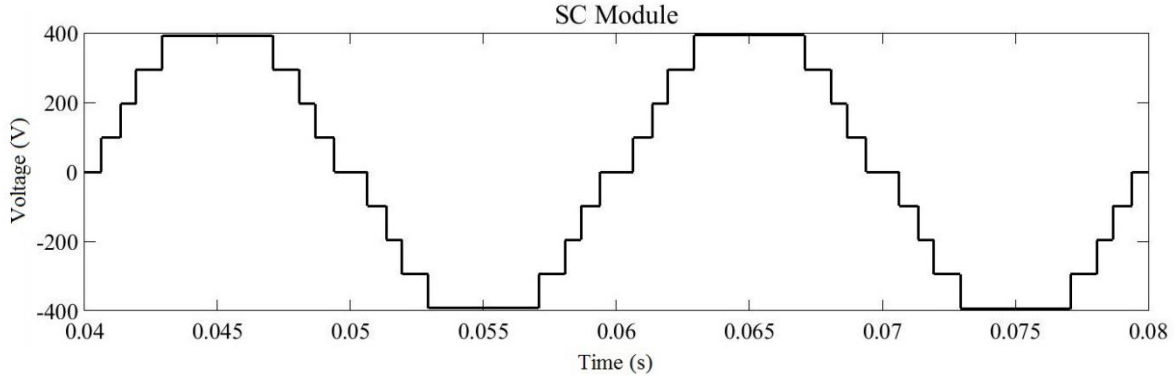
Figure 5.2.1 depicts the load current waveform of the proposed inverter module. FFT analysis was performed on the load current and the result obtained is shown in Figure 5.2.2. THD of the load current was found to be 5.80 %. The third harmonic component of the output current was found to be 0.47%.

Frequency (Hz)	Order	%
0	DC	0.00
50	Fnd	100.00
100	h2	0.03
150	h3	0.47
200	h4	0.06
250	h5	0.70
300	h6	0.03
350	h7	0.21
400	h8	0.00
450	h9	0.45
500	h10	0.02

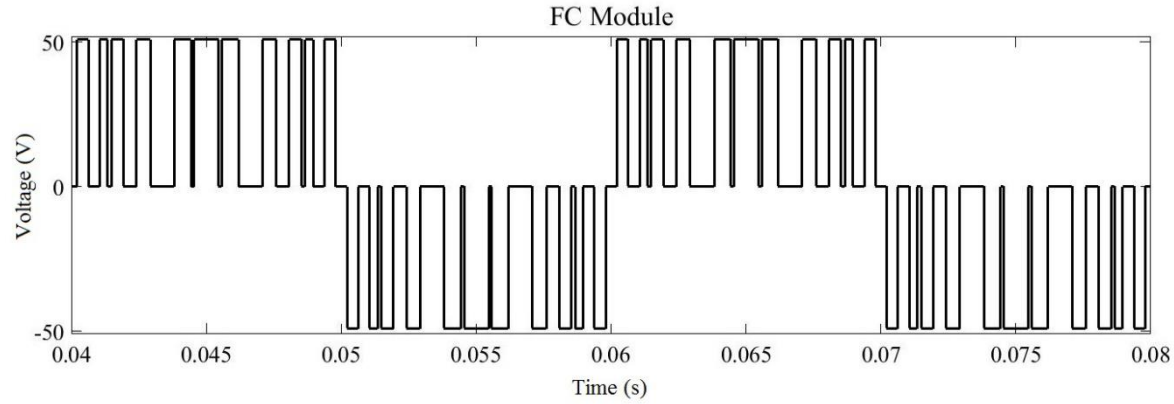
Table 5.2.2 Output harmonics of NT1

Parameter	Value
Input DC Voltage Source in SC Cell	100 V
Input DC Voltage Source in FC Cell	100 V
Design Power	500 W
Capacitor $C1$	$2000\mu F$
Capacitor $C2$	$3000\mu F$
Capacitor $C3$	$1000\mu F$
Capacitor $C4$	$1000\mu F$

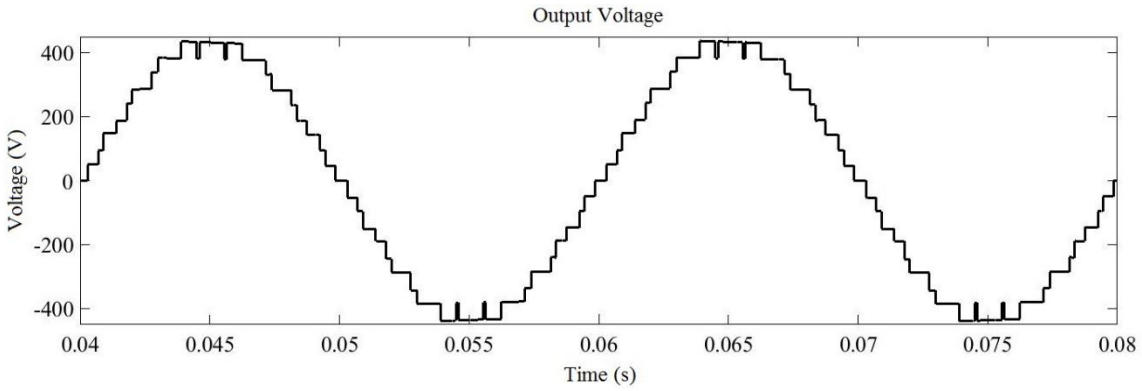
Table 5.2.3 Design parameters of NT1



(a)



(b)



(c)

Fig. 5.2.1 Output waveform of NT1 (a) SC Module (b) FC Module

(c) Overall Output Voltage

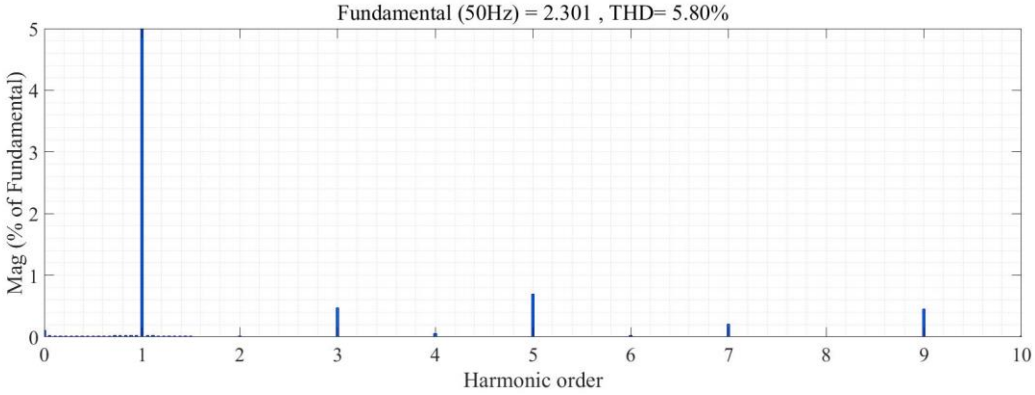


Fig. 5.2.2 THD characteristics of output current of NT1

5.3 Simulation of Novel Topology 2

The proposed 17-level SCMLI was simulated using MATLAB Simulink r2018a. The Simscape PowerSystems toolbox was used for simulation. The Tustin/Backward Euler solver was utilized.

The objective of this project is to minimize THD for a 200 ohm purely resistive load foe both the topologies. The FFT Analyser was used to calculate the THD of the output current and voltage waveforms.

5.4 Design and Output parameters of Novel Topology 2

The output parameters, THD characteristics and circuit design parameters of the inverter are shown in Table 5.4.1, Table 5.4.2 and Table 5.4.3.

Parameter	Value
V_{rms}	527.0V
I_{rms}	2.635A
Output Power	1388.6W

Table 5.4.1 Output parameters of NT2

Figure 5.4.1 depicts the load current waveform of the proposed inverter module. FFT analysis was performed on the load current and the result obtained is shown in Figure 5.4.2. THD of the load current was found to be 6.41 %. The third harmonic component of the output current was found to be 1.71%.

Frequency (Hz)	Order	%
0	DC	0.00
50	Fnd	100.00
100	h2	0.03
150	h3	1.71
200	h4	0.01
250	h5	0.81
300	h6	0.00
350	h7	1.21
400	h8	0.00
450	h9	0.62
500	h10	0.00

Table 5.4.2 Output harmonics of NT2

Parameter	Value
Input DC Voltage 1	100 V
Input DC Voltage 2	100 V
Design Power	1400W
Capacitor $C1$	$2000\mu F$
Capacitor $C2$	$3000\mu F$

Table 5.4.3 Design parameters of NT2

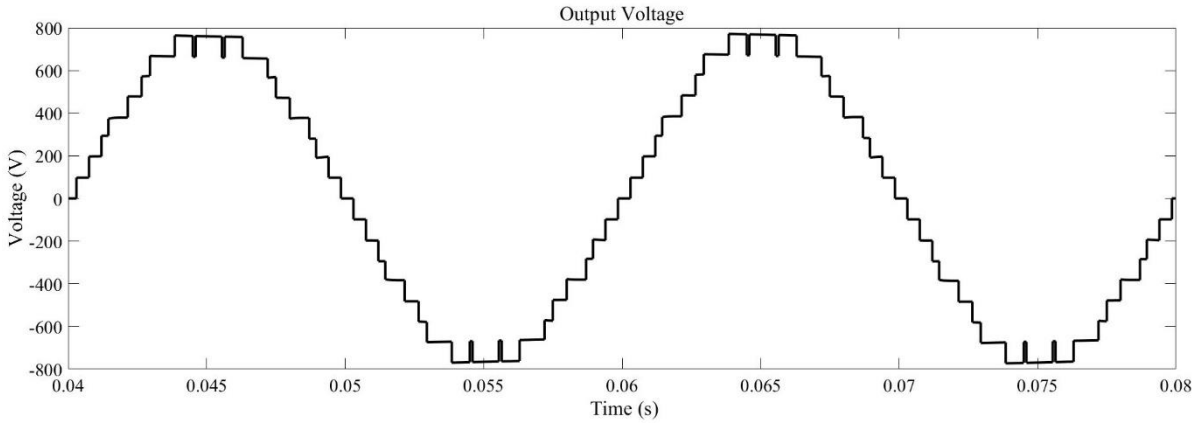


Fig 5.4.1 Output waveform of NT2

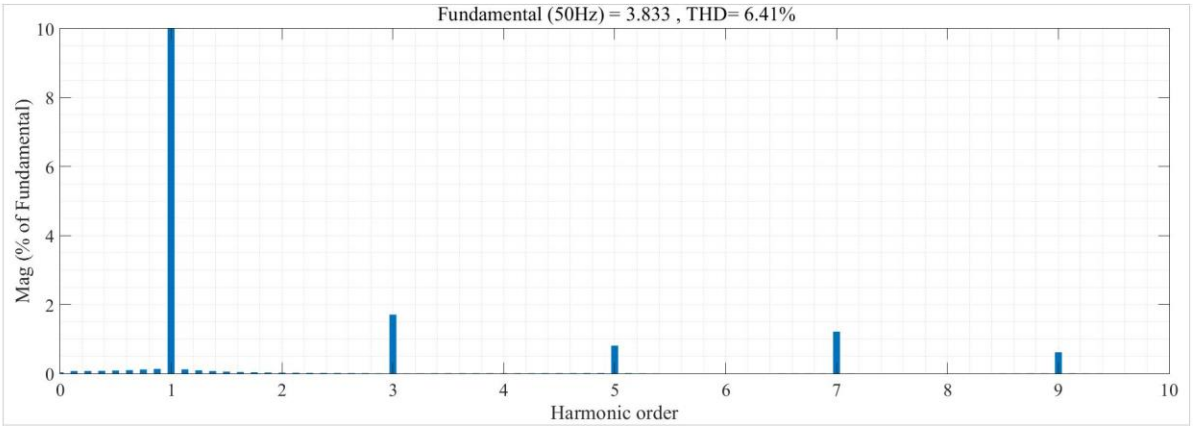


Fig. 5.4.2 THD characteristics of output current of NT2

The modulation index of both the above topologies can be changed according to the needs of the load.

5.5 PWM strategy

As discussed earlier, PDPWM strategy is used for modulation of the above topologies with 9 and 8 carriers respectively. The waveform of PDPWM with reference and carriers are depicted in Fig. 5.5.1.

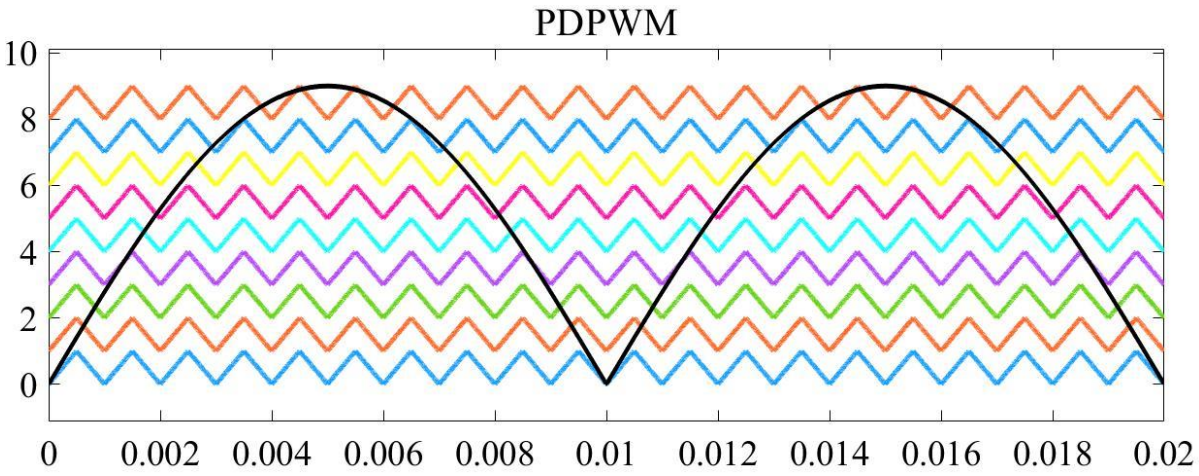


Fig. 5.5.1 PDPWM strategy waveform

The gating pulses for each of the switches are obtained by comparing the reference wave with carrier wave and using logic gates like AND, OR, etc.

CHAPTER 6

CONCLUSION

In this project, a switched capacitor based single phase multi-level inverter with reduced number of devices is first simulated. Then, two novel designs based on the simulated model is proposed, wherein the models focus on reducing losses and costs while increasing reliability. A literature survey of the different topologies of multi-level inverters and new PWM techniques was presented. The carrier based PDPWM technique was used for generating switching pulses. The output waveforms for voltage and current were recorded for a resistive load. Simulation was done in MATLAB Simulink environment using the Simscape PowerSystems toolbox. FFT analysis for output voltage and current was done and the THD was noted.

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