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# Switched Capacitor Based Multilevel Boost Inverter for Smart Grid Applications

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***Abstract*—Inverters are power electronic converters essential for linking sources of DC power to the AC grid. Conventional inverters often use transformers and harmonic filters which are bulky, expensive and lossy. Multilevel inverters are a viable alternative to classical inverters, offering reduced THD, inductor-less design and increased range of control. They produce a stepped waveform, with close resemblance to a sine wave. Smart grids may have several distributed sources and when these sources have minimal THD, there is a reduced stress for filtering them at the point of common coupling. In this paper, a switched capacitor based multilevel inverter offering boost capability and low THD is proposed. The inverter has inherent charge balancing capability, removing the need for voltage sensors and auxiliary circuits. The switches in the inverter are modulated using PODPWM technique, which facilitates voltage balancing and reduced switching losses. The design is validated by simulation and the output waveforms and parameters are presented.**

***Index Terms*—Switched Capacitor, Multilevel Inverter, Smart Grid**

## I. Introduction

Inverters are power electronic circuits that convert fixed DC voltage to AC voltage of variable amplitude and frequency. When the output waveform of the inverter closely resembles a sine wave, it has the least harmonic content. The harmonic distortion increases with increase in deviation of the output voltage waveform from a pure sine wave.

Multilevel inverters are effective in Motor Drives [1]- [2], FACTS [3] and Static VAR Generators [4]- [5]. In drives, these harmonics cause increased losses and undersirable effects such as pulsating torques when applied to an AC Motor [6]- [7]. Multilevel inverters (MLIs) are a breed of inverters that produce a stepped waveform resembling a sine wave. They are a more efficient and effective alternative to classical inverter topologies as they don't require inductors and transformers for power conversion [8]. The desired stepped waveform is achieved by using one of the many available Pulse-Width Modulation techniques.

There are three classical multilevel inverter topologies: neutral point clamped (NPC), cascaded H-bridge (CHB), and flying capacitor (FC) topologies. The cascaded multilevel inverters offer reliable performance and can reach higher voltage levels [9]. These inverters offer high power quality associated with reduced number of power switches [10]. Traditional multilevel inverters suffer from requiring many auxiliary circuit devices for charge balancing for proper operation [11]- [12]. In these inverters, the magnitude of the output voltage is simply the sum of the scalar superimposition of the DC link voltages [13] and cannot be greater. Currently, research in multilevel inverters are directed towards reducing the number of switches for the same power rating while improving THD, thereby making them a suitable alternative for the CHB topology [14].

A smart grid has several distributed sources of which many are renewable energy sources. The injection of harmonics into the grid becomes an issue and reducing the harmonics at the point of common coupling (PCC) becomes paramount. MLIs reduce the harmonics at the distributed sources and therefore mitigate the need for costly filters at the PCC. One of the major issues faced in harnessing the power from photovoltaic panels is the small magnitude of available DC voltage. It therefore becomes necessary to boost this voltage for meaningful utilisation. Conventionally, a suitable boost converter is employed to elevate the input voltage before converting it into AC using an inverter. Switched capacitor-based MLI designs are a lucrative option due to inherent voltage boosting capability and reduced complexity of design.

In this paper, an improved configuration of a switched capacitor-based step-up MLI is presented. The operating modes, design of passive elements, modulation strategy used and the simulated results are discussed subsequently.

## II. Power Circuit Description

The power circuit of the proposed topology, shown in Figure 1, consists of two distinct switched capacitor-based cells, Switched capacitor(SC) cell and Floating Capacitor(FC) cell, which work in tandem to produce the desired 19-level output

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waveform. Each cell employs a single DC voltage source and 2 capacitors, which are then switched suitably to produce distinct 9-level and 3-level waveforms.

Cell 1 operates at low switching frequency, while the Cell 2 operates at higher switching frequency. Cell 1 produces a nine level waveform consisting of four positive levels, four negative levels and a zero level. Cell 2 produces a three level waveform consisting of one positive level, one negative level and a zero level. A series connection of Cells 1 and 2 allows the inverter to produce a stepped sine wave with a peak amplitude of nine times the DC voltage source. This is achieved using ten MOSFET switches, four capacitors and three diodes. The capacitor and diodes form the switched capacitor network, providing the voltage boosting capability.

Voltage balancing of capacitors is achieved by series-parallel switching of the capacitor network through the semiconductor switches which gives uniform charging and discharging cycles. The Phase Opposition Disposition PWM (PODPWM) technique is used and this allows the circuit to operate with reduced switching losses and minimized switching frequency.

### A. Cell 1: Switched Capacitor Circuit

Figure 2 shows the operation of the SC circuit. Zero voltage level is achieved by turning ON the switches $H_1$ and $H_2$ or $H_3$ and $H_4$. Also, power diode $D_1$ becomes forward biased, charging capacitor $C_1$ to $2V_{dc}$.

The first pair of positive and negative voltage levels ($\pm 2V_{dc}$) is obtained by using only the DC source $2V_{dc}$ without any capacitors in the load path. Capacitor $C_1$ maintains its voltage at $2V_{dc}$ by being connected to the voltage source.

When $S_1$ is ON, the source voltage added with the voltage of the capacitor $C_1$ gives the second positive and negative voltage levels ($\pm 4V_{dc}$). When $S_3$ turns ON, power diode $D_3$ becomes forward biased and $C_2$ charges to $4V_{dc}$.

When $S_2$ is ON, the source voltage added with the voltage of the capacitor $C_2$ gives the third positive and negative voltage levels ($\pm 6V_{dc}$). $C_1$ charges to $2V_{dc}$ as the diode $D_1$ becomes forward biased.

When $S_1$ and $S_2$ are both turned ON, the source voltage added with the voltages of the capacitors $C_1$ and $C_2$ gives the fourth positive and negative voltage levels ($\pm 8V_{dc}$).

### B. Cell 2: Floating Capacitor Circuit

Figure 3 shows the Floating Capacitor circuit. Switch S, with diodes $D_4$, $D_5$, $D_6$ and $D_7$, facilitate bidirectional flow of current. Capacitors $C_3$ and $C_4$ have been strategically placed to facilitate their charging to voltage $V_{dc}$ simultaneously, with opposing polarity. When either of the switches $S_L$ or $S_R$ are closed, the capacitors get discharged to the load, contributing to the output waveform. When switch S is ON, the capacitors do not add to the upper cell. Thus, the voltage source is never directly connected to the load and is used only to charge the two capacitors.

During the positive half cycle, only capacitor $C_3$ is used and during the negative cycle, only capacitor $C_4$ is used. By using

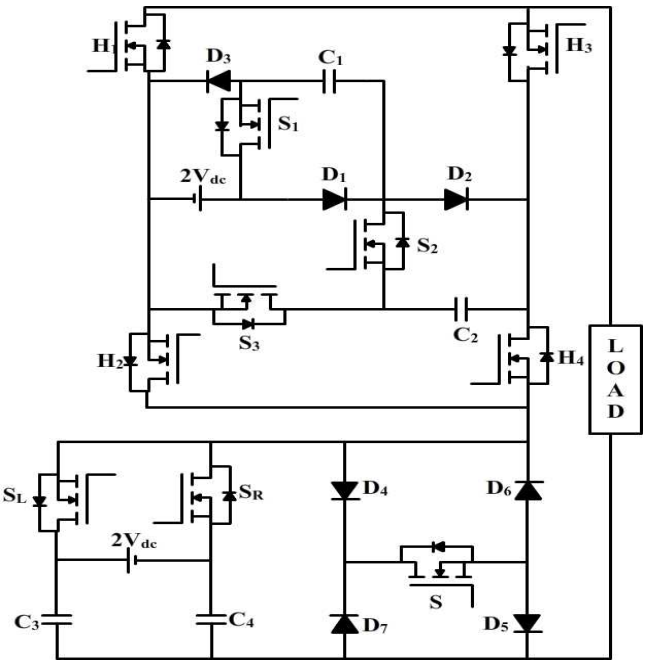


Fig. 1. Proposed 19-level MLI Power Circuit

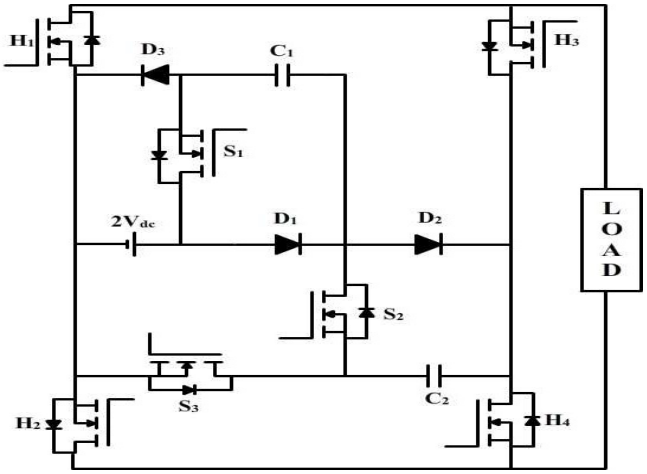


Fig. 2. Cell 1 - Switched Capacitor circuit

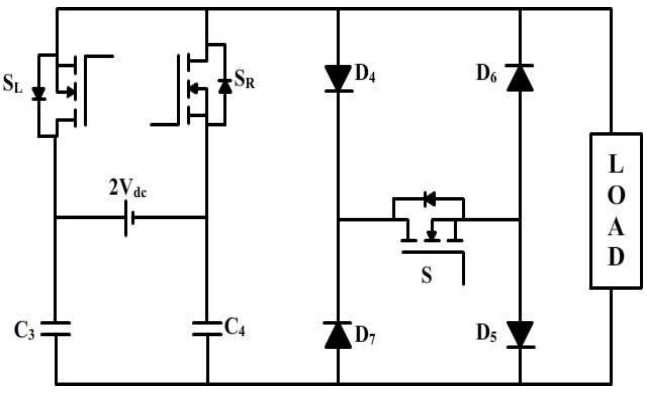


Fig. 3. Cell 2 - Floating Capacitor circuit

switches $S_L$ and $S_R$ in tandem with S, voltage balancing of capacitors is achieved without any external circuitry.

## III. Operation of Proposed Converter

The 19-level stepped waveform is obtained by switching ON and OFF switches in the following pattern:

- Zero level is produced by turning ON $H_2$, $H_4$, $H_2$, $H_4$ and S.
- First positive level $V_{dc}$ is produced by turning ON $H_2$, $H_4$, $H_2$, $H_4$ and $S_L$.
- Second positive level $2V_{dc}$ is produced by turning ON $H_2$, $H_4$ and S.
- Third positive level $3V_{dc}$ is produced by turning ON $H_2$, $H_4$ and $S_L$.
- Fourth positive level $4V_{dc}$ is produced by turning ON $H_2$, $H_4$, $S_1$, $S_3$ and S.
- Fifth positive level $5V_{dc}$ is produced by turning ON $H_2$, $H_4$, $S_1$, $S_3$ and $S_L$.
- Sixth positive level $6V_{dc}$ is produced by turning ON $H_2$, $H_4$, $S_2$ and S.
- Seventh positive level $7V_{dc}$ is produced by turning ON $H_2$, $H_4$, $S_2$ and $S_L$.
- Eighth positive level $8V_{dc}$ is produced by turning ON $H_2$, $H_4$, $S_1$, $S_2$ and S.
- Ninth positive level $9V_{dc}$ is produced by turning ON $H_2$, $H_4$, $S_1$, $S_2$ and $S_L$.
- First negative level -$V_{dc}$ is produced by turning ON $H_2$, $H_4$, $H_2$, $H_4$ and $S_R$.
- Second negative level -$2V_{dc}$ is produced by turning ON $H_2$, $H_4$ and S.
- Third negative level -$3V_{dc}$ is produced by turning ON $H_2$, $H_4$ and $S_R$.
- Fourth negative level -$4V_{dc}$ is produced by turning ON $H_2$, $H_4$, $S_1$, $S_3$ and S.
- Fifth negative level -$5V_{dc}$ is produced by turning ON $H_2$, $H_4$, $S_1$, $S_3$ and $S_R$.
- Sixth negative level -$6V_{dc}$ is produced by turning ON $H_2$, $H_4$, $S_2$ and S.
- Seventh negative level -$7V_{dc}$ is produced by turning ON $H_2$, $H_4$, $S_2$ and $S_R$.
- Eighth negative level -$8V_{dc}$ is produced by turning ON $H_2$, $H_4$, $S_1$, $S_2$ and S.
- Ninth negative level -$9V_{dc}$ is produced by turning ON $H_2$, $H_4$, $S_1$, $S_2$ and $S_R$.

## IV. PWM Strategy

The gating pulses are generated by employing Phase Opposition Disposition Pulse-Width Modulation (PODPWM). This technique minimizes the harmonics present in the output waveform. Nine triangular carrier waves of frequency 1kHz are compared to the absolute function of a sine wave at power frequency of 50 Hz. The modulation index is calculated using the following expression,

$$m = \frac{A_r}{N_c * A_C} \tag{1}$$

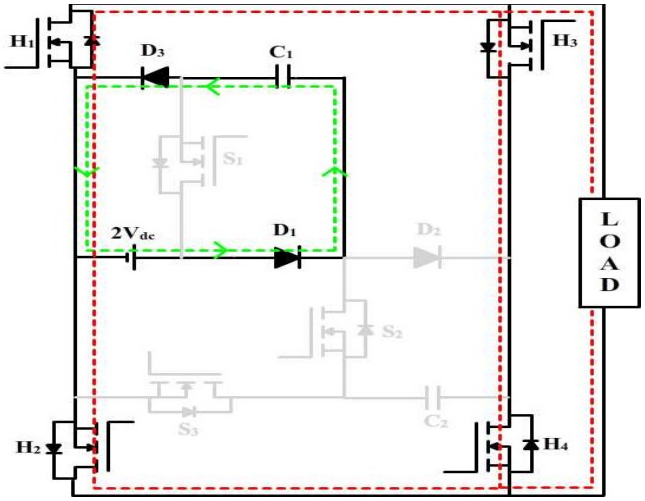


Fig. 4. Output Voltage = $0V_{dc}$

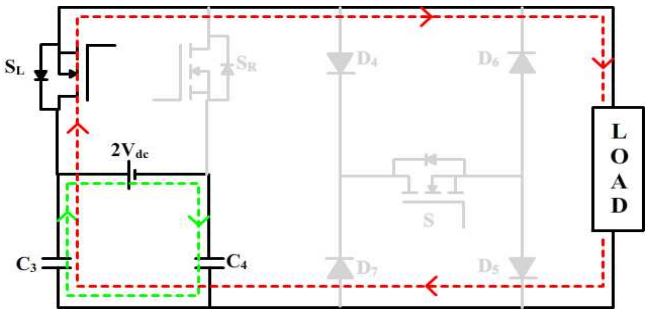


Fig. 5. Output Voltage = $1V_{dc}$

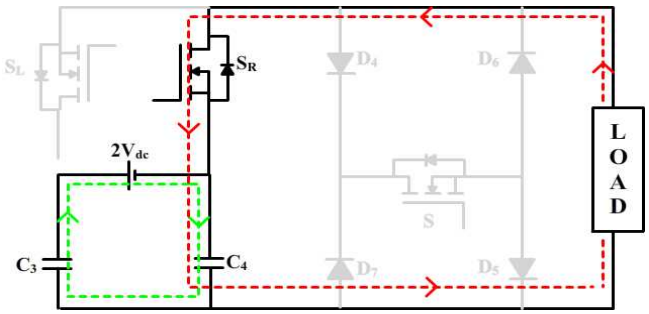


Fig. 6. Output Voltage = -$1V_{dc}$

where, m is the modulation index, $A_r$ and $A_c$ are the amplitudes of the reference and carrier waves respectively, and $N_c$ represents the number of carrier waves. A modulation index of unity has been chosen to minimize THD.

A constant CM, called the Commander Coefficient is used to select the positive and negative half of the reference signal. It is calculated using equation 2,

$$CM = \frac{(1 + sgn(V_{ref}))}{2} \tag{2}$$

where, $V_{ref} = A_r sin(wt)$.

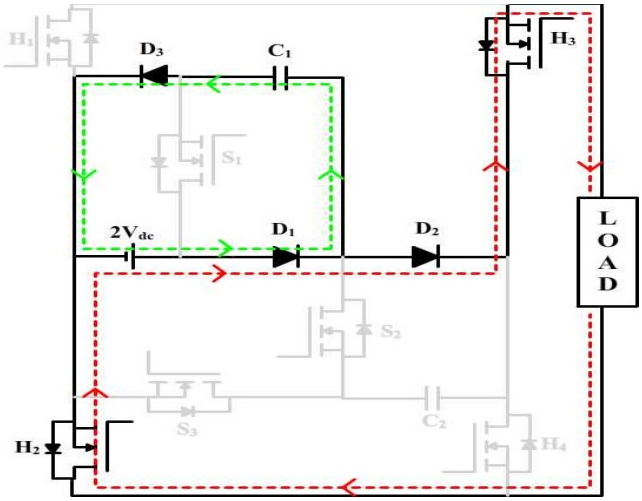


Fig. 7. Output Voltage from SC Cell = $2V_{dc}$

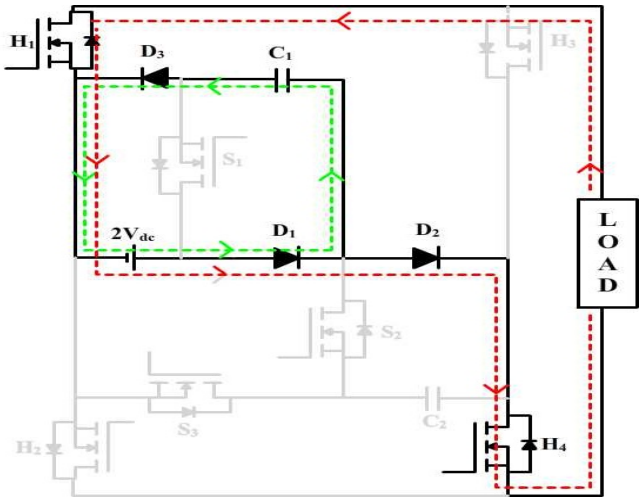


Fig. 8. Output Voltage from SC Cell = $-2V_{dc}$

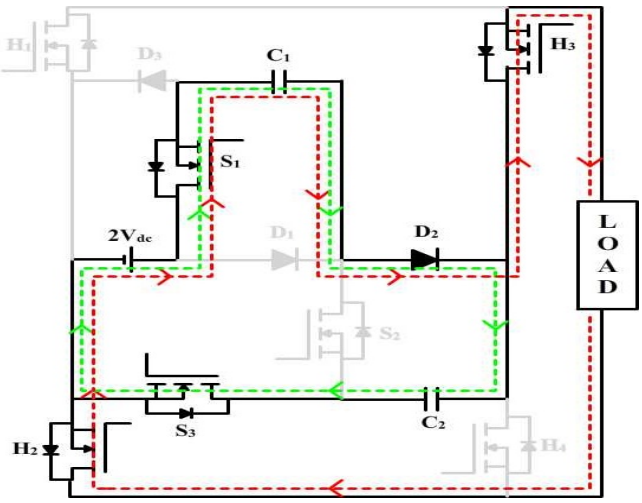


Fig. 9. Output Voltage from SC Cell = $4V_{dc}$

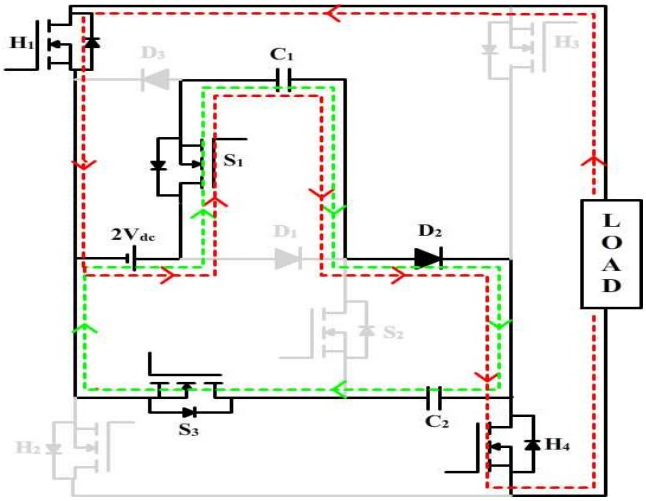


Fig. 10. Output Voltage = $-4V_{dc}$

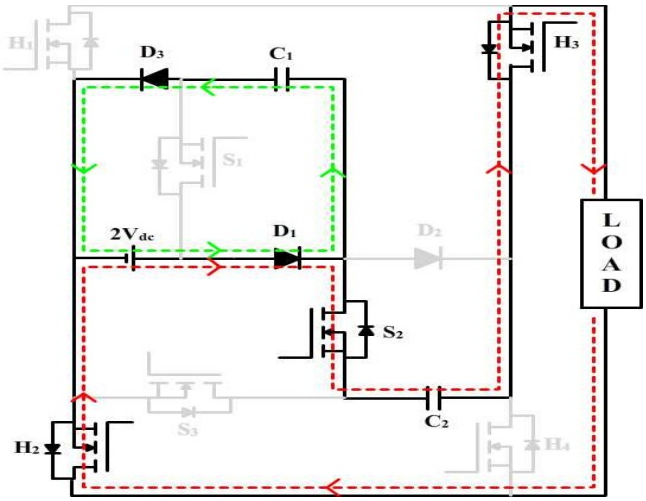


Fig. 11. Output Voltage = $6V_{dc}$

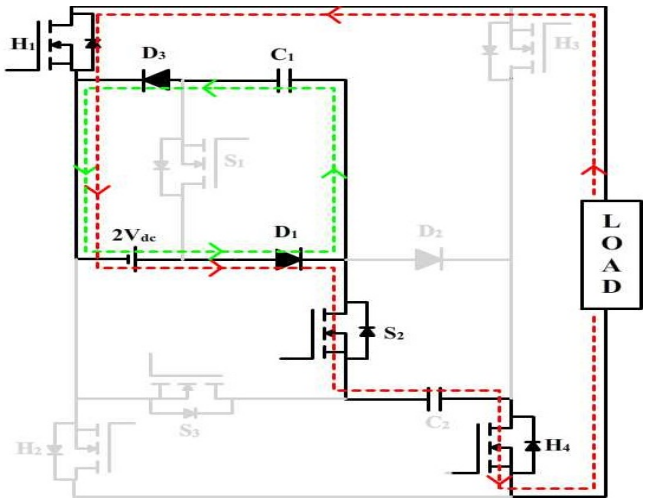


Fig. 12. Output Voltage = $-6V_{dc}$

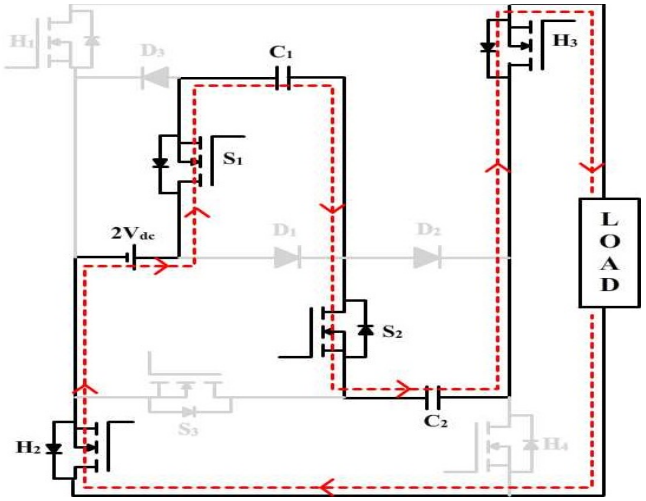


Fig. 13. Output Voltage = $8V_{dc}$

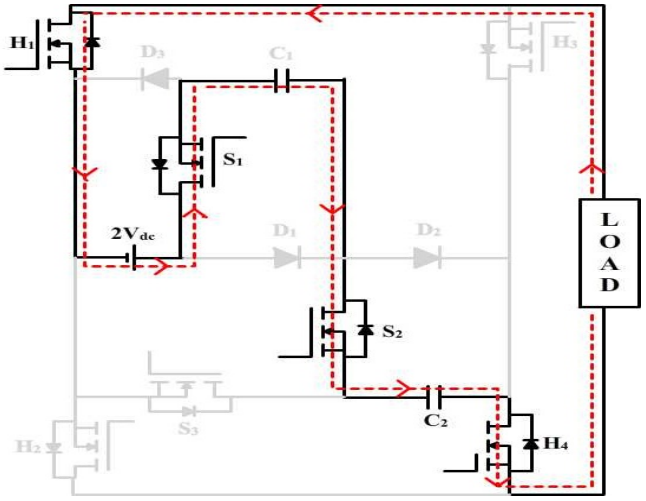


Fig. 14. Output Voltage = -$8V_{dc}$

## V. Results and Discussion

The proposed inverter module was simulated using MATLAB Simulink. The design parameters and output parameters of the proposed 19-Level MLI are as follows:

TABLE I
DESIGN PARAMETERS OF THE PROPOSED 19-LEVEL MLI

| Parameter | Value |
|---|---|
| Input DC Voltage Source in SC Cell | 100 V |
| Input DC Voltage Source in FC Cell | 100 V |
| Design Power | 500 W |
| Capacitor $C_1$ | $2000\mu F$ |
| Capacitor $C_2$ | $3000\mu F$ |
| Capacitor $C_3$ | $1000\mu F$ |
| Capacitor $C_4$ | $1000\mu F$ |

The output voltages from the Floating Capacitor circuit and Switched Capacitor circuit are shown in Figures 15 and 16 respectively. As intended, the required three-level waveform is obtained from the FC Cell and the nine-level waveform is obtained from the SC Cell. This confirms the operation of the MLI topology.

TABLE II
OUTPUT PARAMETERS OF THE PROPOSED 19-LEVEL MLI

| Parameter | Value |
|---|---|
| $V_{rms}$ | 302.9 V |
| $I_{rms}$ | 1.59 A |
| Output Power | 481.61 W |

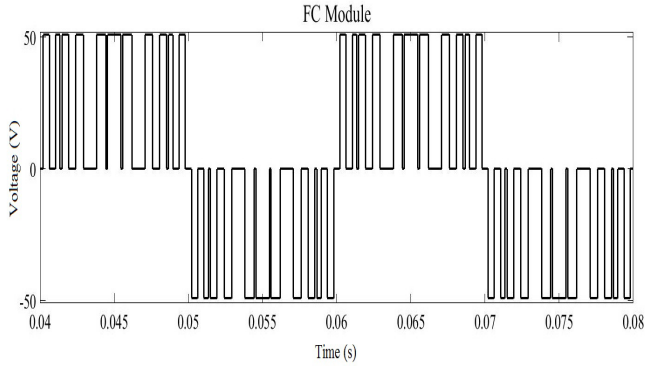


Fig. 15. Output Voltage from Floating Capacitor Cell

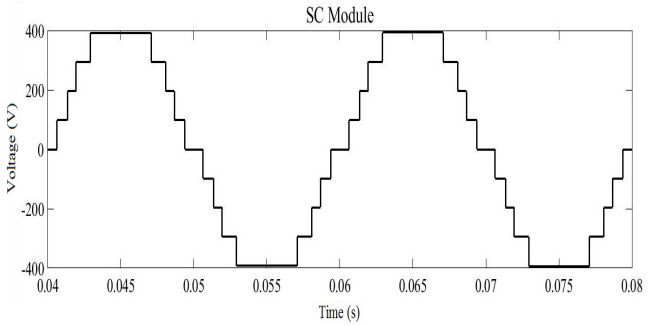


Fig. 16. Output Voltage from Switched Capacitor Cell

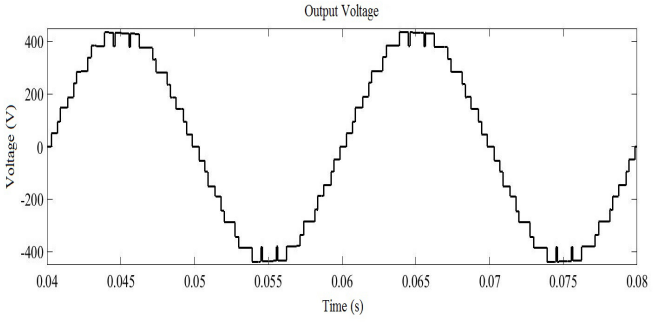


Fig. 17. Output Voltage of the proposed inverter module

Figure 17 depicts the output voltage waveform across the load. The designed 19-level output is obtained with a boost in the output voltage and it can be seen that the waveform is nearly equivalent to that of a sine wave. Figure 18 depicts the load current waveform of the proposed inverter module.

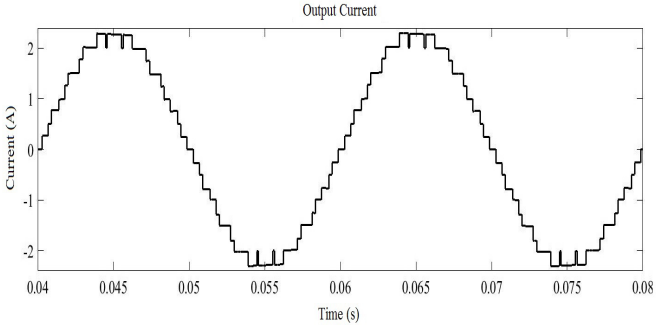


Fig. 18. Output Current of the proposed inverter module

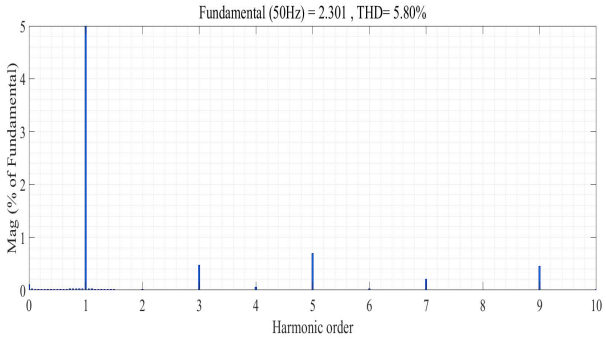


Fig. 19. FFT analysis of the Output Current

FFT analysis was performed on the load current and the result obtained is shown in Figure 19. THD of the load current was found to be 5.80 % .

The harmonics closest to the fundamental are the components which affect the output of the inverters. By optimizing the modulation index, the output harmonic profile has been modified to reduce the $3^{rd}$ harmonic and its multiples, while also producing an overall minimized THD. The third harmonic component of the output current of the proposed inverter was found to be 0.47%. Thus, the harmonic distribution can be changed by modifying the modulation index according to the needs of the load.

## VI. Conclusion

An improved topology of switched capacitor-based boost MLI has been proposed. Quantitative improvement is achieved using reduced number of semiconductor devices. Qualitative improvement is achieved by reducing the THD to 5.80 %. The theoretical waveform and the simulated outputs are similar to each other. The advantages of this topology is that it has reduced number of semiconductor devices. The PODPWM scheme employed results in a simpler control design and voltage balancing of capacitors can be achieved, without the use of external circuits.

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