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Switched Capacitor based Multilevel Inverter for Smart Grid Applications

Raghuram S
(EEE/SEEE)
119005096

Girish Ganesan R
(AP-II/SEEE)

Motivation & Objective

Motivation

- 80% electrical loads – Induction motors – AC supply
- Enhance the efficiency – Reduction in harmonics

Objective

- To design an inverter that offers lower blocking voltage rating across the switches & low Total Harmonic Distortion (THD)
- To increase the output voltage levels to improve quality of output voltage
- To reduce switching losses using low switching frequency

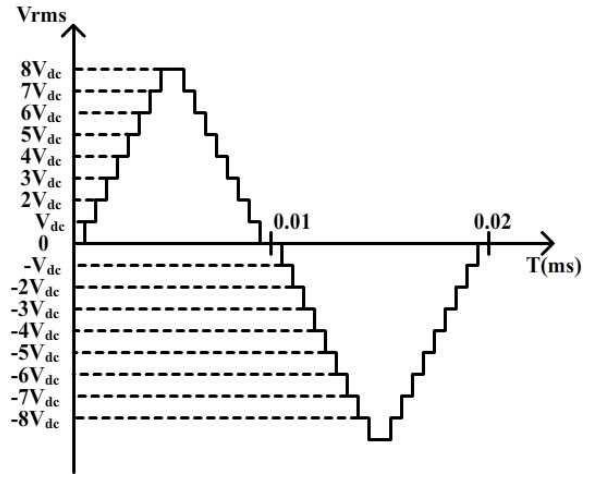


Fig. 1 Multilevel Inverter output waveform

Fig. 2 Fundamental and its harmonics

Block Diagram of Base Circuit

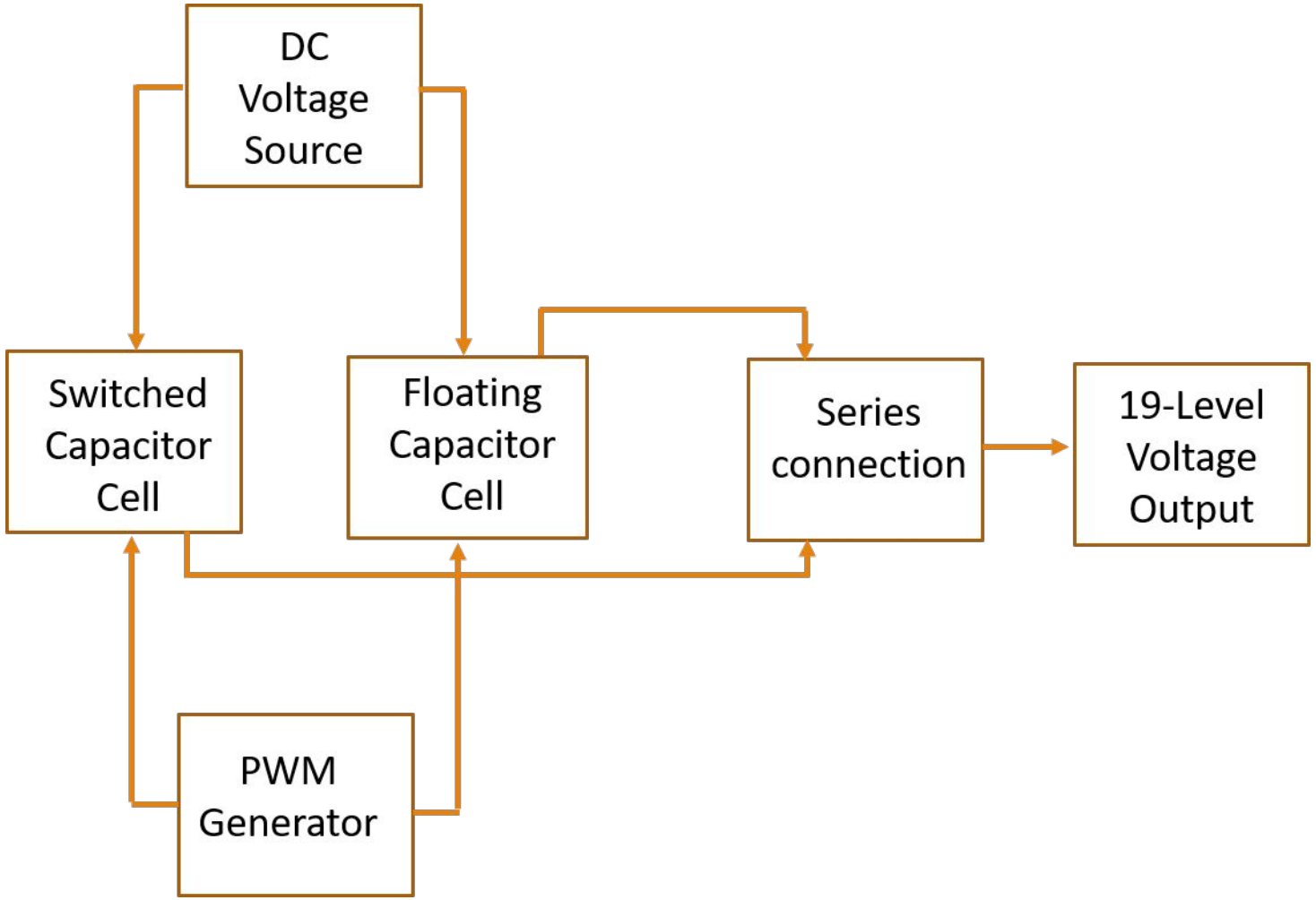
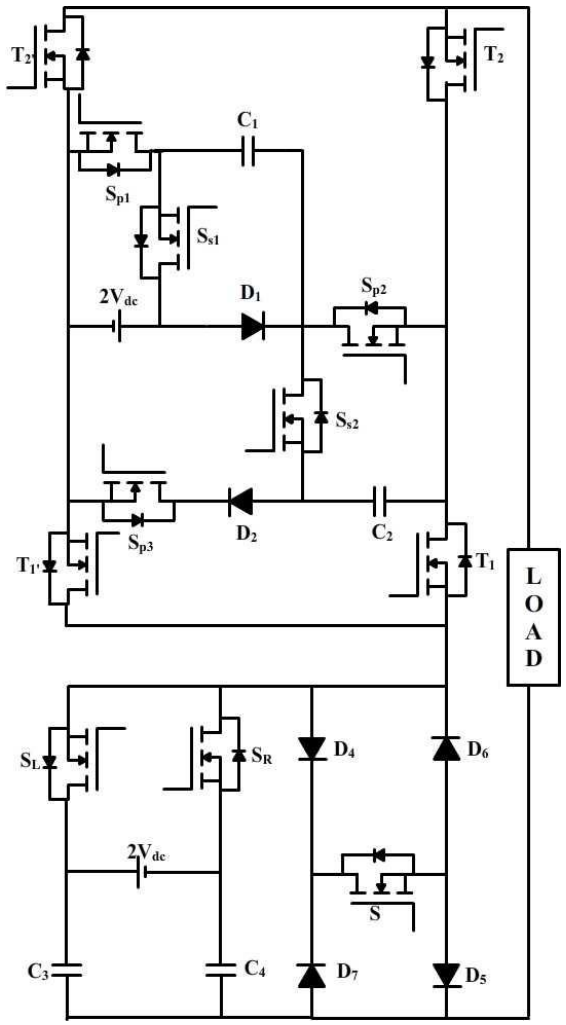


Fig. 3 Block Diagram of base circuit

Base Circuit Operation



- 12 switches, 6 diodes, 4 capacitors, 2 DC voltage sources
- FCB cell switches – high switching frequency
- SC cell switches – low switching frequency
- 19 – level output voltage waveform at 0.95 modulation index

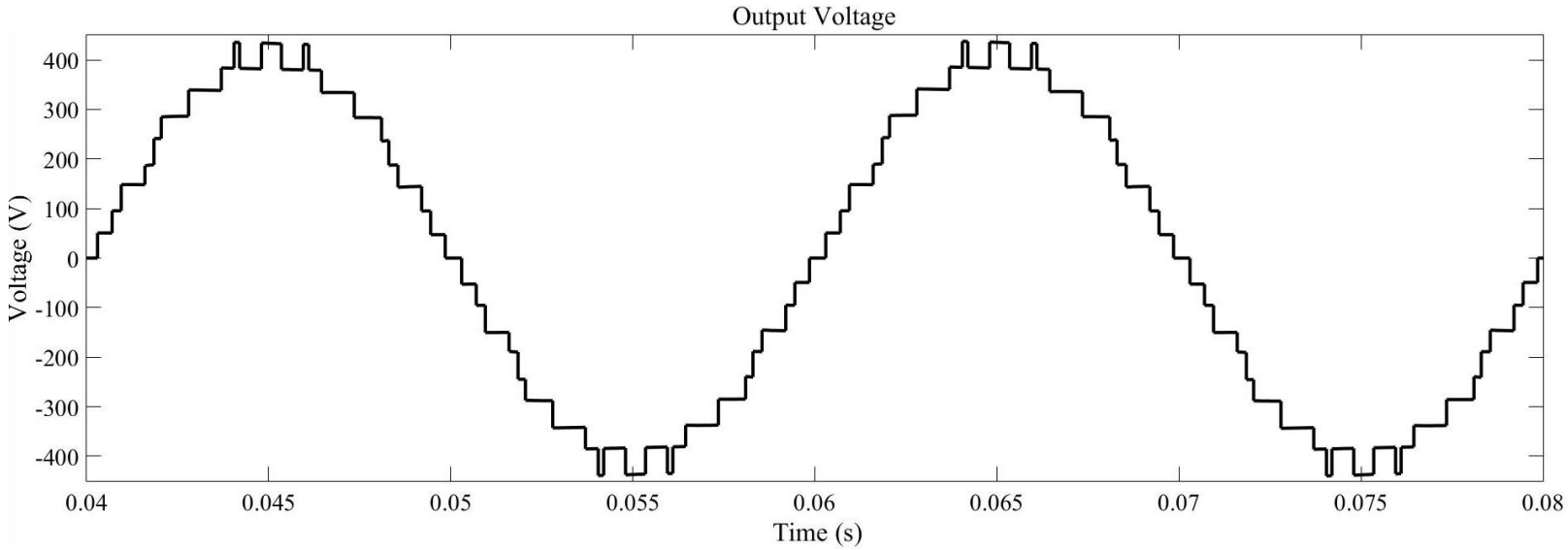


Fig. 4 Circuit Diagram of base circuit

Fig. 5 Output Voltage waveform of base circuit

Novel Topology 1

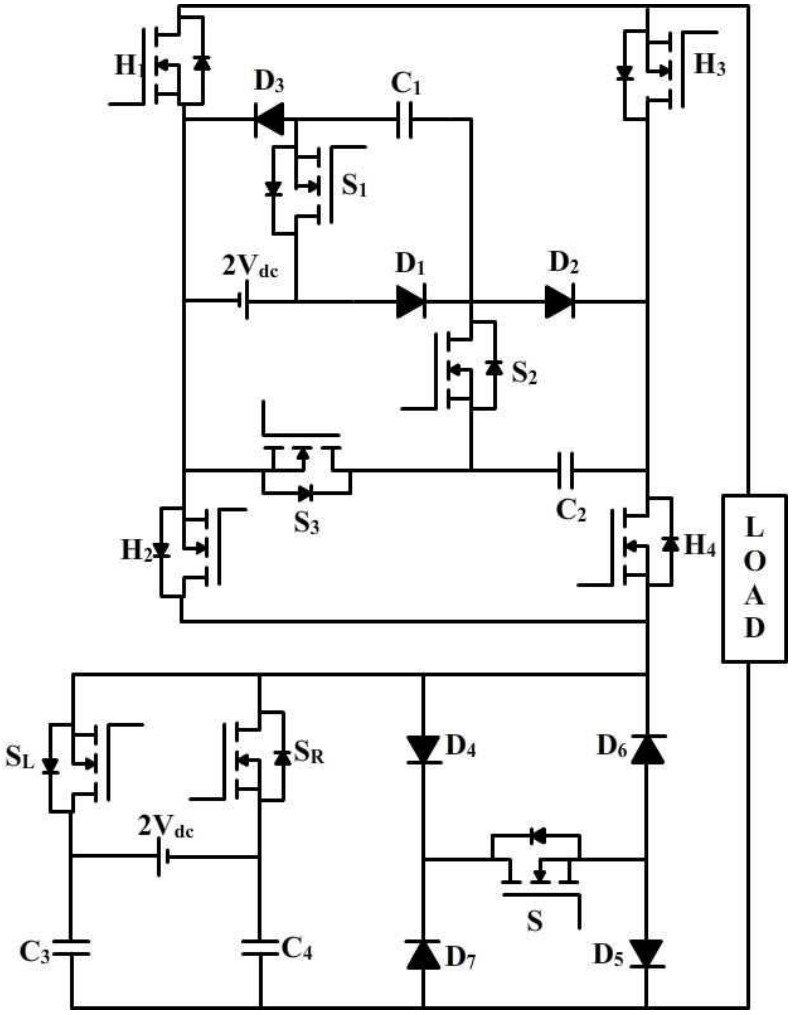


Fig. 6 Novel Topology 1 power circuit

- 10 switches, 7 diodes, 4 capacitors, 2 DC voltage sources
- Removed 2 switches from base circuit
- Reduced circuit complexity, conduction losses and number of gate drivers required
- Optimized FC cell operation - reduced switching losses
- Produces 19-level output waveform at unity modulation index
- Modulation index can be changed as per needs of the load

Novel Topology 1 Operation

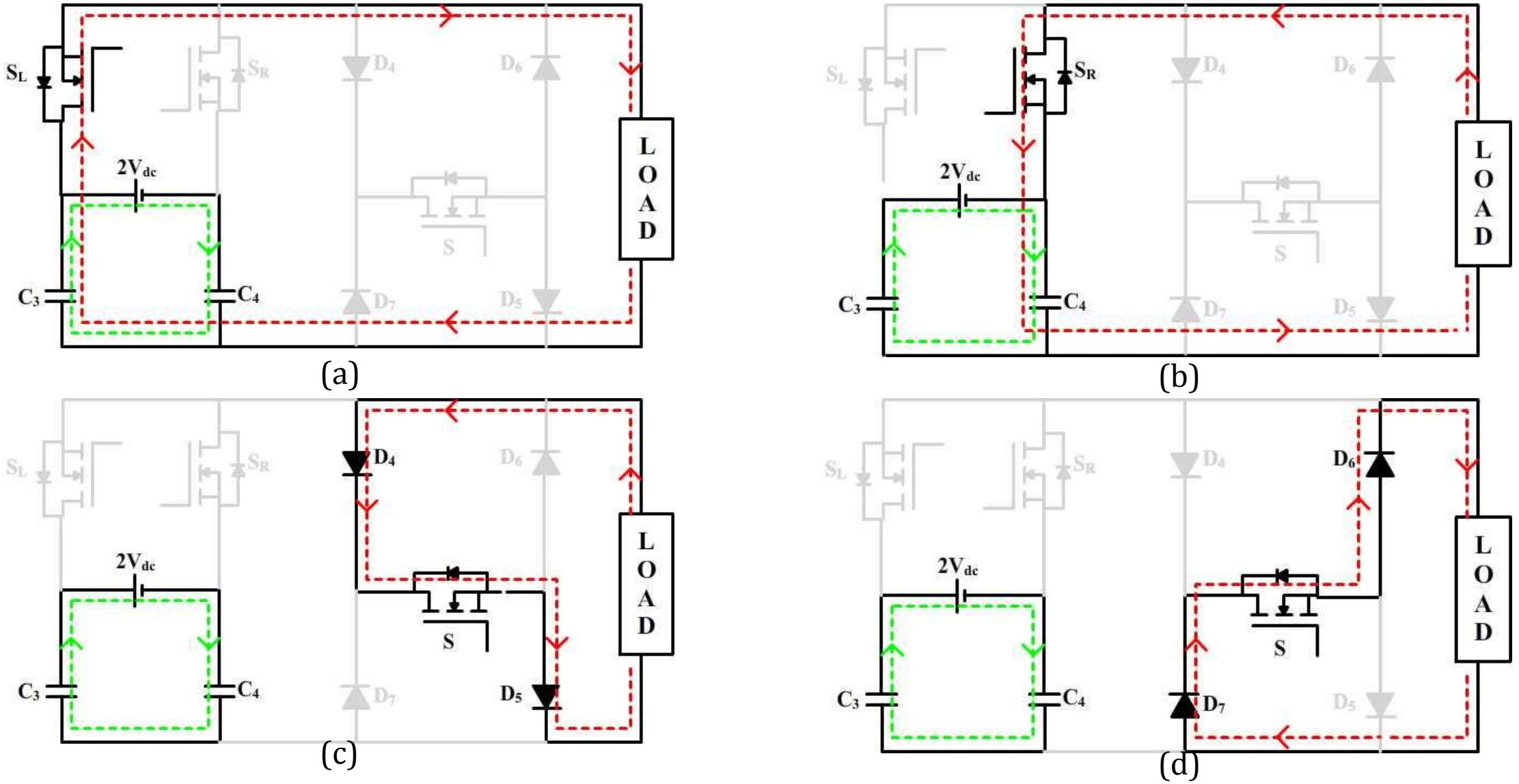
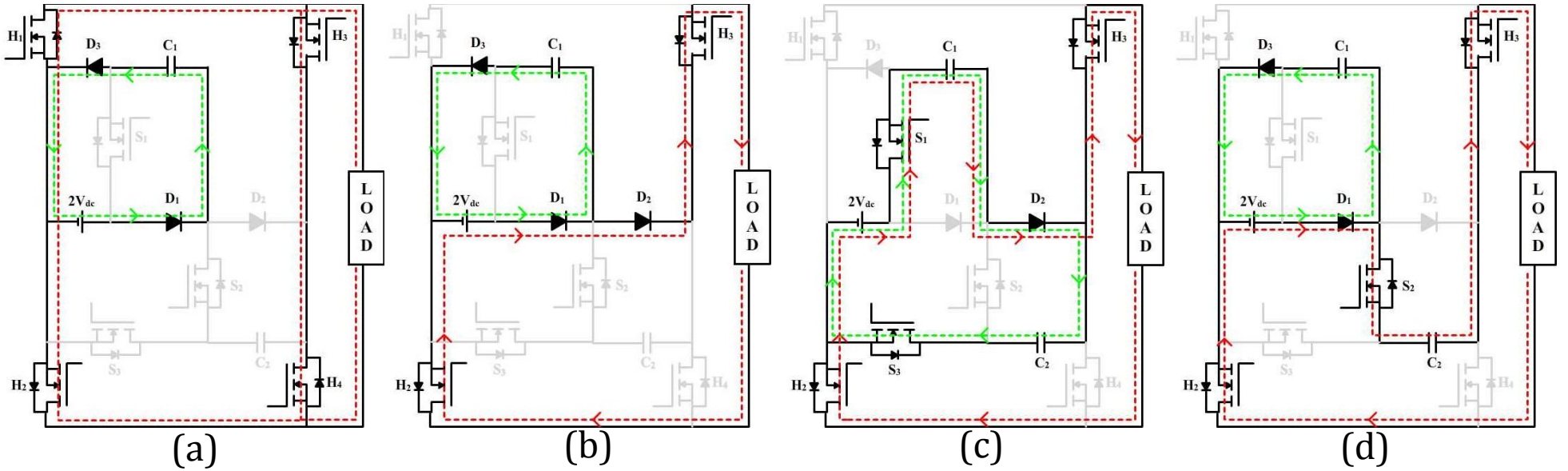


Fig. 7 NT1 FC Circuit Operation (a) $+V_{dc}$ (b) $-V_{dc}$ (c) & (d) Zero

Novel Topology 1 Operation



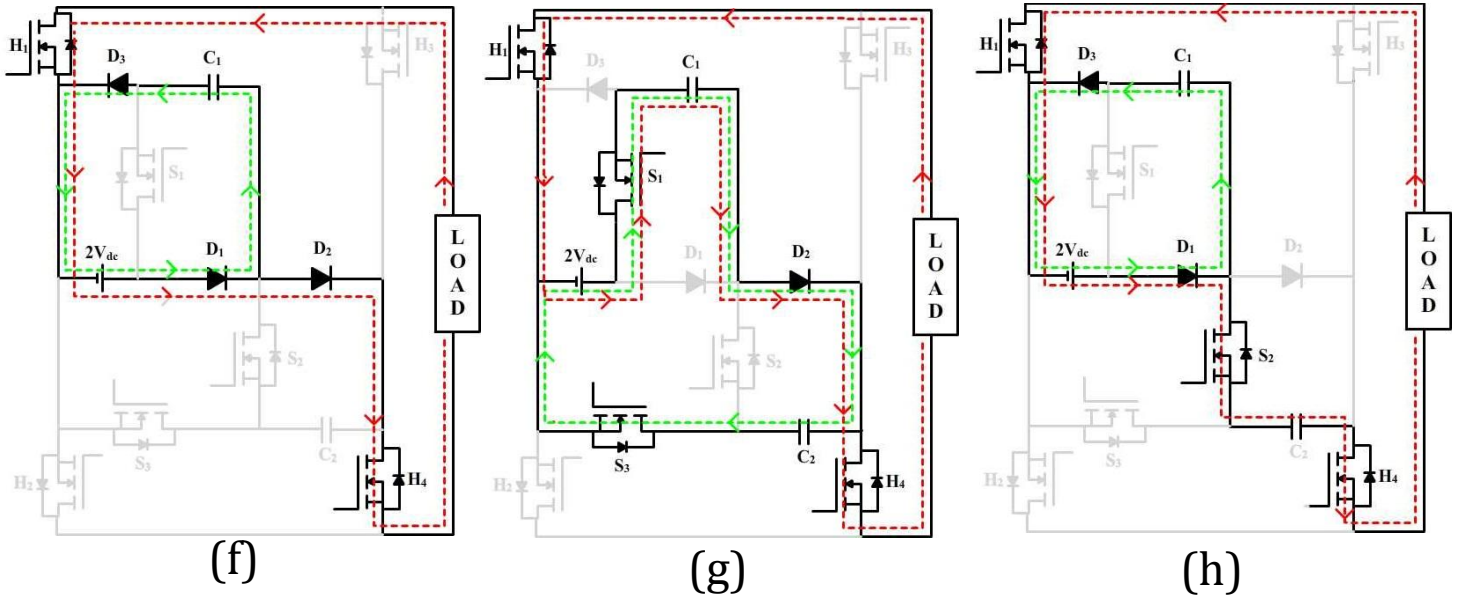


Fig. 8 NT1 SC Circuit Operation
(a) Zero
(b) $+2V_{dc}$ (c) $+4V_{dc}$
(d) $+6V_{dc}$ (e) $+8V_{dc}$
(f) $-2V_{dc}$ (g) $-4V_{dc}$
(h) $-6V_{dc}$ (i) $-8V_{dc}$

Novel Topology 1 Operation

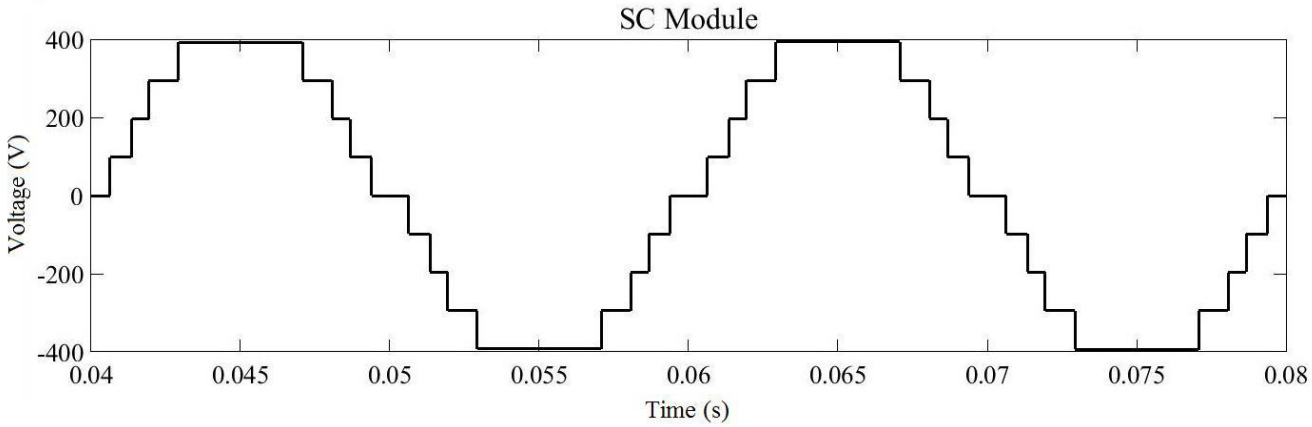


Fig. 9 SC Module Output Voltage

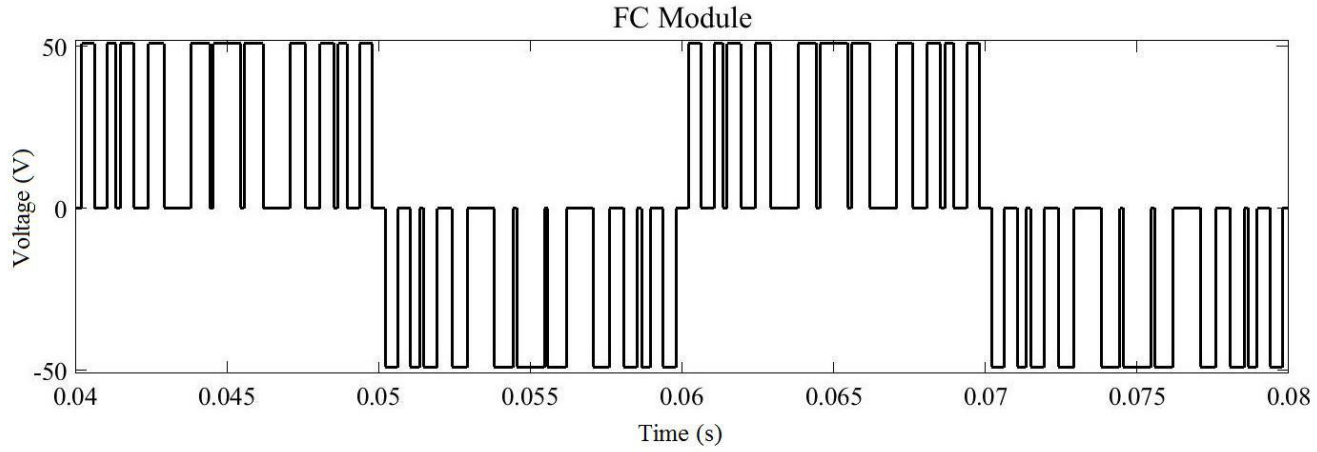


Fig. 10 FC Module Output Voltage

Novel Topology 1 Output

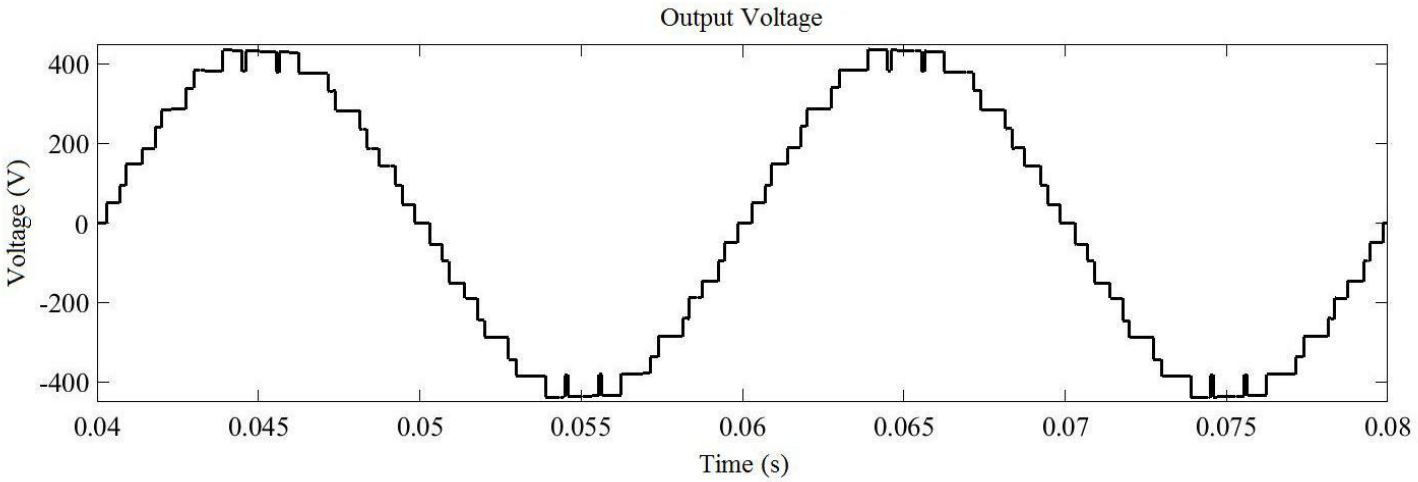


Fig. 11 Output voltage waveform

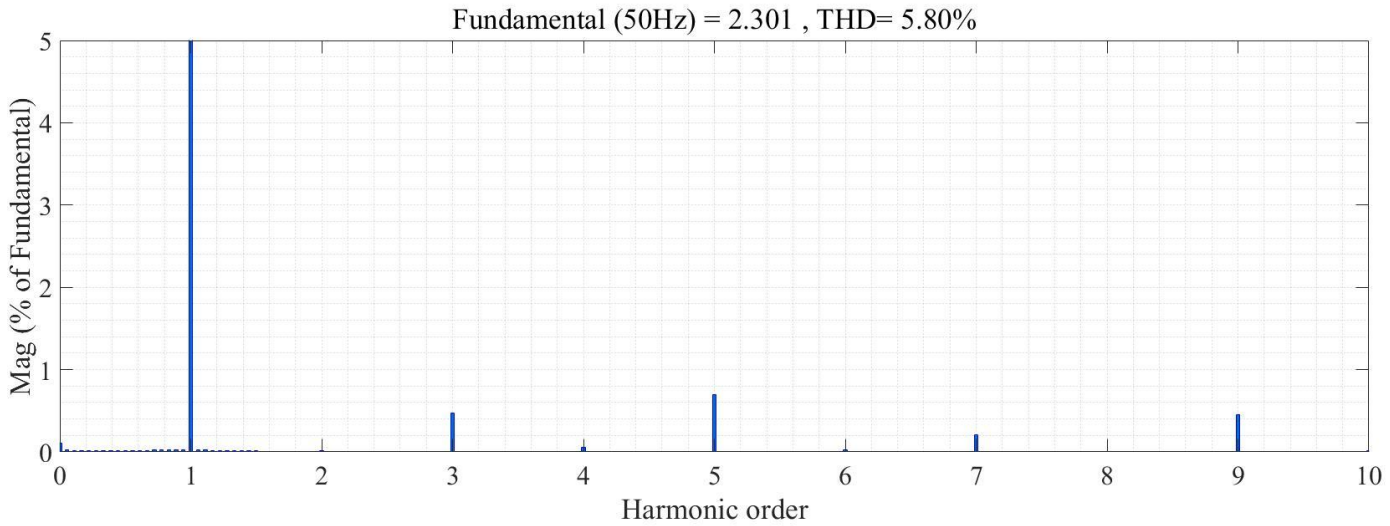


Fig. 12 Output current harmonic profile

Novel Topology 2

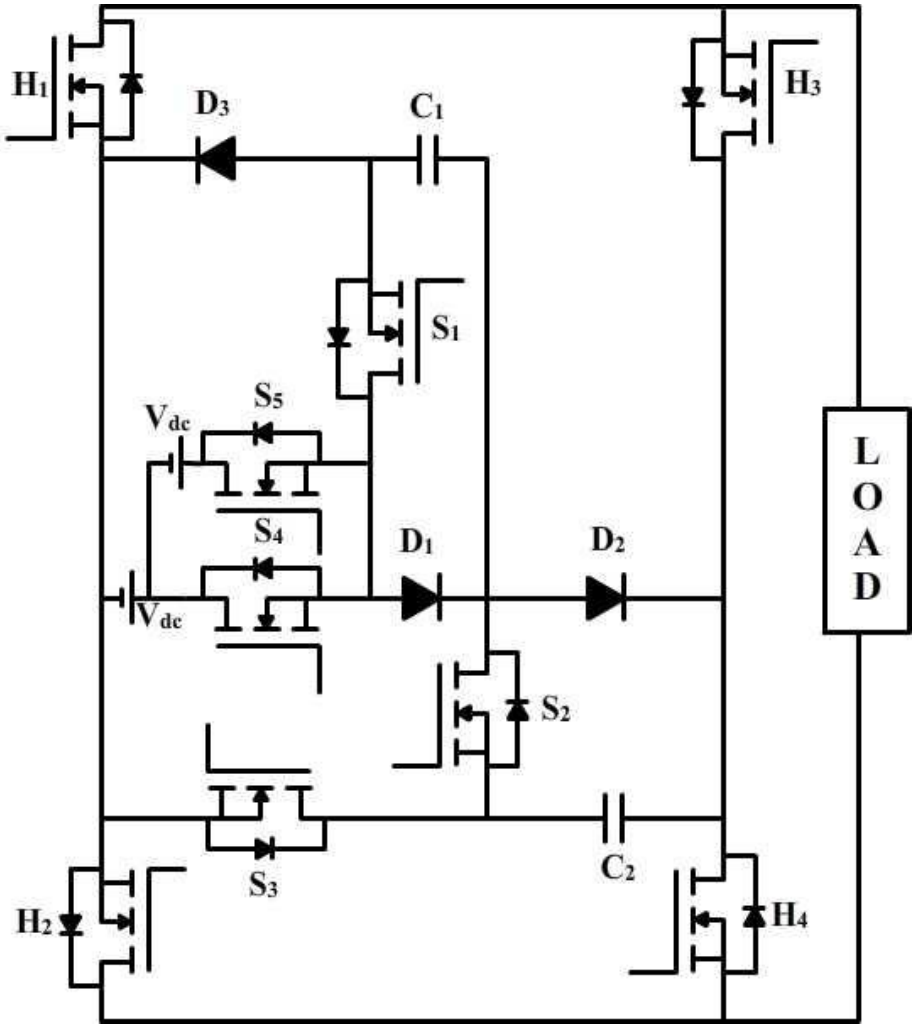


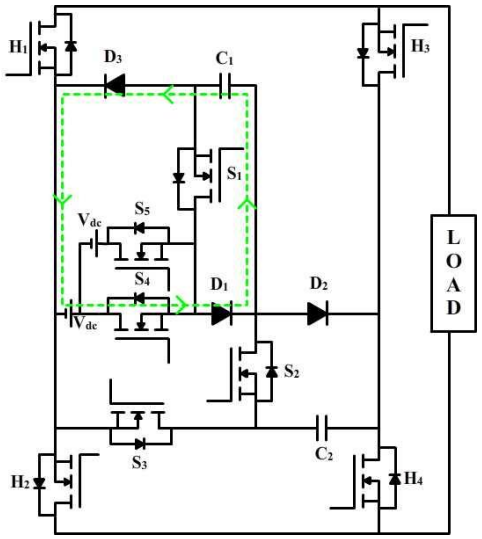
Fig. 13 Novel Topology 2 power circuit

- 9 switches, 7 diodes, 2 capacitors, 2 DC voltage sources
- Removed 3 switches, 2 capacitors from base circuit
- Reduced conduction losses and number of gate drivers 2

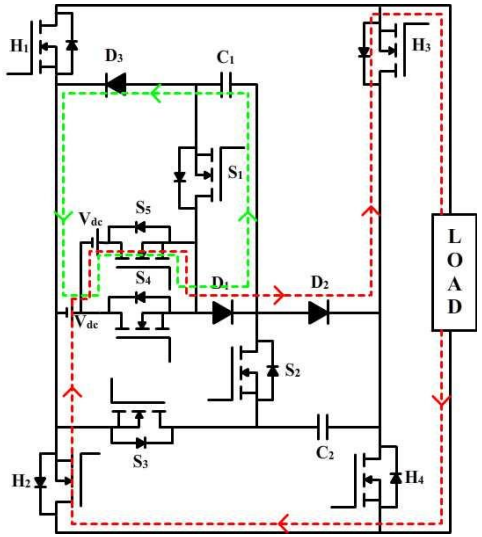
  modes of operation:
  - Mode 1: S_4 is ON and S_5 is OFF
  - Mode 2: S_5 is ON and S_4 is OFF
- Only 2 high frequency switches - reduced switching

  losses
- Produces 17-level output waveform at unity MI
- Modulation index can be changed as per needs of the load

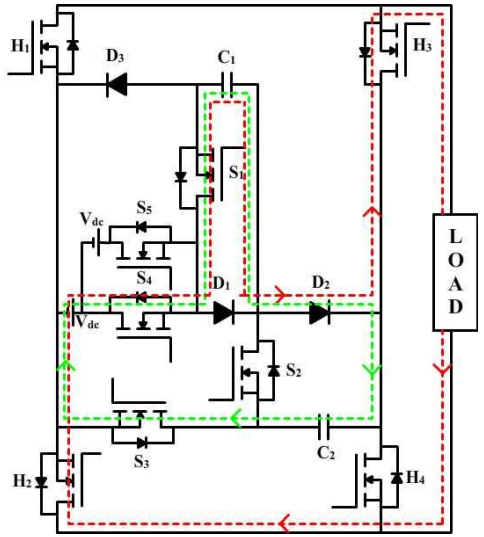
Novel Topology 2 Operation



(a)



(b)



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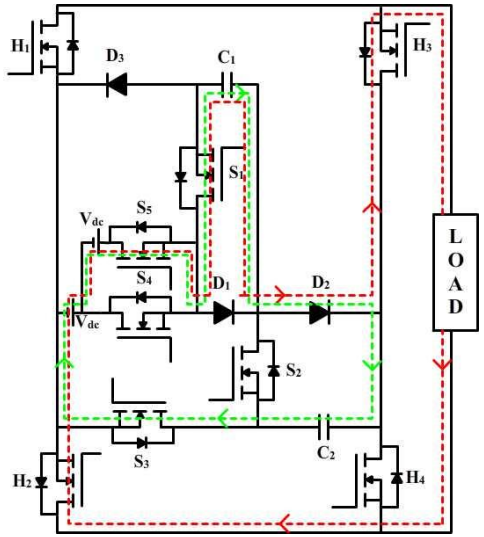
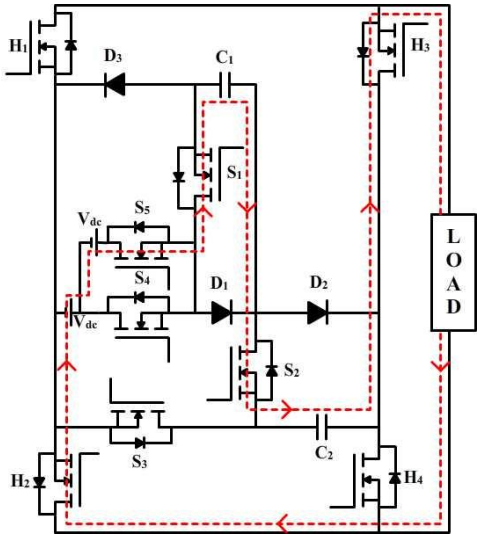
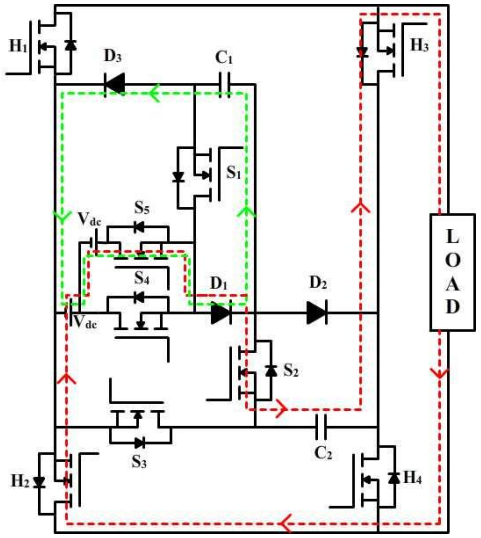


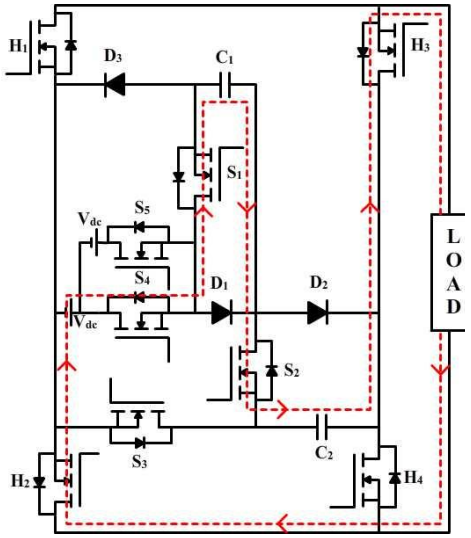
(d)



(e)



(f)



(g)

(h)

(i)

Fig. 14 NT2 Circuit Operation
(a) Zero
(b) $+V_{dc}$ (c) $+2V_{dc}$
(d) $+3V_{dc}$ (e) $+4V_{dc}$
(f) $+5V_{dc}$ (g) $+6V_{dc}$
(h) $+7V_{dc}$ (i) $+8V_{dc}$

Novel Topology 2 Operation

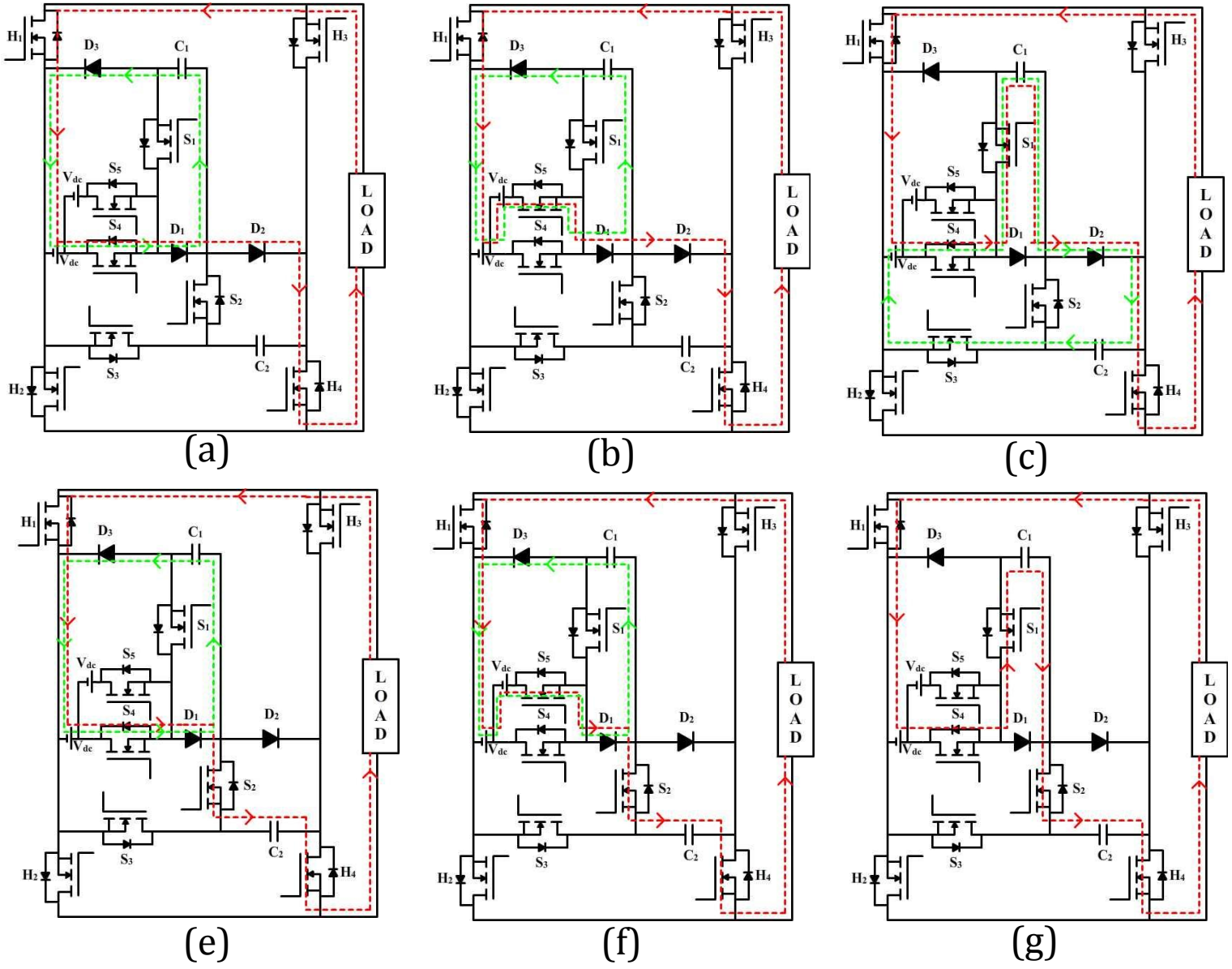


Fig. 15 NT2 Circuit Operation
(a) -V_{dc} (b) -$2V_{dc}$
(c) -$3V_{dc}$ (d) -$4V_{dc}$
(e) -$5V_{dc}$ (f) -$6V_{dc}$
(g) -$7V_{dc}$ (h) -$8V_{dc}$

Novel Topology 2 Output

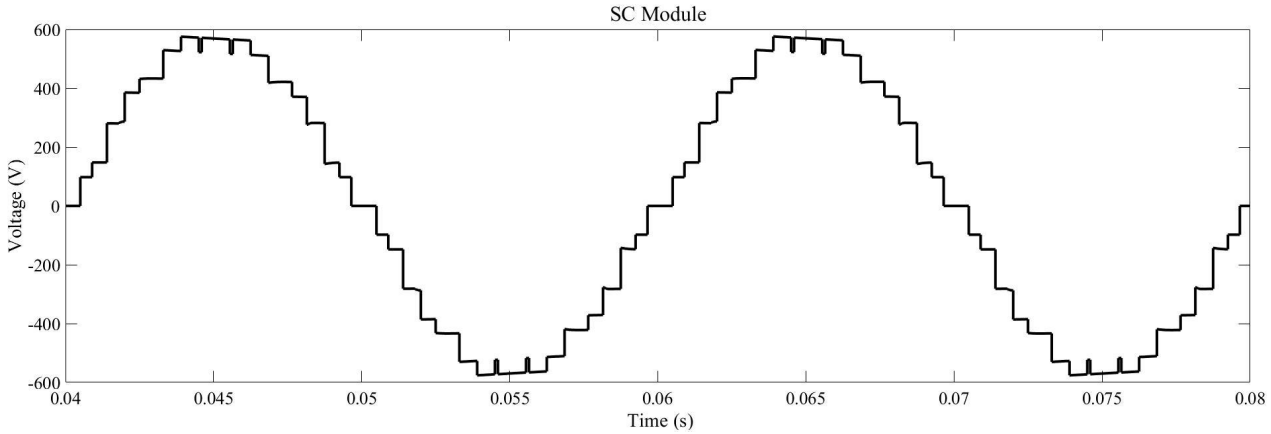


Fig. 16 Output voltage waveform

Fig. 17 Output current harmonic profile

References

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3. **Barzegarkhoo, R., Zamiri, E., Moradzadeh, M., & Shadabi, H.** (2017). Symmetric hybridised design for a novel step-up 19-level inverter. IET Power Electronics, 10(11), 1377- 1391
4. **Barzegarkhoo, R., Zamiri, E., Vosoughi, N., Kojabadi, H. M., & Chang, L.** (2016). Cascaded multilevel inverter using series connection of novel capacitor-based units with minimum switch count. IET Power Electronics, 9(10), 2060-2075
5. **Hosseinzadeh, M. A., Sarbanzadeh, M., Sarbanzadeh, E., Rivera, M., Babaei, E., & Muñoz, J.** (2017, December). Cascaded multilevel inverter based on new sub-module inverter with reduced number of switching devices. In 2017 IEEE Southern Power Electronics Conference (SPEC) (pp. 1-6)

Thank you!