

Transistor:

- It is a solid state device whose operation depends upon the flow of electric charge carriers within the solid.
- It transfers the input signal from one resistance circuit to other so it is called transfer - Resistor or transistor.
- The transistors are the current device that may be current or voltage controlled.
- It can be used as amplifier or as switch.
- It has two types:
 - i) Bi-polar Junction Transistor (BJT)
 - ii) Field Effect Transistor (FET)

i) Bi-Polar Junction Transistor: (BJT)

- It is a three-layer, three-terminal semi-conductor device which consists of both electrons and holes as charge carriers.
- It is commonly used for amplifying and switching electrical currents in circuits. A junction transistor is

simply a sandwich which of one type of semiconductor material between two layers of other types. It has two P-N junction.

→ It is named as bipolar as both majority and minority carriers take part in current flow. It has three terminals.

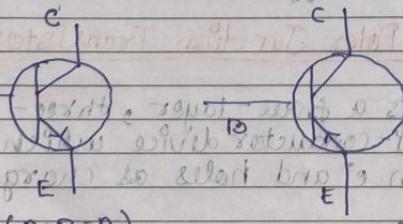
→ BJT is classified into two types

- ① NPN
- ② PNP

→ It has three terminals:

- Emitter
- Base
- Collector

→ Symbol of BJT;



(n-p-n)

The arrow indicates the direction of conventional current flow which is

opposite of electron flow and same as hole flow.

Generally, n-p-n transistor is widely used because e- have greater mobility than holes.

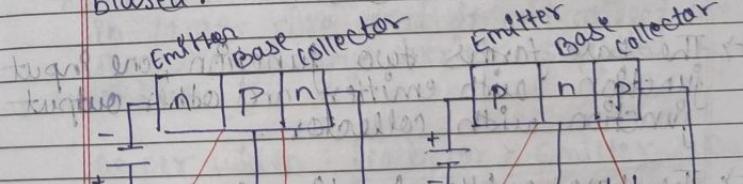
Transistor terminal

→ Every transistor has three terminal called emitter, collector and base.

→ It has two junctions.

Emitter-Base is known as Input junction and Collector-Base is known as Output junction

Generally, Input junction is forward biased and output junction is reverse biased.



Forward biased
Reverse biased
Forward biased
Reverse biased
Forward biased
Reverse biased

Emitter

- The section on one side of BJT that supplies large no. of majority carriers is called emitter.
- The emitter is always forward biased with respect to base so that it can supply a large no. of majority carriers to P-N junction, with the base.
- Since emitter is to supply and inject a large amount of majority carriers into base, it is heavily doped and moderate in size.

Base

- The middle section between emitter and collector is called Base.
- The base forms two junction, one input junction with emitter and other output junction with collector.
- The base-emitter junction is forward biased (providing low resistance for the emitter circuit). The base-collector junction is reverse biased (high resistance path to collector circuit).
- The base is lightly doped and very thin.

so it can help to pass majority carriers from emitter to collector.

Collector

- The section on the other side of the bi-polar transistor (BJT) that collects major portion of the majority carriers supplied by the emitter is called collector.

The collector-base junction is reverse biased.

- Its main function is to remove majority charge carriers from its junction with base.

- The collector is moderately doped but in larger size that it can collect most of the majority carriers supplied by the emitter.

As per width : collector > Emitter > Base

As per doping : Emitter > collector > base

Transistor Current: It is the sum of collector current and base current.

$$I_E = I_B + I_C \quad \text{where, } I_E : \text{Emitter current}$$

I_B : Base current

I_C : Collector current

Also, $I_C = I_{C\text{major}} + I_{C\text{min}}$

The minority collector current ($I_{C\text{min}}$) is due to reverse biasing between collector and base junction.

The minority current is also known as collector leakage current.

$$\text{So, } I_{C\text{min}} = I_C_0$$

→ BJT is used as an amplifier and as a switch also.

Application of BJT:

- Switch
- Amplifier

Transistor Configuration

→ Transistor has three terminals but we need four terminals as two for input and two for output for connecting a two port network. So one of the terminal (either emitter, base, collector) is made common to input as well as output of the network.

So there are three types of transistor configuration

- Common Emitter (CE) configuration
- Common Base (CB) configuration
- Common Collector (CC) configuration

Characteristics of Transistor Configuration:

There are two types:

- Input characteristics
- Output characteristics
- Input characteristics

This graph is plotted in between input voltage and input current at constant output voltage. Though input junction is forward biased. The input characteristics is similar with diode characteristics.

→ The characteristics is used to determine the input impedance of transistor.

ii) Output characteristics

→ This graph is plotted in between output voltage and output current at constant input current. (forward biasing)

→ There are three regions of transistor operation in output characteristic curve.

a) Active region:

This is the region where input junction is forward biased and output junction is reverse biased.

Here transistor is used as amplifier.

b) Saturation Region:

Here both the junction are forward biased.

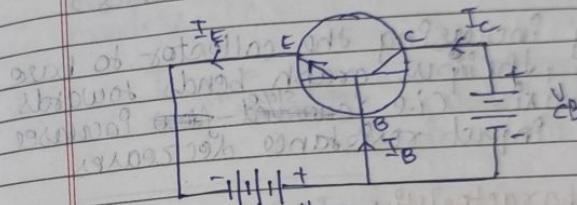
Here transistor is used as closed switch.

c) Cutoff Region

This is the region where both junction are reverse biased.

Here transistor is used as open switch.

Common Base Configuration

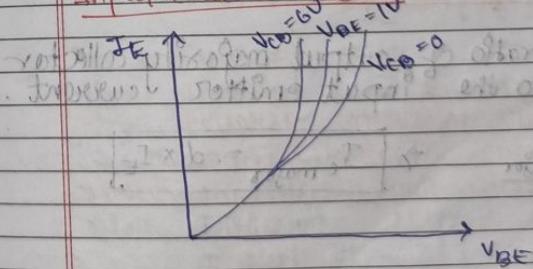


→ In CB config, input is connected in between emitter and base and output is connected in between collector and base.

where, $I_E \rightarrow$ Input current
 $V_{BE} \rightarrow$ Input voltage

$I_C \rightarrow$ Output current
 $V_{CO} \rightarrow$ Output voltage

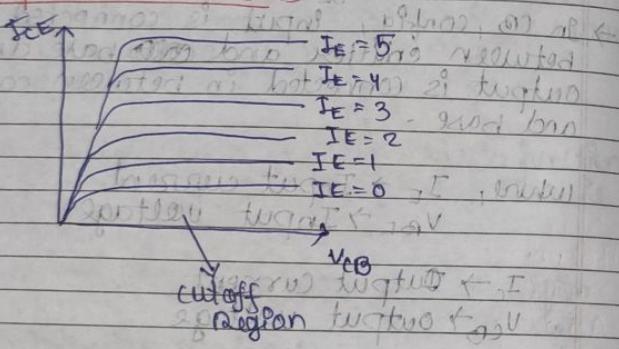
Input characteristics



Here with increase in V_{BE} then I_E will also increases. (Diode characteristics)

Here by increasing the collector to base voltage, the input graph bends towards current axis - (i.e. ~~current~~ ^{slope} increases) (i.e. Input resistance decreases).

Output characteristics



Current Amplification factor (α)

→ It is the ratio of output majority collector current to the input emitter current.

$$\rightarrow \alpha = \frac{I_c}{I_E} \Rightarrow I_c = \alpha \times I_E$$

Due to output junction is reverse biased there is some flow of minority current carriers.

$$I_{min} = I_{CBO} \quad (\because \text{collector - Base minority current when emitter is open})$$

$$I_c = I_{CBO} + \alpha \times I_E$$

a) In a transistor operating in active region, collector current = 6.4 mA and $I_E = 6.6 \text{ mA}$. Compute value of $\alpha = ?$ (neglect I_{CBO})

$$\text{Given } I_c = 6.4 \text{ mA}$$

$$\text{and } I_E = 6.6 \text{ mA}$$

$$\text{As we know, } \alpha = \frac{I_c}{I_E} = \frac{6.4}{6.6} = 0.96$$

b) The current gain n-p-n transistor, $\alpha = 0.98$. It is connected in CB configuration and gives reverse saturation current. Find the base and collector current for an emitter current of 2 mA, where $I_{CBO} = 10 \text{ mA}$. Given, $I_E = 2 \text{ mA}$, $I_C = ?$, $I_B = ?$, $\alpha = 0.98$

$$I_c = \alpha I_E + I_{c0}$$

$$= (0.98 \times 2 + 10 \times 10^{-3}) \text{ mA}$$

$$\boxed{I_c = 1.97 \text{ mA}}$$

$$I_B - I_E - I_c = 2 - 1.97 = 0.03 \text{ mA}$$

$$\boxed{I_B = 0.03 \text{ mA}}$$

Common Base (Dynamic Input Resistance)

Dynamic Input Resistance for a common base configuration transistor is the ratio $\frac{\Delta V_{BE}}{\Delta I_E}$: change in emitter voltage / change in emitter current

$$R_i = \Delta V_{BE}$$

$$\Delta I_E = 0.03 \text{ mA}$$

- (Q) A transistor is connected in CB configuration when emitter voltage is changed (by) 200 mV. The emitter current is changed by 5 mA. Calculate R_i at constant I_{c0} .

$$R_i = \frac{\Delta V_{BE}}{\Delta I_E} = 200 \approx 40 \text{ k}\Omega$$

$$\Delta I_E @ 5$$

- (Q) The current gain of an n-p-n transistor $\alpha = 0.98$. It is connected in CB config. and gives reverse saturation current $I_{c0} = 10 \mu\text{A}$. Find the base and collector

same

PAGE NO.:
DATE:

PAGE NO.:
DATE:

(Q) The reverse saturation current for an n-p-n transistor in CB is 10^{-5} A . For an emitter current of 2 mA, collector current is 1.97 mA . Determine the current gain and base current.

$$I_E = 2 \text{ mA}, I_c = 1.97 \text{ mA}, I_{c0} = 10^{-5} \text{ A} = 0.0125 \text{ mA}$$

$$\therefore I_c = \alpha I_E + I_{c0}$$

$$\Rightarrow \alpha = \frac{I_c - I_{c0}}{I_E} = \frac{1.97 - 0.0125}{2} = 0.979$$

$$I_B = I_E - I_c = 2 - 1.97 = 0.03 \text{ mA}$$

- (Q) In a grounded base config., the voltage drop across $4 \text{ k}\Omega$ is 3 V. Determine the base current when $\alpha = 0.96$.

Load resistance = $4 \text{ k}\Omega$

Voltage drop across load resistance

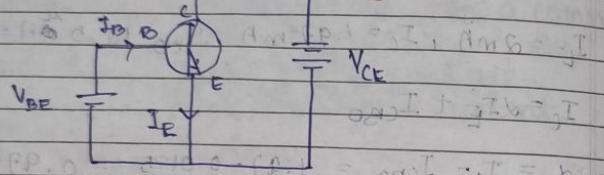
$$I_c R_L = 3 \text{ V}$$

$$\text{Collector Current } (I_c) = \frac{I_c R_L}{R_L} = \frac{3}{4} = 0.75 \text{ mA}$$

$$\text{Emitter current } (I_E) = \frac{I_C}{\alpha} = \frac{0.75}{0.96} = 0.78 \text{ mA}$$

$$\text{Base current } (I_B) = I_E - I_C = 0.78 - 0.75 = 0.03 \text{ mA}$$

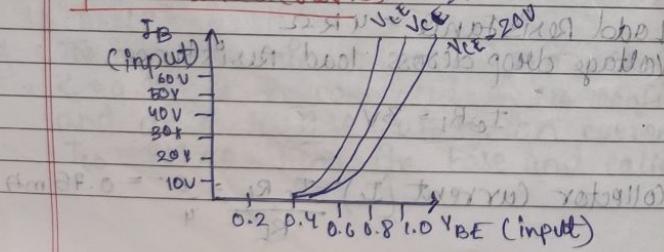
Common Emitter Configuration:



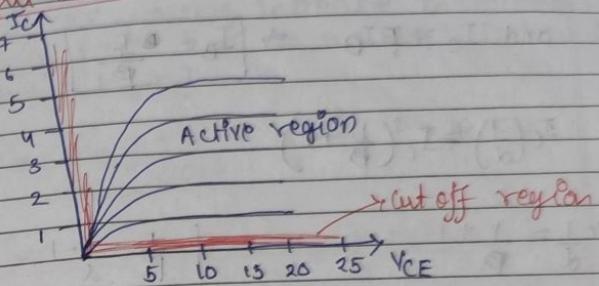
In Common Emitter configuration, Input is given at Base with respect to emitter and output is collected at collector w.r.t emitter.

so, emitter is common to both Input as well as Output that's why it is called common emitter.

Input Characteristics



Output characteristics



Common Amplification Factor (β)

It is the ratio of majority collector current to the input base current.

$$\beta = \frac{I_{C\text{max}}}{I_B} \rightarrow I_{C\text{max}} = \beta I_B$$

$$P_D = P_{D,0} - \frac{1}{2} I_B^2 R_D$$

Due to reverse biasing of collector and base there is minority collector current.

So, $I_{C\text{min}} = I_{CE0}$ = collector to Emitter minority current.

Relationship b/w α and β

$$\alpha = \frac{\beta}{1+\beta}, \quad \beta = \frac{\alpha}{1-\alpha}$$

We know, $I_E = I_B + I_C$
and $I_C = \beta I_B \rightarrow I_B = \frac{I_C}{\beta}$

$$I_C(\frac{1}{\beta}) = I_C(\frac{1}{\beta} + 1)$$

$$\begin{aligned} \frac{1}{\alpha} &= \frac{1}{\beta} + 1 \\ \frac{1}{\alpha} &= \frac{1+\beta}{\beta} \rightarrow \alpha = \frac{\beta}{1+\beta} \quad \left| \begin{array}{l} \frac{1}{\beta} = \frac{1}{1-\alpha} \\ \beta = \frac{\alpha}{1-\alpha} \end{array} \right. \end{aligned}$$

Q1 A certain transistor has current gain of 0.99 in CB config, calculate current gain CE.

$$\text{Given } \alpha = 0.99$$

$$\beta = \frac{\alpha}{1-\alpha} = \frac{0.99}{1-0.99} = 99.01$$

Q1 A change of 250 mV in base emitter voltage possess a change of 100 uA in collector current. Determine γ_i ?

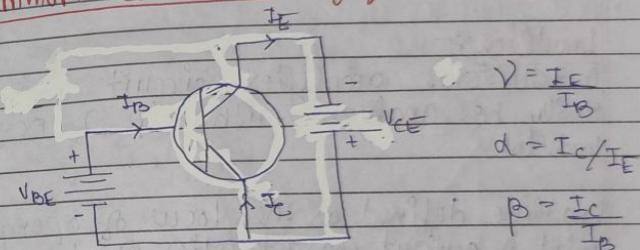
$$\text{Given, } \Delta I_B = 100 \mu\text{A}$$

$$\gamma_i = \frac{\Delta V_{BE}}{\Delta I_E} = \frac{250}{100} = 2.5$$

Q1 Increase in collector, emitter voltage from 6V to 10V possess increase in collector current from 5 mA to 6.5 mA. Determine dynamic γ_i ?

$$r_o = \frac{\Delta V_{CE}}{\Delta I_C} = \frac{5}{0.8} = \frac{50}{8} = 6.25 \text{ k}\Omega$$

Common-Collector Configuration



Relationship between α , β & γ

$$\text{We have } I_E = I_B + I_C$$

$$\therefore \Delta I_E = \Delta I_B + \Delta I_C$$

$$\alpha = \frac{\Delta I_C}{\Delta I_E} = \frac{\Delta I_C}{\Delta I_B + \Delta I_C} \rightarrow \frac{\Delta I_C}{\Delta I_B} = \frac{\alpha}{1+\alpha}$$

$$\left| \alpha = \frac{\beta}{1+\beta} \right.$$

PAGE NO.: 6
DATE:

$$\beta = \frac{\Delta I_C}{\Delta I_B} = \frac{\Delta I_E + \Delta I_B}{\Delta I_B} = \frac{\Delta I_E / \Delta I_B - 1}{1} = \frac{I_{C0}}{I_{B0}}$$

$$\beta = \frac{\Delta I_C}{\Delta I_B} = \frac{\Delta I_C}{\Delta I_E - \Delta I_C} = \frac{1}{1 - \alpha} \Rightarrow \beta = \frac{1}{1 - \alpha}$$

Load line :-

A transistor amplifier circuit can more easily be analyzed with help of DC & AC load line.

Load line defined as the locus of operating point of output characteristics of transistor.

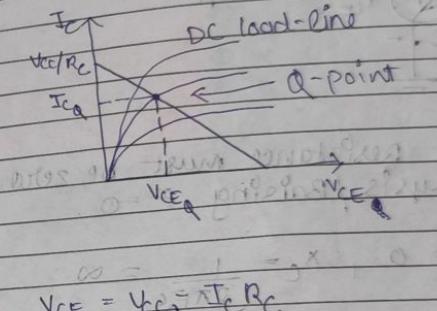
Two types of load line \rightarrow DC and AC

DC Load line :-

A line drawn on output characteristics of a transistor circuit which give the value of collector current I_C , V_{CE} corresponding to '0' signal condition (i.e. DC condition) is DC load line.

AC Load line :-

A line drawn on output characteristics of a transistor which gives value of I_C & V_{CE} when signal is applied (i.e. AC condition).



$$V_{CE} = V_{CC} - I_C R_C$$

when $I_C = 0$, $V_{CE} = V_{CC}$

when $V_{CE} = 0$

$$I_C = \frac{V_{CC}}{R_C}$$

Operating / Quiescent Point :-

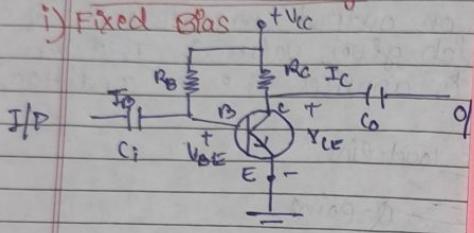
The point that corresponds to collector current and V_{CE} in the absence of signal is known as Q point.

Generally Q-point is chosen in middle of active region.

It is obtained by intersection of DC load line with transistor output characteristic curve.

Transistor Biasing:

i) Fixed Bias



Here, $C_1 + C_2$ are coupling capacitors, so coupling capacitors blocks DC component at Input and output.

Standard V_{BE} :-
Silicon $\Rightarrow 0.7$

→ Here, emitter resistance must be zero.
For DC analysis / Biasing $F = 0$.

$$\text{Thus, } R_E = 0, \quad X_C = \frac{1}{2\pi f L} \approx 0$$

→ Applying KVL in I/P loop, $V_{CC} - I_B R_B - V_{BE} = 0$

$$\frac{V_{CC} - V_{BE}}{R_B} = I_B$$

$0 = 22V - 0.7V$

$22V = 0.7V$

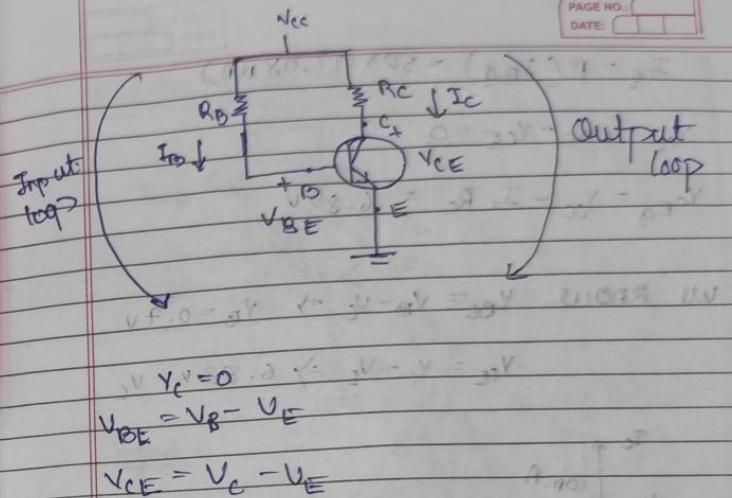
So, here I_B is fixed value so it's fixed biasing.

→ Applying KVL in Output loop,

$$V_{CC} - I_C R_C - V_{CE} = 0$$

$$V_{CE} = V_{CC} - I_C R_C$$

$$4) I_C = \beta I_B$$



→ Determine the following parameters for the fixed bias config.

- i) I_B and I_C
- ii) V_{CE}
- iii) V_O and V_C
- iv) V_{BE}

Given, $V_{CC} = 12V$, $\beta = 50$
 $R_B = 240 \text{ k}\Omega$
 $R_C = 22 \text{ k}\Omega$
 $C_1 = C_2 = 10 \text{ nF}$

$$\text{I/P : } V_{CC} - I_B R_B - V_{BE} = 0$$

$$I_B = \frac{V_{CC} - V_{BE}}{R_B} = \frac{12 - 0.7}{240 \text{ k}\Omega} = 47.08 \text{ mA}$$

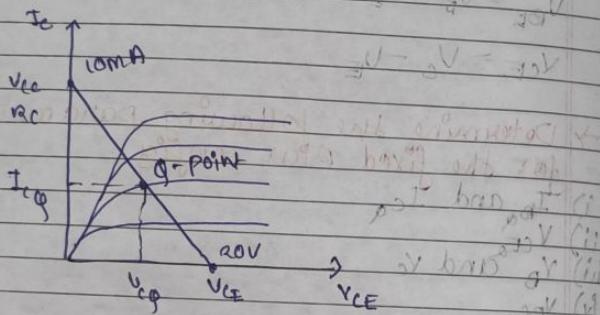
$$I_{CQ} = \beta (I_{BQ}) = 50 \times 14.9 = 0.745 \text{ mA}$$

$$V_{CE} - I_C R_C - V_{CE} = 0$$

$$\Rightarrow V_{CEQ} = V_{CC} - I_C R_C = 6.88 \text{ V}$$

$$\text{we know } V_{BE} = V_B - V_C \Rightarrow V_B = 0.7 \text{ V}$$

$$V_{CE} = V_C - V_E = 6.88 - 0.7 = 6.18 \text{ V}$$



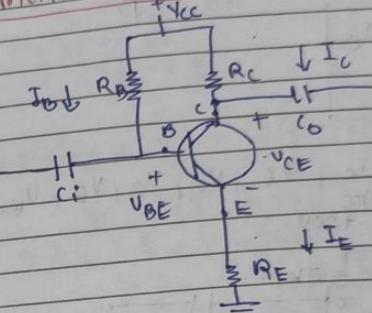
Calculate V_{CE} , R_C , I_B for fixed bias.

$$V_{CE} = V_{CC} - I_C R_C = 6.88 \text{ V}$$

$$0 = 30 \text{ V} - 6.88 \text{ V} - 20 \text{ V}$$

$$I_B = \frac{V_{CC} - V_{BE} - V_{CE}}{R_B} = \frac{30 \text{ V} - 0.7 \text{ V} - 6.88 \text{ V}}{20 \text{ k}\Omega} = 0.745 \text{ mA}$$

Emitter Bias Config.



Input:

$$V_{CC} - I_B R_B - V_{BE} - I_E R_E = 0$$

$$\Rightarrow V_{CC} - I_B R_B - V_{BE} - (I_B + I_C) R_E = 0 \quad [\because I_E = I_B + I_C]$$

$$\Rightarrow V_{CC} - I_B R_B - V_{BE} - (I_B + \beta I_B) R_E = 0 \quad [\because I_C = \beta I_B]$$

$$\Rightarrow V_{CC} - I_B R_B - V_{BE} - I_B R_E (\beta + 1) = 0$$

$$\Rightarrow I_B = \frac{V_{CC} - V_{BE}}{R_B + R_E (\beta + 1)}$$

Output:

$$V_{CC} - I_B R_B - V_{CE} - I_E R_E = 0 \quad (\because I_E = I_B + I_C)$$

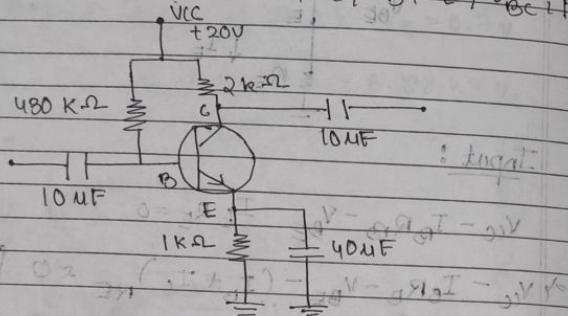
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$$\Rightarrow I_E = \frac{I_C}{\beta} + I_C$$

$$\Rightarrow V_{CC} - I_C R_C - V_{CE} - I_C R_E - I_C R_E = 0$$

$$\frac{V_{CC} - V_{CE}}{R_C + R_E + \frac{R_E}{B}} = I_C$$

Q) Determine I_B , I_C , V_{CE} , V_C , $V_B + V_E$, V_{BE} , V_{PC} , $\beta = 50$



Applying KVL in I/P Loops - $I_1 = I_2$

$$\begin{aligned} & V_{CC} - (I_B R_B) - V_{BE} - I_E R_E = 0 \quad (I_E = I_B) \\ \Rightarrow & V_{CC} - I_B R_B - V_{BE} - (I_D + I_C) R_E = 0 \\ \Rightarrow & V_{CC} - I_B R_B - V_{BE} - (I_{D_s} + B I_B) R_E = 0 \end{aligned}$$

$$I_{DQ} = \frac{V_{CC} - V_{BE}}{R_B + R_E(1+\beta)}$$

$$= \frac{20 - 0.7}{480 \times 10^3 + (4+50) \times 10^3} = 19.3 \times 10^{-3}$$

481

$$= 40.12 \mu\text{A}$$

$$\begin{aligned}
 I_C &= \beta I_B \\
 &= 50 \times 40.12 \mu A \\
 &= 2006 \mu A \\
 &= 2.006 \text{ mA}
 \end{aligned}$$

Applying KVL in O/P loop,

$$\begin{aligned}
 V_{CC} - I_C R_C - V_{CE} - I_E R_E &= 0 \\
 \Rightarrow V_{CE} &= V_{CC} - I_C R_C - I_E R_E \\
 &= V_{CC} - I_C R_C - (I_B + I_C) R_E \\
 &= 20 - 2 \cdot 006 \times 10^{-3} \times 2 \times 10^3 - \\
 &\quad 2 \cdot 006 \times 10^{-3} \times 10^3 \\
 &= 20 - 3 \times 2.006 \\
 &= 13.482 \text{ V}
 \end{aligned}$$

$$V_C = V_{CC} - I_C R_C$$

$$\Rightarrow 20 - 2.006 \times 10^{-3} \times 2 \times 10^3$$

$$= 15.988 \text{ V}$$

$$V_{CE} = V_C - V_E$$

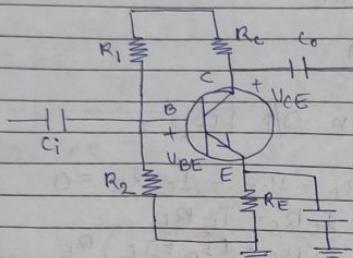
$$V_E = V_c - V_{CE} = 15.988 - 13.983 = 2.006 \text{ V}$$

$$U_{BE} = U_B - V_E$$

$$= 0.7 + 2.006 \\ = 2.706 \text{ V}$$

$$\begin{aligned}V_{BC} &= V_B - V_C \\&= 2.706 - 15.988 \\&= -13.282 \text{ V}\end{aligned}$$

Voltage Divider Bias :-



Here two resistors are used as input junction so that the whole DC supply is not given to input rather a part of it is given. So it is voltage divider bias.

- i) Exact Analysis
- ii) Approximate Analysis

i) Exact Analysis :-

First using Thévenin's theorem the input circuit connected between base emitter can be replaced by voltage V_{th} and series with R_{th} .

$$\text{Here, } R_{th} = (R_1 \parallel R_2), \quad R_{th} = \frac{R_1 R_2}{R_1 + R_2}$$

$$\text{and } V_{th} = \frac{V_{cc} R_2}{R_1 + R_2}$$

Applying KVL in the input loop the eq

$$V_{th} - I_B R_{th} - V_{BE} - I_E R_E = 0$$

$$\Rightarrow V_{th} - I_B R_{th} - V_{BE} - (I_B + I_C) R_E = 0$$

$$\Rightarrow V_{th} - I_B R_{th} - V_{BE} - (I_B + \beta I_B) R_E = 0$$

$$I_B = \frac{V_{th} - V_{BE}}{R_{th} + R_E(1 + \beta)}$$

For output loop applying KVL,

$$I_C = \beta I_B$$

$$V_{cc} - I_C R_C - V_{CE} - I_E R_E = 0$$

$$V_{cc} - I_C R_C - V_{CE} - (I_B + I_C) R_E = 0$$

$$\Rightarrow V_{cc} - I_C (R_C + R_E) - V_{CE} = 0$$

$$I_C = \frac{V_{cc} - V_{CE}}{R_C + R_E}$$

$$I_E \approx I_D$$

ii) Approximate Analysis :-

The approximate analysis is applicable if it satisfies the following condition

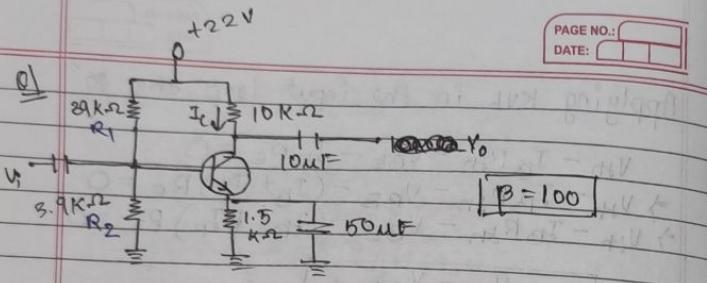
$$\beta R_E \gg R_1 + R_2$$

$$V_B = \frac{R_2 V_{cc}}{R_1 + R_2}$$

$$V_{BE} = V_B - V_E$$

$$V_C = V_{cc} - I_C R_C$$

$$V_E = I_E R_E$$



$$\frac{V_f}{V_i} = \frac{V_{CE} - V_{CE}}{V_{CE}} = \frac{V_{CE}}{V_{CE}} = 100$$

$$R_{TH} = R_1 \parallel R_2 = 3.55 \text{ k}\Omega$$

$$V_{TH} = \frac{V_{CE} \times R_2}{R_1 + R_2} = 2 \text{ V}$$

$$I_B = 8.38 \text{ mA}$$

$$I_C = 0.86 \text{ mA}$$

$$V_{CE} = 12.03 \text{ V}$$

$$P_{RE} \gg 10 R_2$$

If yes / satisfy,

$$V_O = \frac{V_{CE} R_2}{R_1 + R_2}$$

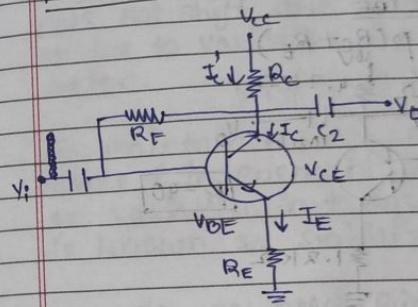
$$V_{BE} = V_B - V_E$$

$$\approx V_{IE} = V_B - V_{BE} = 1.3 \text{ V}$$

$$V_E = I_C R_E \Rightarrow I_C = \frac{V_E}{R_E} = 0.867 \text{ mA}$$

$$V_{CE} = V_{CC} - I_C (R_C + R_E) = 12.03 \text{ V}$$

DC Feedback / collector Feedback



$$V_{CC} - I_B R_E - V_{BE} - \beta I_B (R_C + R_E) = 0$$

$$I_B = \frac{V_{CC} - V_{BE}}{R_F + \beta (R_C + R_E)}$$

$$V_{CC} - I'_C R_C - I_B R_F - V_{BE} - I_E R_E = 0$$

\therefore Current through R_C is not I_C it is I'_C

$$\boxed{\text{So, } I'_C = I_C + I_B}$$

$$I'_C \approx I_C (\text{Approx}) = \beta I_B \text{ and } I_E \approx I_C$$

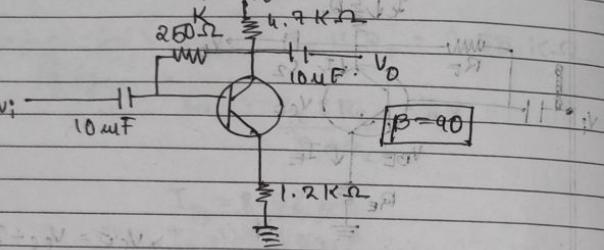
$$\text{So, } V_{CC} - \beta I_B R_C - I_B R_F - \beta I_B R_C = 0$$

$$V_{CC} - V_{BE} - \beta I_B (R_C + R_E) - I_B R_E = 0$$

$$\Rightarrow V_{CC} - I_B R_F - V_{BE} - \beta I_B (R_C + R_E) = 0$$

$$\Rightarrow I_B = \frac{V_{CC} - V_{BE}}{R_F + \beta (R_C + R_E)}$$

$250\text{ k}\Omega \parallel 4.7\text{ k}\Omega$



Calculate V_{CE} and I_C .

$$I_B = \frac{V_{CC} - V_{BE}}{R_F + \beta (R_C + R_E)}$$

$$= \frac{10 - 0.7}{250 + 90} \cdot \frac{4.7}{1.2} = 0.011 \text{ mA}$$

$$V_{CE} = 10 - 0.011 \text{ mA} \cdot 1.2 \text{ k}\Omega = 9.3 \text{ V}$$

~~581~~

$$\left| \frac{\Delta I_C}{I_C} \right| = \left| \frac{\Delta V_{BE}}{V_{BE}} \right| = \left| \frac{\Delta T}{T} \right|$$

$$0 = 0.011 \text{ mA} \cdot 1.2 \text{ k}\Omega = 13.2 \text{ mV}$$

Bias Stabilization :-

The suitable operating point is not sufficient but also to be ensured that the operating point remains stable (it does not shift due to change in temp. or due to variation in transistor parameter).

The maintenance of operating point stable (independent of temp. variations or variation in transistor parameter) is known as stabilization.

Why do we need Bias Stabilization? The stabilization of operating point is essential (because of temp. dependence of collector current (I_C)).

Individual variations and ~~normal~~ thermal run away (the self destruction of an un-stabilized transistor) is called thermal run away.

Stability Factor :

It is the ratio of change in collector current with change in any transistor constant.

It is of three types:

$$S_{IC_0} = \frac{1}{\beta} \frac{dI_C}{dV_{BE}} \quad | \quad V_{BE} + \beta \text{ const}$$

$$S_{V_{BE}} = \frac{1}{\beta} \frac{dI_C}{dV_{BE}} \quad | \quad I_C + \beta \text{ const}$$

$$S_P = \frac{1}{\beta} \frac{dI_B}{dV_{BE}} \quad | \quad I_C + V_{BE} \text{ const}$$

* General expression for S_{IC_0}

$$\text{We know, } I_C = \beta I_B + (\beta + 1) I_{C_0}$$

Now differentiate w.r.t I_C constant β constant

$$\frac{dI_C}{dI_C} = \frac{\beta dI_B}{dI_C} + (\beta + 1) \frac{dI_{C_0}}{dI_C}$$

$$\Rightarrow I_C = \beta \frac{dI_B}{dI_C} + \frac{\beta + 1}{S_{IC_0}}$$

$$S_{IC_0} = \frac{\beta + 1}{1 - \beta \frac{dI_B}{dI_C}}$$

* General Expression for S_P

$$I_C = \beta I_B + (\beta + 1) I_{C_0}$$

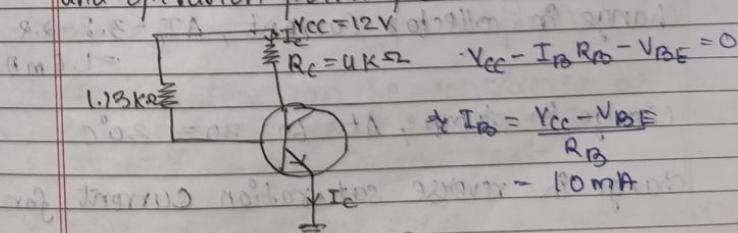
Differentiate w.r.t I_C constant I_B constant

$$I = \left(\beta \frac{dI_B}{dI_C} + I_B \frac{dB}{dI_C} \right) + I_{C_0} \frac{dP}{dI_C}$$

$$\Rightarrow I = \beta \frac{dI_B}{dI_C} (I_B + I_{C_0}) \frac{1}{S_P}$$

$$\Rightarrow S_P = \frac{I_{C_0} + I_B}{1 - \beta \frac{dI_B}{dI_C}}$$

Q For the fixed Bias config. using a β Transistor with $\beta=100$. Determine Base current, collector current, V_C , V_B , V_{CE} and operation point, s .



$$I_C = \beta I_B = \frac{V_{CC} - V_{BE}}{R_C}$$

$$V_{CE} = I_C R_E - V_{CE} = 0 \text{ (neglecting } I_{CBO})$$

$$V_{CE} = 12 - 4 \times 10^3$$

$$V_{CE} = 8 \text{ V}$$

$$V_{BC} = V_B - V_C$$

$$\frac{\partial(V_{CE}, I_C)}{\partial T} + \left(\frac{\partial h_{FE}}{\partial T} + \frac{\partial h_{ie}}{\partial T} \right) I_C$$

$$\frac{\partial}{\partial T} (I_C + \alpha T)$$

For Fixed Bias config. stability factor,

$$S = B + 1$$

In a fixed Bias circuit, using transistor with $\alpha = 0.97$, temp. changes from 30°C to 60°C producing change in I_C from 2.2 mA to 3.8 mA . Assume reverse saturation current changes $1.7 \text{ nA}/^\circ\text{C}$. What is stability Factor.

$$\text{Change in collector current, } \Delta I_C = 3.8 - 2.2 = 1.6 \text{ mA}$$

$$\text{Change in temp., } \Delta t = 60 - 30 = 30^\circ\text{C}$$

Change in reverse saturation current for

$$\Delta t \text{ of } 30^\circ\text{C, } \Delta I_{C0} = 30 \times 1.7 \times 10^{-6} = 51 \times 10^{-6} \text{ A}$$

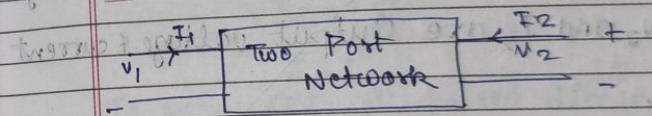
$$\text{So, stability factor } = \frac{\Delta I_C}{\Delta I_{C0}} = \frac{1.6 \times 10^{-3}}{51 \times 10^{-6}} = 31.37$$

Small Signal Analysis of BJT :-

Generally there are two types of models are chosen for the actual behaviour of transistor. They are:

- i) Hybrid Model
- ii) h model

Two Port Network :-



→ A network that has two parts Input, output port and current should enter to the network from both parts.

→ It is specified by two voltages and two current (one pair is used for Input and another pair is used for output)

→ The transistor can be considered as two port network as it has one Input port as well as one Output port

→ There are different types of two-port networks:

- i) Z - Parameter Model (Impedance)
 ii) Y - Parameter Model (Admittance)
 iii) H - Parameter Model (Hybrid)

~~H - Parameter Model (Hybrid)~~:

In this model ~~out~~ ~~input~~ ~~voltage~~

$$\begin{bmatrix} V_1 \\ I_2 \end{bmatrix} = \begin{bmatrix} h_{11} & h_{12} \\ h_{21} & h_{22} \end{bmatrix} \begin{bmatrix} I_1 \\ V_2 \end{bmatrix}$$

Here, I_1 and V_2 are Input current & voltage

V_2 and I_2 are Output voltage & current

Now,

$$V_1 = h_{11} I_1 + h_{12} V_2$$

$$I_2 = h_{21} I_1 + h_{22} V_2$$

~~Hybrid Equivalent Model~~:

An equivalent model is combination of circuit elements properly chosen to best represent actual behaviour of device under specific operating point.

We cannot apply network theorem directly on the practical devices. So we need equivalent model to use this theorem to find out different network parameters.

~~Hybrid Model :-~~

~~calculation of H-parameters~~

The parameter has mixed dimensions
~~like Z-parameter & Y-parameter~~

V_1 and I_2 are dependent quantity.

V_2 and I_1 are independent quantity.

We can say

$$V_1 = f(I_1, V_2)$$

$$I_2 = f(V_2, I_1)$$

PAGE NO.:
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$$\frac{dV_1}{dI_1} = \frac{\partial V_1}{\partial I_1} + \frac{\partial V_1}{\partial V_2} \cdot dV_2 \rightarrow \text{small change in } V_1$$

PAGE NO.:
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small change in V_1 small change in I_1

rate of change of V_1 w.r.t. V_2

change of V_1 w.r.t. V_2 w.r.t. I_1

$dI_2 = \left(\frac{\partial I_2}{\partial I_1} \right) \cdot dI_1 + \left(\frac{\partial I_2}{\partial V_2} \right) \cdot dV_2$

$\gamma_1 = h_{11} i_1 + h_{12} v_2 \rightarrow \text{eq. ③}$

$i_2 = h_{21} i_1 + h_{22} v_2 \rightarrow \text{eq. ④}$

make $v_2 = 0$, so from eq. ③ $h_{11} = \frac{v_1}{i_1} \Big|_{v_2=0} = h_1$

(input impedance, when output is short circuit)

PAGE NO.:
DATE:

from eq. ④, when output is short circuit

$h_{21} = \frac{i_2}{v_2} \Big|_{v_2=0} = h_f$ (forward current gain when output is short circuit)

when $i_1 = 0$, from eq. ③

$h_{12} = \frac{v_1}{v_2} \Big|_{i_1=0} = h_r$

(reverse voltage gain, when input is open circuit)

from eq. ④,

$h_{22} = \frac{i_2}{v_2} \Big|_{i_1=0} = h_o$

(output admittance when input is open circuit)

h-parameter :

(h_1, h_f, h_r, h_o)

Nomenclature : h_1, h_f, h_r, h_o

h_i : nature of parameter
 (input impedance, forward current gain, reverse voltage gain, output admittance)

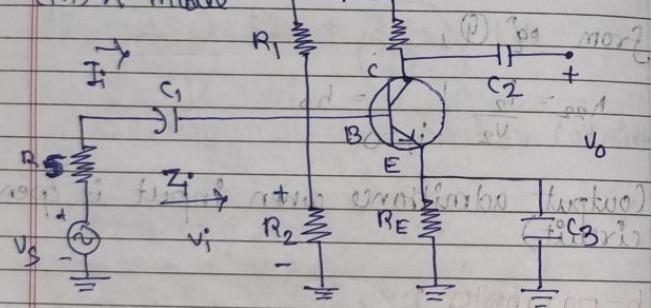
I_2 : Transistor Configuration (CB, CE, CC)

BJT Transistor Modelling:

A model is combination of circuit element property chosen that best approximate the actual behaviour of a semi-conductor device under specific operating condition.

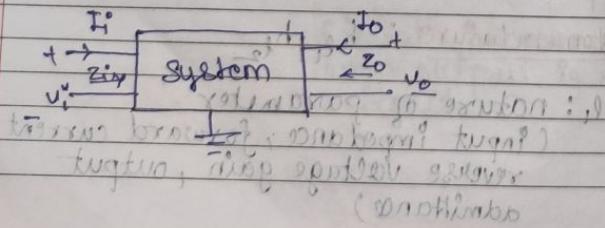
There are 3 models as to describing BJT transistor

- (i) hybrid model (no position 9289197)
- (ii) π -model (for AC analysis)
- (iii) π -model

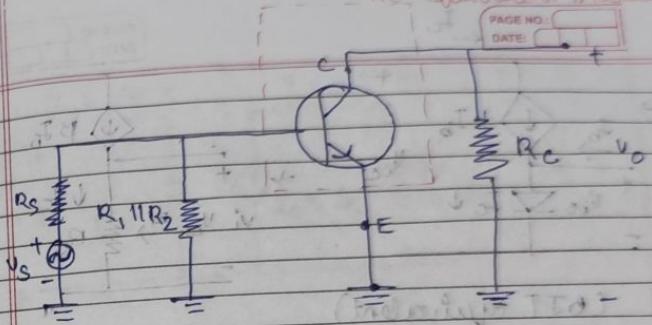


π -model

($i_d = u_A + j\omega I_d$)



Transistor small signal AC equivalent model



The AC equivalent of a transistor is obtained by:

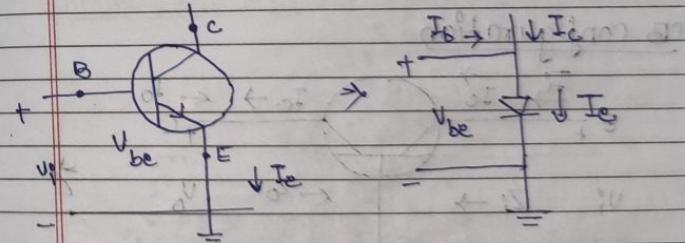
- make all DC sources to zero and
- replacing them by short circuit equivalent

~~except~~

Transistor π Model

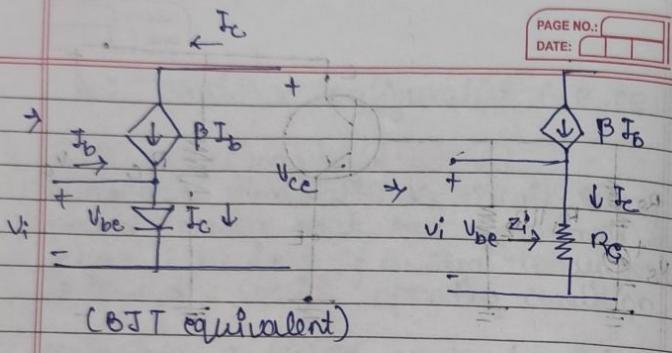
(Johnson Equivalent (JE))

CE configuration

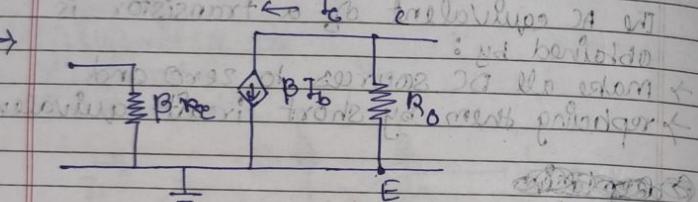


Equivalent circuit
for a BJT

Equivalent circuit
for input side of
BJT

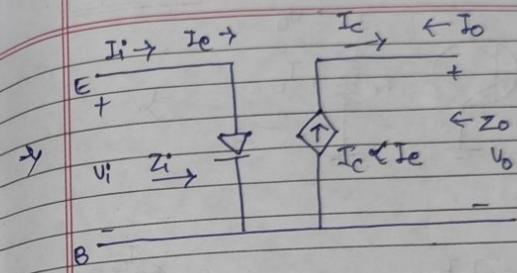
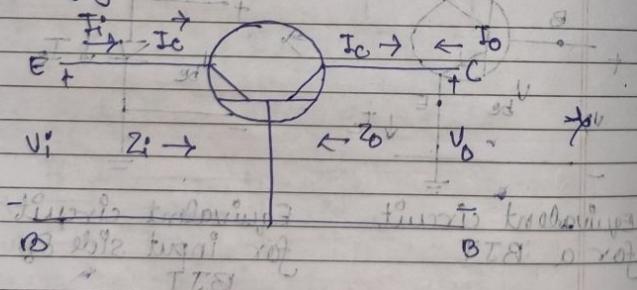


(BJT equivalent)

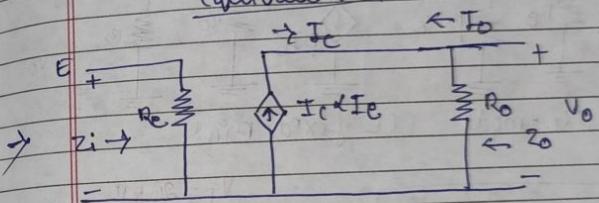


(BJT equivalent model)
Re model no bias voltage V_B

CB configuration



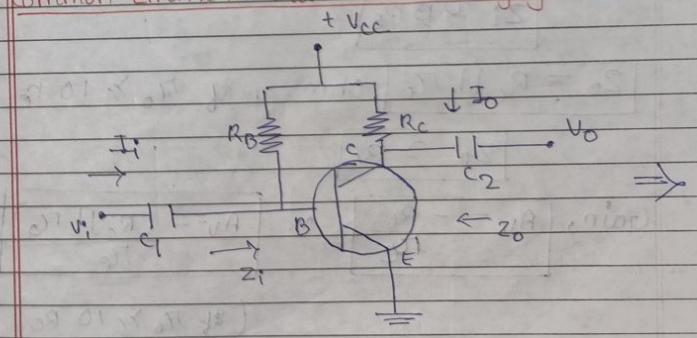
equivalent

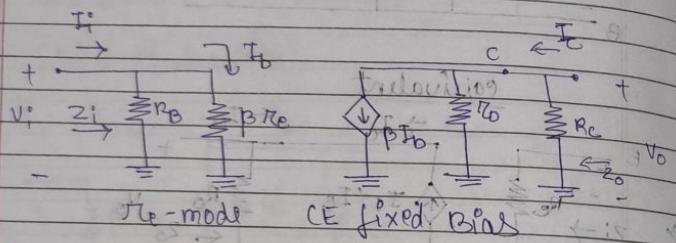
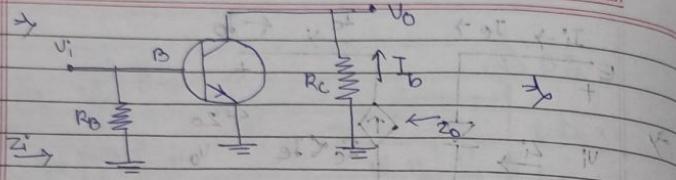


Re-equivalent model

RE - model

Common Emitter Fixed Bias configuration:





$$Z_i = R_B \parallel (\beta R_C) \quad \boxed{Z_i = \frac{V_T}{I_E}}$$

for majority cases $R_B \gg 10 \beta R_C$

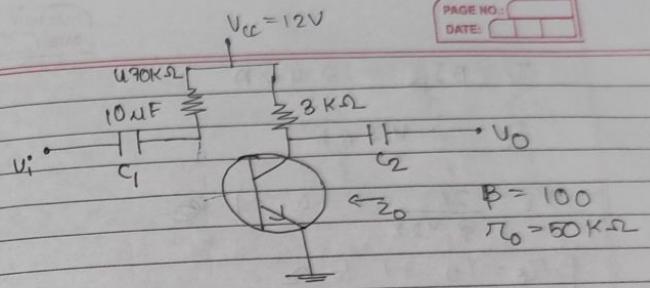
$$Z_i \approx \beta R_C$$

$$Z_o = R_C \parallel \tau_o \text{ ohms, if } \tau_o \gg 10 R_C$$

$$Z_o \approx R_C$$

$$\text{Gain, } A_V = -\frac{R_C}{\tau_{i_e}} \quad \text{or} \quad A_V = -\frac{(R_C \parallel \tau_o)}{\tau_{i_e}}$$

(if $\tau_o \gg 10 R_C$)



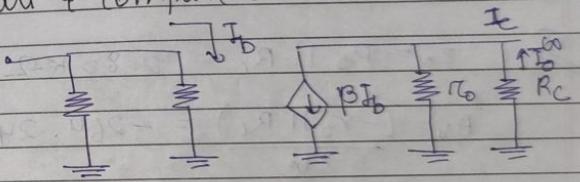
(i) Determine τ_{i_e} ;

(ii) $Z_i = ? \quad (\tau_o = \infty)$

(iii) $Z_o = ? \quad (\tau_o = \infty)$

(iv) $A_V = ?$

(v) Repeat questions by $\tau_o = 80 \text{ k}\Omega$. Calculate & compare.



$$\tau_{i_e} = \frac{26 \text{ mV}}{I_E}$$

From Input circuit:

$$V_{CE} - I_B R_B - V_{BE} = 0$$

$$\Rightarrow 12 - I_B (490 \times 10^3) - 0.7 = 0$$

$$\Rightarrow I_B = \frac{12 - 0.7}{490} \times 10^{-3}$$

$$= 24.04 \mu\text{A}$$

$$I_C = \beta I_{BQ} = 2.4 \text{ mA}$$

$$I_E = 2.42 \text{ mA}$$

$$V_E = \frac{26}{2.428} = 10.71 \text{ V}$$

$$\beta R_E = 10.71 \text{ k}\Omega$$

$$Z_i = R_E \parallel \beta R_E = 1.07 \text{ k}\Omega$$

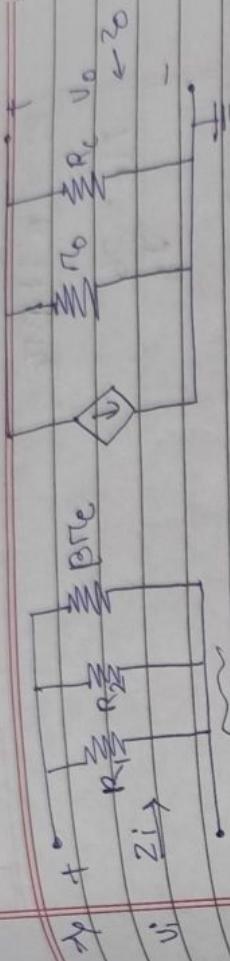
$$A_V = -\frac{R_C}{r_E} = \frac{3000}{10.71} = -280.11$$

$$Z_o = R_C = 3 \text{ k}\Omega$$

~~$$Z_o = R_C \parallel R_L = 2.83 \text{ k}\Omega$$~~

$$A_V = \frac{(-r_o \parallel R_C)}{r_E} = -264.24$$

Voltage Divider Bias: $V_{BE} = 0.7 \text{ V}$



$$R' = \frac{R_1 \parallel R_2}{R_1 + R_2}$$

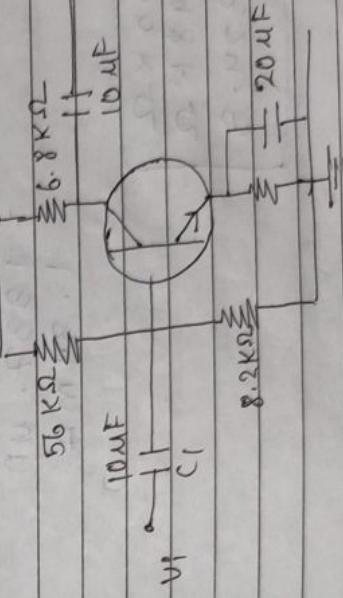
$$Z_1 = R' \parallel \beta r_E \Rightarrow R' \gg r_E \Rightarrow Z_1 \approx \beta r_E$$

$$Z_o = r_o \parallel r_E \Rightarrow r_o \gg r_E \Rightarrow Z_o \approx r_o$$

$$A_V = -\frac{R_C}{r_E + r_o}$$

$$A_V = -\frac{R_C}{r_E} \quad \text{for } r_o \gg r_E$$

$$V_{CE} = 22 \text{ V}$$



$$B = 90, R_E = 1.5 \text{ k}\Omega, r_o = 50 \text{ k}\Omega, Z_1 = ? \text{ V}, Z_o = ? \text{ }\Omega, A_V = ?$$

$$Z_i = r' || \beta \pi_e$$

$$\pi_e = \frac{26}{I_E}$$

$$V_{DH} - I_B R_{DH} - V_{BE} - I_E R_E = 0$$

$$\begin{aligned} V_{DH} &= \frac{V_{CE} R_2}{R_1 + R_2} \\ &= \frac{22 \times 8.2}{56 + 8.2} \\ &= 2.809 \text{ V} \end{aligned}$$

$$\begin{aligned} R_{DH} &= \frac{R_1 R_2}{R_1 + R_2} \\ &= \frac{56 \times 8.2}{64.2} \\ &= 7.15 \text{ k}\Omega \end{aligned}$$

$$\begin{aligned} I_B &= \frac{V_{DH} - V_{BE}}{(\beta + 1) R_E + R_{DH}} \\ &= \frac{2.809 + 0.7 \times 10^{-3}}{91 \times 1.5 + 7.15} \\ &= \frac{2.109 \times 10^{-3}}{143.65} \\ &= 14.7 \mu\text{A} \end{aligned}$$

$$\begin{aligned} I_E &= 91 \times 14.7 \mu\text{A} \\ &= 1337 \mu\text{A} \\ &= 1.34 \text{ mA} \end{aligned}$$

$Z_i = 1.35 \text{ k}\Omega$
$Z_o = 5.98 \text{ k}\Omega$
$A_V = -324.3$

1. *Geography* is the study of the earth's surface, its physical features, and the distribution of people and their activities. It includes the study of climate, vegetation, soil, water resources, and human settlements. Geography is a broad subject that covers both physical and human geography.

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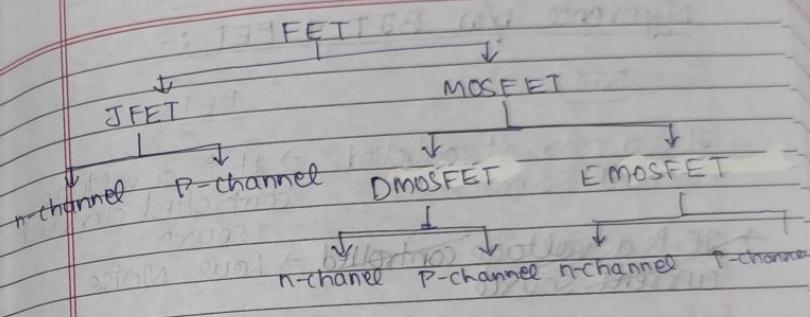
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FET (Field Effect Transistor) :-

A FET is a semi-conductor device where the output current is controlled by an electric field applied at the gate terminal.

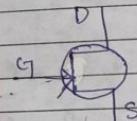
- It is a voltage control and its operation depends upon only one type of charge i.e. either holes or electrons. So it is unipolar device.
 → Its input impedance is high and more thermal stability which are advantages of BJT.
 → It has 3 terminals, they are Source, Drain & Gate.
 → Between the Gate Regions and from source to drain there is presence of channel.
 → Depending on type of channel, FETs are two types
 (i) n-channel (ii) p-channel
 → In some FET there is an extra terminal known as substrate.
 → In N-channel FET source + drain are n-type (Gate) is p-type.
 → In P-channel FET source + drain are p-type (Gate) is n-type.
 → Source + Drain terminals are inter-changeable.
 → There are two types of FET
- JFET (Junction Field Effect Transistor)
 - IGFET (Insulated Gate Field Effect Transistor)
↳ commonly known as Metal Oxide Semiconductor FET (MOSFET)



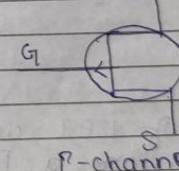
DMOSFET → Depletion type of MOSFET
 EMOSFET → Enhancement type of MOSFET

Symbol:

JFET



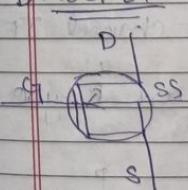
n-channel



p-channel

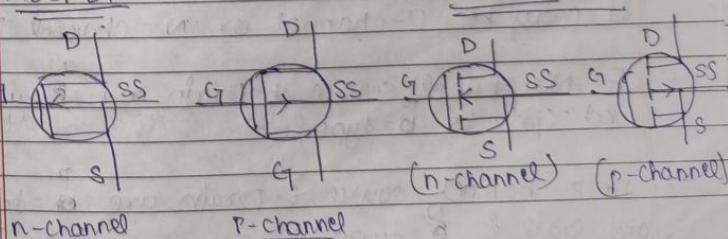
D → Drain
 S → Source
 G → Gate
 SS → Substrate

DMOSFET

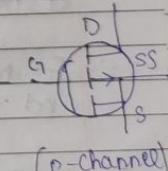


n-channel

EMOSFET



(n-channel)



(p-channel)

Difference b/w BJT & FET :-

BJT

→ It is a current controlled current source.

→ High Noise

→ It is a bi-polar device. → It is a unipolar device.

→ Low Input Impedance

→ Less temperature stability

FET

→ It is a voltage controlled current source.

→ Low Noise

→ High Input Impedance

→ More temperature stability

JFET :-

→ It is a type of FET where Junction is present (Gate forms a P-N Junction with channel).

It may be P-channel or N-channel JFET.

→ In N-channel source & drain are ^NP-type and Gate is ^NP-type.

→ In P-channel source & drain are ^PN-type and Gate is ^PN-type.

Important Notations

i) Source :

The terminal through which majority carriers enter the channel is called source terminal (S)

The conventional current entering the channel is denoted by (I_S)

ii) Drain :

The terminal through which majority carriers leave the terminal is Drain.

The conventional current leaving the channel is denoted by (I_D)

iii) Gate :

There are two internally connected heavily doped Impurity regions formed by allowing or Diffusion or any other method available to create two P-N Junctions. These impurity regions are called gate.

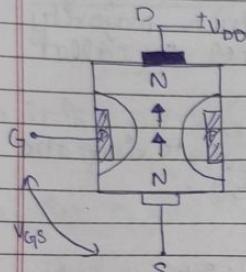
The conventional current is (I_G)

iv) Channel :

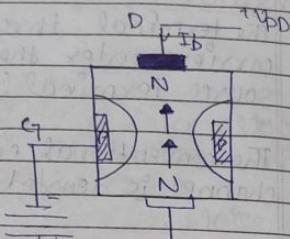
The region b/w source & drain, sandwiched b/w Gate is called region.

The majority carrier moves from source to drain through this channel.

Operation of JFET :-



JFET with no-bias



JFET with -ve Gate Source bias

→ Let us consider an N-Channel JFET operation :

→ If ($V_{GS} = 0V$) & ($V_{DS} = 0V$) then the depletion region around P-N Junction are of equal thickness and symmetrical.

when +ve voltage is applied to Drain terminal D w.r.t source (s) without connecting Gate terminal (G) to supply.

→ The electrons (majority charge carriers) flow from terminal source to Gate where the I_D (conventional Drain current) flows from Drain to source to the channel.

→ Due to flow of this current, there is a uniform voltage drop across the channel resistance as we move from terminal 'D' to terminal 'S'. These voltage drop reverse biases your Diode.

→ The gate is more -ve w.r.t those points in the channel which are nearer to drain than the source. Hence depletion layers penetrate more deeply into the channel are points lying closer to drain than to source, the wedge shape depletion regions are formed.

when the gate is biased -ve w.r.t source while the drain is applied with +ve bias w.r.t source the P-N Junction are reverse biased and depletion region formed. 'Pd' region are heavily doped connected to 'N' channel so the depletion region penetrate deeply into the channel. The result is that the channel is narrowed and drain current I_D is reduced.

The gate source voltage V_{GS} at which the drain current ' I_g ' is cutoff completely

(Pinched-off is called pinched-off voltage and it is noted as V_p .)

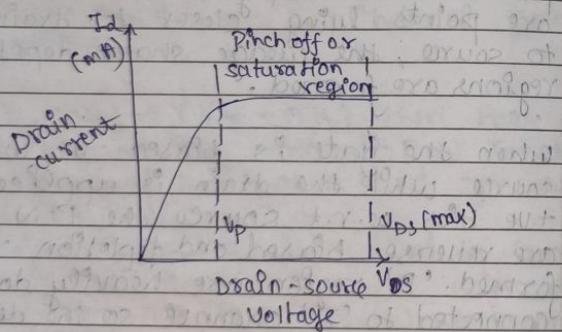
Characteristics of JFET :-

There are two types of characteristics of JFET :-

- i) Output or drain characteristics
- ii) Transfer characteristics

i) Output or drain characteristics :

The curve b/w drain current (I_d) & drain-source voltage (V_{ds}) with gate-source voltage (V_{gs}) as the parameter is called drain or output characteristics.



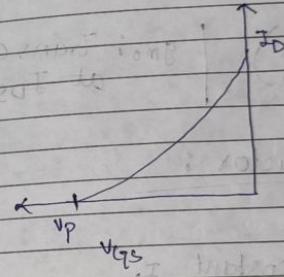
Drain-current in the pinch-off region is given by Shockley's eq

$$I_d = I_{dss} \left(1 - \frac{V_{gs}}{V_p}\right)^2$$

I_{dss} = Drain Source Saturation current .

ii) Transfer characteristic (Input) :-

The transfer characteristics gives the relationship b/w drain current & gate-source voltage .



JFET Parameters :-

JFET has certain parameters which determine the performance .

- (i) AC drain resistance
- (ii) Trans conductance
- (iii) Amplification factor
- (iv) DC - Drain Resistance

i) AC Drain Resistance :-

It is defined as the ratio of change in drain source voltage to change in drain current (I_d) at constant V_{ds} .

$R_d = \frac{\Delta V_{DS}}{\Delta I_D}$ at constant V_{GS}
 (dynamic drain resistance)

(iii) Trans Conductance :-

$$g_m = \frac{\Delta I_D}{\Delta V_{GS}}$$
 at constant V_{DS}

$$g_m = g_{mo} \left(1 - \frac{V_{GS}}{V_P}\right) \quad | \quad g_{mo}: \text{Transconductance at } I_{DS}$$

(iv) Amplification factor :-

$$\mu = \frac{\Delta V_{DS}}{\Delta V_{GS}}$$
 at constant I_D

$$\therefore \mu = \frac{\Delta V_{DS}}{\Delta V_{GS}} = \frac{\Delta V_{DS}}{\Delta I_D} \times \frac{\Delta I_D}{\Delta V_{GS}}$$

$$\therefore \mu = R_d \times g_m$$

(v) DC Drain Resistance :-

$$R_{DS} = \frac{V_{DS}}{I_D}$$

Q) When reverse voltage of 10V is applied between Gate & Source of JFET, the gate current is 0.1 μA . Determine the resistance between gate & source.

$$R_{GS} = \frac{V_{GS}}{I_g} = \frac{10 \times 10^6}{0.1} = 10^8 \Omega$$

Q) When drain-source voltage is changed by 1.5V, the change in drain current is of 120 μA . The gate-source voltage remains unchanged. Determine the AC drain resistance of JFET.

$$R_D = \frac{\Delta V_{DS}}{\Delta I_D} = \frac{1.5 \times 10^{-6}}{120 \times 10^{-6}} = \frac{10^5}{120} = 12.5 k\Omega$$

JFET Biasing:-

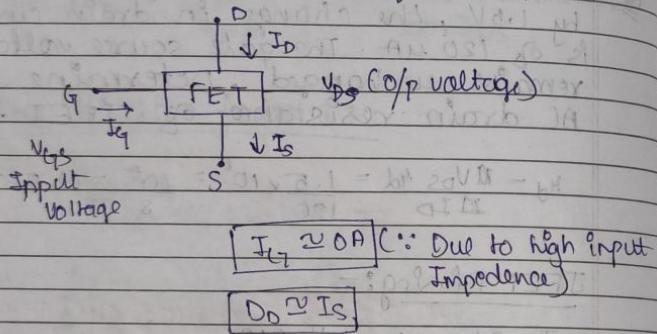
$$I_G \approx 0 \text{ also, } V_G \approx 0$$

$$I_D \approx I_S \rightarrow \text{source current}$$

The Input Impedance of JFET is reverse biased so the Input Impedance is very high so the Input or gate current (I_g) nearly equal to zero.

- There are generally three types of biasing
- Fixed-biasing
 - Self-sourced stabilized biasing
 - Voltage-divider biasing.

The relationship b/w Input or Output are non-linear due to squared term



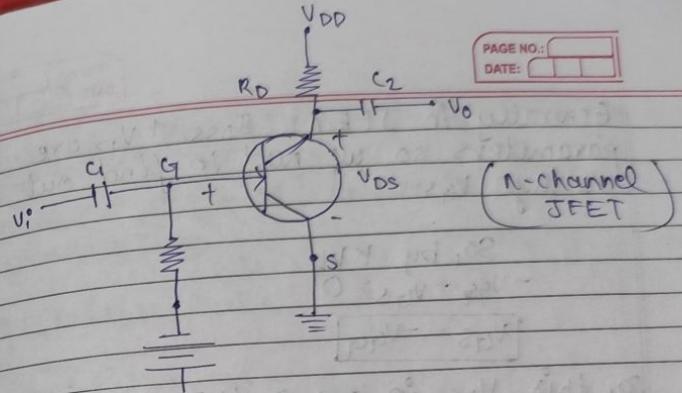
For JFET, + D - MOJFET

$$I_D = I_{DSS} \left(1 - \frac{V_{GS}}{V_T} \right)^2$$

Q-point (V_{GSQ} , I_{DQ})

E-MOFET

$$I_D = k(V_{GS} - V_T)^2$$



dc-analysis in
we have to perform n-channel,
 C_1 and C_2 are the coupling capacitors
and the reactance offered by $C_1 + C_2$ is
ac signal is ' ∞ '.

$$X_C = \frac{1}{2\pi f_C}$$

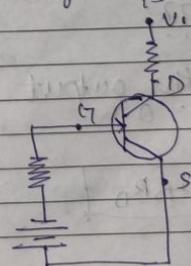
[for dc $\rightarrow f_C = 0$]

$$\Rightarrow X_C = \infty$$

so, $C_1 + C_2$ are open circuit.
 $V_i + V_o$ are input and output voltage
of circuit.

So, Input Voltage V_{GS} & output voltage V_{DS} .

$$V_{R_{D1}} = I_{DQ} R_G = 0$$



Generally in JFET, I_{DSS} + V_P are parameters so we need to find out input voltage V_{GS} .

$$\text{So, by KVL: } -V_{GG} - V_{GS} = 0$$

$$[V_{GS} = -V_{GG}]$$

so, this V_{GS} is one of the co-ordinates of Q-point i.e. Q-point (V_{GS}, I_D)

V_{GS} - x-coordinate of Q-point

though V_{GG} is fixed, for this reason we called this biasing configuration as fixed bias config.

Now we have to calculate I_D . To find I_D we know Shockley's Eqn,

$$I_D = I_{DSS} \cdot \left(1 - \frac{V_{GS}}{V_P}\right)^2$$

$$\Rightarrow I_D = ??$$

To determine the output voltage V_{DS} , $V_{DD} - I_D R_D - V_{DS} = 0$

$$\Rightarrow [V_{DS} = V_{DD} - I_D R_D]$$

Graphical method :-

To follow graphical approach we need Shockley's Eqn

Assuming,

case-I:

$$[V_{GS} = 0]$$

$$I_D = I_{DSS} \quad P_1 (0, I_{DSS})$$

case-II:

$$I_D = 0$$

$$[V_{GS} = V_P] \quad P_2 (V_P, 0)$$

case-III:

$$I_D = \frac{I_{DSS}}{4}$$

$$[V_{GS} = \frac{V_P}{2}] \quad P_3 (\frac{V_P}{2}, \frac{I_{DSS}}{4})$$

By using these point P_1, P_2, P_3 we plot the transfer characteristics \rightarrow Plot b/w output current (I_D) & Voltage Get-Source (V_{GS})

I_{DSS} + V_P are given.

To find out Q-point in fixed bias config of JFET, V_{GS} is equal to $-V_{GG}$ (fixed)

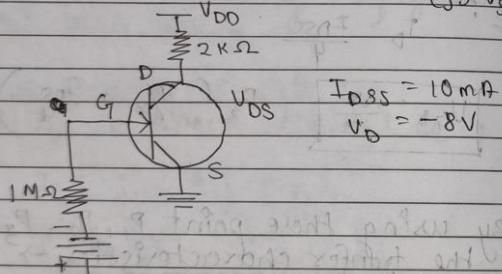
Put a vertical straight line concerning the fixed V_{GS} value towards the transfer curve

Determine the I_{DQ} concerning the intersection point (i.e. Q-point) across the y-axis.

Then we are able to find Q-point (V_{GSS}, I_{DQ})

Q Determine the following for the network

- (a) V_{GSS}
- (b) I_{DQ}
- (c) V_{DS}
- (d) V_D
- (e) V_G
- (f) V_S



Sol:-

Q. Point (V_{GSS}, I_{DQ})

V_{DS} : o/p voltage

V_p : potential between D and G

Source is connected to ground so, $V_S = 0V$.

$$V_{DS} = V_D - V_S \Rightarrow V_D = V_{DS}$$

$$V_{GS} = V_G - V_S = V_G$$

$$I_G \approx 0A$$

$$-av - 0V - V_{GS} = 0 \Rightarrow V_{GSS} = -2V$$

$$V_G = -2V$$

$$I_D = I_{DSS} \left(1 - \frac{V_{GS}}{V_D} \right)^2$$

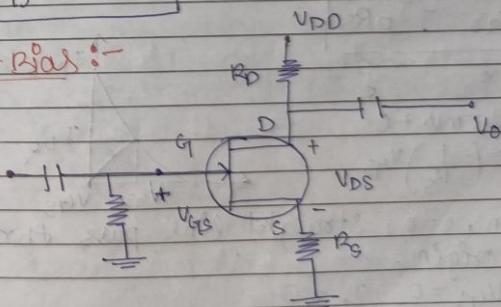
$$\Rightarrow I_D = 5.625 \text{ mA}$$

$$\Rightarrow 16 - (5.625 \text{ mA})(2 \text{ k}\Omega) - V_{DS} = 0$$

$$\Rightarrow V_{DS} = 4.75V$$

$$\Rightarrow V_D = 4.75V$$

Self-Bias :-



If we want to differentiate fixed bias and self bias configuration there are two different source.

(i) In fixed bias configuration there are two DC supply i.e. V_{DD} & V_{GG} , but in case of self-bias configuration there is only one DC supply V_{DD} i.e. V_{GG} is absent.

(ii) In case of self-bias we have extra resistor ' R_S '.

C_1 & C_2 are coupling capacitor

By KVL in I/p loop

$$-V_{GS} - I_S R_S = 0 \quad (\text{At } V_{GS} = 0)$$

$$\Rightarrow V_{GS} = -I_S R_S \quad (\because I_D \approx I_S)$$

$$I_D = I_{DSS} \left(1 - \frac{V_{GS}}{V_P}\right)^2$$

$$I_D^2 + (K_1) I_D + K_2 = 0$$

$$V_{GS} = -I_S R_S$$

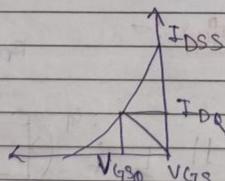
$$y = mx + c$$

$$I_D = \left(-\frac{1}{R_S}\right) V_{GS}$$

when, $c=0$, straight line pass through the origin.

→ If $V_{GS} = 0$, $I_D = 0$

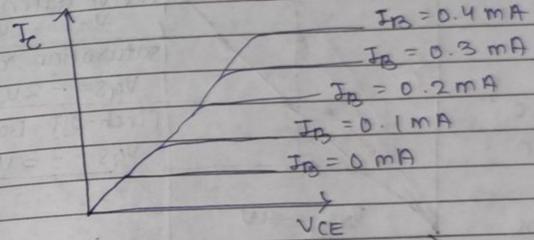
$$\rightarrow I_D = \frac{I_{DSS}}{2}, \quad V_{GS} = -\frac{I_{DSS} R_S}{2}$$



Assignment : Pg - U26 , P.g 7.1, 7.2, 7.3, 7.4

Input and Output characteristics of JFET

i) Output / Drain characteristics



(For CE Configuration BJT)

i.e. graph between I_C y/s V_{CE} at I_B (Input current)

$\begin{matrix} \text{o/p} \\ \text{current} \end{matrix}$ $\begin{matrix} \text{o/p} \\ \text{voltage} \end{matrix}$

→ In case of JFET whether n-channel or p-channel the output characteristic between I_D and V_{DS}

↓
Drain current

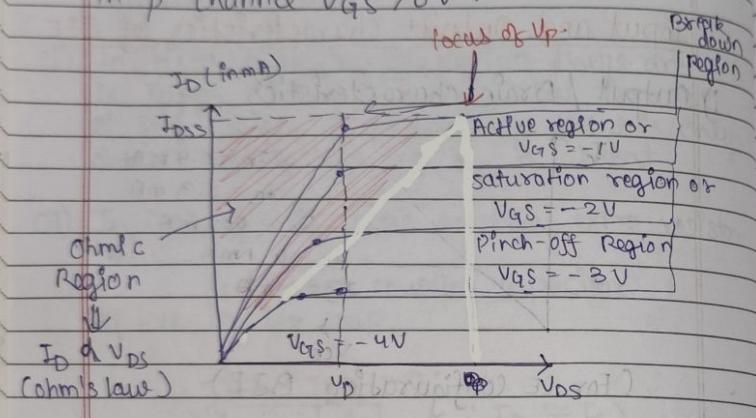
→ Drain to source voltage

In BJT ' I_C ' depends on ' I_B '

$$I_C = f(I_B)$$

controlling current

In FET V_{GS} is controlled in voltage
in n-channel $V_{GS} < 0V$ (lower potential)
in p-channel $V_{GS} > 0V$.



$$I_{DSS} = \text{maximum drain current}$$

$$V_P = \text{pinch-off voltage}$$

Initially $V_{DS} = 0V$ means $I_D = 0V$.
At $V_{DS} \uparrow \rightarrow I_D \uparrow$, depletion width \uparrow

ii) Transfer / Input characteristics

I_D vs V_{GS} plot at keeping constant V_{DS} .

where, $V_{GS} \rightarrow$ Input voltage
 $I_D \rightarrow$ Output current
 $V_{DS} \rightarrow$ Output voltage

In case of BJT, $I_C = f(I_B) \Rightarrow I_C = \beta I_B$
i.e. linear relationship between ' I_C ' and ' I_B '
Amplification factor
controlled variable

In JFET, no linear relationship between I/P and O/P, i.e. $I_D = f(V_{GS})$

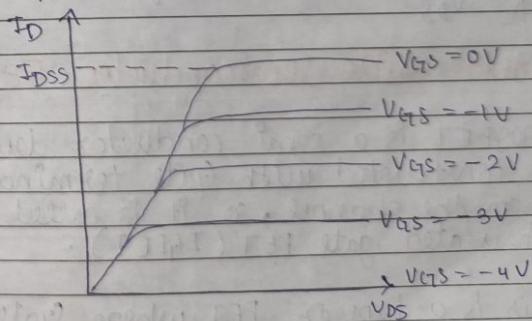
$$I_D = I_{DSS} \left(1 - \frac{V_{GS}}{V_P} \right)^2$$

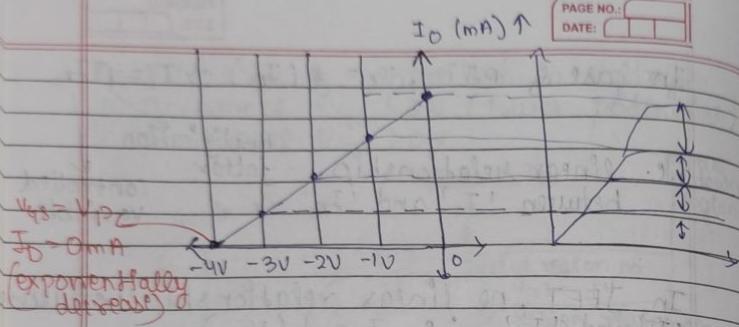
$V_{GS} \uparrow \rightarrow I_D \uparrow$
(i.e. exponentially)

How we calculate I_D ?

$$1) I_D = I_{DSS} \left(1 - \frac{V_{GS}}{V_P} \right)^2$$

2) Using O/P or drain characteristics





We know I_D v/s V_{GS} is non-linear
Draw the vertical lines in each V_{GS} points
or V_P points.

Why non-linear?

- If we see output characteristics
- If we decreasing V_{GS} (making it more -ve)
 - ○ ○
- The vertical spacing decrease.
- This means V_{GS} decreasing is not same as $I_D \sim V_{GS}$.

Metal Oxide Semiconductor - FET :-

- MOSFET is a semi-conductor device which is constructed with Gate terminal insulated from the channel, so it is called as insulated gate FET (IGFET).
- This is a type of FET where Gate is made up of SiO_2 layer and metal is used to have contacts, so it is named as MOSFET.

This is a type of FET where Gate is made up of SiO_2

- In MOSFET there are four terminals
 - Source (S)
 - Gate (G)
 - Drain (D)
 - Substrate (SS)

→ Substrate is a large block semi-conductor on which source, gate & drain are created.

- It can be used as 4 terminal devices or 3 terminal devices.

↓
Source is shorted with substrate

- Between the source to drain there is a presence of channel.

- The channel may be n-type or p-type.

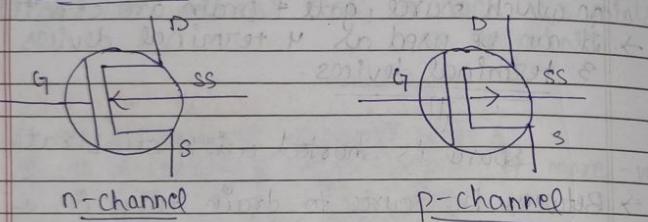
→ In n-channel MOSFET substrate is p-type, source & drain are n-type.

→ In p-channel MOSFET substrate is n-type and source & drain are p-type.

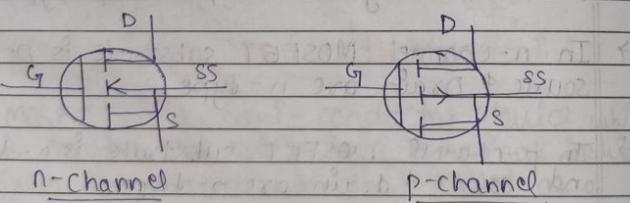
→ The channel may be initially present or may be later created by suitable supply

- The channel is initially present or may be later to be created by suitable supply.
- If the channel is initially present then it is Enhancement MOSFET (E-MOSFET).
- Here input junction is also reverse biased (i.e. $I_g = 0A$).

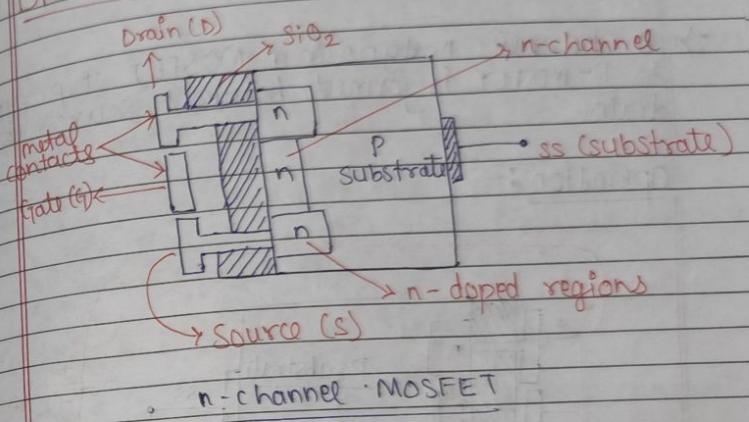
D-MOSFET



E-MOSFET



DMOSFET :-



- In this type of MOSFET the channel is initially present.

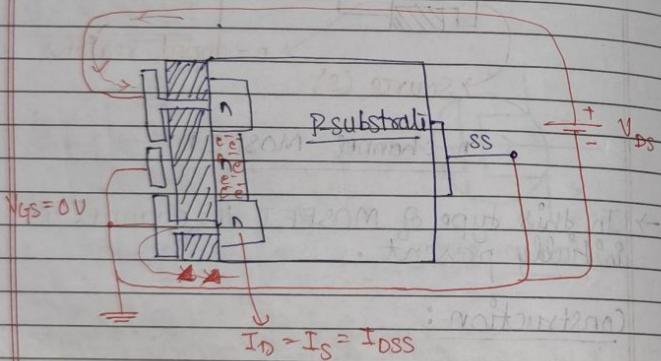
Construction :

- The large block of semi-conductor is known as substrate (n-type in p-MOSFET & p-type in n-MOSFET) is taken.
- On the substrate source & Drain are formed.
- Source and Drain are n-type in n-MOSFET & p-type in p-MOSFET.
- A SiO_2 layer forms the gate region.

→ The metal contacts are taken from each terminal.

→ A channel n-type in n-MOSFET + p-type in P-MOSFET is formed between source to drain.

Operation :-



→ Let us consider n-channel D-MOSFET.

→ Substrate is shorted to source to use as 3-terminal devices.

Case-I :- ($V_{GS} = 0V$, $V_{DS} > 0$)

→ Under this condition the '-'ve terminal of V_{DS} connected to source will repel the e^- while the '+'ve terminal connected to drain attract e^- .

→ Due to presence of channel current flow occurs.

→ As V_{DS} is increased then current increases to a certain value. After that saturates.

→ The maximum current of I_D attained where $V_{GS} = 0V$ is known as Drain to Source saturation current I_{DSS} .

Case-II :- ($V_{GS} < 0$, $V_{DS} > 0$)

→ When V_{DS} is +ve then maximum current will flow when $V_{GS} = 0V$.

→ Now if $V_{GS} < 0$, -ve terminal of V_{GS} is connected to Gate.

→ It will repel e^- from channel. So channel width decreases.

→ Due to decrease in channel, drain current decreases.

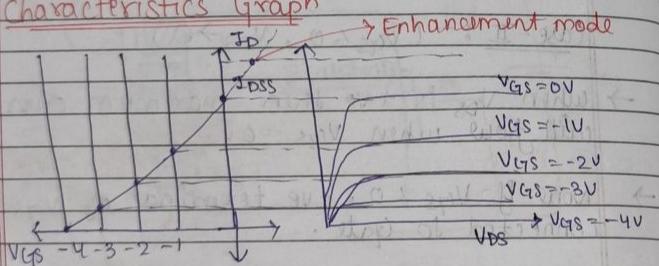
→ At a particular value of V_{GS} , $I_D = 0$, known as pinch off voltage.

→ Here, as channel gradually decreases it is known as depletion mode of operation of D-MOSFET which is the same as of JFET.

case - III :- ($V_{GS} > 0$, $V_{DS} > 0$)

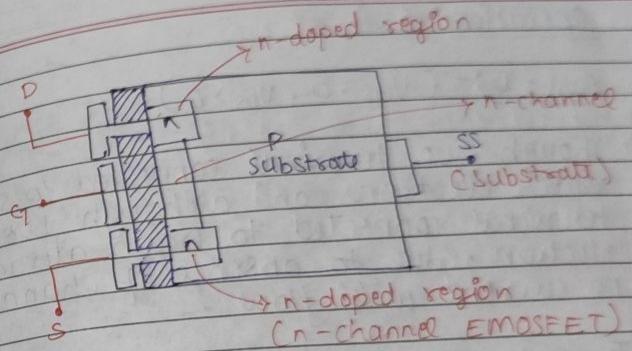
In this condition the terminal is connected to gate that will attract electrons and accumulate at channel by which channel width increase (i.e. I_D increases). This is known as Enhancement mode at operation. It is violating the name so this mode is not used.

Characteristics Graph



Enhanced-MOSFET (E-MOSFET) :-

In this type of MOSFET the channel is initially absent and it can be created by giving suitable input supply.



Construction :-

- A large block of semi-conductor is known as substrate, n-type in P-MOSFET & p-type in N-MOSFET is taken.
- On the substrate source & drain are formed.
- Source & Drain are n-type in n-MOSFET & p-type in P-MOSFET.
- A SiO_2 layer forms the Gate region.
- The metal contacts are taken from each terminal.
- The channel is initially absent and later will be created by suitable supply.

Operation:-

Case - I :- ($V_{GS} = 0$, $V_{DS} \geq 0$)

- Though -ve terminal connected to source repels electrons and although +ve terminal connected to Drain attracts electron, due to absence of channel, no current will flow.
- To make the current flow first ~~flow~~ the channel is to be created.

Case - II :- ($V_{GS} < 0$, $V_{DS} \geq 0$)

- The channel is of n-type, channel can be created when e's are deposited near gate.
- Now giving -ve supply to V_{GS} the e's are repel not accumulated near gate that can be current flow.

Case - III :- ($V_{GS} > 0$, $V_{DS} \geq 0$)

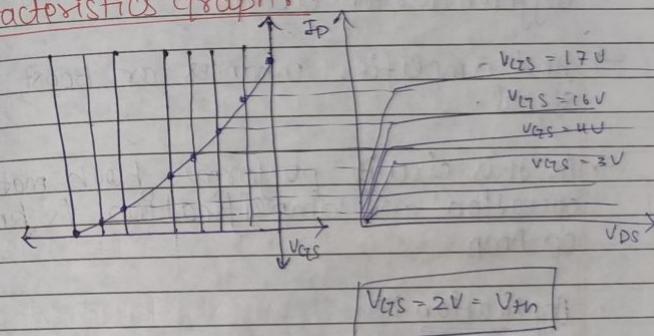
- The +ve supply at Gate accumulates e's near gate, so channel starts to create.
- The channel is completely created at a particular value of a V_{GS} after which current flow starts

→ This voltage is known as threshold voltage.

→ Out of total V_{GS} supply threshold voltage (V_{th}) amount is used to create the channel rest is used to drive the current.

$$I_D = k(V_{GS} - V_{th})^2 \quad (\because k = \text{constant})$$

Characteristics Graph :-



Operational Amplifier (OpAmp) :-

An op-Amp is a multistage very high gain direct coupled differential amplifier.

- The word operational stands for various mathematical operation like addition, subtraction, multiplication, integration, differentiation etc.
- An amplifier enhances or boost the input signal.
- As this circuit performs both mathematical operation and amplification, is known as Op-Amp.

Application :-

- The application of op-Amp is used for designing filters & oscillator circuits.

Characteristics :-

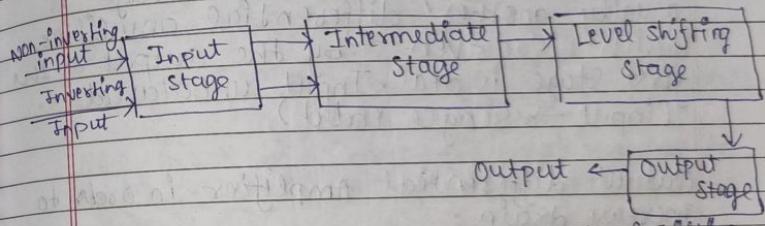
- High Input impedance (ideally ∞)
- Low output impedance (ideally 0)
- High bandwidth
- High differential gain

→ High value of CMRR (Common Mode Rejection Ratio)

→ High slew rate

→ Stabilized output

Block Diagram



Input Stage

- Dual Input
- Balanced output
- Differential
- Amplifiers

Intermediate Stage

- Dual Input
- Unbalanced output
- Differential
- Amplifier

Level shifting stage

- Emitter follower with constant source.

Output Stage

- Complementary symmetry
- Push-Pull Amplifier

→ The block diagram of op-Amp consists of 4 stage direct coupled Amplifier in cascade.

→ The first stage / Input stage is double ended high gain differential Amplifier with a constant current source (to increase value of CMRR)

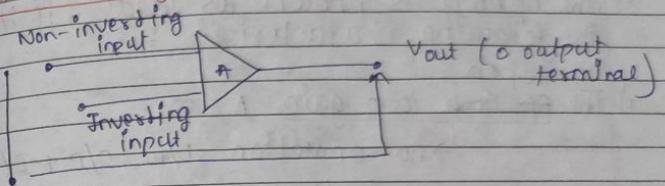
→ The second stage / intermediate stage is usually another differential amplifier, which is driven by the output of the first stage is ideal. Input unbalanced (Input → single ended)

Output differential Amplifier in order to increase drain.

→ The third stage / Level shifting stage is usually emitter follower circuit in order to shift the DC level at the output of the intermediate stage.

→ The final stage / output stage is usually a push-pull complementary. This stage increases the output supply voltage swing and current supplying capability of amplifier.

Schematic symbol of Op-Amp



$$V_{in} \text{ or } V_d = V_1 - V_2$$

$$V_{out} = A(V_{in}) = A(V_1 - V_2)$$

→ It consists of two Input & Output signals.

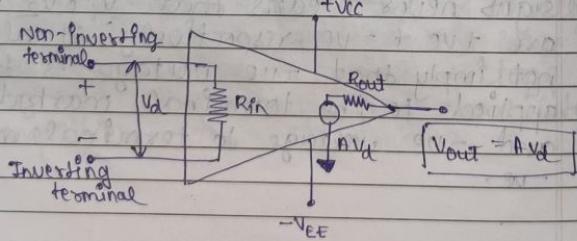
Here Input are (+ve) and (-ve) marked to indicate non-inverting and inverting respectively.

→ The signal applied to (+ve) input appears with the same polarity and Amplifier are the output, while an Input applied to the (-ve) terminal appears amplified but inverted at the output. (+ve & -ve signs never means that V_1 & V_2 voltages are +ve & -ve respectively. It also does not imply that +ve voltage is to be applied to the terminal marked +ve and -ve voltage to terminal marked -ve.)

Ideal OP-Amp :-

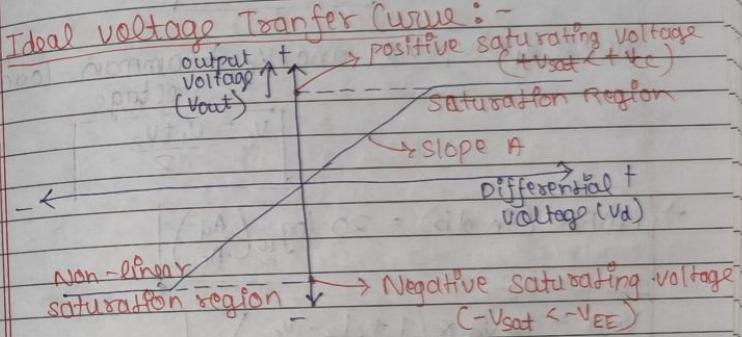
- The OP-Amp is known as Ideal, if it has the following characteristics :
- open loop gain $A = \infty$.
- 1) The OP-Amp loop gain $A = \infty$.
 - ↳ no connection b/w O/P + I/P
 - no feedback
- 2) Input resistance is ∞ .
- 3) Perfect Balance
- 4) Infinite frequency bandwidth.
- 5) CMRR is infinite
- 6) Slew rate is Infinite.
- 7) Output voltage is zero when Input voltage is zero. (Offset voltage is $= 0$.)

Equivalent Circuit of Op-Amp :-



→ The output voltage $V_{out} = A V_d = A (V_1 - V_2)$
 where, $A \rightarrow$ Large signal voltage gain
 $V_d \rightarrow$ Differential Input voltage
 $V_1 + V_2 \rightarrow$ Input voltages at non-inverting + inverting terminals respectively w.r.t ground.

Ideal voltage Transfer Curve :-



→ The curve drawn b/w V_{out} and Input V_d keeping Gain (A) constant represents the equation $V_{out} = A V_d = A (V_1 - V_2)$ Graphically is known as Ideal Voltage-transfer curve. (Here, offset voltage is assumed to be zero.)

→ This transfer curve gives the idea that the output voltage cannot exceed the +ve and -ve saturation voltage.

Common Mode Rejection Ratio :- (CMRR)

→ It is ratio of differential voltage gain to common mode voltage gain.

$$\rightarrow \text{It is given as: } CMRR = \frac{Ad}{Ac}$$

Here, $V_d = V_1 - V_2$ and $V_c \rightarrow$ common load voltage

$$V_c = \frac{V_1 + V_2}{2}$$

$$\rightarrow CMRR (\text{in dB}) = 20 \log_{10} \left(\frac{Ad}{Ac} \right)$$

$$V_{out} = Ad V_d \times \left(1 + \frac{1}{CMRR} \cdot \frac{V_c}{V_d} \right)$$

Q1 A differential DC Amplifier has Differential mode Gain $Ad = 100$ & Common mode Gain (Ac) = 0.01, what is CMRR in db.

$$CMRR = 20 \log_{10} 10^4$$

$$= 80 \text{ dB}$$

For a given Op-Amp $(CMRR = 10^5 \text{ & } Ad = 10^5)$
Determine Ac of op-amp?

$$CMRR = \frac{Ad}{Ac}$$

$$\Rightarrow [Ac = 1]$$

Q1 A differential Amplifier has $V_1 = 10 \text{ mV}$ & $V_2 = 8 \text{ mV}$, $Ad = 60 \text{ dB}$ & CMRR of 80 dB. Find Output voltage (V_{out}) = ?

$$V_d = V_1 - V_2 = 1 \text{ mV} = 10^{-3} \text{ V}$$

$$V_c = \frac{V_1 + V_2}{2} = \frac{18}{2} \text{ mV}$$

$$CMRR = 80 \text{ dB}, Ad = 60 \text{ dB}$$

$$\downarrow 10^{\frac{80}{20}} \quad \text{Anti-log} \rightarrow 10^{\frac{50}{20}} = 10^3$$

$$V_{out} = 10^3 \times 10^{-3} \left(1 + \frac{1}{10^4} \times \frac{1}{10^3} \right)$$

$$= 10.0095 \text{ V}$$

Q2 Find % of error in output voltage and the error voltage.

$$\text{error voltage} = V_{out} - Ad V_d$$

$$= 1.0095 - 1 = 0.00095$$

$$\frac{V_{out} - V_{out} + Ad V_d}{V_{out}} = \frac{Ad V_d \times 100}{V_{out}}$$

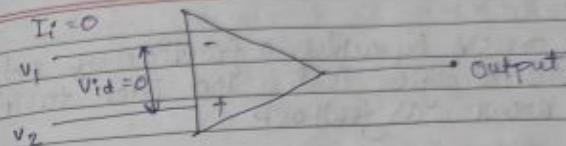
$$= 0.00095 \times 100$$

$$1.00095$$

$$= 0.095 \text{ V}$$

Virtual Ground Concept :-

- This is a concept which is practically not possible in Op-Amp. Hence, it is applicable to Ideal Op-Amp.
- In ideal Op-Amp Input Impedance is ∞ , so, there is no current in Op-Amp.
- Again there is 'no' differential gain in Ideal ~~Op~~ Op-Amp.
- It happens when there is no difference b/w inputs at two terminal.
- i.p. $V_{id} = 0$
- So, the two input terminals are virtually grounded.
- So according to this concept there is no input current and no input differential voltage to the op-amp.



Slope Rate (SR) :-

- It is the rate, which output of op-amp changes in volts/time change in us.

$$SR = \frac{\Delta V_o}{\Delta t} \text{ V/us}$$

Open loop Op-Amp configuration :

- It means there is no connection b/w input and output terminals either directly or by any network.

- It means that the output signal is not fed back in any form as part of the input signal.

Closed loop Op-Amp Configuration :-

- An amp that uses feedback is called as feedback amplifier and sometimes referred to as a closed loop between the input + output.

Feedback :-

→ The process by which a fraction of output of device / amplifier is injected back to its input is known as feedback.

→ Generally feedbacks are two types :

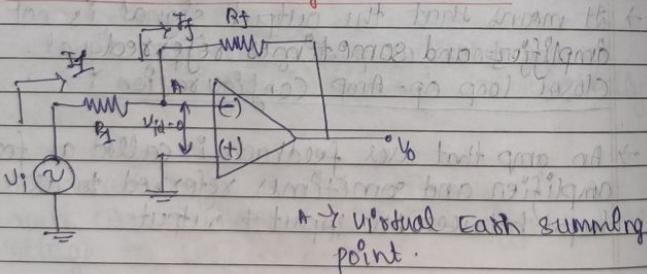
- +ve feedback
- ve feedback

→ The closed loop configuration is considered for most practical application for op-amp because provides stable, linear and controllable gain.

→ There are different op-amp configurations as

- Differential Amplifier
- Inverting Amplifier
- Non-Inverting Amplifier

OP-Amp as Inverting Terminal :-



→ An inverting amplifier is a closed loop op-amp configuration in which the output is opposite in phase to the input and the gain is $-\frac{R_f}{R_1}$.

→ Here, the Input is given to the inverting terminal while non-inverting terminal is grounded.

By virtual ground concept, two terminals are at same potential.

$$V_A = 0 \quad I_s = I_f$$

$$V_1 - 0 = 0 - V_o \quad R_1 \quad R_f$$

$$\Rightarrow V_o = \left(\frac{R_f}{R_1} \right) V_1$$

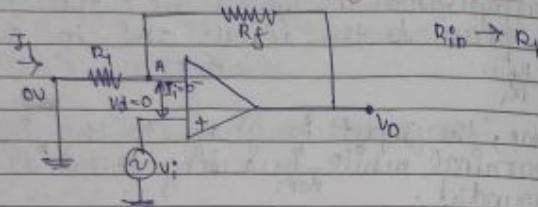
$$\Rightarrow A_v = \frac{V_o}{V_1} = -\frac{R_f}{R_1}$$

* If $R_f = R_1$, then $V_{out} = -V_i$; i.e., the invert of the input is obtained at the output.

Op-Amp has Inverting Amplifier:

An inverting amplifier is a closed loop op-amp configuration in which the output is opposite in phase to the input and the gain is $-\frac{R_f}{R_1}$.

Op-Amp as Non-Inverting Amplifier:-



→ A Non-Inverting Amplifier is a closed loop op-Amp config. in which the output is in same phase with the Input and the gain is $1 + \frac{R_f}{R_1}$.

→ Here, Input is given to non-inverting and inverting terminal is grounded.

→ By virtual ground concept,

$$V_A = V_1$$

Now, $I_1 = I_f$

$$\frac{0 - V_1}{R_1} = \frac{V_1 - V_o}{R_f}$$

$$\Rightarrow \frac{V_o}{R_f} = \frac{V_1 + V_1}{R_f}$$

$$\Rightarrow V_o = V_1 \left[1 + \frac{R_f}{R_1} \right]$$

$$\Rightarrow V_o = V_1 \left[1 + \frac{R_f}{R_1} \right]$$

Q) Design a non-inverting amplifier circuit that is capable of providing voltage gain of 10. (Assume Resistor should not exceed 30 kΩ) in ideal OpAmp.

$$A = 1 + \frac{R_f}{R_1}$$

$$10 = 1 + \frac{R_f}{R_1}$$

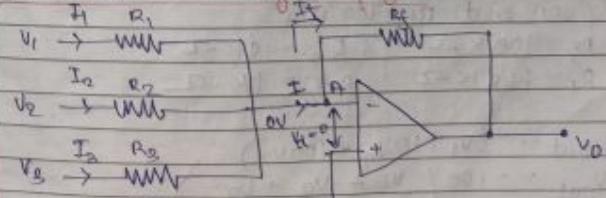
$$\Rightarrow \frac{R_f}{R_1} = 9$$

$$\Rightarrow R_f = 9 R_1 \quad \text{so, } \frac{R_f}{R_1} = \frac{1}{9} \approx 3 \text{ k}\Omega$$

Q) An inverting amplifier has $R_f = 500 \text{ k}\Omega$ and $R_1 = 5 \text{ k}\Omega$. Determine the amplifier circuit voltage.

$$A_v = -\frac{R_f}{R_1} = -\frac{500}{5} = -100$$

Adder or Summing Amplifier:-



→ Here, summing means output is on the form of sum of its inputs.

Three inputs are connected by virtual ground concept $V_A = 0V$.

$$\text{Now, } I_f = I_1 + I_2 + I_3$$

$$\frac{0 - V_o}{R_f} = \frac{V_1 - 0}{R_1} + \frac{V_2 - 0}{R_2} + \frac{V_3 - 0}{R_3}$$

$$\Rightarrow V_o = -R_f \left[\frac{V_1}{R_1} + \frac{V_2}{R_2} + \frac{V_3}{R_3} \right]$$

If $R_f = R_1 = R_2 = R_3$ then

$$V_o = [V_1 + V_2 + V_3]$$

Q) Design an Adder circuit using an Op-Amp to get the output expression as

$$V_{out} = -(V_1 + 10V_2 + 100V_3)$$

where V_1, V_2 and V_3 are the inputs

Given that $R_f > 100 K\Omega$

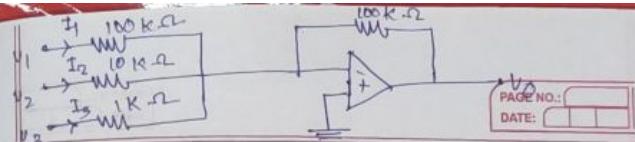
$$R_f = 100 K\Omega, R_2 = 10 K\Omega$$

$$R_1 = 100 K\Omega, R_3 = 1 K\Omega$$

$$V_{out} = -(V_1 + 10V_2 + 100V_3)$$

$$V_{out} = -100 \left(\frac{V_1}{100} + \frac{V_2}{10} + V_3 \right)$$

PAGE NO.:
DATE:



$$V_o = -I_f \left[\frac{V_1}{R_1} + \frac{V_2}{R_2} + \frac{V_3}{R_3} \right] = -a + b - c = b - a - c$$

Q) An Op-Amp assuming as summing circuit
feedback ~~resistor~~ Resistor $R_f = 12 K\Omega$, and the
resistance of input sides are $R_1 = 12 K\Omega$,
 $R_2 = 9 K\Omega$, $R_3 = 3 K\Omega$. The corresponding inputs
are $V_1 = +9V$, $V_2 = -3V$, $V_3 = 1V$. Non-inverting
terminal is grounded. Calculate V_{out} ?

Q) Sketch the circuit of summing circuit
using Op-Amps to get

$$V_o = -6 \left[\frac{V_1}{6} - \frac{V_2}{3} + \frac{V_3}{2} \right]$$

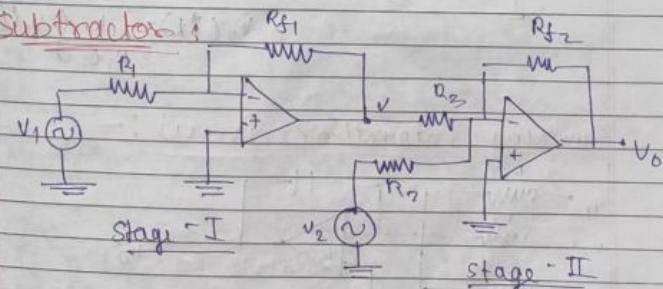
$$V_o = V_1 + 2V_2 - 3V_3$$

$$R_f = 6 K\Omega$$

$$R_2 = 3 K\Omega$$

$$R_3 = 2 K\Omega$$

H) Differentiator :-



Here, $V = -\frac{R_{f1}}{R_1} V_1$ (Stage - I)

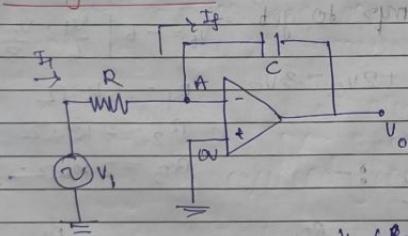
Stage - II (Summing Amplifier circuit)

$$V_o = R_{f2} \left[\frac{V}{R_3} + \frac{V_2}{R_2} \right]$$

$$\Rightarrow V_o = -R_{f2} \left[\frac{V_2}{R_2} - \frac{R_{f2}}{R_3 R_1} V_1 \right]$$

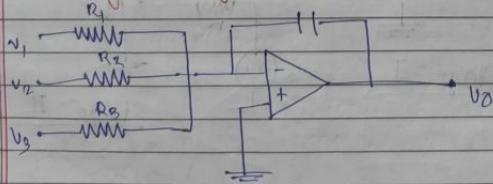
~~Output~~

Integrator :-



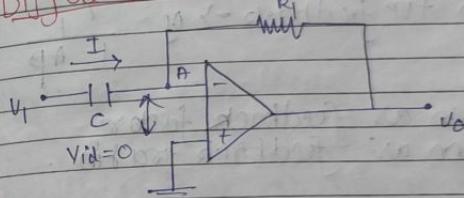
$$V_o(t) = -\frac{1}{RC} \int V_i(t) dt$$

Summing Integrator circuit :-



$$V_o(t) = -\frac{1}{C} \int \left(\frac{V_1(t)}{R_1} + \frac{V_2(t)}{R_2} + \frac{V_3(t)}{R_3} \right) dt$$

Differentiator :



$$V_o(t) = -RC \frac{dV_i(t)}{dt}$$

Feedback :

Positive : feedback

When energy of device / Amp is in phase with input signal, it is +ve feedback.

→ Regenerative / in-phase / direct feedback.

→ It increases the gain of amplifier.

→ It is used in oscillator circuits.

Negative : (de-generative or reverse)

When feedback energy of Amplifier is 180° out of phase with the input signal and thus opposes it. Then it is known as negative feedback. It is used in Amp. circuit.

$$A_v = \frac{V_o}{V_i} \quad (\text{Voltage gain})$$

$$\text{Gain with feedback } \rightarrow A_f = \frac{1}{1 + AP}$$

$$\text{Gain with +ve feedback } \rightarrow A_f = \frac{1}{1 - AP}$$

βA is known as feedback factor
 β is known as feedback ratio.

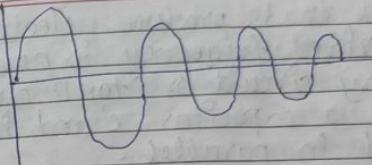
Oscillator :-

- An oscillator is the basic element of all AC signal sources and generates sinusoidal signals of known frequency and Amplitude
- An oscillator is just an electronic circuit which converts DC-Energy into AC-Energy of required frequency.

Types of Electrical Oscillations :-

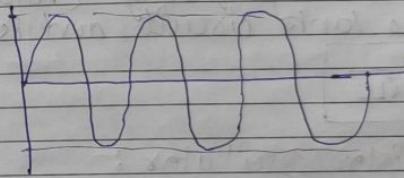
- Damped Oscillation
- Undamped Oscillation
- Damped oscillation -

The electrical oscillations in which Amplitude decreases with time, is known as damped oscillation.

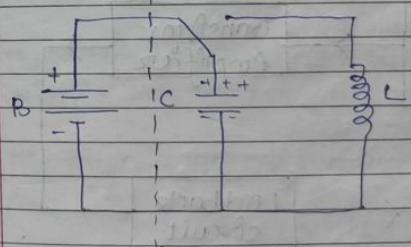


ii) Undamped Oscillation -

The electrical oscillations in which Amplitude does not change with time is known as undamped oscillation.



Oscillatory Circuit :-

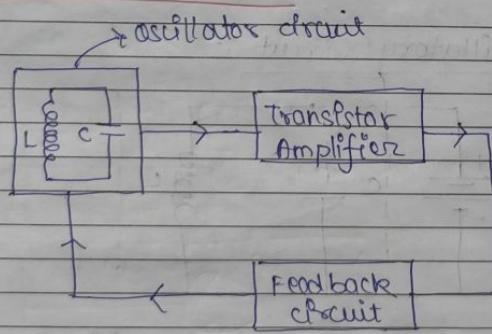


Oscillatory circuit

- PAGE NO.:
DATE:
- A circuit that produces electrical oscillation of a desired frequency is known as oscillatory circuit or tank circuit. It contains a capacitor 'C' and Inductor coil 'L' connected in parallel.
 - The frequency of oscillation produced by this oscillatory circuit is determined by the value of 'C' and 'N'.
 - The actual frequency of oscillation is the resonant frequency (natural frequency) of the tank circuit and is given by,

$$f_r = \frac{1}{2\pi\sqrt{LC}}$$

Transistor Oscillator :-



- PAGE NO.:
DATE:
- A transistor can work as oscillator to produce continuous undamped oscillations and hence the name is ~~known as~~ of any desired frequency. If oscillatory & feedback circuits are properly connected to it.

There are different oscillators employed in electronic circuit :-

- 1) Tuned Collector oscillator
- 2) Hartley oscillator
- 3) Colpitt's oscillator
- 4) Phase shift oscillator
- 5) Wien bridge oscillator
- 6) Crystal Oscillator

Barkhausen Criteria:-

The Barkhausen criteria is the fundamental condition required for an electronic circuit to generate continuous oscillations.

There are two conditions of Barkhausen criteria :

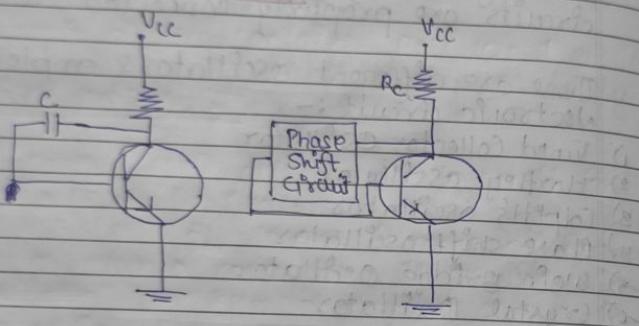
- 1) The magnitude of loop gain must be equal to unity.

$$|AB|=1$$

(product of Amplifier gain (A) + feedback factor (B))

2) Total phase shift around the feedback oscillator circuit β is 0° or 360° .

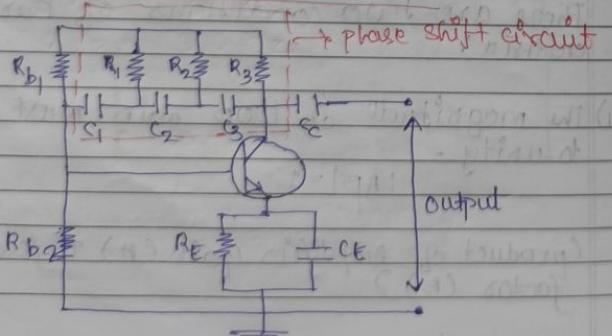
Phase Shift Oscillator :-



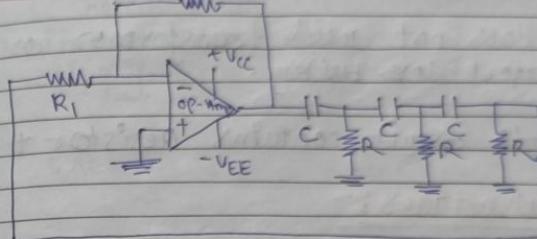
$$\tan \phi = \frac{1}{2\pi f C R}$$

$$\rightarrow \phi = \tan^{-1} \frac{1}{2\pi f C R}$$

R-C phase shift oscillator:



Phase Shift Oscillator 3-



→ A phase shift oscillator employs an R-C network and is commonly called R-C phase oscillator.

Generally, R_1, R_2, R_3 & C_1, C_2, C_3 are made equal.

Frequency of oscillation:

It can be shown, $R_1 = R_2 = R_3 = R$ and $C_1 = C_2 = C_3 = C$.

The operating frequency (f) is

$$f = \frac{1}{2\pi RC \sqrt{6}}$$

Assume,
 $B = \frac{1}{29}$

$$\text{phase shift} = 180^\circ$$

Also, $|A| \geq 29$

Advantages :-

- It does not need transformer or inductor. Therefore less bulky.
- Simple circuit contains Resistor + capacitor.

Disadvantages :-

- It gives small output, due to small feedback.

Q1 A resistance of $10\text{ k}\Omega$ is connected in series with a capacitor. If an alternating voltage of 1 kHz is applied across the network. Find the value of C for the phase shift of 60° .

$$\tan \phi = \frac{1}{2\pi f C R}$$

$$\phi = 60^\circ$$

$$R = 10\text{ k}\Omega = 10^3 \Omega$$

$$f = 1\text{ kHz} = 1000\text{ Hz}$$

$$\therefore C = \frac{1}{2\pi \times 1000 \times 10^3 \times R}$$

$$C = \frac{1}{2\pi \times 1000 \times 10^3 \times \sqrt{3}} = 0.0092\text{ uF}$$

In a phase shift oscillator ~~the~~ resistor is $10\text{ k}\Omega$ while each capacitor has a value of 0.01 uF . Find the operating frequency of circuit.

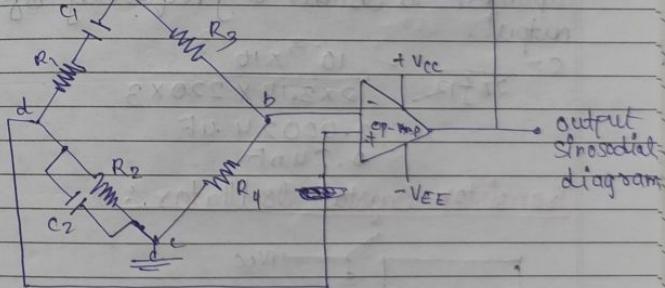
$$f = \frac{1}{2\pi R C \sqrt{3}}, \text{ where, } C = 0.01\text{ uF}$$

$$R = 10\text{ k}\Omega$$

$$f = ?? = \frac{10^{-3} \times 10^6}{2\pi \times 10 \times 10^{-2} \times \sqrt{3}}$$

$$\text{then, put } \tan \phi = \frac{1}{2\pi f C R}$$

Wein-Bridge Oscillator :-



$$f = \frac{1}{2\pi \sqrt{R_1 C_1 R_2 C_2}}$$

$$\left. \begin{array}{l} R_1 = R_2 = R_3 = R \\ C_1 = C_2 = C_3 = R \end{array} \right\}$$

$$f = \frac{1}{2\pi R C}$$

Advantages :-

- It has far better stability
- Output is constant
- Overall gain is high
- Simple & Easy.

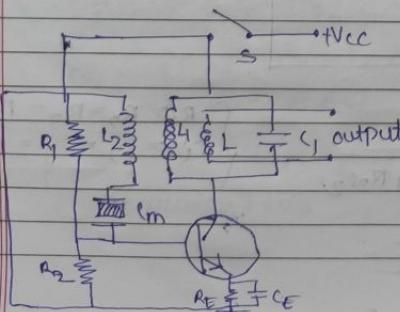
Disadvantages :-

- It cannot be used for generating high frequency. (i.e. 1 MHz)

Q) In a R-C phase shift bridge oscillator, $R_1 = R_2 = 220\text{ k}\Omega$. Determine the value of capacitor to obtain a frequency of 3 kHz output.

$$C = \frac{1}{2\pi f R} = \frac{10^{-3} \times 10^{-3}}{2 \times 3.14 \times 220 \times 3} = 0.00024 \mu\text{F} = 0.24 \text{nF}$$

Transistor Crystal Oscillator :-



→ When a constant high frequency (25 kHz to 15 MHz) for radio broadcast Png transmitters is required, a transistor crystal oscillator is always preferred.

→ A tank circuit $L_1 - C_1$ is placed in the collector and crystal is connected in the base circuit through a feed back coil L_2 where L_2 is inductively coupled to the coil L_1 .

The natural frequency of $L_1 - C_1$ circuit is made nearly equal to the natural frequency of crystal.

Another coil $B'L'$ is inductively coupled to L_1 to obtain output.

→ Entire circuit starts operating at the natural frequency of crystal. Hence the name is crystal oscillator.

Advantages :-

- As frequency of crystal is independent of temperature these oscillators have a high order of frequency stability.

Disadvantages :-

→ Frequency of oscillations cannot be changed if desired.

Q If $L = 800 \text{ mH}$, $C = 0.01 \text{ pF}$, $R = 1000 \Omega$, $C_m = 20 \text{ pF}$ are the various values of an AC equivalent circuit of a piezoelectric crystal. Determine f_s and f_p of the crystal.

$$f_s = \frac{1}{2\pi\sqrt{LC}} = 1779.40 \text{ kHz}$$

$$C_T = \frac{C \times C_m}{C + C_m} = 9.975 \times 10^{-9} \text{ pF}$$

$$f_p = \frac{1}{2\pi\sqrt{L C_T}} = 1779.85 \text{ kHz}$$