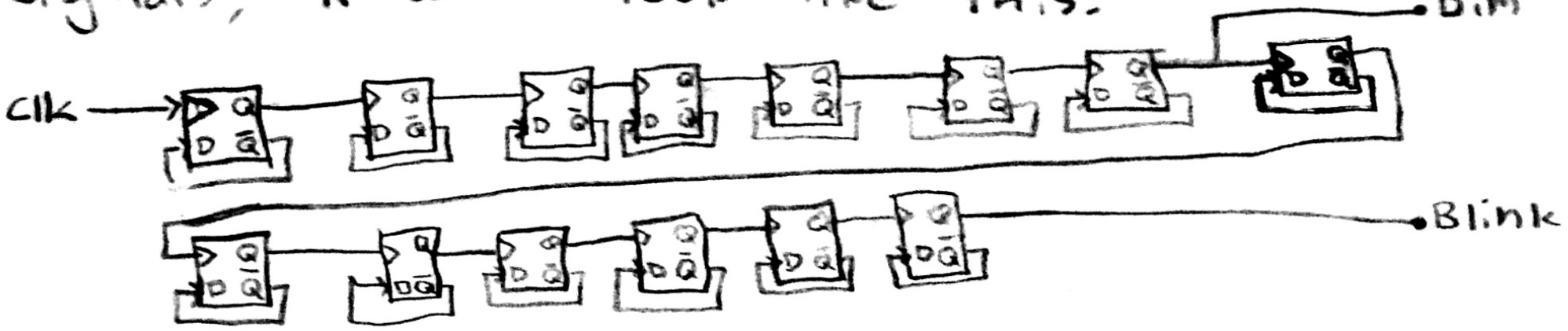
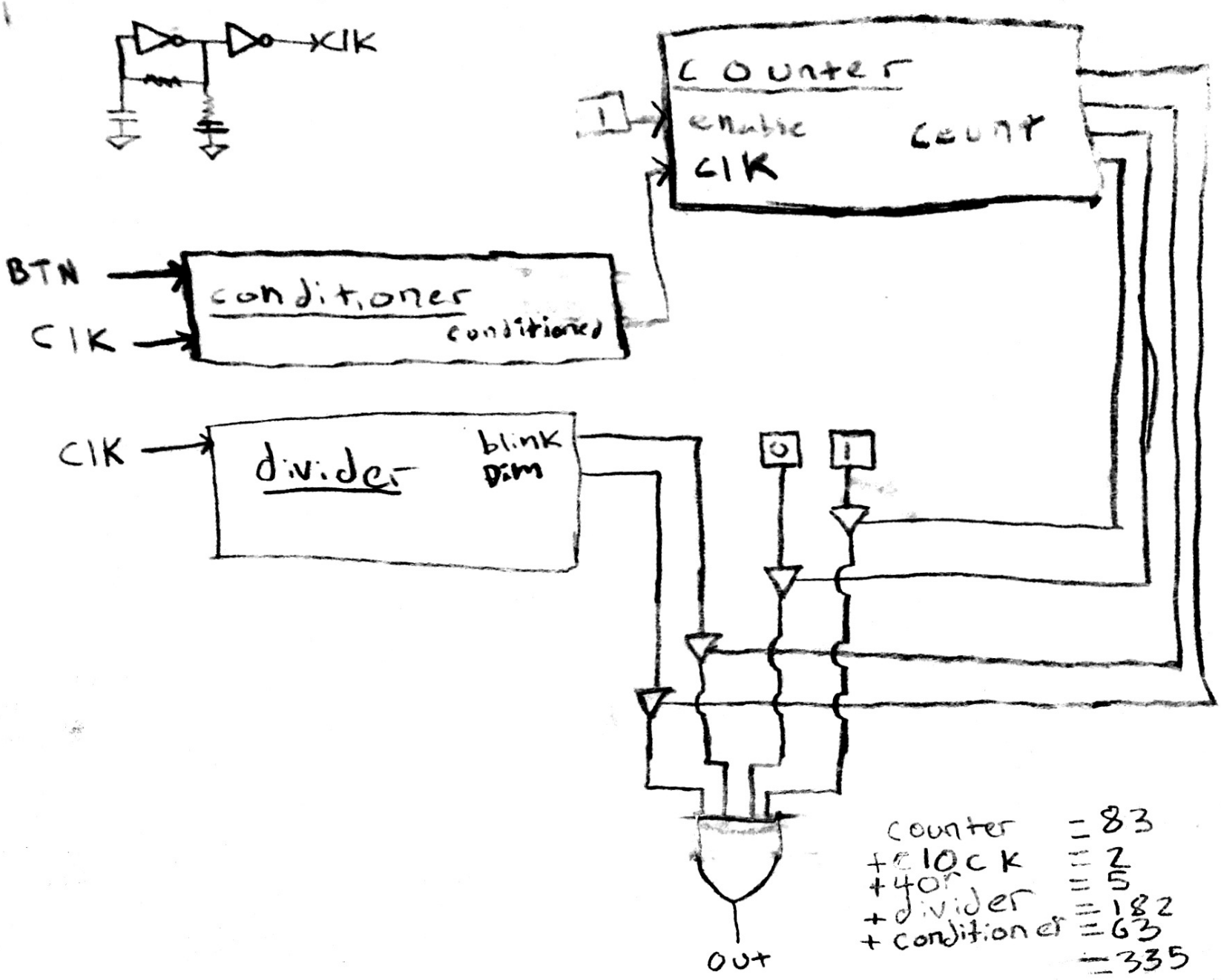
The mother of all clock dividers. Because the 2 operational modes that aren't on or off can both be thought of as square waves with duty cycles of 50% at a frequency lower than the clock they can both be generated using a series of clock dividers. Taking clock as an input and outputting the Dim and blink signals, it would look like this.

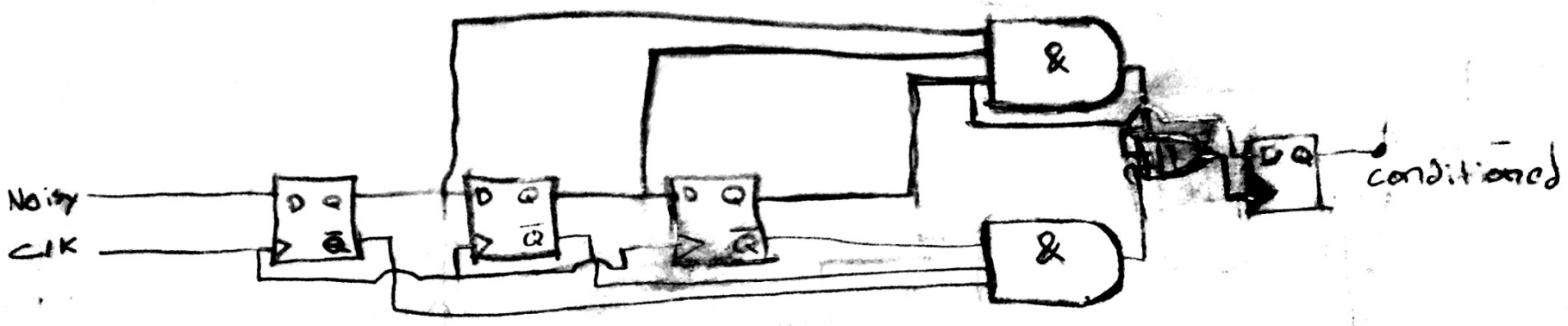


14 x 13 gates = 182 gates



counter = 83
+ clock = 2
+ 4or = 5
+ divider = 182
+ conditioner = 63
= 335

Input conditioner. To avoid debounce related issues a signal conditioner is necessary. Taking in a clock signal and an unconditioned input and outputting the conditioned signal. Sustained depression is detected by sampling the signal at 3 times and checking their equality. If they're equal the signal is shifted out.



	4x flip flop	= 52 gates
+	2 x 3 And	= 8 gates
+	2 Or	= 3 gates
		= 63 gates