Schmitt-Trigger-based Low Power SRAM implemented using 45-nm CMOS Technology

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***Abstract*—This paper presents a Schmitt-trigger-based SRAM with a separated read port, which significantly improves read static noise margin (RSNM) and consumes low energy. Post-layout simulation results show that the proposed design performed better than the conventional 6T SRAM cell. The SNM of the designed cell is 1.16 mV higher than the conventional 6T SRAM cell in write mode, and 232.37 mV and 207.46 mV in read mode 1 and 0, respectively. The impact of the process, voltage, and temperature variations on cell performance parameters such as read, write and hold SNM, power per access, power per bit, delay, and energy per bit was investigated. Aside from this, the DNM of the cell was also measured to determine the noise tolerance of the cell during the write operation. Monte Carlo simulation results verified how robust the proposed cell is. The design was implemented in a 45-nm technology in which the cell occupies 4.53×4.53 μm^2 and the system is 568.55×568.55 μm^2. This cell consumes only 0.396 fJ, which is lower than the energy per bit consumed on the 6T conventional cell which is 7.265 fJ. All-corner simulation results show that the proposed cell is suitable for low-power applications.**

***Index Terms*—SRAM, energy per bit, static and dynamic noise margin, PVT testing, Monte Carlo**

I. Introduction

Memories are necessary for a fast-paced digital systems environment. The storing of data and program instructions takes up a considerable percentage of the silicon area in many modern digital ICs. One of the types of memory is the Static Random Access Memory (SRAM), the SRAMs are random access memory that gives access to any bit of stored data whenever it is needed [1]. SRAM takes up 90% of the overall capacity of a network on chip (NoC) or system on chip (SoC), according to the International Technology Roadmap for Semiconductors (ITRS) 2013 [2].

Along with its substantial area occupancy, SRAM is the dominant consumer of total chip power. As a result, the power consumed by the SRAM determines the total chip power consumption. Thus, an SRAM architecture that consumes the least amount of power is essential [3]. Furthermore, the rapid development in demand for mobile devices and other emerging applications, like implanted medical devices and wireless body sensing networks necessitates a high need for low-power SRAMs [1].

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However, the existing SRAM has an issue with regards to energy consumption as it consumes more power caused by static and dynamic power dissipation, resulting in the frequent replacements of batteries and a reduction in the life span of the devices [3]–[5].

In addition, the design's potential stability issue emerges during the hold and read operations, when the cell is most susceptible to noise and thus, the cell's operation is degraded and reliable-stored data cannot be achieved. Thus, an SRAM cell that can efficiently address the problem of power consumption and stability was designed which will be applicable to any low power applications. The designed cell will also be tested with the help of peripheral circuits. The results will then be compared with the conventional 6T SRAM cell.

II. Schmitt-Trigger-Based SRAM Design

The system view of the proposed Schmitt-trigger-based SRAM is presented in Fig. 1, consisting of twelve blocks, namely 1-kb SRAM array, control circuit, row and column decoder, word line, and column signal block, write driver, column multiplexer, pre-charge, read driver, output multiplexer, and output buffer. The memory array is made up of 11T Schmitt-trigger-based SRAM cells with separated ports for read bit line and write bit lines.

A. Conventional 6T SRAM Cell

The conventional 6T SRAM cell is composed of a cross-coupled inverter along with two access transistors and bit lines (BL and BLB) as reported in Fig. 2. The cross-coupled inverters that are used for data storage are MP201 and MN201 (left-facing inverter) and MP202 and MN202 (right-facing inverter). In addition, the access transistors that control the access to the SRAM cell are MN203 and MN204. During a read operation, the bit lines of the cell are pre-charged to Vdd and the word line is activated. When the word line is asserted, either the bit line or bit line bar pulls down indicating the stored data.

The read operation results in the formation of a voltage divider network that consists of access and pull-down transistors and thereby increases the voltage in the node storing logic '0'. This unintended change in the stored state of the cell during read operation is defined as read failure.

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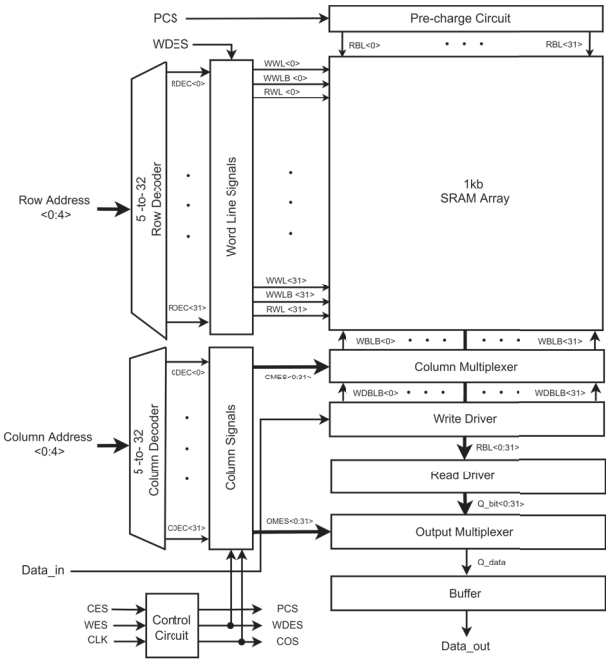

Fig. 1. ST-based SRAM Architecture Design

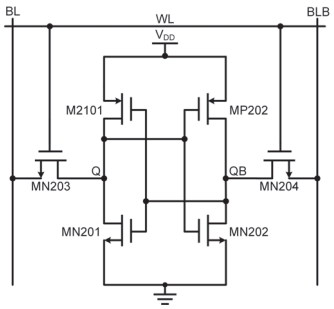

Fig. 2. Conventional 6T SRAM cell schematic diagram

Moreover, the stability of a conventional inverter used in the cell core of an SRAM cell at a low supply voltage is not promising. Furthermore, the degraded characteristics of the conventional inverter result in a high power consumption.

B. Proposed Schmitt-trigger-based SRAM Cell

The cross-coupled inverters of the conventional 6T SRAM cell were replaced by modified Schmitt trigger inverters based on [6]. The modified P-type ST inverter is placed in the left part of the cell core, while the N-type ST inverter is in the right-facing part. The P-type ST inverter comprises transistors MP301, MP302, MP303, and MN301. On the other hand, the N-type ST inverter includes transistors MP304, MN302, MN303, and MN304. These are with access transistors MN305 and MN306 for connecting the cell core to the write bit lines and MN307 for connecting the cell core to the read bit line.

The designers adapted this technique since the Schmitt-trigger inverter has a higher and lower switching point voltage also known as the hysteresis.

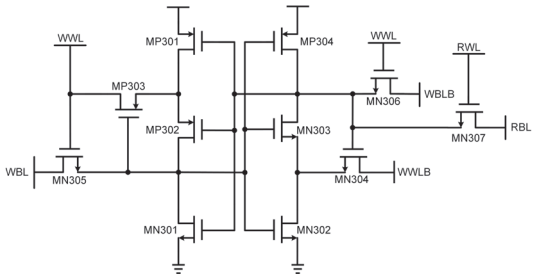

Fig. 3. Schmitt-Trigger-Based SRAM cell with single read port

The hysteresis of a Schmitt-trigger circuit provides a better noise margin and noise stable performance. To emphasize, according to Baker (2010) [7], a better value of noise margin can be achieved with the use of Schmitt-trigger inverters. This is primarily due to the usage of feedback in both inverters, which causes shifting of inverter transfer characteristics. Thus, the modified P and N-type Schmitt-trigger inverters are suitable to achieve a better value of noise margin.

However, this technique, replacing the data storage latch with ST inverters suffers from read disturbance. To address the issue, the designers adapted the separate read port technique which is represented by the transistor MN307 for the read port and transistor MN305 and MN306 for the write ports. The separated single read port helped to enable the hysteresis of the P-type ST inverter during read operation. With both ST inverter's hysteresis during read operation, the read disturbance was resolved. Furthermore, transistors MN304 and MP303 are connected to ground and VDD respectively during a write operation to reduce power dissipation. Moreover, separate read word line (RWL) and write word line (WWL) can be used to access the cell during read and write operations.

C. Read, Write, and Hold Operations

Write Operation

For the write operation, the memory has an initial value of '0' this means that Q is '0' and QB is '1'. During this operation, the write word line (WWL) is set to high and there will be control over the write bit line (WBL) and write bit line bar (WBLB) because they are input ports. These ports are complemented with each other and simply support that in order to write '1', the input data in Q which is '0', is required to overcome. Furthermore, the read word line (RWL) signal is deactivated making the read bit line (RBL) port isolated during the write operation. Let the write bit line bar (WBLB) be put into the ground, hence QB is '1', which results in a potential difference. Thus, it will discharge and as voltage decreases, the left-facing inverter is affected. To simply write, the voltage of the QB (right-facing ST inverter) should be less than the threshold voltage of pull-down (left facing ST inverter) but greater than its pull-up transistors in the P-Type ST inverter. This means that the pull-down transistor is turned off and pull-up transistors are turned on when the pull-up is on (left-facing inverter), hence, the output is '1'. The operation is successfully implemented since the data written is '1'.

TABLE I
READ AND WRITE CYCLE TIMING

	Operation		
Signal	**Write**	**Read**	**Hold**
Write Word Line (WWL)	HIGH	LOW	LOW
Write Word Line Bar (WWLB)	LOW	HIGH	HIGH
Read Word Line (RWL)	LOW	HIGH	LOW
Port			
Write Bit Line (WBL)	HIGH/LOW	-	-
Write Bit Line Bar (WBLB)	LOW/HIGH	-	-
Read Bit Line (RBL)	-	HIGH	-

Read Operation

In the read operation, the read bit line (RBL) signal is pre-charged at the supply voltage. The write word line (WWL) signal is deactivated making the write bit line (WBL) and write bit line bar (WBLB) port isolated from the read operation. The read bit line (RBL) port is considered as the output port during the operation. As the read word line (RWL) is being activated as well as the write word line bar (WWLB), the read operation begins. The access transistors are enabled by read word line (RWL), thus, there will be a connection between the cross-coupled inverter and read bit line (RBL). In the read operation, the content of the SRAM cell will be assessed and identified. Node Q contains a logic '1' and node QB holds a logic '0' before the read operation starts. The voltage in the read bit line (RBL) and node QB creates a voltage difference which results in successfully reading the stored data, which is logic '0' in node QB.

Hold Operation

On the hold operation, the write word line (WWL) and the read word line (RWL) is set to low making all the signals isolated from the cell. It denotes that the cell is inaccessible, the current taken from VDD at this operation is known as idle current. The cross-coupled inverters will keep feeding back to one another. Thus, data will remain in the latch mode. This simply shows the bi-stability property.

Table I summarizes the operation of the proposed ST-based SRAM cell with a separate single read port, taking into account the word line signals and ports.

D. Peripherals

In order to determine the performance of the designed Schmitt-trigger-based SRAM, the array and peripheral circuits were designed and simulated. The array is formed by populating the SRAM cell. On the other hand, the peripheral design consists of the control circuit, row and column decoder, word line, and column signal block, write driver, column multiplexer, pre-charge, read driver, output multiplexer, and output buffer.

1) Control Circuit: The control circuit is composed of clock (clk), control enable signal (CES), write enable signal (WES) as the inputs and the outputs are write driver enable signal (WDES), pre-charge signal (PCS) and control output signal (COS). Basically, the memory read and write operations contains a sequence of steps. The control circuit is in charge of these sequences. The control circuit designed by the researchers used a synchronous approach while considering the Table II.

TABLE II
CONTROL CIRCUIT TRUTH TABLE

Input Signals			**Output Signals**		
Clk	1 period for write and 2 periods for pre-read and read		**Precharge Signal**	0 (pre-charge)	1 (either read or read)
Control Enable Signal (CES)	0 (working)	1 (not working)	**Control Output Signal (COS)**	0 (either write or pre-read)	1(read)
Write Enable Signal (WES)	0 (write operation)	1 (read operation)	**Write Driver Enable Signal (WDES)**	0 (write operation)	1 (either pre-read or read)

Table II shows the operation of the control circuit using the input and output signals. The control circuit generates the precharge signal (PCS) required to operate the pre-charge circuit. Another signal that could be created by the control circuit is the write driver enable signal (WDES) which allows the write driver to operate. This also means that when the write driver enable signal is combined with the row signal, it could create a write word line signal. When the WDES is also combined with the column signal, the specific column multiplexer is also activated. The other signal that the control circuit generates is the COS. This signal is required to combine in the column signal to select the specific output multiplexer.

2) Row and Column Decoder: In this study, the researchers used a 5-to-32 line decoder, which means they used a decoder with a 5-bit input row address, resulting in 32 outputs. To avoid using the 5 input NAND, the coincident decoder was chosen as the design topology. This is because the 5 input NAND has a longer delay and is not deemed to work in the saturation area, therefore it does not switch properly.. The coincident decoder having some k number of inputs has outputs of 2^k. This type of decoder necessitates 2^k NAND gates, with k inputs at each gate. By using two decoders in a two-dimensional system, the total number of inputs per gate can be reduced. In a bi-dimensional matrix method, one decoder is used for row selection and the other for column selection. The Row Decoder is used to select the row of the SRAM array. The unselected row of the row decoder was automatically put into hold mode. The output signal of the row decoder is also employed in the circuit block for word line signals. Moreover, the column decoder is used to select the column. This is also used to choose one of the 32-column and output multiplexers during write and read operations. The unselected column of the column decoder was automatically put into hold mode.

3) Word line and column signals block: The row signal (RDEC) must be high and the write driver enable signal (WDES) must be low in order to write (WWL=1). The write word line (WWL) and write word line bar (WWLB) input data must be complementary to one another; high and low state, respectively. The read word line is in a low state since the mode is in read mode.

The column signal circuit is composed of a write driver enable signal (WDES) which can be either in the low state or high state (active low). The output signals such as the column multiplexer enable signal (CMES) and output multiplexer enable signal (OMES) are in the low state. During this operation,

when the write driver enable signal (WDES) is high during this operation, the column output signal (COS) is high as well. Furthermore, during the write process, the write driver enable signal (WDES), as well as the column output signal (COS) and the output multiplexer enable signal, are all low (OMES). The CMES (column multiplexer enable signal) is turned off.

4) Write driver: The write driver is in charge of writing a certain value into the bit-cell in the study. To write, this write driver must be enabled. The signal from the write driver enables the signal (WDES) to be used to activate this circuit. The write driver circuit includes two output signals that charge or discharge the bit lines, allowing the desired bit to be written into the memory cell. These bit lines are write bit line (WBL) and write bit line bar (WBLB), which are complemented by each other.

5) Column Multiplexer: The column multiplexer used in the study is connected from the write driver enable signal (WDES) to bit lines (WBL and WBLB). This circuit controls whether data from the write driver is used to write bit lines in a specific column. During the write operation, just one of the 32-column multiplexers in the design must be engaged. To explain further, only one column is selected, and the data word to be written goes from the data bus to the desired bit lines.

6) Pre-charge: The read bit line port must be pre-charged in VDD during the read operation for a time duration of 10ns. It is held high before each read operation to make sure that when the data in the cell is read out, it will output the correct data. Because there is only one read-bit line port, only one pre-charge port is required.

The pre-charge circuit is active low since the single PMOS will only be activated when the input is low. When the precharge signal is set to 0, this circuit is triggered (activate low). After the pre-read, there is a potential difference between the read bit line (RBL) and the node in QB. As presented in the schematic, the input data in QB = 0 is inverted which results in Q = 0. In the architecture, 32 PMOS is 2530 used as a pre-charge circuit since the array is composed of 32 columns. The width required for PMOS is 1.2 µm and the length is still fixed at 45nm.

7) Output Multiplexer: During read operations, the output multiplexer is used. This is triggered when the column signal is selected and the operation is in read mode. The operation is in read mode when both the write driver enable signal and the control output signal are high. The study used CMOS pass transistors, as seen in the figure. The widths of the PMOS and NMOS transistors were 3um and 1.5 µm, respectively, with a length of 45nm.

8) Output Buffer: The output buffer is employed to handle a high current coming from the SRAM cells and transfer the required energy to the load. The buffer allocates some settling time in conjunction with the Q data signal. The output buffer's gate level is an eight-stage inverter. Wherein there is a 1:3:3:3:3:3:3:6 ratio between the inverters to drive a 20 pF load.

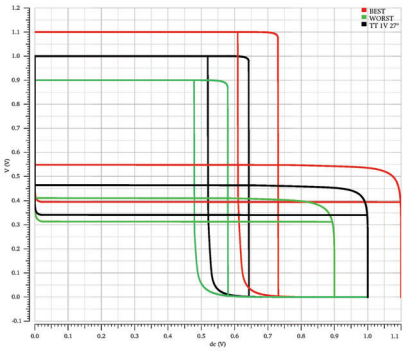

Fig. 4. Hold SNM of the proposed ST-based SRAM Cell

III. Simulation Results

The proposed design is implemented using 45-nm CMOS Technology. The SRAM Architecture Floor Plan as well as the SRAM Cell Layout is shown in Fig. 8 and Fig. 7. The SRAM Architecture has an area of 568.55 µm with a core area of 4.53 µm. The worst-case static noise margin (SNM) of hold 0, hold 1, read 0, read 1 and write are 455.2 mV, 455.1mV, 565.7 mV, 523.3 mV, and 478.2 mV, respectively. Since the design is implemented using the combination of P-type and N-type Schmitt-trigger inverters which produce hysteresis, the Schmitt-trigger-based SRAM cell provides a better noise margin and noise stable performance. The further explanation of three SNM results showing the stability of the cell are shown in the following figures.

Fig. 4 shows three Hold SNM values of the ST-based SRAM Cell. These results are from the best, worst, and typical PVT set-ups. The best case is found at SS 1.1V 27°C with 706.3 mV, while the worst case is found at SS 0.9V 27°C with 455.4mV SNM. For the typical setup, its SNM is found to be with a margin of 478.2 mV. This indicates that in a PVT corner of slow-slow process with 1.1 V and of temperature of 27°C the designed SRAM cell shows best hold ability.

In the Fig. 5, the result shows of Read SNM of three PVT set-ups in which the best PVT corner for SNM is found at slow-fast process with 1.1V and on 75°C with 707.1 mV, while the worst case is found at FF 0.9V and 75°C with 565.7 mV RSNM. For the typical setup, its SNM is found to be with a margin of 636.4 mV. Result shows that in a slow-fast process with 1.1V and at 75°C the designed SRAM Cell will perform read operation best. Thus, RSNM is improved, using the final design of Schmitt-trigger based SRAM cell. The read stability of the final design provides a read-disturb-free process.

The write SNM results are shown in the Fig. 6, like in two previous SNM results, wherein three PVT set-ups were shown for write SNM, the best case is found at slow-slow process 1.1V and on 0°C with 555.6 mV, while the worst case is found at FS 0.9V and 0°C with 478.2 mV SNM. For the typical setup, its SNM is found to be with a margin of 496 mV. Based on the results, in a process of slow-slow with 1.1V and at 0°C the designed SRAM cell performs write operation best. Hence, it is evident that the final design showcased good stability to

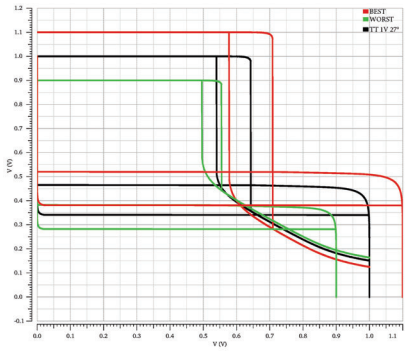

Fig. 5. Read SNM of the proposed ST-based SRAM Cell

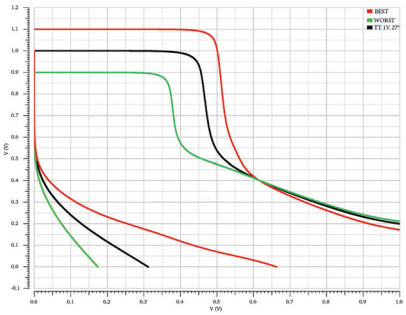

Fig. 6. Write SNM of the proposed ST-based SRAM Cell

perform the operation in its right working condition. Next is the dynamic noise margin (DNM) shown in Fig. 9, indicates that the proposed SRAM cell can operate for as high as 0.8V with 10-40ps.

Fig. 10 shows the array of ST-based SRAM cells which is simulated under PVT analysis (Process, Voltage, and Temperature). The simulation results in Fig. 11 shows that the ST-based SRAM cell passed in 60 corners in all processes with voltage variations of 0.8V-1.1V and with temperature variations of 0 °C, 27 °C, and 75 °C.

The results of the Monte Carlo analysis for energy per bit is presented in Fig. 12. At the same time, the delay is shown in Fig. 13. This analysis provides information on how the PVT variation affects the cell's performance. The standard

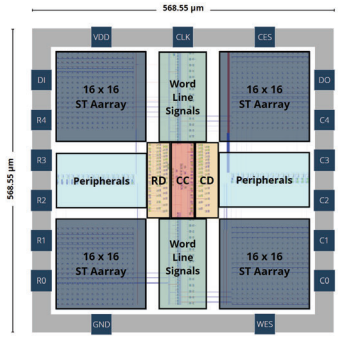

Fig. 7. Proposed 1-kb SRAM layout

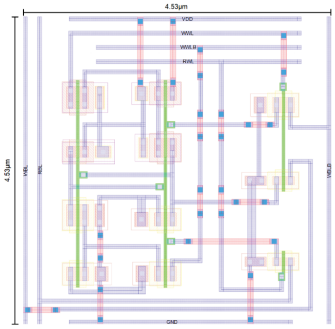

Fig. 8. Proposed SRAM Cell Layout

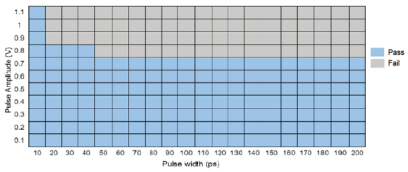

Fig. 9. Dynamic noise margin (DNM) simulations

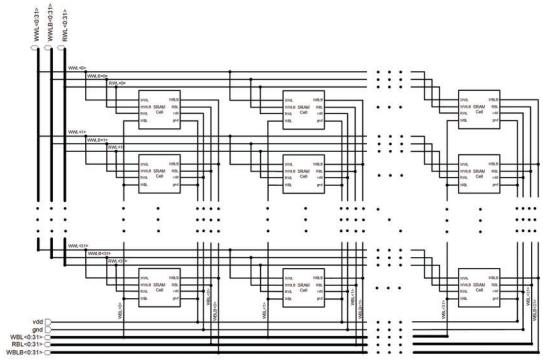

Fig. 10. ST-based SRAM Array Design

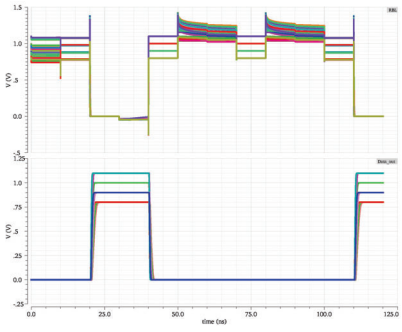

Fig. 11. All corner post-layout simulation result

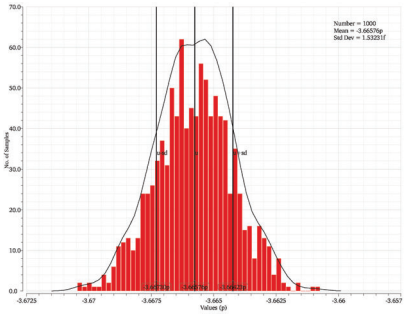

Fig. 12. Energy per bit Monte Carlo simulation result

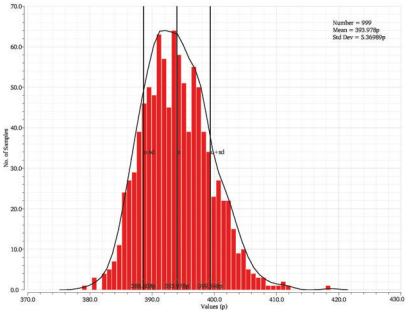

Fig. 13. Access delay Monte Carlo simulation result

deviation, $\pm 6\sigma$ was used to vary the values of 1000 random samples, which is also the number of Monte Carlo simulations. The mean energy per bit was 3.66576pJ while the mean delay was 393.978 ps. The simulated result for the standard deviation of the energy per bit is 1.53231 fJ, while the delay is at 6.36989ps, which indicates that all cases are within the mean value and that process variation has little effect on the proposed SRAM cell.

As shown in Fig. 14, the energy per bit of the proposed design shows that it consumes lesser energy than most of the gathered literature and Fig. 15 manifested that the proposed design has better stability as compared to the other designs. In addition, Shown in Table III is the performance metrics of SRAM design and other literature. The proposed design has 455.1 mV SNM in its worst-case which is significantly higher than the other literature and best SNM as compared to the literature that has a cell type of 6T. Furthermore, the proposed design has 0.396 Energy/bit (fJ/bit) which is significantly lower as compared to most gathered literature. Hence, the proposed SRAM cell design belongs in the 70^{th} percentile.

Table IV shows better performance metrics of the designed ST-based SRAM cell compared to conventional 6T SRAM cell.

IV. Conclusion

A Schmitt-trigger-based SRAM Cell design implemented using 45-nm CMOS technology is designed with a separated port for write and read bitlines SRAM and two types of Schmitt-trigger Inverters: P-Type and N-Type Inverter is presented in this investigation. Our proposed design shows a very low energy/bit and SNM compared to conventional 6T thanks to the novel cell design that uses Schmitt-trigger inverters and the separated port for write and read bitlines.

TABLE III
Performance Comparison of SRAM Design with other State-of-the-Art

Year	Cell Type	Process (nm)	SNM (mV)	Energy per bit (fJ/bit)	FOM* (fJ/bit)
2012 [8]	8T	45	668.6	N/A	N/A
2012 [9]	5T	90	326.9	N/A	N/A
2014 [10]	5T	40	N/A	57	64.13
2014 [10]	5T	40	353	N/A	N/A
2015 [11]	5T	40	353	N/A	N/A
2015 [12]	9T	90	61	N/A	N/A
2016 [11]	5T	40	N/A	188.22	211.75
2016 [4]	11T	45	130	N/A	N/A
2017 [13]	5T	28	249	N/A	N/A
2017 [14]	9T	65	N/A	3.58	2.48
2017 [15]	9T	65	N/A	68.75	47.60
2018 [16]	6T	65	N/A	18.5	12.81
2018 [17]	5T	90	N/A	56.67	28.34
2019 [18]	7T	7	213	N/A	N/A
2019 [19]	6T	40	N/A	1	1.13
2019 [19]	6T	40	412.3	N/A	N/A
2019 [20]	14T	45	75	N/A	N/A
2020 [21]	6T	28	N/A	0.041	0.07
2020 [19]	6T	28	292	N/A	N/A
2020 [22]	6T	40	377	N/A	N/A
2020 [22]	8T	40	N/A	67	75.38
2020 [23]	6T	40	N/A	0.0675	0.08
2020 [24]	12T	45	205	N/A	N/A
2020 [25]	12T	45	205	N/A	N/A
2021 [26]	6T	16	N/A	0.0068	0.02
2021 [23]	6T	16	504.76	N/A	N/A
2021 [27]	9T	16	110	N/A	N/A
2021 [28]	6T	65	42	0.536	0.37
2022 [29]	8T	40	608.11	5.97	6.72
2023 [30]	6T	40	412.3	1.0	1.125
This work	11T	45	455.1	0.396	0.40

*$FOM = \text{Epb} \times \frac{45-nm}{\text{process}}$

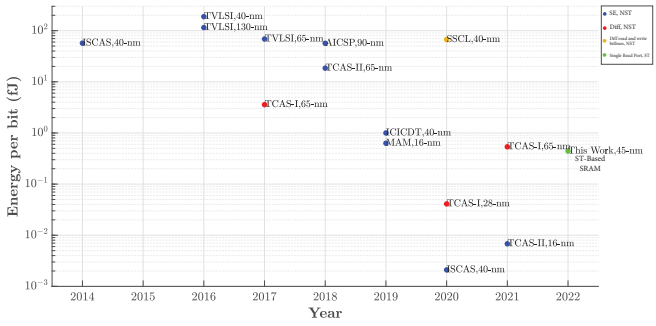

Fig. 14. Energy per Bit Technology Roadmap

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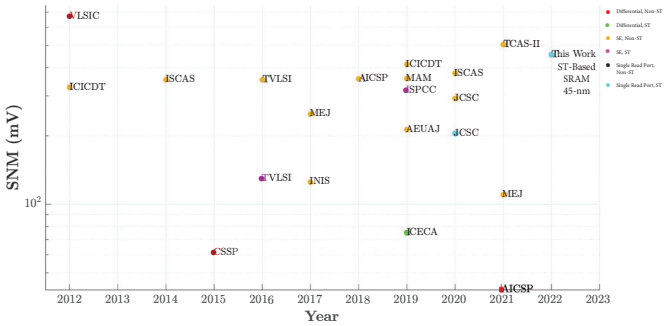

Fig. 15. SNM Technology Roadmap

TABLE IV
PERFORMANCE METRICS COMPARISON OF CONVENTIONAL 6T AND ST-BASED SRAM

Performance Metrics	Conventional 6T	Proposed
Configuration	1-kb	1-kb
Cell Type	6T	Schmitt-trigger(11T)
Technology	45 nm	45 nm
Hold-0 SNM	576.8 mV	455.1 mV
Hold-1 SNM	576.8 mV	455.2 mV
Read-0 SNM	170.2 mV	523.3 mV
Read-1 SNM	170.2 mV	565.7 mV
Write SNM	472.7 mV	478.2 mV
Power per Acess	23.247 μW	1.270 μW
Power per Bit	726.454 nW	39.681 nW
Energy per bit	7.265 fJ	0.396 fJ
Delay (ns)	4.728 ns	1.039 ns

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