IIIT BANGALORE

VLS 503

Digital CMOS VLSI Design

Project Report

Authors:
Abu Saleh Khan - MS2024001
Shruti Singh - MS2024020
Keerthana B - MS2024010
Raghav Khurana - IMT2022550
Divyansh Kumar - IMT2022509
Puneet Kalyan Upadrasta - IMT2021516

November 12, 2024

Project Title

Schmitt-Trigger-based Low Power SRAM implemented using 45-nm CMOS Technology

Introduction

Our group numbered 6, has been tasked with the project titled:-Schmitt-Trigger-based Low Power SRAM implemented using 45-nm CMOS Technology. To undertake the completion of our project, we have broken the work down into specific tasks as listed below:

- Design of Conventional 6T SRAM Cell
- Design of Schmitt-Trigger-Based SRAM Cell
- Read and Write Ports Operations
- Simulation and Analysis
- Static Noise Margin (SNM) Analysis
- Process, Voltage, Temperature (PVT) Analysis
- Performance Comparison with the Conventional 6T SRAM

Motivation

Memories play a crucial role in the fast-paced environment of digital systems. The storage of data and program instructions occupies a significant portion of the silicon area in many modern digital integrated circuits (ICs). One type of memory is Static Random Access Memory (SRAM), which allows access to any bit of stored data whenever it is needed. In network-on-chip (NoC) or system-on-chip (SoC) designs, SRAM can account for up to 90% of the overall capacity.

Additionally, SRAM is the primary consumer of total chip power. Therefore, the power consumed by SRAM largely determines the overall power

consumption of the chip. This makes it essential to develop SRAM architectures that use minimal power. Moreover, the growing demand for mobile devices and emerging applications, such as implanted medical devices and wireless body sensing networks, further highlights the need for low-power SRAM solutions.

Conventional 6T SRAM Cell

1. Continuous evolution is crucial for improving the performance of SRAM cells. As a result, various types of SRAM cells have been introduced in the literature, such as the 6T, 7T, 8T, and 9T SRAM cells. Among these, the most commonly used SRAM cell in digital systems is the 6T SRAM cell, which can store 1 bit of data. The bit remains in the cell as long as power is supplied.

   A conventional 6T SRAM cell consists of two inverters connected back-to-back. The data that needs to be stored is latched within these two inverters. The process of storing data is referred to as the WRITE operation, while the process of retrieving data is known as the READ operation.

   The Read operation utilizes sense circuits that detect the bit line (BL) and bit line bar (BLB) data lines before discharging them completely. In essence, SRAM performs three main operations: Hold, Read, and Write. When the two access pass transistors connected to the word line (WL) are in the OFF state, both the bit line and bit line bar (BL & BLB) are also turned OFF, placing the memory cell in a hold state.

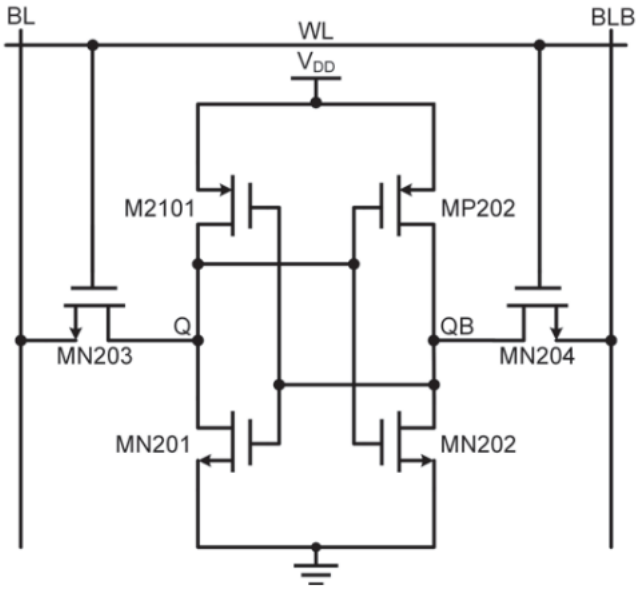

Figure 1: Conventional 6T SRAM cell schematic diagram

Proposed Schmitt-trigger-based SRAM Cell

The proposed Schmitt-trigger-based SRAM cell is an advanced 11-transistor (11T) design that enhances stability and noise resistance by using Schmitt-trigger inverters instead of traditional cross-coupled inverters. By incorporating both P-type and N-type Schmitt-trigger inverters, this cell takes advantage of hysteresis, which adjusts the switching threshold levels. This improvement significantly enhances the static noise margin (SNM) during read and hold operations, increasing the cell's tolerance to noise and voltage fluctuations. As a result, it helps maintain data integrity even in low-voltage environments, where conventional SRAM cells might face data corruption.

Additionally, the design features separate read and write ports. This innovation isolates the read and write bit lines, minimizing disturbances during read operations. Such separation ensures that data remains stable when accessed, addressing a common issue in traditional 6T SRAM cells, where shared ports can unintentionally lead to data flips during reads. The combination of Schmitt-trigger inverters and isolated

read/write architecture makes this SRAM cell particularly suitable for applications that require reliable data retention and robust noise resistance, such as mobile and wearable devices, where stability is crucial.

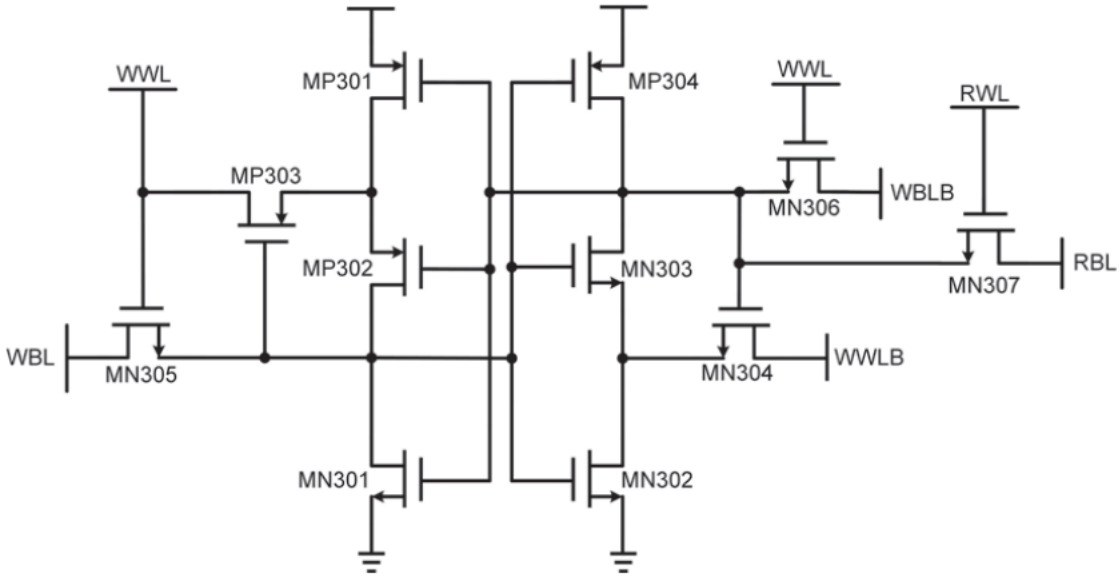

Figure 2: Schmitt-Trigger-Based SRAM cell with single read port

Read and Write Ports Operations

Read Port Operation:

In SRAM, the read port is responsible for retrieving stored data without changing the existing values in the memory cells. During a read operation, the word line associated with the target memory cell is activated, allowing a connection between the cell and the bit lines. The data stored in the cell then affects the bit lines, which, with the assistance of sense amplifiers, detect and amplify the signal to output the stored data. The read port is designed to be non-destructive, ensuring that the data within the cell remains unchanged after the read operation.

For a read operation, the Read Word Line (RWL) is set to HIGH to activate the read access, while both the Write Word Line (WWL) and Write

Word Line Bar (WWLB) are set to LOW and HIGH, respectively, ensuring that the write port is inactive. The Read Bit Line (RBL) is then used to sense and output the data stored in the cell.

Write Port Operation:

The write port in SRAM manages data storage by overwriting the existing contents in the targeted memory cells. In a write operation, both the word line and the bit lines are activated. The bit lines are set to the desired data values (either high or low) that need to be written. Once the word line is activated, the write drivers force these values into the memory cell, replacing the previous data. The operation concludes when the new data stabilizes within the cell, completing the write process.

During a write operation, the Write Word Line (WWL) is set to HIGH to enable access to the cell, while the Write Word Line Bar (WWLB) is set to LOW. The Read Word Line (RWL) remains LOW to disable read access during the write cycle. The data to be written is provided through the Write Bit Line (WBL) and its complement through the Write Bit Line Bar (WBLB), with WBL toggling between HIGH/LOW based on the data being written and WBLB set to the opposite.

	Operation		
Signal	**Write**	**Read**	**Hold**
Write Word Line (WWL)	HIGH	LOW	LOW
Write Word Line Bar (WWLB)	LOW	HIGH	HIGH
Read Word Line (RWL)	LOW	HIGH	LOW
Port			
Write Bit Line (WBL)	HIGH/LOW	-	-
Write Bit Line Bar (WBLB)	LOW/HIGH	-	-
Read Bit Line (RBL)	-	HIGH	-

Figure 3: READ AND WRITE CYCLE TIMING

Simulation and Analysis

Static Noise Margin (SNM) Analysis

The Static Noise Margin (SNM) analysis for the proposed 11T Schmitt-trigger-based SRAM cell shows significant stability improvements compared

to conventional 6T SRAM cells. The integration of P-type and N-type Schmitt-trigger inverters introduces hysteresis, which enhances the noise margins and makes the SRAM more resilient to variations in process, voltage, and temperature (PVT). This capability helps the SRAM cell maintain data integrity during hold, read, and write operations under various conditions. The Schmitt-trigger inverters also enable higher switching threshold voltages, decreasing susceptibility to noise and minimizing read disturbance issues.

In the analysis, the 11T SRAM cell achieves higher SNM values across all operations. During the hold operation, the SRAM cell demonstrates a strong noise margin, ensuring data retention even under challenging conditions. The read SNM is also significantly improved, thanks to a separate read port and reduced read disturbance, which supports stable operation at lower voltages. Additionally, the write SNM shows slight enhancements, providing reliable write functionality. These improvements make the Schmitt-trigger-based SRAM cell particularly well-suited for low-power applications, as it effectively combines noise resilience with efficient energy usage.

6T SRAM Static Noise margin graphs

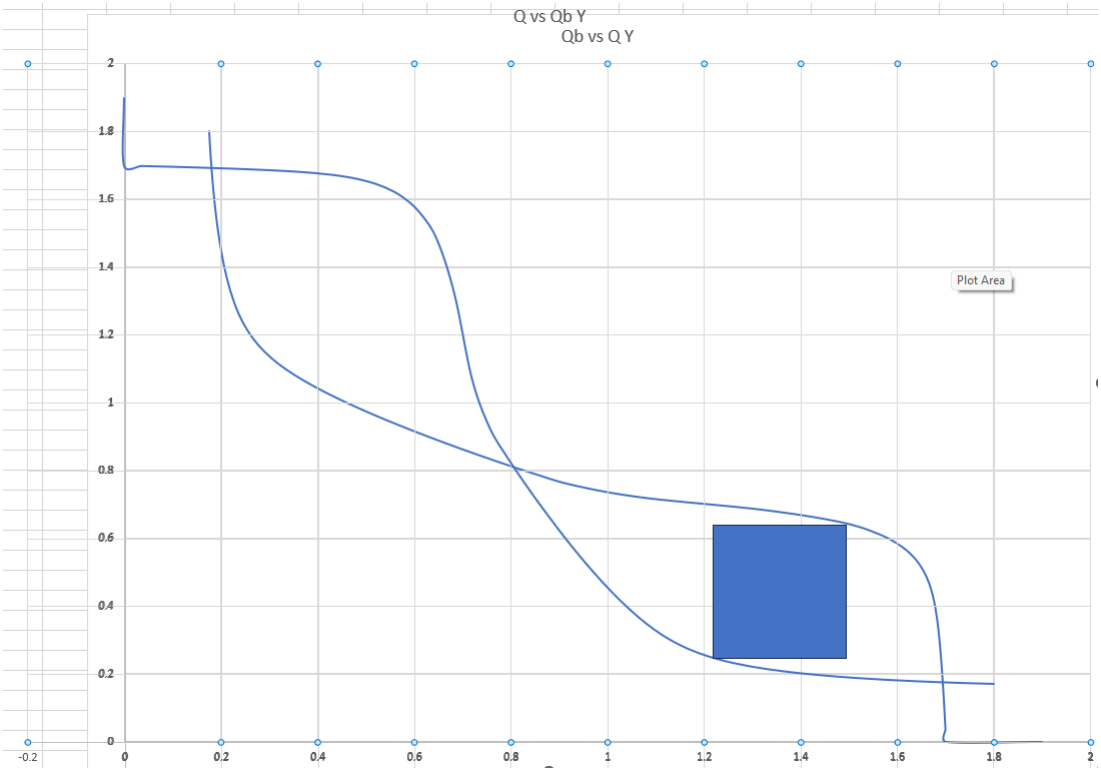

Figure 4: Read 0

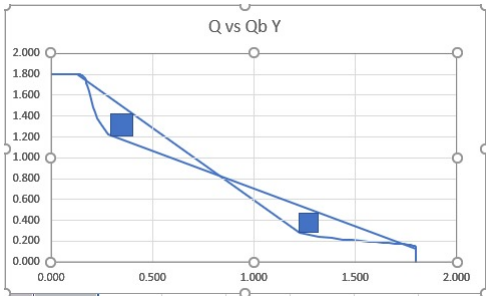

Figure 5: Write 0

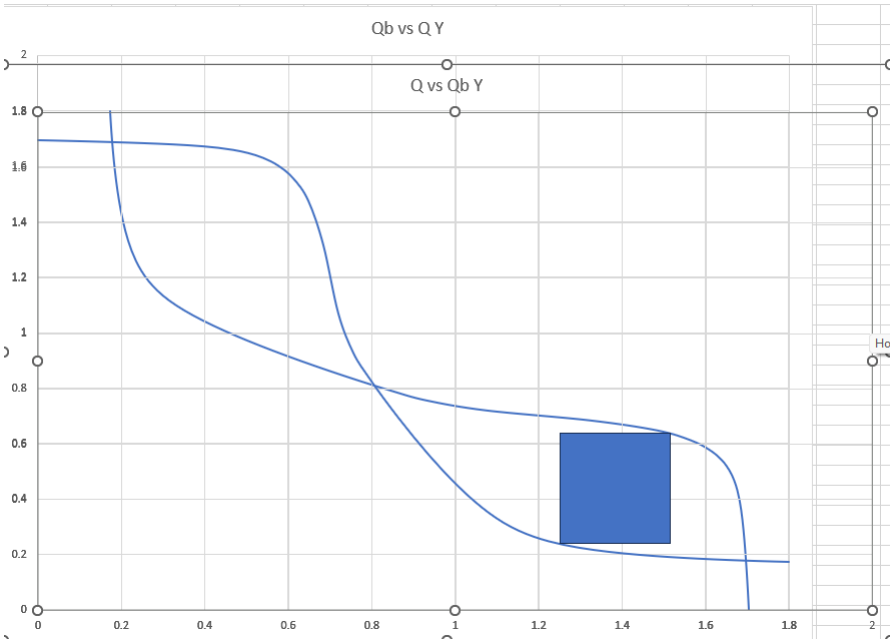

Figure 6: Read 1

Proposed 11 T Schmitt-trigger-based SRAM Cell Static Noise margin graphs

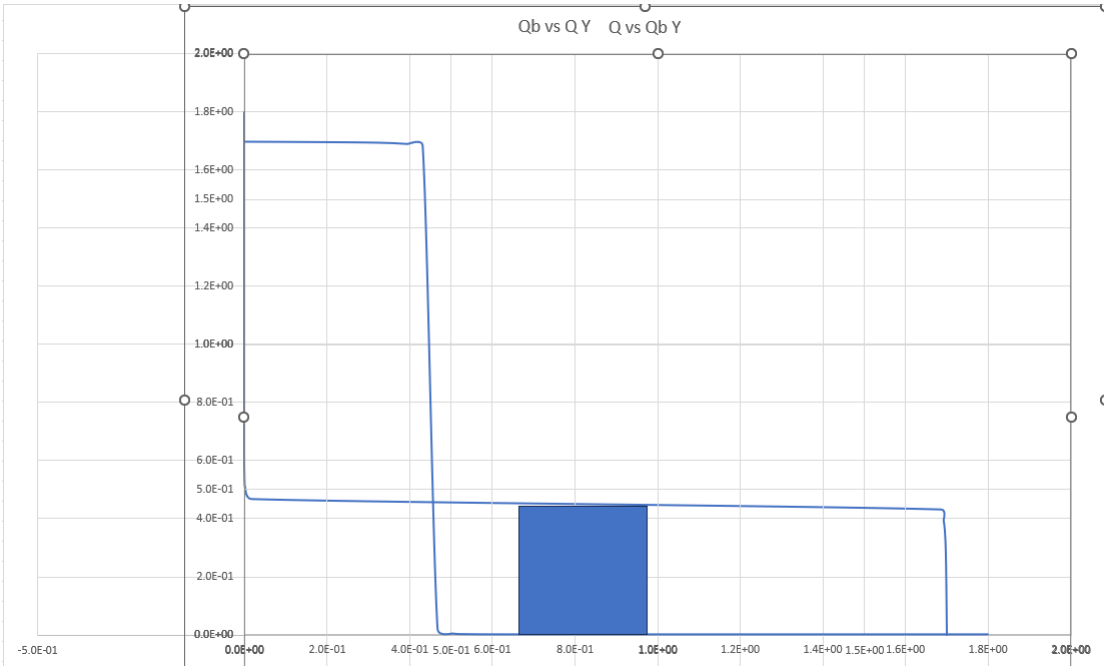

Figure 7: Read 0

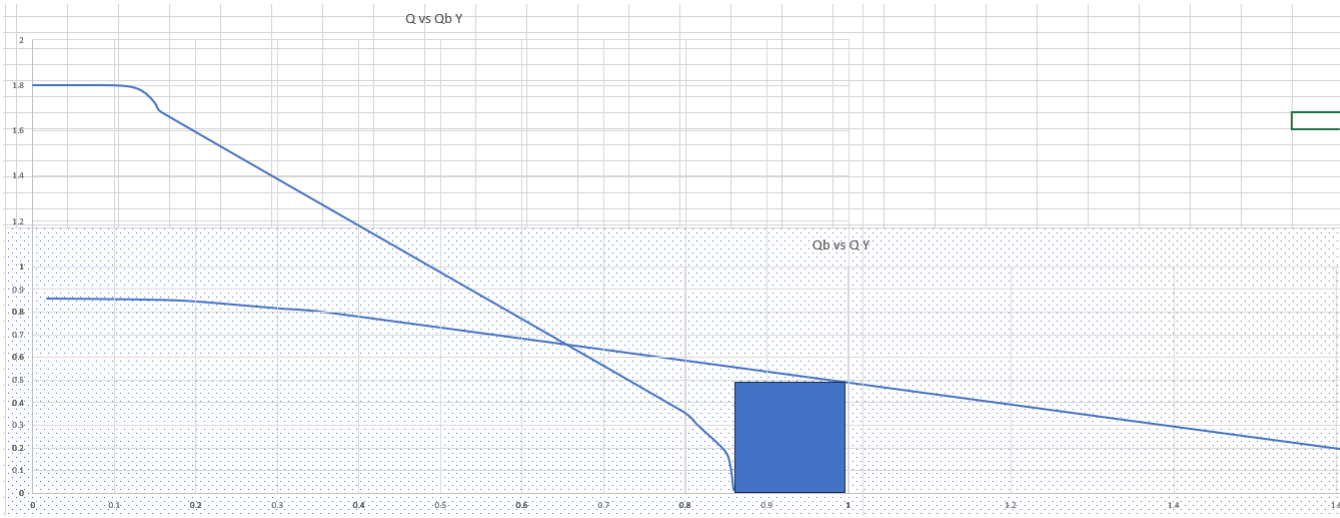

Figure 8: Write 0

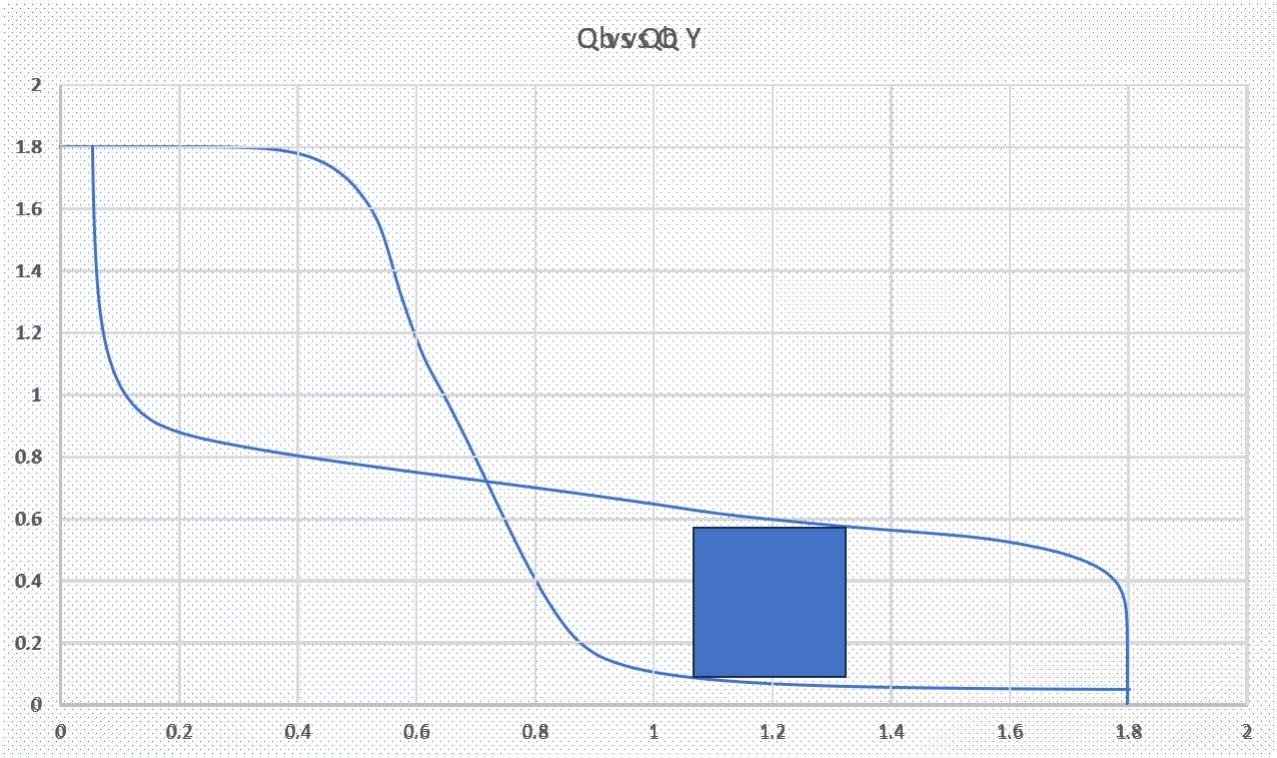

Figure 9: Hold 0

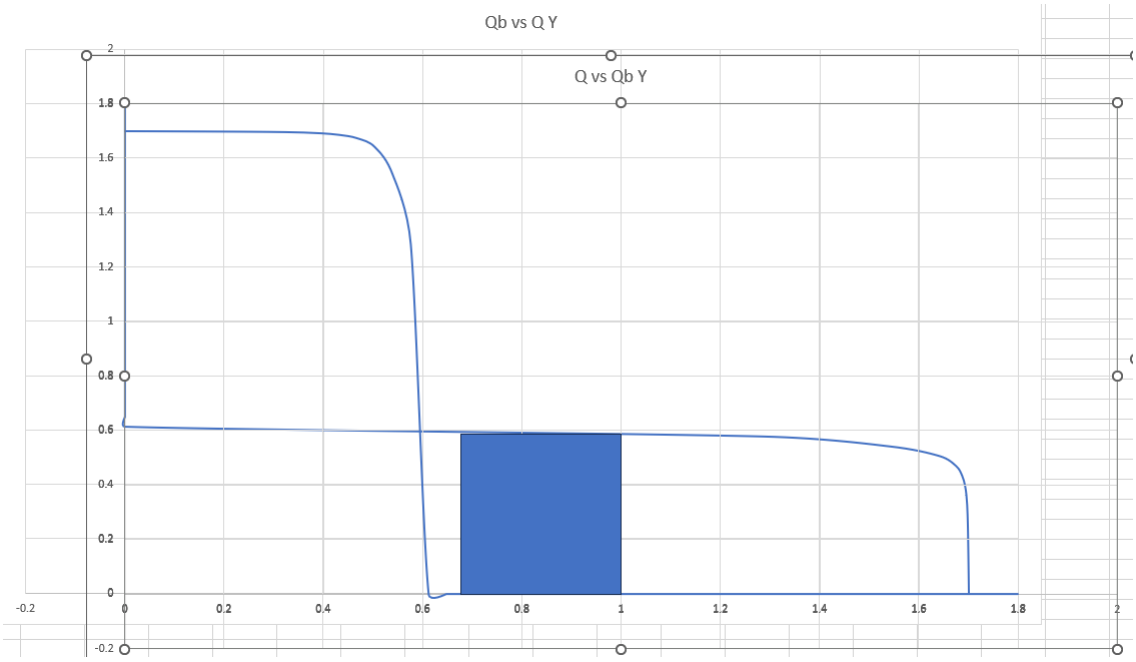

Figure 10: Read 1

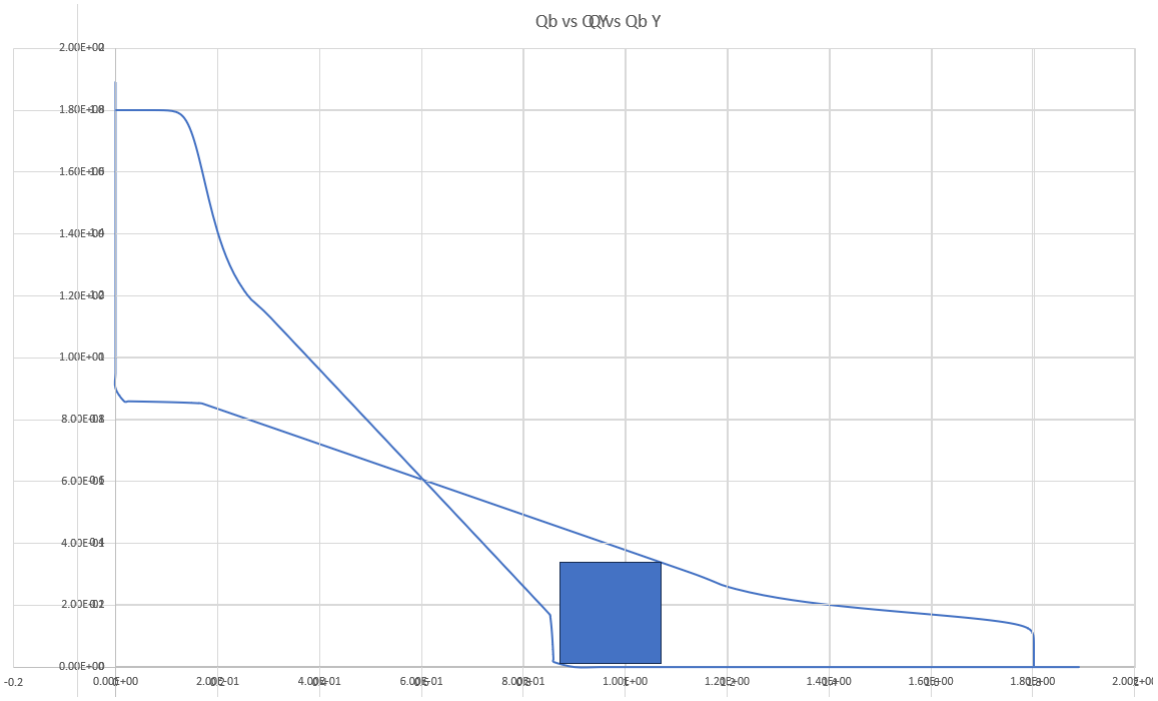

Figure 11: Write 1

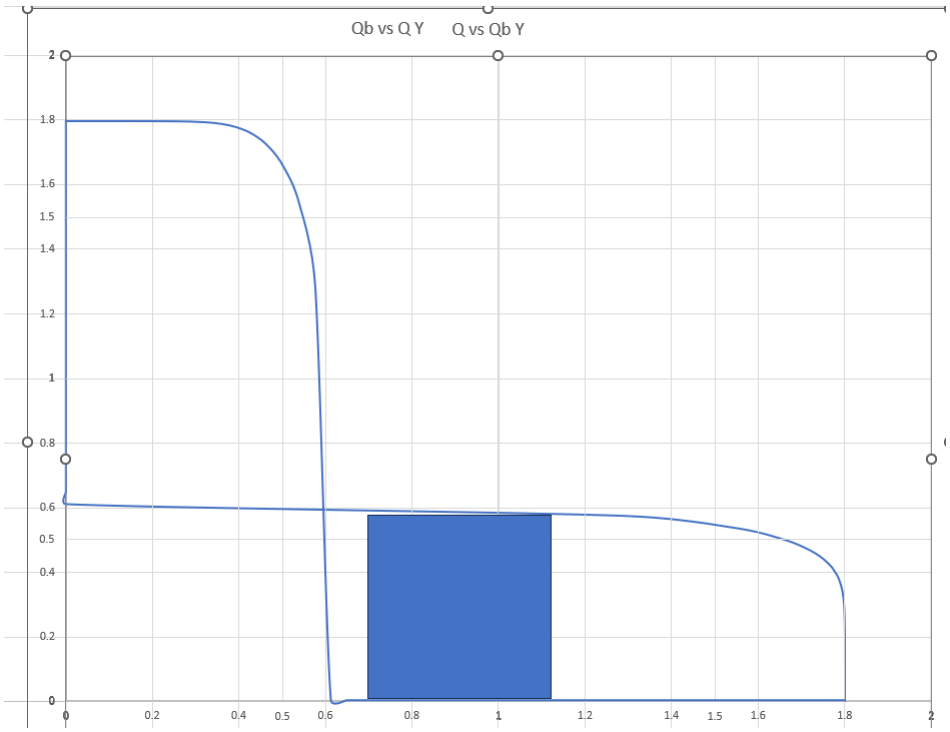

Figure 12: Hold 1

Process, Voltage, Temperature (PVT) Analysis

The Process, Voltage, and Temperature (PVT) analysis of the 11T Schmitt-trigger-based SRAM cell provides valuable insights into its robustness in the face of variations in fabrication processes, operating voltage, and ambient temperature. This analysis is essential for understanding how effectively the SRAM cell can maintain performance and stability under real-world conditions, which can be highly variable.

In this 11T SRAM design, the pairing of P-type and N-type Schmitt-trigger inverters significantly enhances noise tolerance through the creation of hysteresis effects. These effects are especially advantageous during PVT variations. Notably, at higher temperatures and slower process corners, the SRAM cell exhibits impressive hold and read static noise margins (SNM), ensuring stable data retention and read stability, while minimizing potential read disturbances.

Moreover, the design incorporates mechanisms for reliable operation during voltage scaling, commonly implemented for power-saving purposes. This allows the SRAM to function effectively at reduced voltage levels, all while optimizing read and write margins across PVT variations. Overall, the PVT analysis reveals that the Schmitt-trigger architecture of the 11T SRAM not only ensures consistent stability and resilience but also positions it as an excellent choice for low-power and high-stability applications.

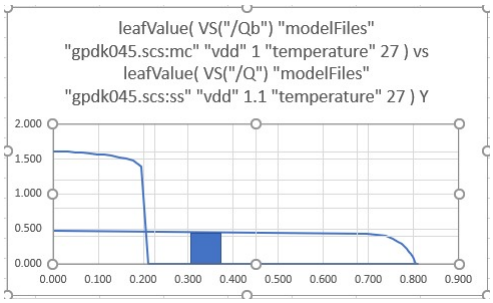

Figure 13: Hold typ

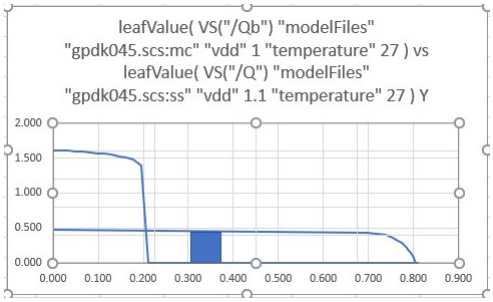

Figure 14: Hold best

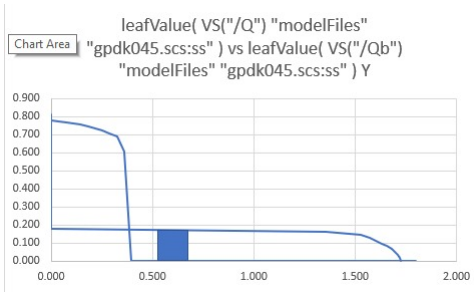

Figure 15: Hold worst

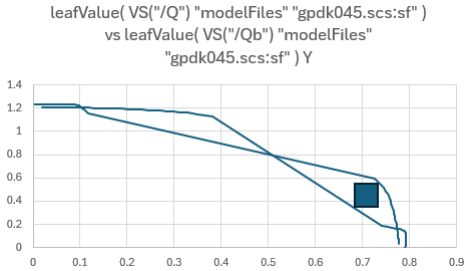

Figure 16: write best

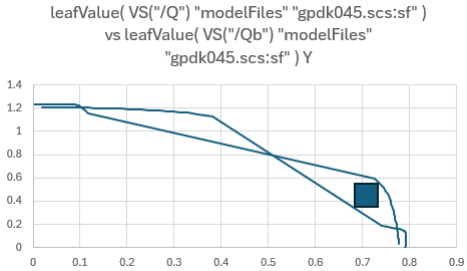

Figure 17: write worst

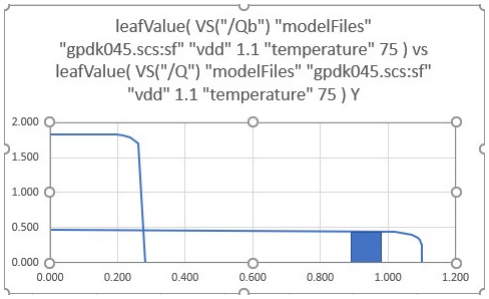

Figure 18: Read best

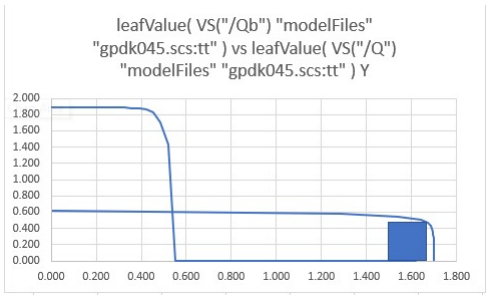

Figure 19: read typ

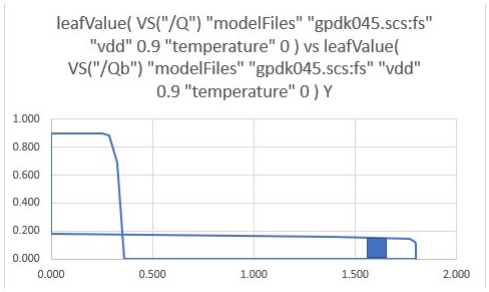

Figure 20: read worst

Performance Comparison with the Conventional 6T SRAM

Future Work

For future work, further improvements can be explored in SRAM technology, especially through the integration of memristors. Memristors, as resistive

SNM	6T SRAM	11T SRAM
Read 0	276 mv	310 mV
Write 0		135 mV
Hold 0	520 mv	256 mV
Read 1	265 mv	324 mV
Write 1		198 mV
Hold 1		425 mV

Table 1: Comparison of 6t and 11t srams based on our implementation

memory elements with inherent non-volatility, have the potential to drastically reduce static power consumption and enhance data retention capabilities in low-power SRAM designs. Incorporating memristors into the SRAM cell structure could allow for more compact designs and lead to more efficient memory systems. Additionally, memristor-based hybrid SRAM could support improved noise margins and stability, building on the benefits achieved with Schmitt-trigger inverters. Future work may also include experimenting with different configurations of memristor-based crossbars to further optimize read and write operations, potentially reducing the latency and enhancing the robustness of the memory under process variations.

Conclusion

In this work, we propose an SRAM cell design based on Schmitt-trigger technology, implemented in 45-nm CMOS. The cell features separate bitlines for reading and writing, along with P-Type and N-Type Schmitt-trigger inverters. Our design offers notably lower energy per bit and enhanced static noise margin (SNM) when compared to the conventional 6T SRAM cell. These gains are achieved through the novel combination of Schmitt-trigger inverters and segregated read and write bitline ports, leading to improved performance and robustness in memory operations.

References

[1] Single-Ended Schmitt-Trigger-Based Robust Low-Power SRAM Cell.
[2] Static Noise Margin Analysis of Various SRAM Topologies.
[3] Dokic, "CMOS schmitt triggers," IEE Proceedings G (Electronic Circuits

and Systems), vol. 131, no. 5, p. 197, 1984.
[4] S. Ahmad, M. K. Gupta, N. Alam, and M. Hasan, "Single-ended schmitttrigger-based robust low-power SRAM cell," IEEE Trans. on Very Large Scale Integr. (VLSI) Syst., vol. 24, no. 8, pp. 2634–2642, Aug. 2016.
[5]N. Surana and J. Mekie, "Energy efficient single-ended 6T SRAM for multimedia applications," IEEE Transactions on Circuits and Systems II: Express Briefs, vol. 66, no. 6, pp. 1023–1027, Jun. 2019.