CMOS VLSI FINAL INTEGRATION

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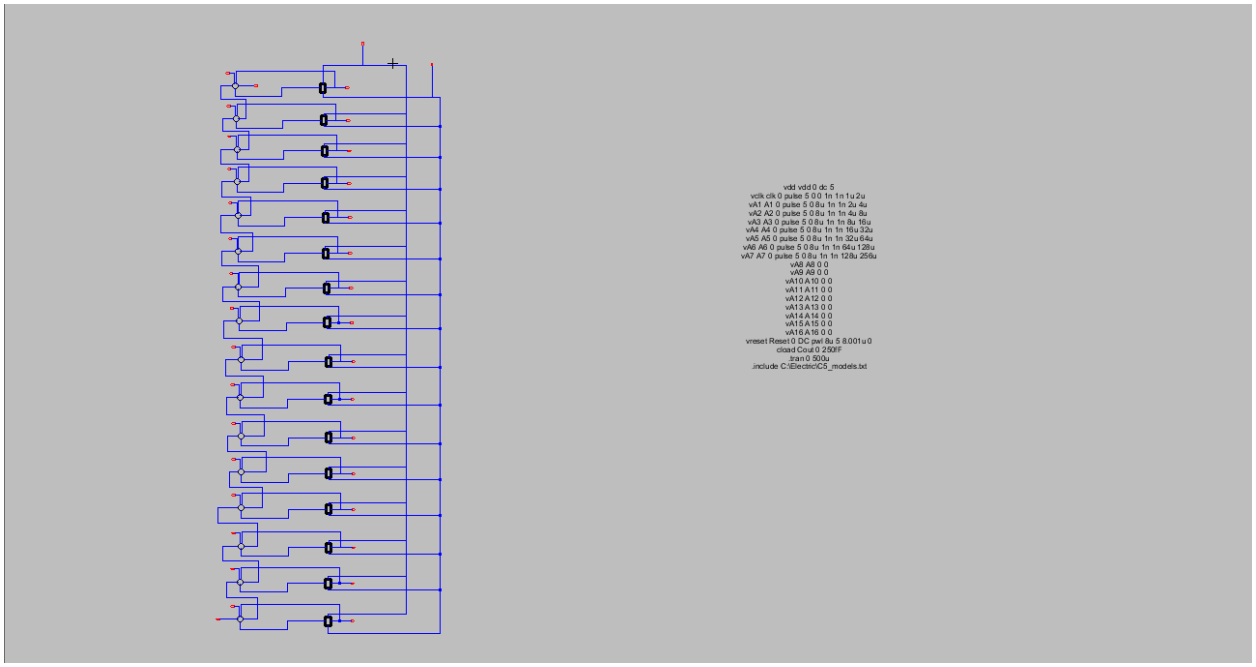
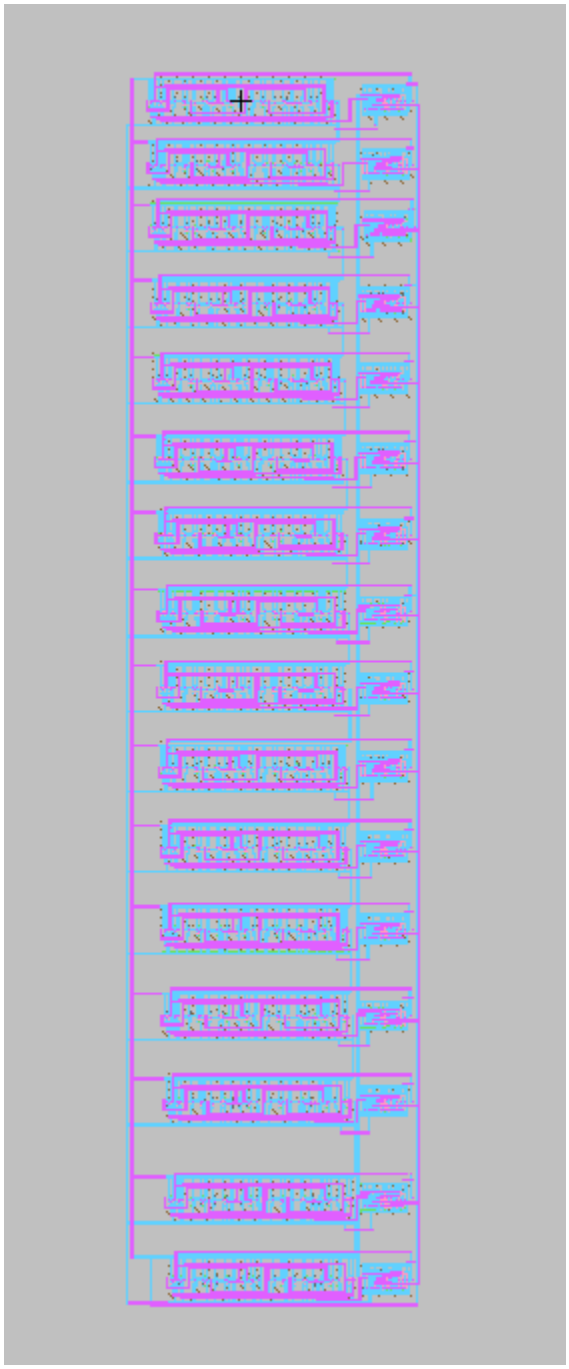
16_Bit Accumulator:

SCHEMATIC:



LAYOUT:



SIMULATION VALIDATION:

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----------------------------------14----------------------------------
Running DRC with area bit on, extension bit on, Mosis bit
Checking again hierarchy .... (0.006 secs)
Found 2102 networks
Checking cell 'accum{lay}'
        No errors/warnings found
0 errors and 0 warnings found (took 1 mins, 8 secs)
Job Design-Rule Check cell 'accum{lay}' (done) took: 1 mins, 8 secs (started at Sat Dec 07 12:05:57 EST 2024, ended at Sat Dec 07 12:07:05 EST 2024 )
==================================15==================================
Checking Wells and Substrates in '16_bit-accumulator:accum{lay}' ...
   Geometry collection found 3666 well pieces, took 0.159 secs
   Geometry analysis used 16 threads and took 0.025 secs
NetValues propagation took 0.005 secs
Checking short circuits in 64 well contacts
   Additional analysis took 0.005 secs
No Well errors found (took 0.21 secs)
==================================16==================================
Hierarchical NCC every cell in the design: cell 'accum{sch}'  cell 'accum{lay}'
Comparing: 16_bit-accumulator:accum{sch} with: 16_bit-accumulator:accum{lay}
  exports match, topologies match, sizes match in 0.206 seconds.
Summary for all cells: exports match, topologies match, sizes match
NCC command completed in: 0.228 seconds.
```

SIMULATION WAVEFORM: