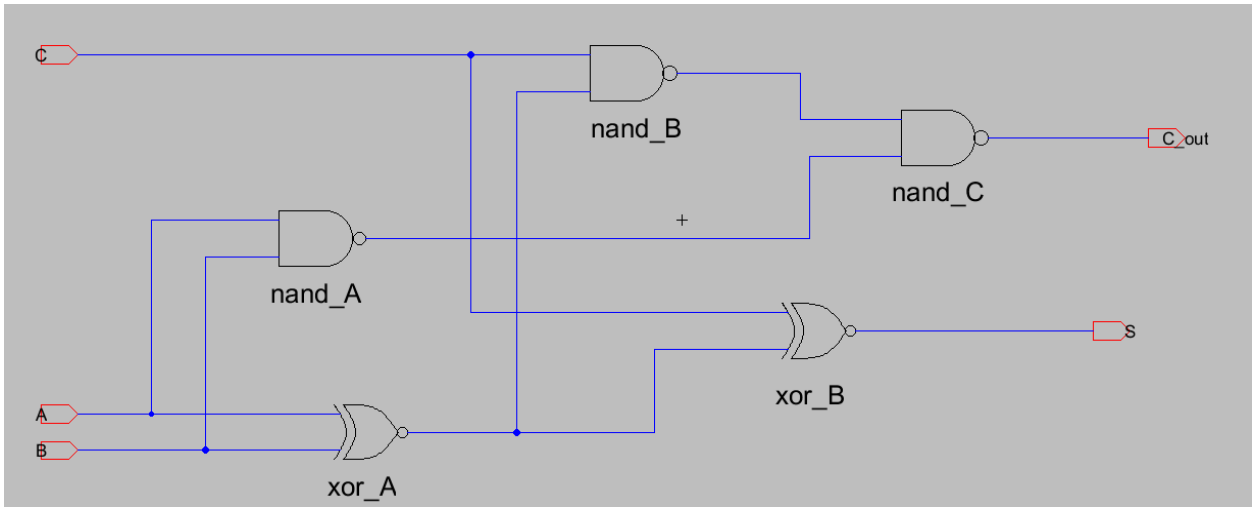
VLSI MILESTONE - 2

NAME: Ragul Ganesh Anitha Palanivel
B-NUMBER: B01038692

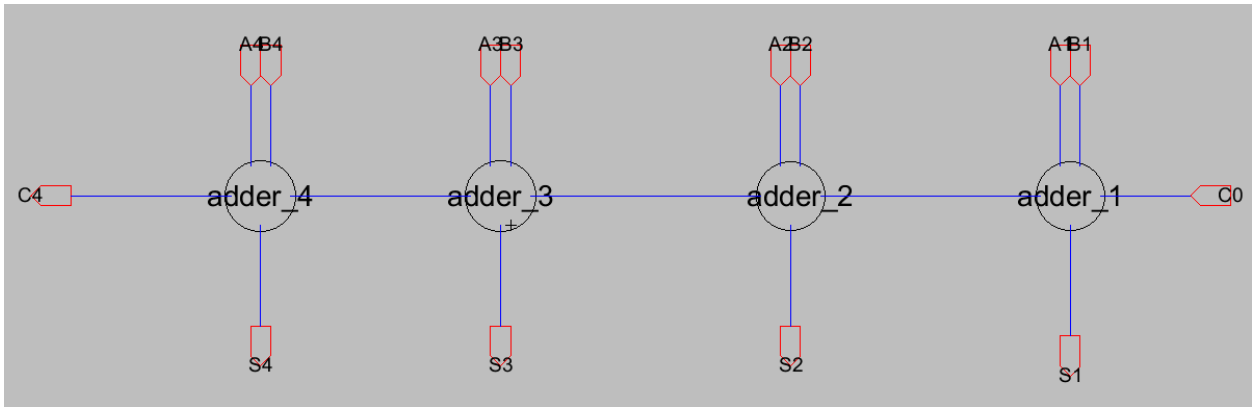
1-Bit Full Adder and Multi-Bit Full Adder.

SCHEMATIC:

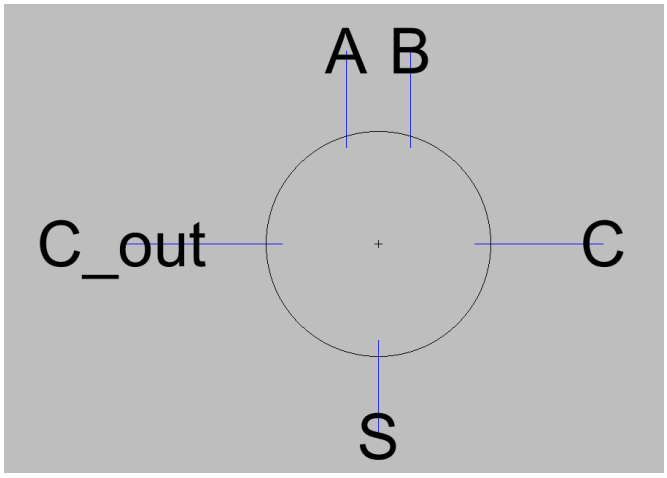
1-Bit Full Adder:



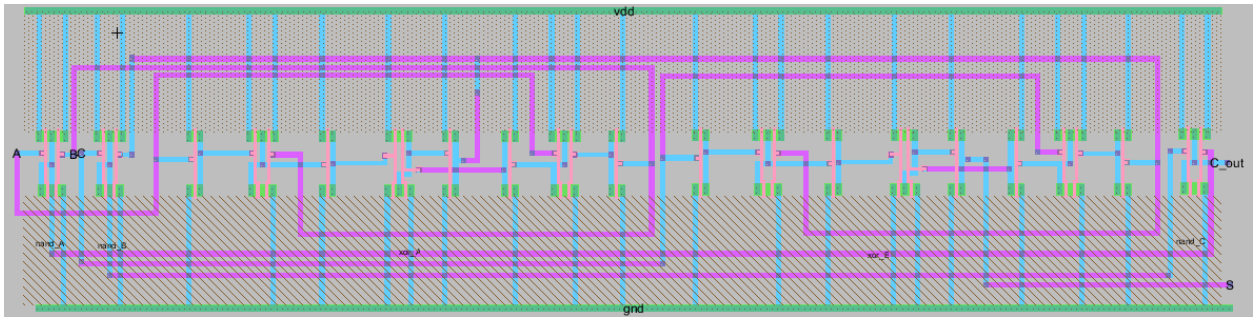
Multi-Bit Full Adder:



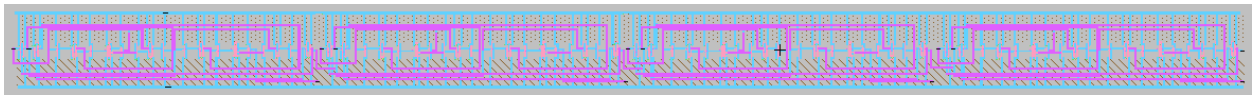
ICON:



1-Bit Full Adder:



Multi-Bit Full Adder:



Simulation validation:

1- Bit Full Adder:

```
Checking schematic cell 'FULL_ADDER:f_adder{sch}'
   No errors found
0 errors and 0 warnings found (took 0.004 secs)
================================7================================
Running DRC with area bit on, extension bit on, Mosis bit
Checking again hierarchy .... (0.0 secs)
Found 92 networks
0 errors and 0 warnings found (took 0.002 secs)
================================8================================
Checking Wells and Substrates in 'FULL_ADDER:f_adder{lay}' ...
   Geometry collection found 248 well pieces, took 0.005 secs
   Geometry analysis used 16 threads and took 0.011 secs
NetValues propagation took 0.0 secs
Checking short circuits in 2 well contacts
   Additional analysis took 0.0 secs
No Well errors found (took 0.016 secs)
================================9================================
Hierarchical NCC every cell in the design: cell 'FULL_ADDER:f_adder{sch}'  cell 'FULL_ADDER:f_adder{lay}'
Comparing: FULL_ADDER:f_adder{sch} with: FULL_ADDER:f_adder{lay}
  exports match, topologies match, sizes match in 0.01 seconds.
Summary for all cells: exports match, topologies match, sizes match
NCC command completed in: 0.012 seconds.
```

Multi-Bit Full Adder:

```
Checking schematic cell '4_bt_adder{sch}'
   No errors found
0 errors and 0 warnings found (took 0.02 secs)
================================11================================
Running DRC with area bit on, extension bit on, Mosis bit
Checking again hierarchy .... (0.0 secs)
Found 350 networks
0 errors and 0 warnings found (took 0.023 secs)
================================12================================
Checking Wells and Substrates in '4_BIT_ADDER:4_bt_adder{lay}' ...
   Geometry collection found 986 well pieces, took 0.019 secs
   Geometry analysis used 16 threads and took 0.0 secs
NetValues propagation took 0.0 secs
Checking short circuits in 8 well contacts
   Additional analysis took 0.0 secs
No Well errors found (took 0.019 secs)
================================13================================
Hierarchical NCC every cell in the design: cell '4_bt_adder{sch}'  cell '4_bt_adder{lay}'
Comparing: 4_BIT_ADDER:4_bt_adder{sch} with: 4_BIT_ADDER:4_bt_adder{lay}
  exports match, topologies match, sizes match in 0.112 seconds.
Summary for all cells: exports match, topologies match, sizes match
NCC command completed in: 0.112 seconds.
```

Simulation Waveform: