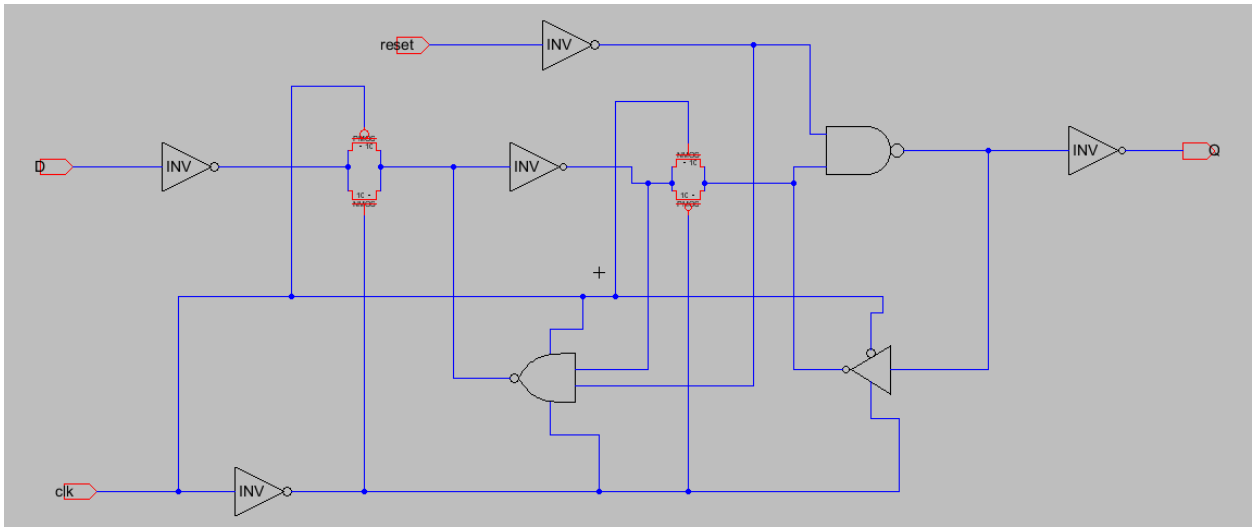
CMOS VLSI MILESTONE - 1

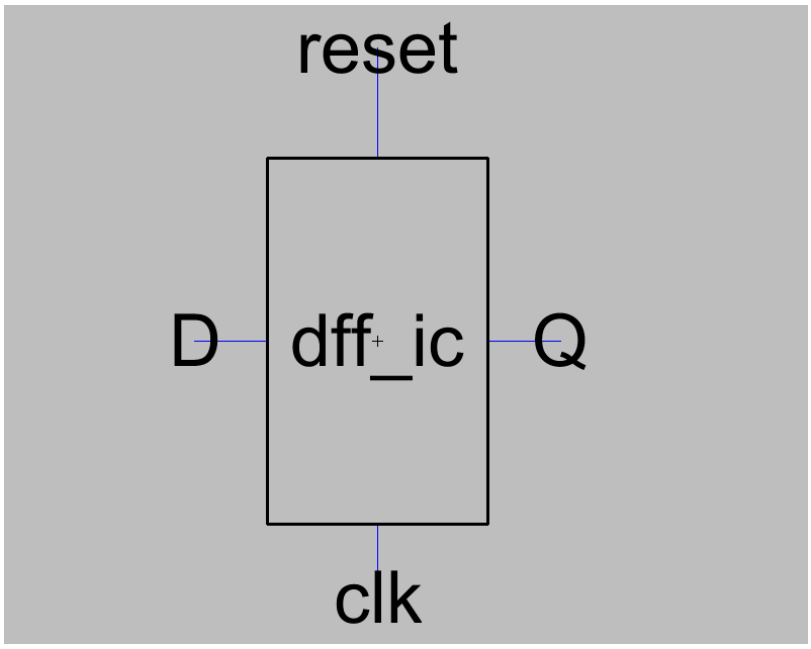
NAME: Ragul Ganesh Anitha Palanivel
B-NUMBER: B01038692

Asynchronous Positive Edge Triggered D- Flip Flop

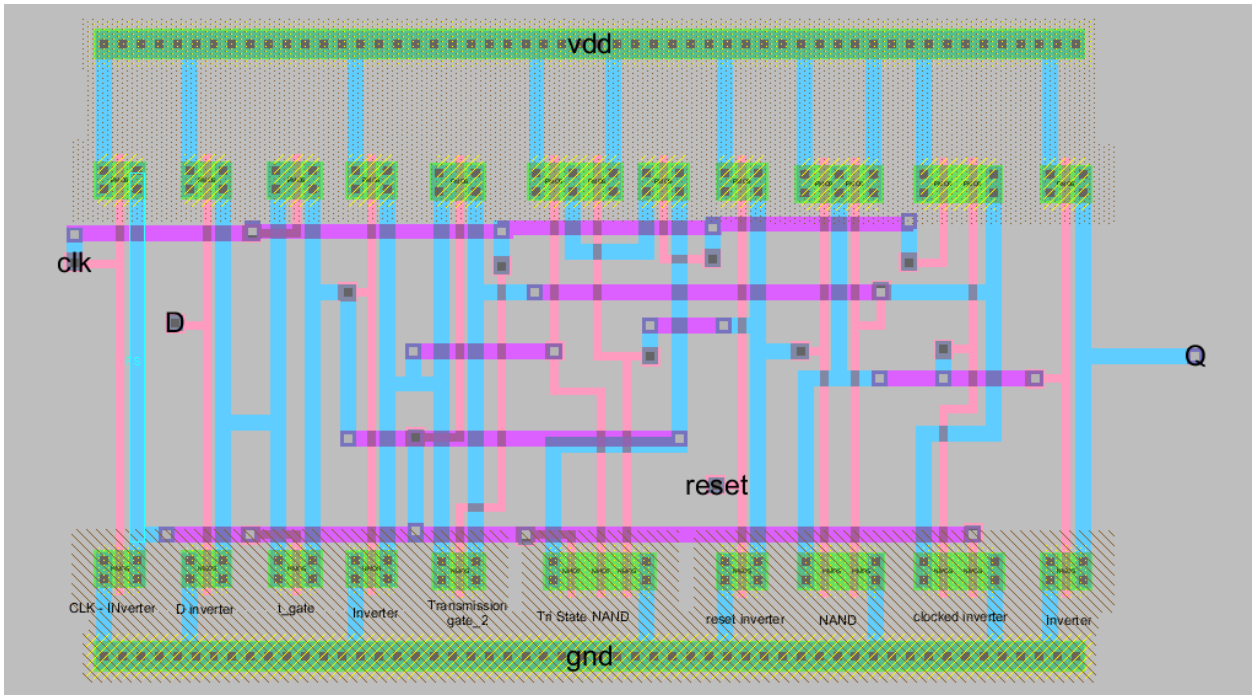
SCHEMATIC:



ICON:


reset
D
dff_ic
Q
clk

LAYOUT:


vdd
clk
D
Q
reset
CLK - INverter
D inverter
t_gate
Inverter
Transmission gate_2
Tri State NAND
reset inverter
NAND
clocked inverter
Inverter
gnd

SIMULATION VALIDATION:

```
Checking schematic cell 'dff_ic{sch}'
   No errors found
0 errors and 0 warnings found (took 0.048 secs)
================================4================================
Running DRC with area bit on, extension bit on, Mosis bit
Checking again hierarchy .... (0.0 secs)
Found 50 networks
0 errors and 0 warnings found (took 0.016 secs)
================================5================================
Checking Wells and Substrates in 'DFF:dff_ic{lay}' ...
   Geometry collection found 98 well pieces, took 0.018 secs
   Geometry analysis used 16 threads and took 0.0 secs
NetValues propagation took 0.0 secs
Checking short circuits in 2 well contacts
   Additional analysis took 0.0 secs
No Well errors found (took 0.018 secs)
================================6================================
Hierarchical NCC every cell in the design: cell 'dff_ic{sch}'  cell 'dff_ic{lay}'
Comparing: DFF:dff_ic{sch} with: DFF:dff_ic{lay}
  exports match, topologies match, sizes match in 0.023 seconds.
Summary for all cells: exports match, topologies match, sizes match
NCC command completed in: 0.032 seconds.
```

SIMULATION WAVEFORM: