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# The Platin Multi-Target Worst-Case Analysis Tool

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## Abstract

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With the increasing number of applications that require reliable runtime guarantees, the relevance of static worst-case analysis tools that can provide such guarantees increases. These analysis tools determine resource-consumption bounds of application tasks, with a model of the underlying hardware, to meet given resource budgets during runtime, such as deadlines of real-time tasks.

This paper presents enhancements to the PLATIN worst-case analysis tool developed since its original release more than ten years ago. These novelties comprise PLATIN's support for new architectures (i.e., ARMv6-M, RISC-V, and AVR) in addition to the previous backends for Patmos and ARMv7-M. Further, PLATIN now features system-wide analysis methods and annotation support to express system-level constraints. Besides an overview of these enhancements, we evaluate PLATIN's accuracy for the two supported architecture implementations, Patmos and RISC-V.

**2012 ACM Subject Classification** Software and its engineering → Automated static analysis; Software and its engineering → Compilers; Computer systems organization → Real-time systems

**Keywords and phrases** worst-case resource consumption, WCET, static analysis tool

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**Supplementary Material** Software (*Platin Source Code*): <https://github.com/t-crest/platin>

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## 1 Introduction

**Safety-Critical Applications & Worst-Case Analysis.** The relevance of solving the worst-case execution time (WCET) problem [57] is higher than ever when considering the increasing number and the complexity of today's safety-critical application requirements running on



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modern processors. From small medical (implantable) devices over automotive and avionics applications to large industrial-control scenarios, systems that require resource budget guarantees for safe execution need tooling support to determine resource bounds analytically. The basic principle of worst-case analysis is to combine a representation of the system’s program paths with a cost model of the underlying hardware. With this knowledge, the worst-case analysis generates a mathematically sound problem formulation, such as an integer linear program (ILP). When given to a mathematical solving tool, the solution of this formulation yields resource-consumption bounds, which are used for offline budgeting of runtime resources.

**Resource Other Than Time: Worst-Case Energy Consumption.** This method of combining a program-path model with a cost model was introduced in the 1990s [35, 39] and referred to as the *Implicit Path Enumeration Technique (IPET)*. The original purpose of the IPET targeted the timeliness of real-time systems. However, Jayaseelan et al. later demonstrated the applicability of this approach for determining worst-case energy consumption (WCEC) bounds [28]. In the same way, WCET bounds are crucial for meeting deadlines in real-time systems; WCEC estimates are helpful in energy-constrained settings to guarantee the safe completion of tasks under energy budgets. This paper addresses the two resources: time and energy within the PLATIN tool with WCET/WCEC analyses.

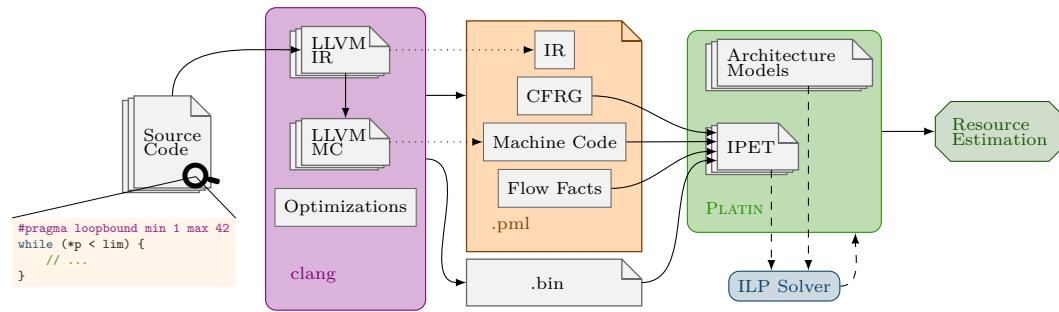
**Necessity for Open Architectures & Open Tooling Infrastructures.** The PLATIN tool was originally introduced more than ten years ago [23, 40] as a portable LLVM annotation and timing toolkit. PLATIN’s development started with the T-CREST project [44], targeting time-predictable multi-core architectures. With the entire technology available as open source, we argue that the research community requires both open processor architectures and the respective worst-case tooling support to advance state-of-the-art without unnecessary barriers (i.e., licensing, closed-source infrastructures). In line with this rationale, all our improvements and extensions to the PLATIN tool have been published as open-source over the last few years.

**Contributions.** The core contribution of this work is an overview of these novelties compared to PLATIN’s initial release [23]. The novelties include both pillars of worst-case analysis: (1) Regarding the hardware-dependent cost modeling, PLATIN now supports four new architectures (ARMv6-M, ARMv7-M, RISC-V, AVR). (2) Given the hardware-agnostic program-path analysis, we give insight into the introduced support for system-wide resource-consumption analysis and PLATIN’s annotation infrastructure. Besides the overview of existing work, we evaluate PLATIN for the Patmos and RISC-V (RV32IMC ISA) architectures.

**Paper Organization.** The paper is structured as follows: Section 2 gives a general overview of the tooling infrastructure of and around PLATIN. The existing and newly introduced architectures are part of Section 3. Section 4 describes extensions of PLATIN for whole system time and energy analysis. Section 5 presents evaluation results. Section 6 discusses related work. Section 7 concludes the paper.

## 2 Overview of the PLATIN Analysis Tool

The PLATIN ecosystem displayed in Figure 1 combines compilation and WCET analysis to make use of high-level information that the compiler already has [40]. The source code, potentially enriched with user-annotated control-flow information (so-called *flow facts*) such



**Figure 1** Overview of PLATIN’s ecosystem for compiler-analysis integration providing analysis-aware compilation to improve accuracy with automatically collected program meta-information.

as loop bounds, is compiled by an extended version of the `clang` compiler into the final binary and a meta-information file (`.pml`). This meta-information contains the program control flow and flow facts in the YAML<sup>1</sup>-based Program Metainfo Language (PML) format specific to PLATIN. Specifically, it contains the program’s control-flow graph (CFG) in an intermediate representation (IR) and on machine-code (MC) level. A control-flow-relation graph (CFRG) [25] matches program paths between the two representations even across different optimization-induced control-flow transformations. The CFRG is thus a useful tool to lower IR-level flow facts (both annotated and compiler-inferred) to the machine-code level, where the actual timing analysis is performed. PLATIN uses the CFGs and the lowered flow facts to derive an IPET formulation and, finally, transforms this formulation together with a target-specific cost model from PLATIN’s architecture models into an integer linear program (ILP). An external ILP solver (e.g., `lp_solve`, `gurobi`) then yields the resource bounds.

At the heart of PLATIN are the architecture models, which provide the translation from control-flow information to platform-specific resource demands. The core component for each of PLATIN’s architecture models is a cost model of the machine instructions, informing PLATIN in how many processor cycles each instruction is executed in the worst case. Modeling of the microarchitecture, such as processor pipelining or caches, refines the model, allowing for more accurate bounds than pessimistic assumptions about cache misses and pipeline stalls.

In the following, we give further insights into the analysis-aware compilation process (Section 2.1) and other tools of PLATIN besides the analysis (Section 2.2).

## 2.1 Analysis-Aware Compilation with Clang

For PLATIN to perform its analyses, it needs the control-flow and flow-fact information provided in the PML format. PLATIN uses this data-serialization format to store and retrieve relevant program information for the worst-case analysis. Our fork of the LLVM compiler framework [32] includes support to automatically create the accompanying PML files for each compilation unit with a mixture of user-annotated and compiler-generated knowledge. The LLVM/clang infrastructure’s code base is rapidly changing, which leads to the challenge of keeping our analysis infrastructure up to date with new LLVM/clang releases. To make

<sup>1</sup> YAML data-serialization language: <https://yaml.org>

 **Table 1** Overview of PLATIN’s supported architectures with respective processor implementations.

| Architecture | Processor Implementation   |
|--------------|--|
| Patmos       | Chisel-based implementation with FPGA synthesis (Altera DE2-115) |
| ARMv6-M      | NXP FRDM-KL46Z with ARM Cortex M0+ [2, 3, 20]                    |
| ARMv7-M      | XMC4500 with ARM Cortex M4 [4, 5, 27]                            |
| RISC-V       | ESP32-C3 supporting RV32IMC extensions [15, 43]                  |
| AVR          | ATmega1284p [6, 7]   |

forward compatibility and version updating as easy as possible, we strive not to change the core LLVM code and only add code specific to our use cases. That way, we can benefit from improvements in the LLVM infrastructure (e.g., novel analysis passes) with minor changes (e.g., adapting the PML export logic).

The compiler first takes the C source code and compiles it into LLVM intermediate representation (LLVM-IR). Any flow fact information, including loop bounds provided as pragmas, is embedded in the LLVM-IR to maintain it through the compilation pipeline [25]. Besides the program code, required standard libraries for the target can be linked on the LLVM-IR level with `llvm-link`. This enables a whole program view for the remaining steps, including optimization and PML export.

For targets that cannot be linked with `clang` or where libraries are not available as source code, the compiler produces object files, which can then be linked (without further optimizations) with an external linker. Library functions are only available at link time; however, they are challenging if they are part of any program path beginning from the analysis entry point. A timing bound can be derived solely from the machine code or must be known from external sources.

The backend exports the control flow and flow-fact information at the last stage of the compilation, where the machine instructions and their final order have been determined. The PML format and the compiler code managing its export are architecture-independent, giving seamless support for all current and future architectures.

## 2.2 PLATIN’s Supporting Tools

Besides worst-case analyses, the PLATIN ecosystem provides several accompanying tools that support the analysis. Visualization of the CFRG allows debugging in cases where the one-on-one mapping is violated. Likewise, ILP visualization makes understanding the analysis results possible, while an interactive version enables live analysis in large projects.

Integration with external analysis tools (e.g., aiT) and transformation tools from and to the PML format allow PLATIN to profit from existing analyses. A configuration tool inspired by `pkg-config` helps to invoke tools with the correct options (e.g., target-specific flags, analysis entry) to guarantee interoperability with PLATIN.

## 3 PLATIN’s Support for Multiple Architectures

The original version of PLATIN had full support for the Patmos processor and initial support for the ARM architecture, expressing the hope that using LLVM as a basis would allow for quick development of further backends [23]. This hope proved warranted, as PLATIN now supports multiple architectures. Table 1 gives an overview of the available architecture backends and corresponding processor models, further described in the following.

**Patmos Architecture.** PLATIN was initially developed for the Patmos architecture as part of the T-CREST project [44]. It provides full support for the architecture, which is also the default target [45]. As Patmos was developed explicitly for real-time systems, it has a unique cache structure: It uses a method instead of an instruction cache [11], which loads complete methods or subsets of them at predefined points in the program. It also has a dedicated stack cache for caching stack-local data. PLATIN supports modeling both of these caches [26, 29]. Patmos also has a traditional data cache. As PLATIN does not have native data-cache modeling, it assumes all data-cache accesses miss. However, when integrating with the AbsInt aiT analysis tool, AbsInt’s data-cache modeling can be leveraged for improved WCET bounds.

**ARM Architectures.** PLATIN currently has support for the ARMv6-M and ARMv7-M versions of the ARM architecture. For the ARMv6-M backend, namely for the NXP FRDM-KL46Z with a Cortex M0+ processor, we demonstrated the feasibility of automatic derivation of the cycle costs of the timing models [50, 51]. The Cortex M0+ has a comparatively simple microarchitecture, which is not modeled explicitly but is part of the derived model. The ARMv7-M backend, which is for the XMC4500 with a Cortex M4 processor, features integrated modeling of the processor pipeline and the instruction cache [41] building upon the concept of microarchitecture execution graphs [52].

**RISC-V Architecture.** Additionally, we introduced support for the open-source hardware standard RISC-V [43] as an additional backend [12]. The supported ESP32-C3 [15] system-on-chip, which uses the RV32IMC instruction set, features a 4-stage pipeline and zero-wait-state memory for both instruction and data access. Due to the lack of documentation on the timing behavior, the timing model is derived from measurements, including the effects of pipelining.

**AVR Architecture.** We further extended PLATIN to support the AVR architecture, often utilized for embedded systems and popular Arduino projects. AVR microcontrollers typically have a relatively simple microarchitecture that allows straight-forward hardware models and their integration into PLATIN, in our case for the ATmega1284p [6]. Almost all instructions are executed with constant timing, documented in the AVR Instruction Set manual [7]. As the ATmega1284p does not have integrated caches, PLATIN’s AVR backend allows for accurate WCET-bound predictions. To underpin this statement based on the exemplary benchmark `count_negative` from the TACLeBench suite [17]: This benchmark avoids overestimations from the program-path analysis and, consequently, helps to reveal pessimism originating from the architecture modeling. PLATIN’s AVR backend reports 24009 cycles while the (straight-line code) measurement counts 22560 cycles: These results indicate minor analysis pessimism with the overestimation by 6 % and highlight PLATIN’s applicability for the predictable AVR architecture.

## 4 PLATIN’s Path-Analysis & Annotation Extensions

Besides PLATIN’s support for several architectures, several works extended the analysis toolkit to support whole-system analyses (see Section 4.1 and 4.2) and express semantic annotations across the system stack (see Section 4.3).

## 4.1 SysWCET: Whole-System Response-Time Analysis

With static real-time analysis, we calculate the response-time bounds of digital systems for (external) events. Usually, we first calculate the WCET of each task in isolation before the worst-case response-time (WCRT) analysis takes the surrounding execution context (i.e., other tasks, the operating system, IRQs) into account. While this two-step approach reduces complexity, it accumulates pessimism as program-level flow constraints cannot interact with system-level constraints. With SysWCET [14], PLATIN can express the WCRT analysis for a task as a WCET analysis of the whole system while executing that task.

SysWCET formulates an ILP that encodes not only the intra- and inter-procedural control flow graphs but also the system-state transition graph (SSTG) [13], thus allowing for function- and system-level flow constraints. To calculate the SSTG, we perform an abstract interpretation of the complete system, including the operating system, preempting interrupts, and all tasks with their (fixed-priority) scheduling semantics. Hence, the SSTG includes all synchronous and asynchronous control-flow transitions between tasks and interrupt handlers.

For SysWCET, we extended PML to store the different control-flow levels (function, task, system) and generalized the IPET to encode those levels into a single ILP simultaneously. Hence, ILP-encoded flow-fact constraints can include variables from all control-flow levels. For example, SysWCET can express that two branches in different tasks are mutually exclusive, further tightening the WCRT bounds. Furthermore, parametric annotation languages (see Section 4.3) allow for more accurate, context-sensitive timing bounds.

## 4.2 SysWCEC: Whole-System Energy-Consumption Analysis

A further extension to the system-state graph provides PLATIN with knowledge about the devices present in the system, their state (on/off), and how much power they draw in the respective state. Combined with the timing analysis, this enables PLATIN to yield worst-case bounds on the energy consumption of the analyzed systems [54]. Comparable to SysWCET, the energy-related analysis can determine the code's worst-case energy demand between two arbitrary program points. Thereby, the analysis determines the *worst-case response energy consumption* of tasks, that is, the demand from start to finish of an operation, including all power-state changes and the scheduling semantics. This interplay between types of worst-case analyses underlines the usability of analysis techniques originally introduced for timeliness to also work for the energy resource.

Beyond the modeling of simple on/off states of devices, an additional enhancement keeps track of internal device states and configurations, enabling fine-grained modeling of device behavior across system states [42]. As a result, this enables PLATIN to derive more accurate resource bounds, for example, for modeling the states of transceiver devices. The scope of these energy-related extensions goes beyond the worst-case execution-time analysis of real-time systems since these analyses are beneficial for highly energy-constrained systems, such as intermittently-powered embedded systems. One example is systems with intermittent power supply that, for example, harvest their energy through solar cells within the battery-free Internet of Things [1].

## 4.3 System-Wide Annotation Support

Within system-wide analyses, the operating system's kernel represents an interesting target for the static timing analysis, as the WCET of a system call is not static but heavily depends on the system state. One solution proposed [37] to resolve this lack of application information within kernel-level analyses is to move to a parametric analysis that can jointly

```

void func(void *data, size_t len) {
    for (size_t i = 0; i < len; i++) {
        #pragma platina lbound "max_len"
        /* ... */
    }
}

#pragma platina let "max_len=12"
func(input, 12);

#pragma platina let \
"max_len=NUM_TASKS"
func(tasks, numReadyTasks());

```

**Figure 2** Parametric loop annotation in function `func` assigning context-sensitive values to the symbolic variable `max_len` at the call sites as manual loopbound (12) and system fact (`NUM_TASKS`).

**Table 2** Reasoning for excluding some of the TACLeBench benchmarks from the evaluation.

| Reason for exclusion  | Benchmarks  |
|-----------------------|---|
| Recursion             | ammunition, anagram, bitcount, bitonic, fac, huff_enc, quicksort, recursion |
| Not self-contained    | DEBIE, PapaBench, rosace  |
| Infeasible loop bound | rijndael_dec, rijndael_enc  |

consider both applications and the backing RTOS. SWAN [48] addresses this challenge by introducing system facts, a unit of information gained from system-level analysis and referenced in source-level, parametric annotations within the operating system code. By evaluating the annotation expressions over the interaction’s system facts and lowering the flow facts gained to the machine-code level with the aid of CFRGs [25], PLATIN can thus yield system-context-specific timing bounds for individual system calls. PragMetis [49] extends this parameterization from a per-system-interaction level to smaller structural contexts such as call- and loop-contexts, as shown by the example in Figure 2. This allows PLATIN to express parametricity within a single system call and eases the use of parametric annotations within application-level libraries that often exhibit similar context sensitivity.

## 5 Evaluation

We evaluate the performance of PLATIN on the TACLeBench benchmark suite [17]. However, we had to exclude some programs. As Table 2 shows, eight programs were excluded for using recursion, as PLATIN cannot handle recursion. The three `Parallel` benchmarks (`DEBIE`, `PapaBench`, `rosace`) were excluded for not being self-contained and needing OS support for threading. Finally, two benchmarks (`rijndael_dec`, `rijndael_enc`) include invalid loop bounds. We excluded the benchmarks as PLATIN requires correct bounds to produce meaningful results. After these necessary exclusions, 47 benchmarks remain for the evaluation.

In Table 3, we give the PLATIN-provided bound for the remaining benchmarks of the TACLeBench suite. We compare the measured execution time for each architecture against the PLATIN bound. The measured times for the Patmos target are with the data cache disabled, equivalent to PLATIN assuming all data-cache accesses miss. This can give us a slight sense of the efficiency of PLATIN, though we must stress that our measured times are not guaranteed to be the true WCETs since TACLe does not guarantee the input exercises the worst-case path. For the RISC-V target, we work with an ESP32-C3 processor, which features an RV32IMC instruction set and a single-cycle-accessible SRAM [15]. The SRAM has a storage capacity of 400 KB, which was large enough for our tests. We employed a measurement-based approach to determine the WCET of each instruction available on the processor. The benchmarks for the ESP32-C3 are executed on the `ESP32-C3-DevKitM-1 v1.0` development board. We use the CPU cycle counter available on the ESP32-C3 to determine the run time of each

benchmark. For floating-point operations, a software-float implementation is used for the ESP32-C3. We omitted a WCET for the floating-point library instructions in PLATIN, and, therefore, the related benchmarks (marked with ) are skipped. For the Patmos target, five additional benchmarks were excluded for incorrect compilation (marked with ). The mark is used when PLATIN failed to provide a valid bound.

The third column of each target is the pessimism, i.e., by how much the given bound is higher than the measured execution time. For the Patmos target, we can see that the pessimism ranges widely. For some of the simpler programs, PLATIN was able to identify the measured execution time as the WCET. This is not surprising in simple cases like `countnegative`, however, it is surprising in more complex cases like `h264_dec`.<sup>2</sup> On the other hand, some benchmarks have very high pessimism. For example, the pessimism of `fft` is 25 820 %, which is likely down to this program having nested loops with big ranges between minimum and maximum loop bounds.<sup>3</sup> A similar picture emerges for the RISC-V evaluations: most of the pessimism ranges from 80 % to 300 %. The pessimism of `fft` again marks an outlier with 42 590 %, with the same reasoning as for the Patmos target. Unlike the Patmos target, PLATIN does not produce any bound equal to the WCET for the RISC-V target. This is mainly due to pessimism introduced by the “C” extension of RISC-V: The `compressed` instruction-set extension offers shorter codes (2-byte instead of 4-byte) for often-used instructions. Therefore, the control flow during branching instructions can enter at addresses that are not 4-byte-aligned. As the bus only supports loading 4-byte-aligned code, a 4-byte instruction may need two loads instead of one to fetch the entire instruction from memory. This pessimism at branching instructions leads to more overestimates than the Patmos target.

## 6 Related Work

**Worst-Case Analysis Tools.** To this point, numerous WCET analyzer tools have been developed for different hardware platforms. Several analyzers stem from academia [8, 16, 19, 21, 22, 24, 30, 31, 34, 36, 40, 46] and, based on these results, commercially available products are available [10, 19, 30]. This underlines the importance of WCET analysis in safety-critical real-time systems.

**Hybrid WCET Analysis.** With the increasing complexity of modern high-performance multi-core microarchitectures, the use of hybrid WCET tools is gaining in importance: Determining accurate timing models of the target architecture can become practically infeasible with the lack of documentation and unpredictable components. In this context, the TimeWeaver tool [30] presents a hybrid approach: This approach combines timing information from measurements with static analysis techniques. Such hybrid resource-consumption approaches are also interesting in the context of PLATIN’s system-wide analysis techniques [14, 54].

**LLVMTA.** The infrastructure of LLVMTA [21] is related to the PLATIN infrastructure, with both projects relying on the LLVM framework. LLVMTA focuses on microarchitectural analysis and implements its analyses on the final assembler representation in the LLVM backend. LLVMTA has no integration into the clang compiler, comparable to PLATIN’s support of control-flow-relation graphs. That is, LLVMTA cannot exploit high-level source code information within the resource-consumption analysis.

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<sup>2</sup> Remember, no data caches are used.

<sup>3</sup> Remember, the suite does not guarantee the programs exhibit WCET.

**Table 3** Comparison of measured execution times and WCET bounds provided by PLATIN. Bounds with a '\*' use the `gurobi` optimizer instead of the default `lp_solve`.

| benchmark       | Patmos        |                  |           | RISC-V      |                 |           |
|-----------------|---------------|------------------|-----------|-------------|-----------------|-----------|
|                 | Measured      | Bound            | Pessimism | Measured    | Bound           | Pessimism |
| lift            | 2 567 285     | 6 506 322        | 153 %     | 1 738 754   | 3 846 697       | 121 %     |
| powerwindow     | 12 601 467    | 24 599 225       | 95 %      | 3 930 880   | 10 387 998      | 164 %     |
| binarysearch    | 369           | 449              | 22 %      | 232         | 409             | 76 %      |
| bsort           | 492 507       | 961 942          | 95 %      | 322 824     | 1 086 659       | 237 %     |
| complex_updates | 591 526       | 1 047 923        | 77 %      |             |                 |           |
| cosf            | 12 755 728    | 37 280 642       | 192 %     |             |                 |           |
| countnegative   | 13 000        | 13 000           | 0 %       | 21 463      | 37 353          | 74 %      |
| cubic           | 89 339 041    | 256 701 960      | 187 %     |             |                 |           |
| deg2rad         | 7 017 167     | 11 842 517       | 69 %      |             |                 |           |
| fft             | 2 474 043     | 641 279 936      | 25 820 %  | 1 288 291   | 549 970 763*    | 42 590 %  |
| filterbank      | 1 687 548 481 | 4 175 572 460    | 147 %     |             |                 |           |
| fir2dim         | 1 874 513     | 3 742 975        | 100 %     |             |                 |           |
| iir             | 90 327        | 301 992          | 234 %     |             |                 |           |
| insertsort      | 10 080        | 16 160           | 60 %      | 2 804       | 7 205           | 157 %     |
| isqrt           |               |                  |           | 1 821 949   | 3 322 333*      | 82 %      |
| jfdctint        | 8 000         | 8 000            | 0 %       | 4 553       | 8 396           | 84 %      |
| lms             | 76 108 993    | 144 454 450      | 90 %      |             |                 |           |
| ludcmp          |               |                  |           |             |                 |           |
| matrix1         | 98 586        | 98 586           | 0 %       | 37 517      | 66 523          | 77 %      |
| md5             | 71 415 634    | 258 563 319      | 262 %     | 36 390 690  | 192 082 391     | 428 %     |
| minver          | 351 107       | 1 568 068        | 347 %     |             |                 |           |
| pm              |               |                  |           |             |                 |           |
| prime           |               |                  |           | 1 580       | 4 879           | 209 %     |
| rad2deg         | 7 065 136     | 11 809 717       | 67 %      |             |                 |           |
| sha             |               |                  |           | 5 526 979   | 12 060 259      | 118 %     |
| st              | 78 350 471    | 134 464 808      | 72 %      |             |                 |           |
| adpcm_dec       | 13 315        | 13 786           | 4 %       | 5 594       | 11 852          | 112 %     |
| adpcm_enc       | 17 724        | 19 454           | 10 %      | 11 615      | 20 526          | 77 %      |
| audiobeam       | 137 166 947   | 241 512 652      | 76 %      |             |                 |           |
| cjpeg_transupp  | 13 591 503    | 125 542 054      | 824 %     | 8 047 222   | 129 576 647     | 1 510 %   |
| cjpeg_wrbmp     | 275 719       | 279 767          | 1 %       | 280 943     | 508 787         | 81 %      |
| dijkstra        | 192 399 577   | 32 480 864 150*  | 16 782 %  | 121 641 591 | 16 510 486 058  | 13 473 %  |
| epic            | 1 406 490 126 | 486 510 736 766* | 34 490 %  |             |                 |           |
| fmref           | 256 117 759   | 795 672 591      | 211 %     |             |                 |           |
| g723_enc        | 2 488 842     | 3 756 308        | 51 %      | 1 402 196   | 4 911 683       | 250 %     |
| gsm_dec         | 4 387 842     | 10 534 654       | 140 %     | 4 688 449   | 25 143 501      | 436 %     |
| gsm_enc         | 14 680 073    | 20 184 547       | 37 %      | 9 834 175   | 31 178 349      | 217 %     |
| h264_dec        | 49 621        | 49 621           | 0 %       | 144 429     | 445 724         | 209 %     |
| huff_dec        | 820 259       | 2 293 420        | 180 %     | 529 762     | 2 104 049       | 297 %     |
| mpeg2           | 1 040 665 400 | 56 804 616 615   | 5 358 %   | 535 872 047 | 41 835 888 109* | 7 707 %   |
| ndes            | 246 594       | 260 249          | 6 %       | 143 728     | 248 207         | 73 %      |
| petrinet        | 8 960         | 36 728           | 310 %     | 2 517       | 7 648           | 204 %     |
| statemate       | 67 364        | 117 113          | 74 %      | 81 270      | 290 443         | 257 %     |
| susan           |               |                  |           |             |                 |           |
| cover           | 2 098         | 2 758            | 31 %      | 58 740      | 199 374         | 239 %     |
| duff            | 2 565         | 2 628            | 2 %       |             |                 |           |
| test3           | 1 943 674 306 | 2 029 568 191    | 4 %       | 487 414 145 | 941 044 973     | 93 %      |

**Compiler & WCET-Analysis Integration.** Bernat and Holsti presented a wish list of compiler features that could aid WCET analysis [9]. The list included various features that would aid analysis, such as providing program control flow structure, various properties of the code, and controlling code generation. Many of the essential features are supported in our compiler, with data export through the PML format to aid PLATIN. This, of course, includes the control flow, flow facts, and user annotations. The compiler is missing most feature sets for source code-to-object code mapping and other features, such as the logical effects of code sub-sequences. Other compilers also implement dedicated support for WCET analysis: Li et al. introduced a framework for maintaining flow information during compiler optimizations [33]. Falk et al. introduced the WCET-aware C Compiler (WCC), which can automatically call the aiT WCET analyzer and change the code generation to minimize the WCET [18]. Schommer et al. extend the CompCert certified C compiler with support for AIS annotations [47]. These annotations are then embedded in a dedicated section in the ELF, which the WCET analyzer can consume.

**Worst-Case Energy-Consumption Analysis.** The original use of the IPET targeted the time resource for real-time systems. Later, Jayaseelan et al. [28] introduced the usability of WCET techniques for the energy resource to yield worst-case energy-consumption estimations, leading to further research on WCEC analysis [28, 38, 42, 53, 54, 55, 56]. With the PLATIN toolkit, we explored system-wide WCEC analysis [54] and the modeling of context-sensitive device states [42]. We consider the PLATIN framework a fundamental basis for our further work in this area for addressing energy-constrained systems.

## 7 Conclusion

Real-time systems need to prove the absence of deadline misses. To ensure this property, we need schedulability analysis and static WCET analysis of the individual tasks. This paper presented PLATIN, an open-source worst-case analysis tool targeting Patmos, RISC-V, ARM, and AVR processors. The PLATIN toolkit, initially introduced for WCET analysis, has also proven to be suitable for analyzing tasks' worst-case energy consumption to address energy-constrained systems. Extensions to PLATIN include system-wide analyses and expressive annotation support. In our evaluations, we show the multi-target capabilities of PLATIN by providing WCET bounds for two different processors (Patmos and a RISC-V variant) for the TACLe benchmarks. We envision that PLATIN will be extended to other real-time processors, e.g., the FlexPRET processor [58]. PLATIN is available as open-source software, simplifying cooperation between research groups on developing static worst-case analysis tools.

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