# CPU Performance Enhancements

CS2052 Computer Architecture

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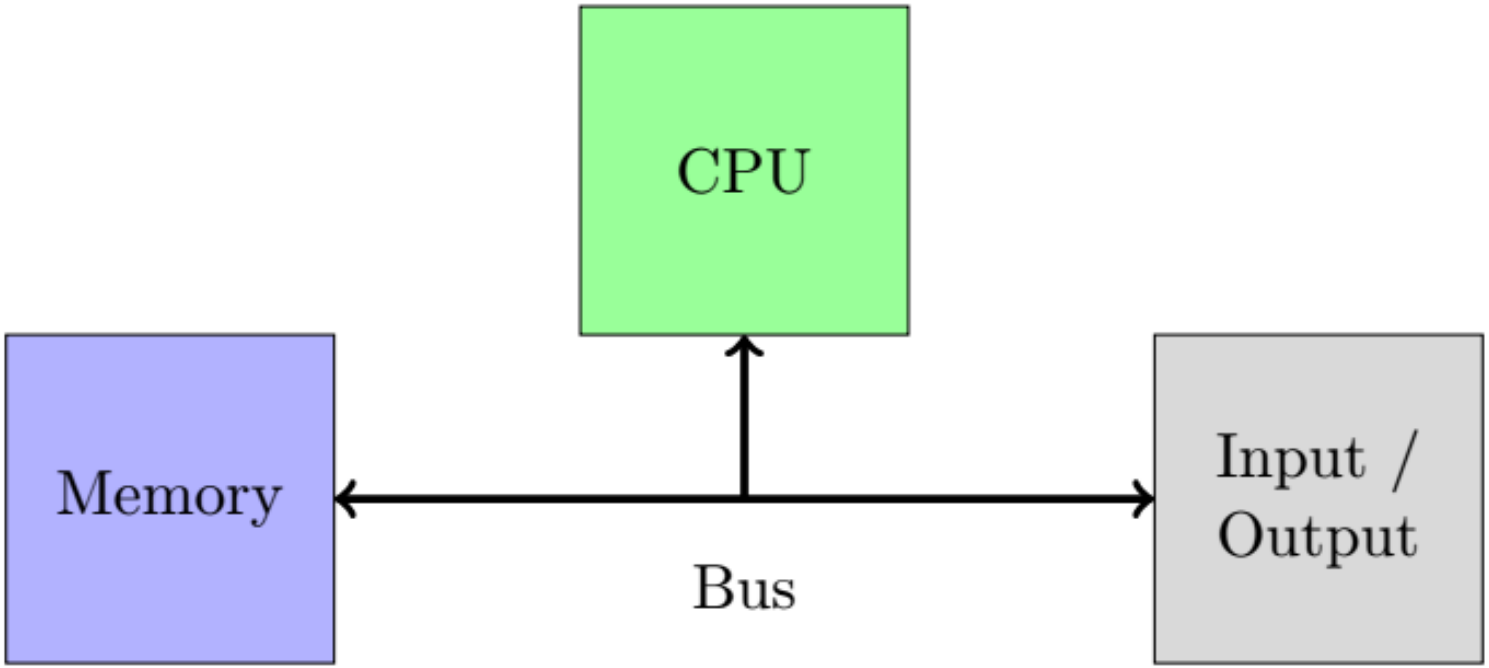
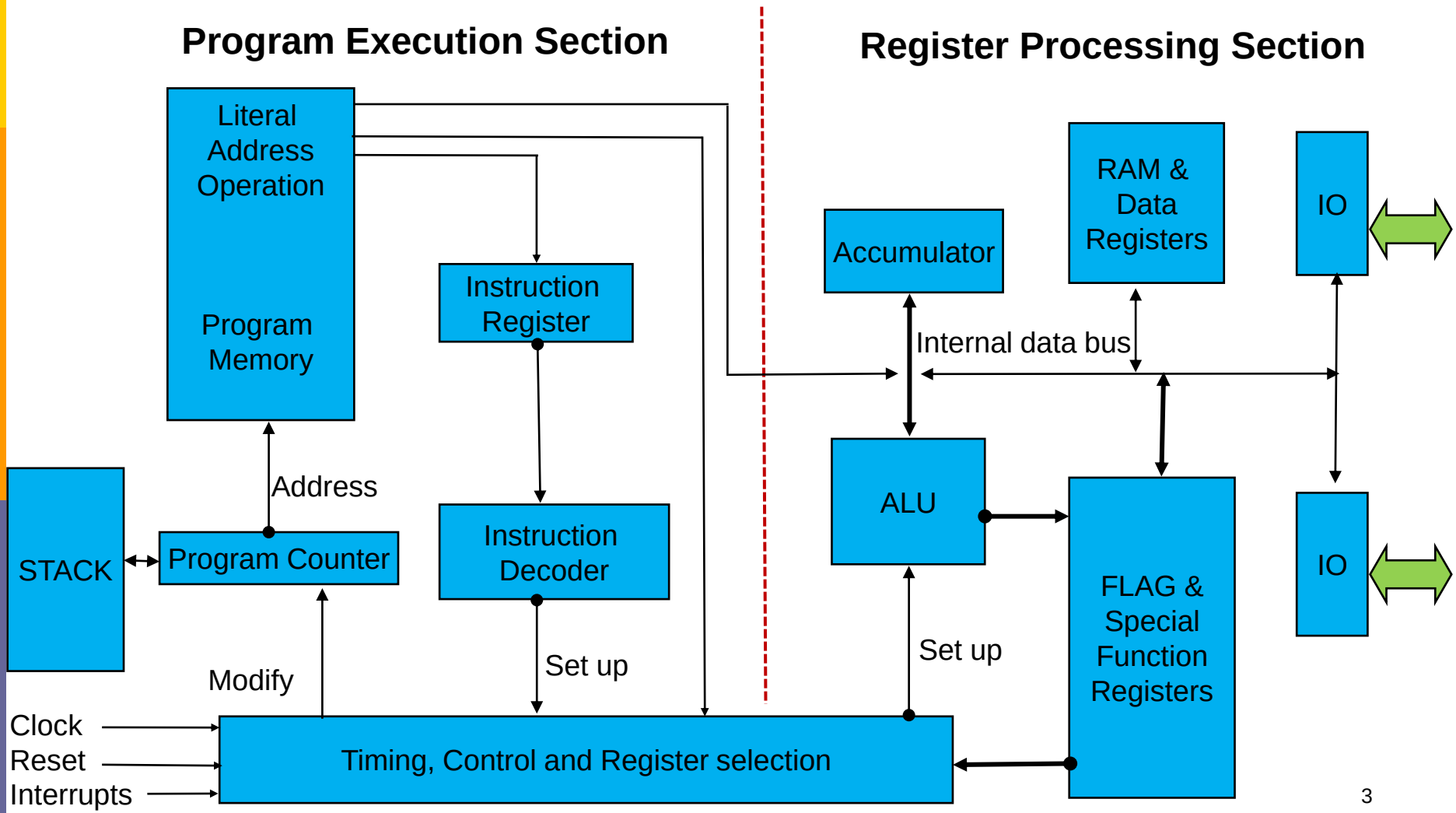
# Introduction



# Introduction (Cont.)





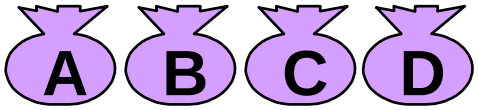

Source: Makis Malliris & Sabir Ghauri, UWE

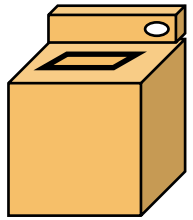
# Introduction (cont.)

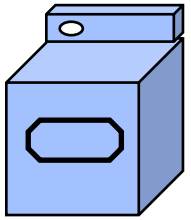
- Pipelining
- Parallelism
- Advanced processor architectures

# Pipelining – It's Natural!

- Laundry example
- Amal, Bimal, Chamal, & Dinal each have one load of clothes to wash, dry, & fold
- Washer takes 30 minutes
- Dryer takes 40 minutes
- Folder takes 20 minutes

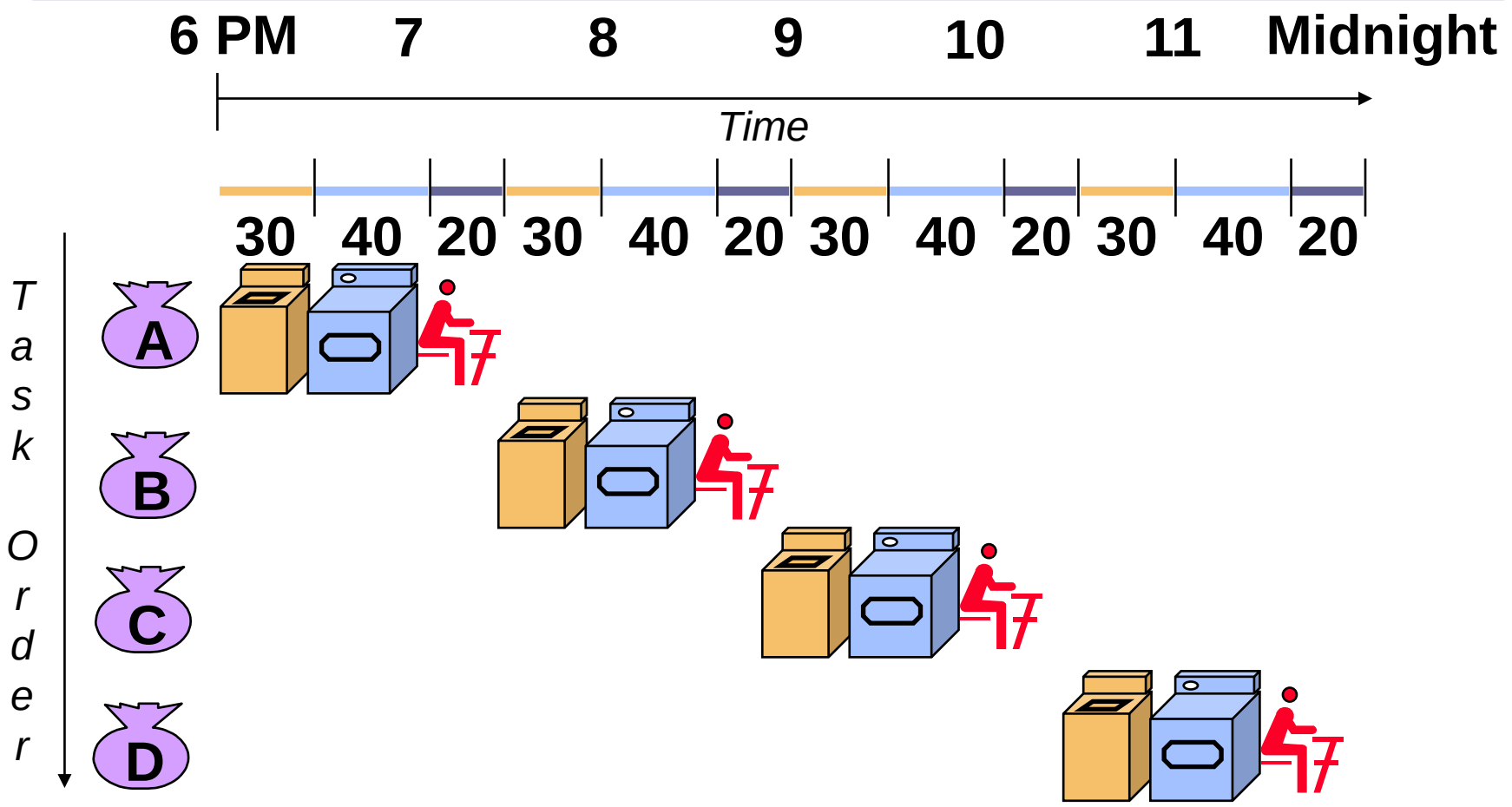




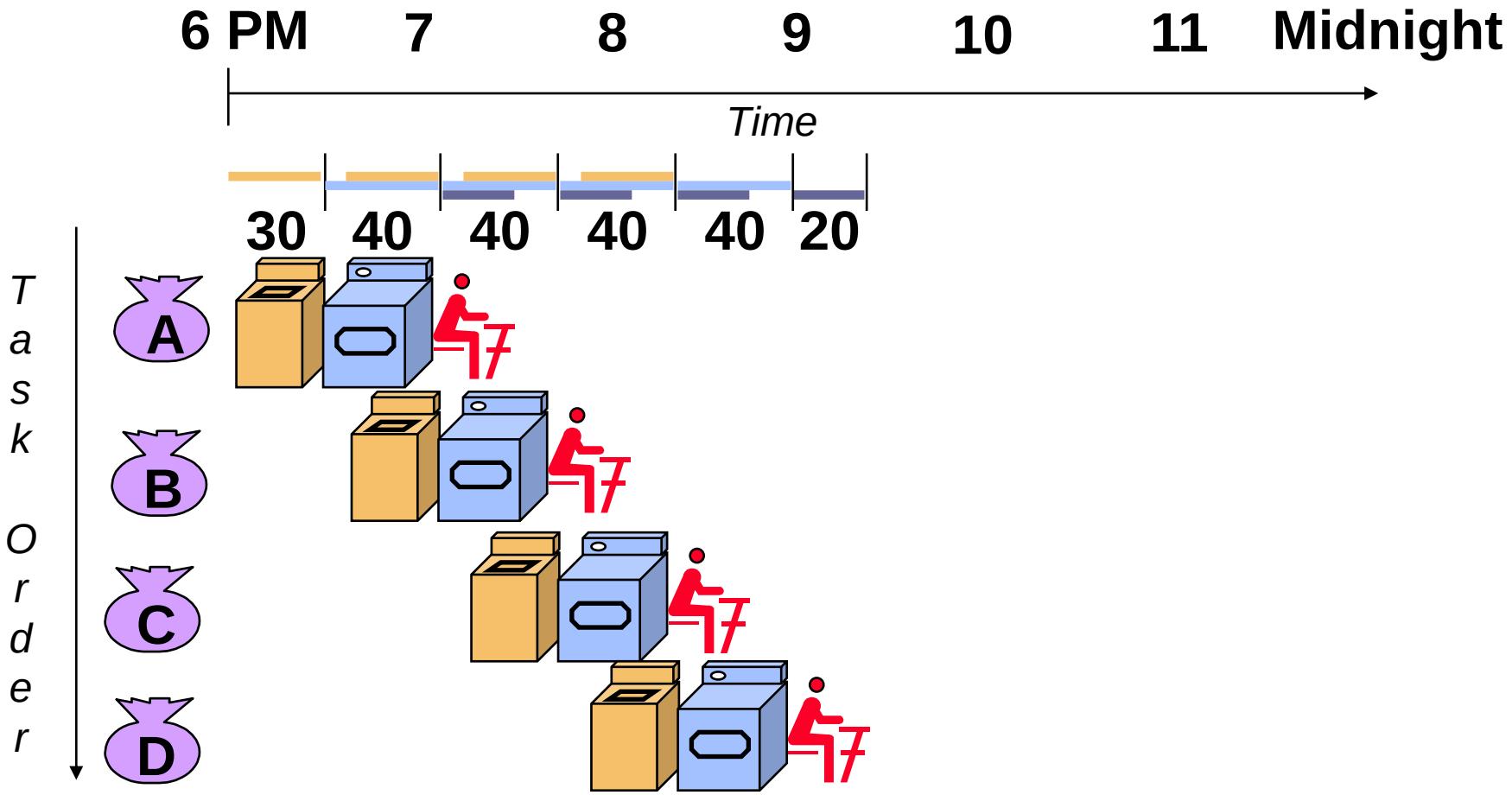
https://www.youtube.com/watch?v=ztw0QG0E23o

# Sequential Laundry



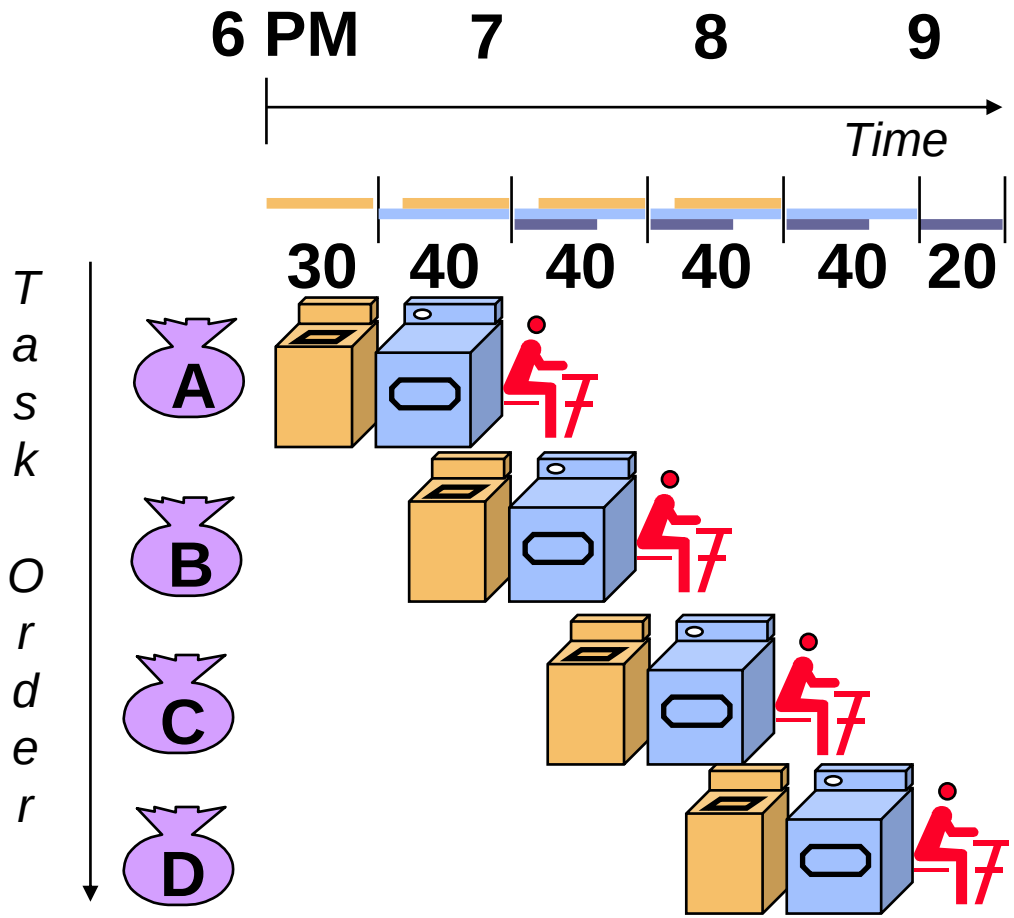

- Sequential laundry takes 6 hours for 4 loads
- If they learned pipelining, how long would laundry take?

# Pipelined Laundry – Start Work ASAP

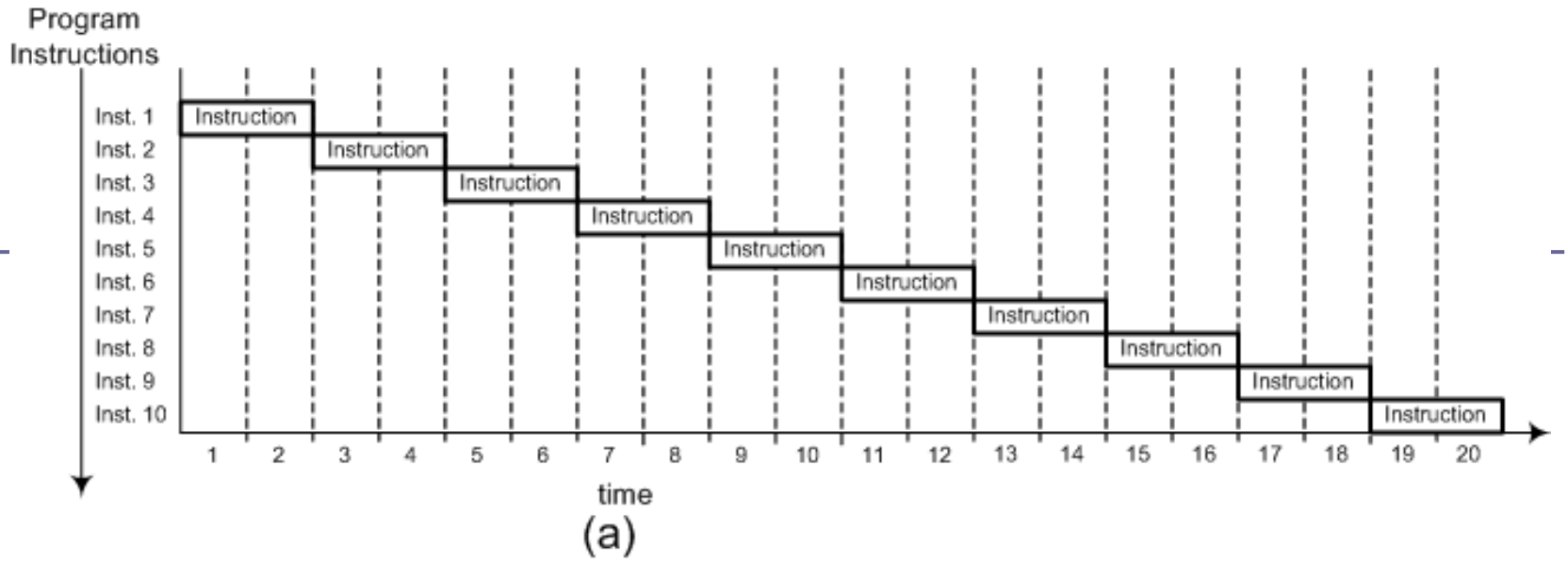


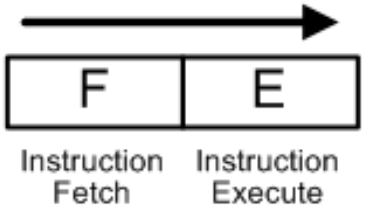

- Pipelined laundry takes 3.5 hours for 4 loads

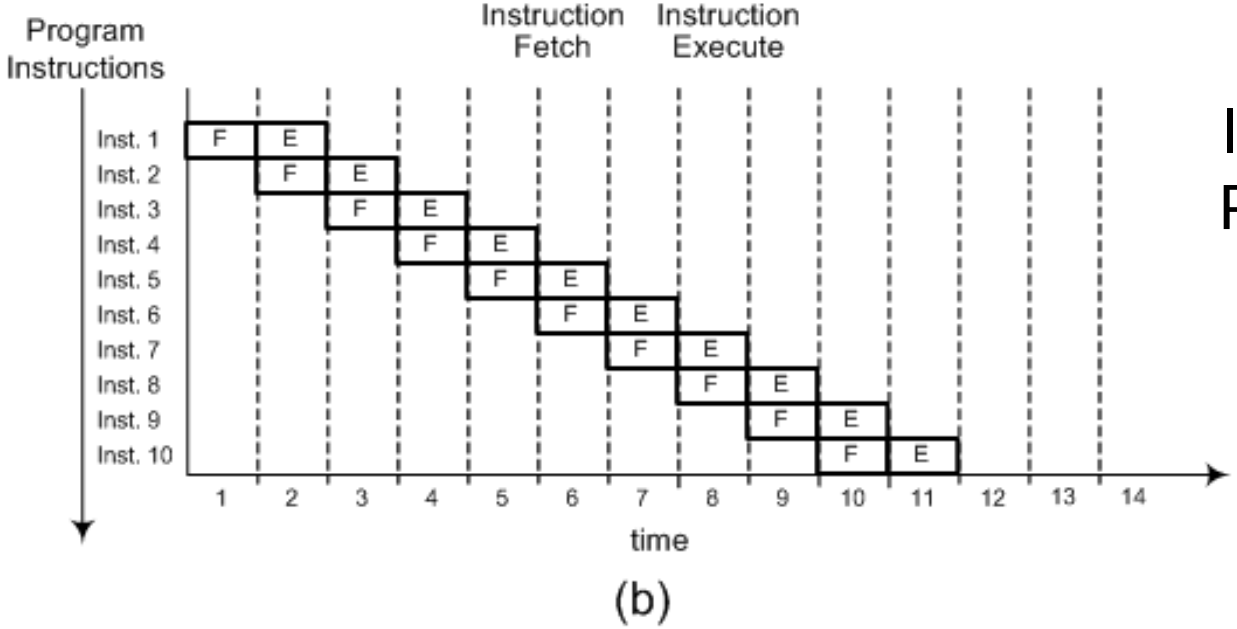
# Pipelining Lessons




- Pipelining doesn't reduce latency of a single task
- Improve throughput of entire workload
- Pipeline rate limited by slowest pipeline stage
- Multiple tasks operating simultaneously
- Potential speedup = No pipe stages
- Unbalanced lengths of pipe stages reduces speedup
- Time to fill pipeline & time to drain/flush it reduces speedup



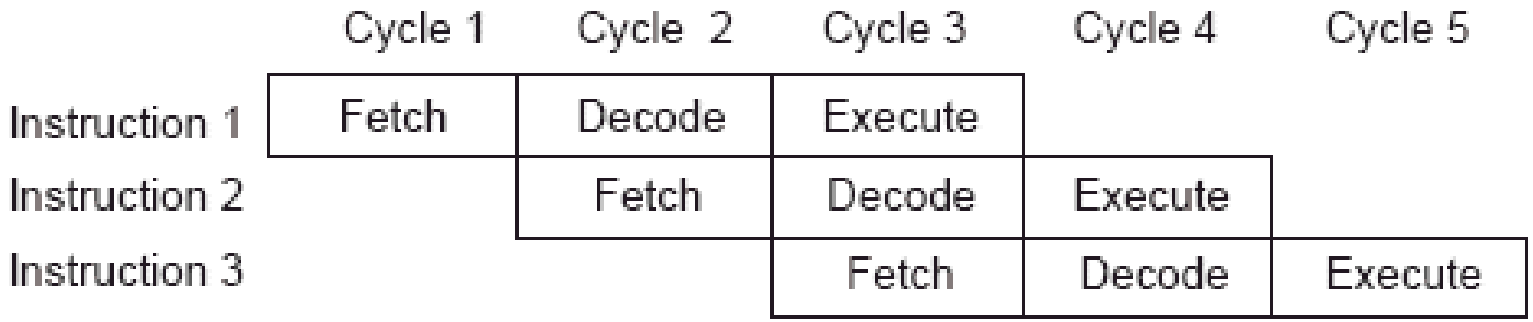



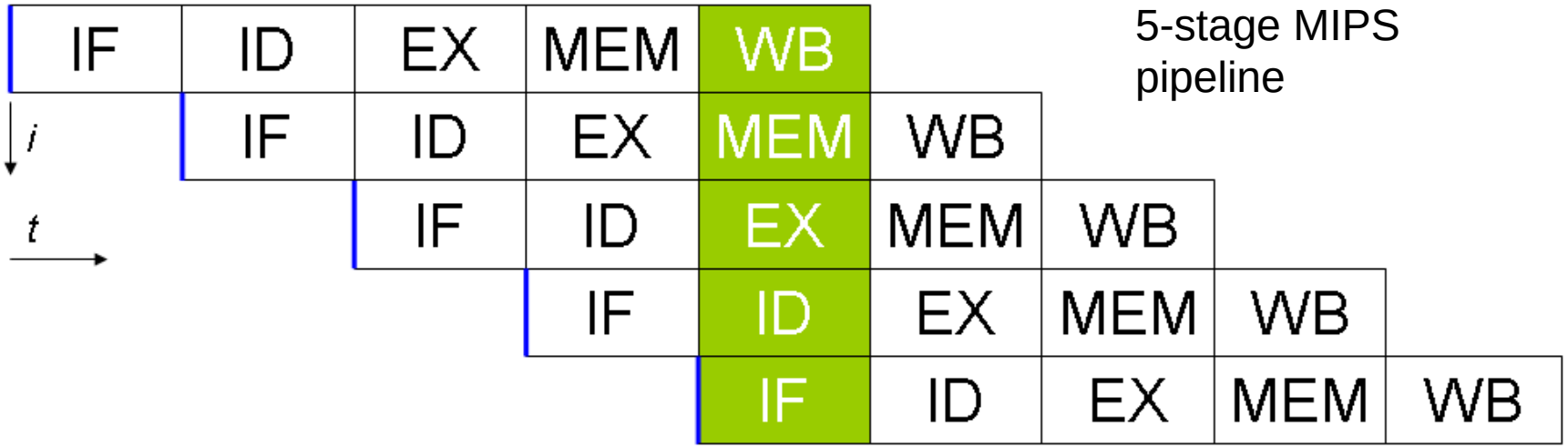




# Instruction Level Parallelism (ILP)

Source: http://mail.humber.ca/~paul.michaud/Pipeline.htm

# CPU Pipelines

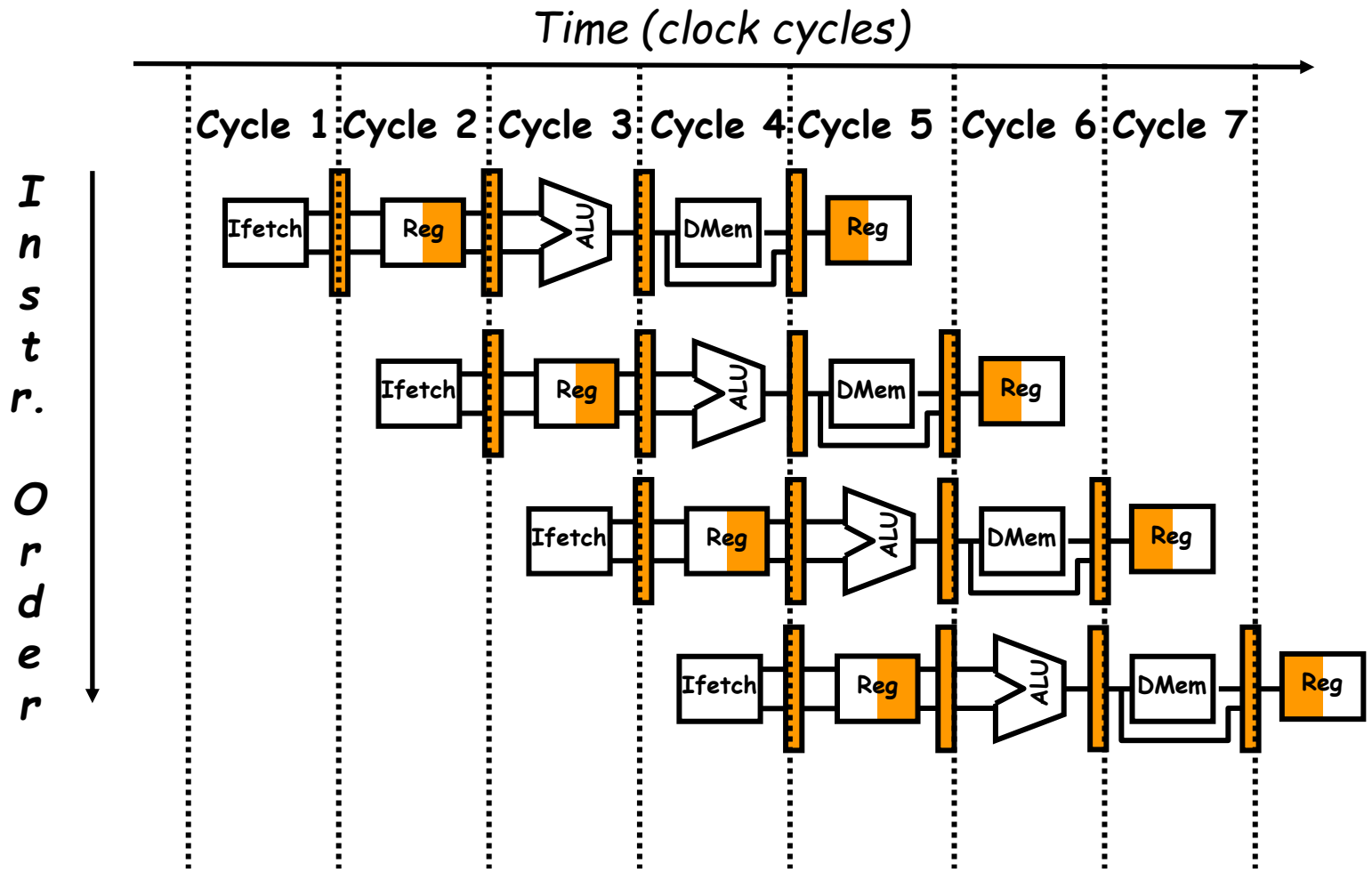



5-stage MIPS pipeline

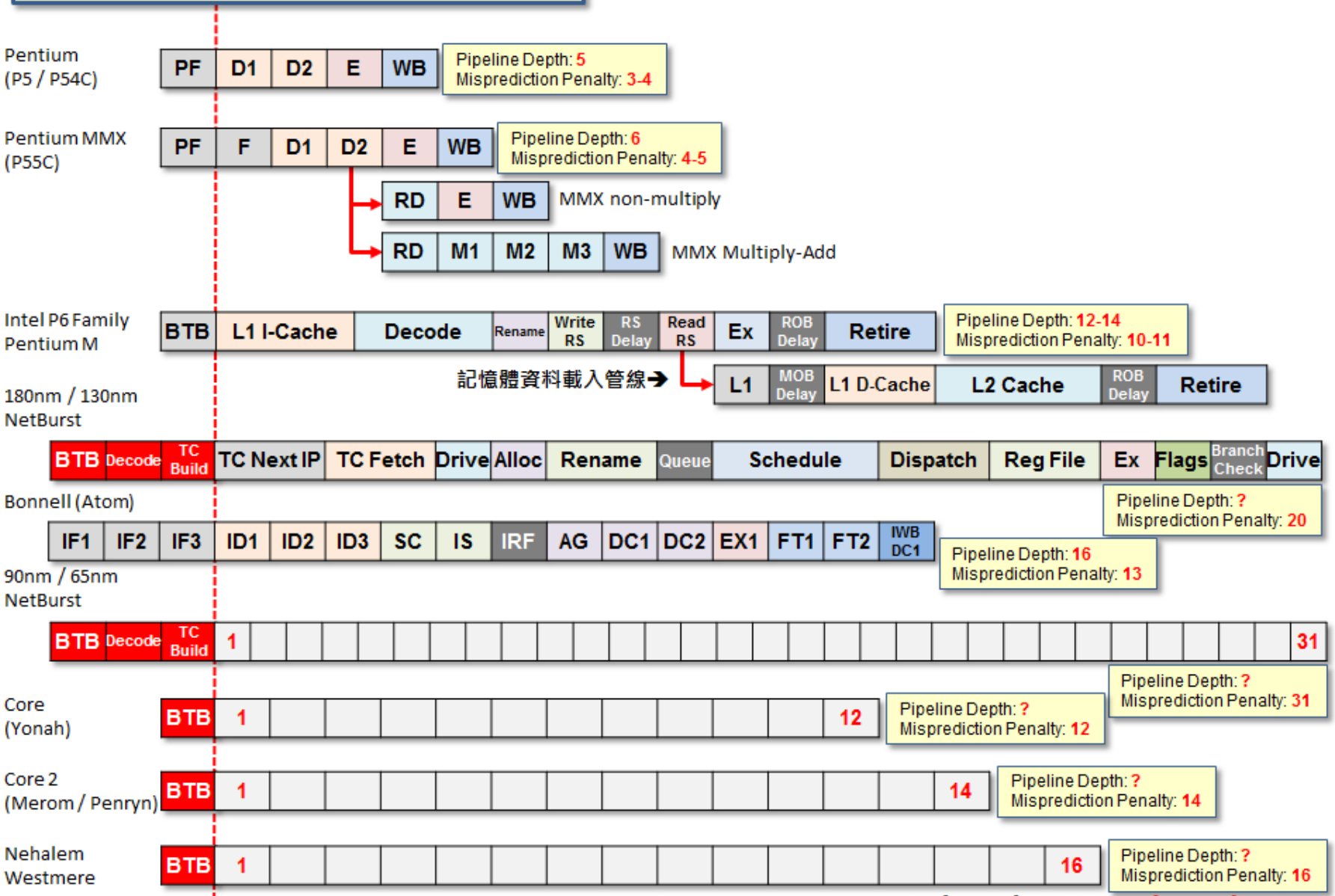
Source: http://en.wikipedia.org/wiki/Classic_RISC_pipeline

# Pipelined Instruction Execution



# Intel x86 Pipeline History

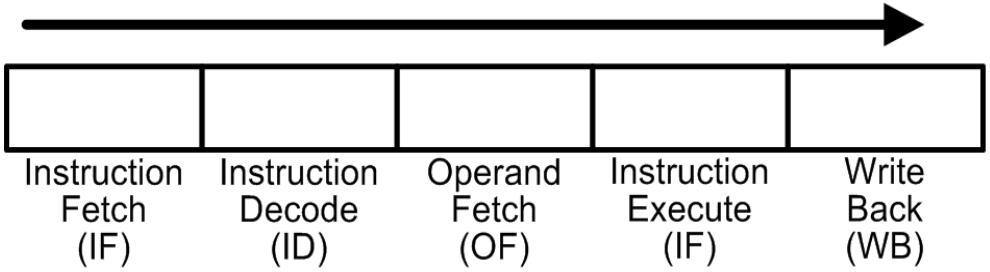




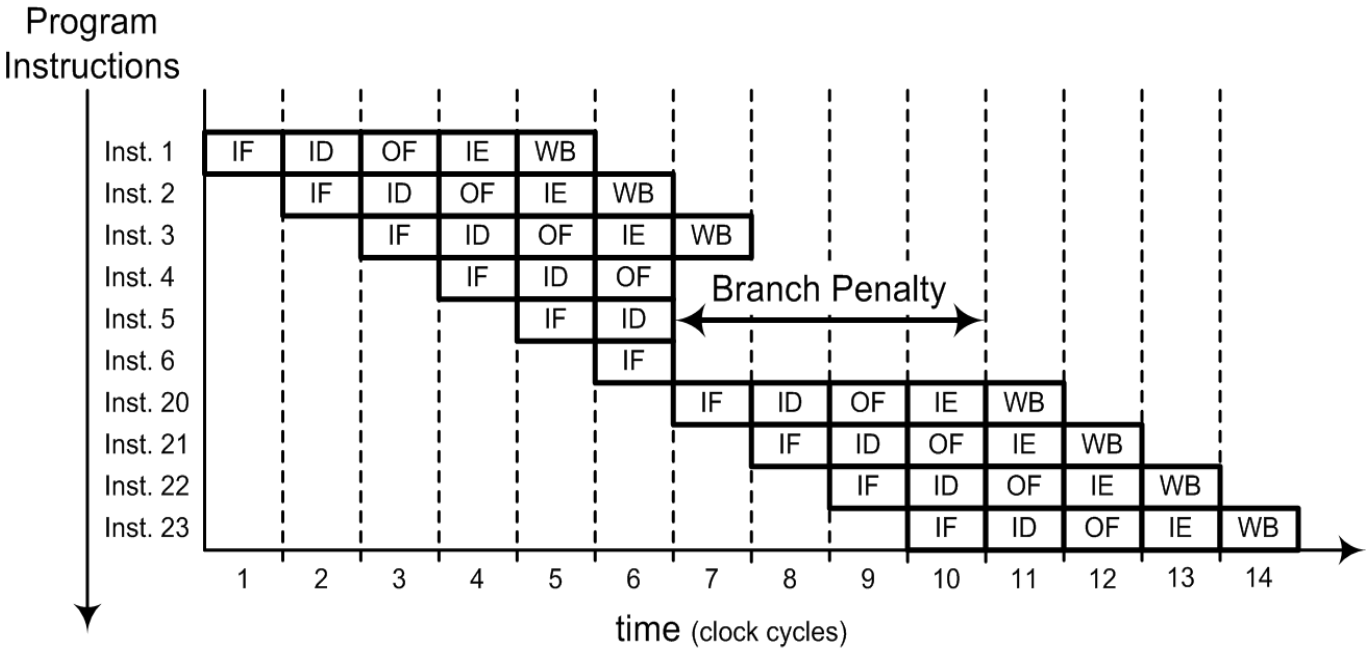



**Dedicated To PC ADV (電腦王) Taiwan**

# Pipeline With a Branch Penalty Due to a Taken Branch




5 Stage Instruction Pipeline




PIC instructions have a branch penalty of 1 CC

Source: http://mail.humber.ca/~paul.michaud/Pipeline.htm