Improved Prediction of Design Physical Area: A Sample Use Case

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***Abstract*—The abstract goes here. The OpenROAD Flow project aims to automate RTL to GDSII conversion, with a turnaround of 24 hours from the final RTL description to manufacturable layout. One important aspect of optimization is the actual silicon real estate occupied by the design, which in turn necessitates tuning of the height and width parameters used by the flow. The designer may choose these parameters directly, or set the utilization ratio and let the flow infer H and W based on that, neither of which yield in optimal results. In this paper, a case is made for an improved inference algorithm, along with a proposal to achieve that.**

1. Introduction

The OpenROAD flow aims to automate RTL to GDSII conversion, decreasing the time needed for getting a production-ready layout from an initial RTL description. It paves the way for many applications in design space exploration, including optimization of area and timing. One vital step is to infer basic parameters, including area and utilization, which are either explicitly set by the designer or implicitly inferred from the designer-provided metrics by the flow.

While studying logic locking [1], I encountered the interesting corner case in which the number of I/O pads relative to the number of cells became large. In this case, the flow sometimes failed to provide an accurate estimation for the design area, leading to errors in different stages and increasing the time needed for optimizing the design.

2. Logic Locking

A motivating example based on ISCAS85 C6288 [2] is shown in Fig. 1. The number of primary inputs and outputs is large (192) compared to the size of the circuit (2406 gates in the original description).

The resulting errors can be classified as follows, in order of the step in which a fatal error occurs:

1) Utilization $>$%70: Fails during IO placement with the message
`Number of pins (137) exceed number of valid positions (###).`

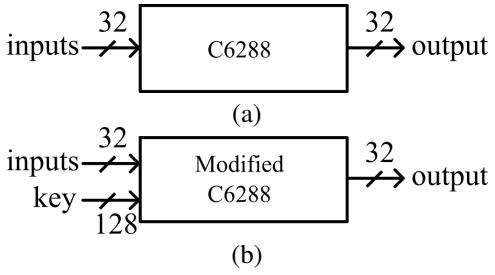

Figure 1. Motivating example. a) The original circuit. b) Modified circuit. This example has been exaggerated in numbers for demonstration.

2) %55 $>$Utilization $>$%70: Fails during resize with the message
`Detailed placement failed.`

Obviously, the sooner the flow terminates in case of an error, the less time needed for failed tests.

3. Proposal

An improved algorithm for estimating the physical dimensions of the designs would decrease the probability of failure. An extra check before resizing and optimization can cause the flow to fail sooner if it has to fail. These two changes would decrease the time needed for design space exploration when optimizing the area.

References

[1] L. Alrahis, S. Patnaik, M. Shafique and O. Sinanoglu, "MuxLink: Circumventing Learning-Resilient MUX-Locking Using Graph Neural Network-based Link Prediction," *2022 Design, Automation & Test in Europe Conference & Exhibition (DATE)*, Antwerp, Belgium, 2022, pp. 694-699, doi: 10.23919/DATE54114.2022.9774603.

[2] Bryan, D. "The ISCAS '85 benchmark circuits and netlist format [online] Available: https://davidkebo.com/documents/iscas85.pdf. Accessed Mar. 19, 2023.