4 December 2025

EECS 119

Project 4

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Introduction:

A 4-bit binary up/down counter is a sequential circuit that's designed with a Up or Down input and a clock input. Together these sequence many operational gates to activate however many bits are implemented into its design. Given our design parameters, there are 4 bits.

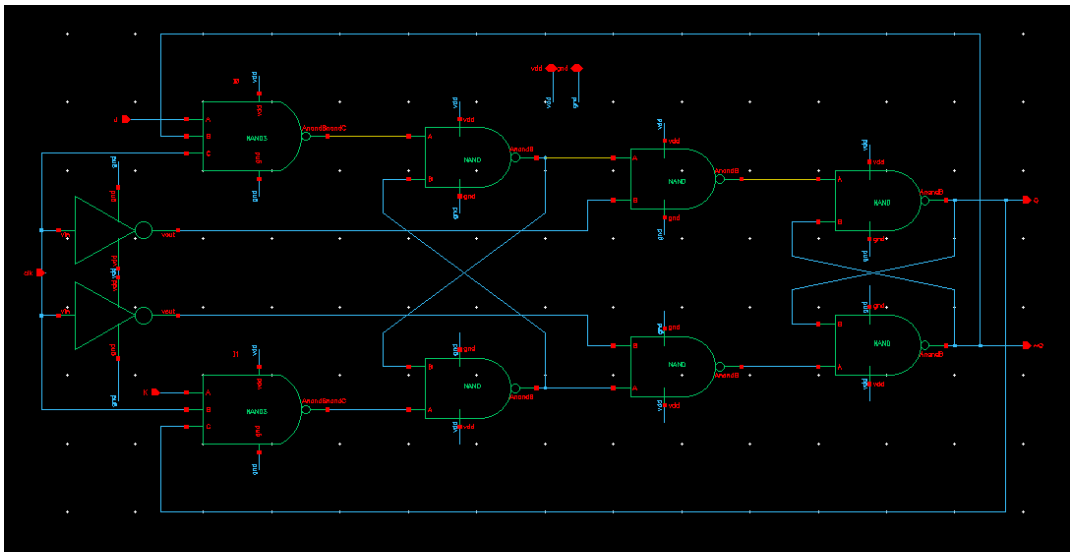
Theory:

To build the 4-bit binary up/down counter we must combine several different logic operation devices. These include an inverter, AND gate, OR gate, and a J-K flip flop with master-slave functionality. The purpose behind this specific Flip-Flop iteration is due to its ability to prevent a phenomenon called 'racing' which causes unintentional rapid toggling which only gets worse when it's necessary to cascade Flip-Flops together which in our case 4 are needed.

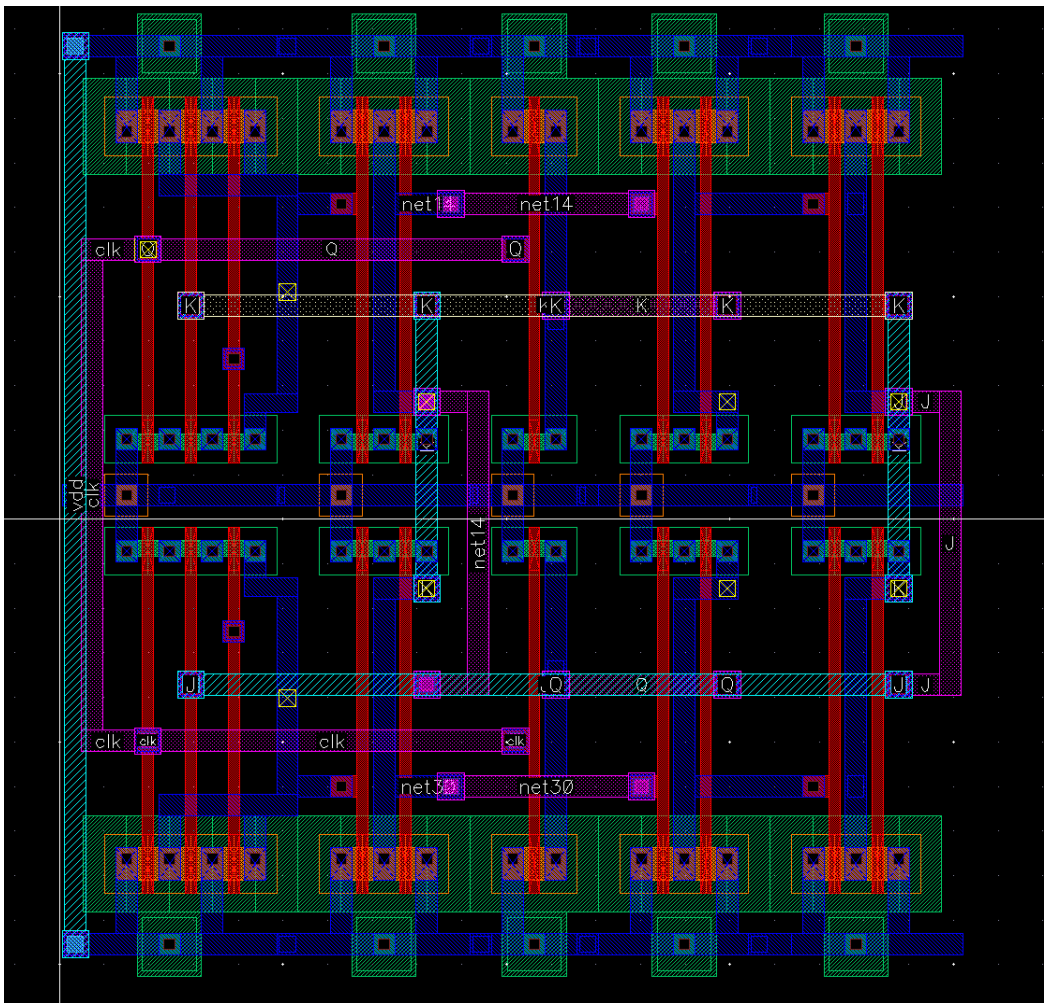
The counting sequence is determined by a single input we will refer to as UorD. UorD in an active state will cause the circuit to count up on each cycle of the clock which will be reflected in which of the 4 bits are active. UorD in a non-active state will cause the circuit to count down on each cycle of the clock, this too is reflected in the 4 output bits.

J-K Flip-Flop Design

J-K Flip Flop Design Schematic



J-K Flip Flop Layout

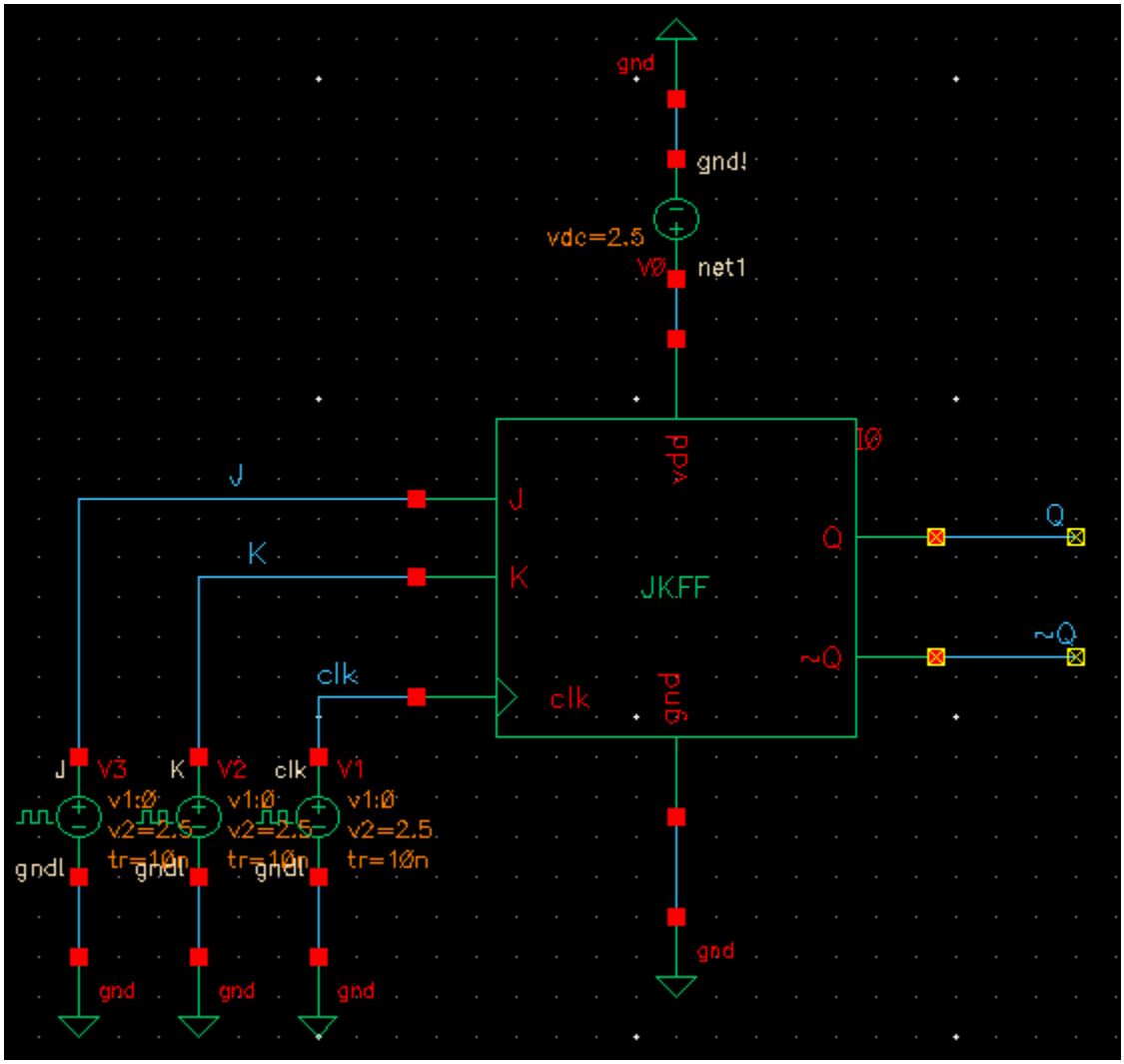


J-K Flip-Flop: LVS and DRC Verification Passing ✅

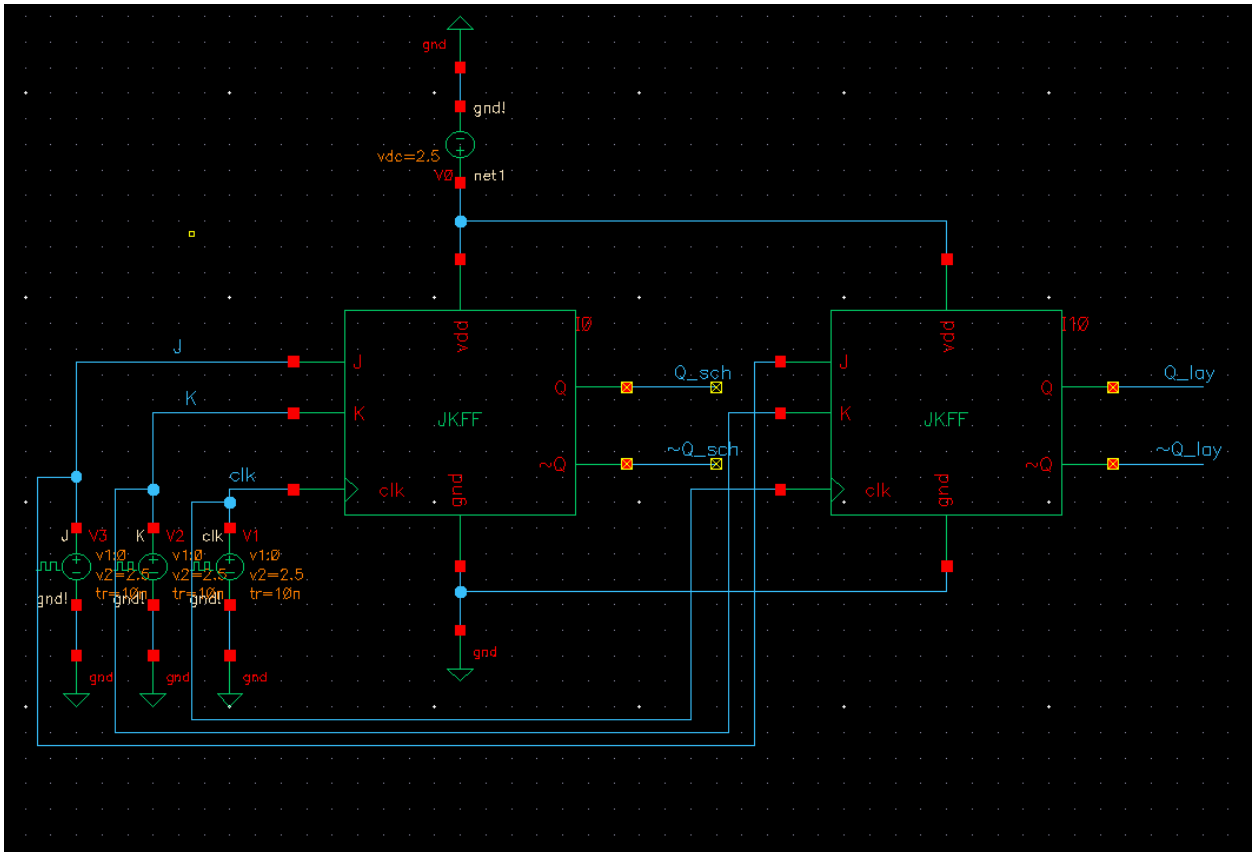
```
*********   Summary of rule violations for cell "JKFF layout"   *********
   Total errors found: 0

Getting layout propert bagGetting layout propert bagLVS job is now started...
The LVS job has completed. The net-lists match.

Run Directory: /users/ugrad/bjpaul/eecs119/Cadence6/LVS
```

*DRC is at the beginning of this console output followed by LVS

J-K Flip-Flop Test Bench

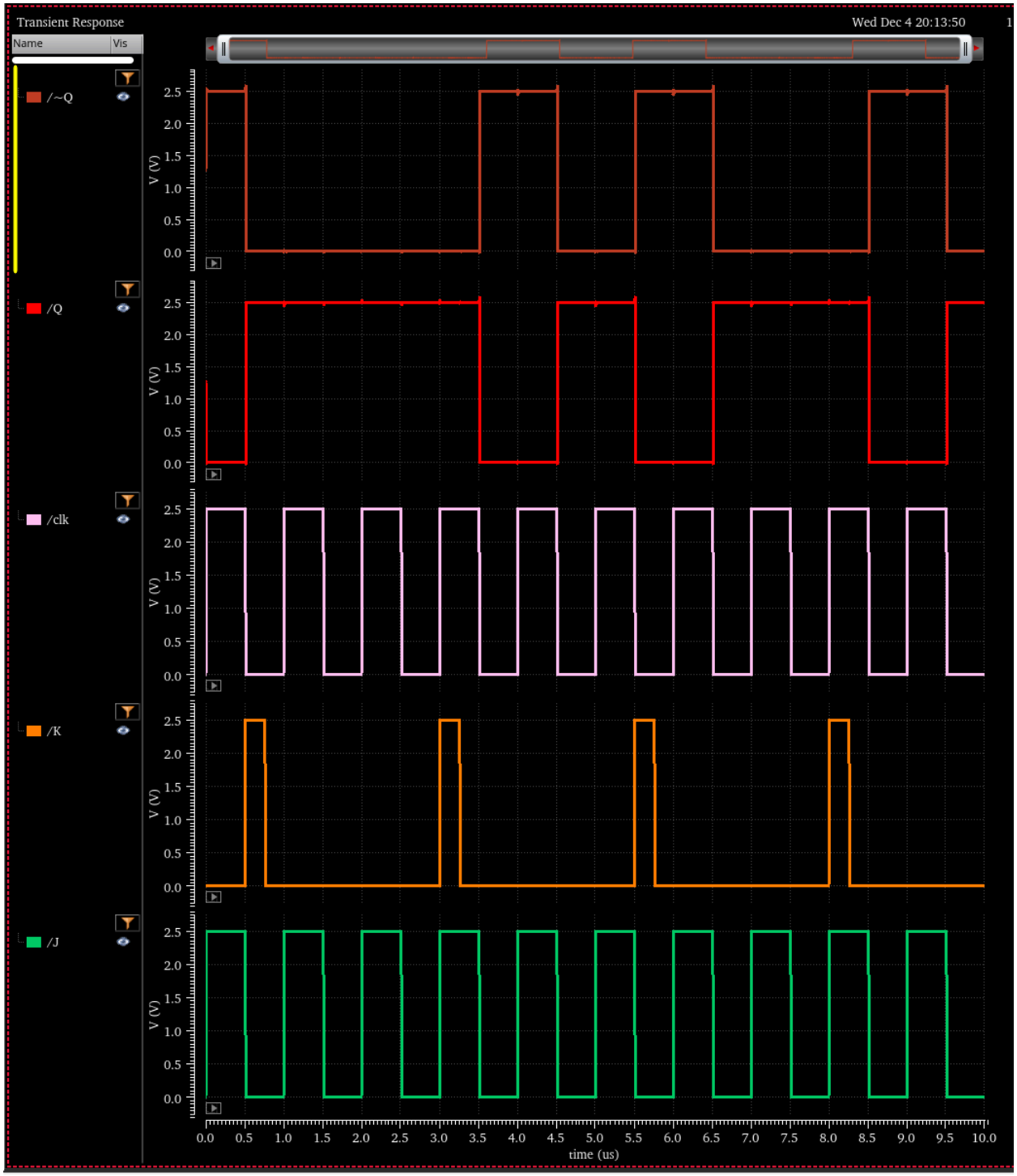


J-K Flip-Flop Layout Test Bench



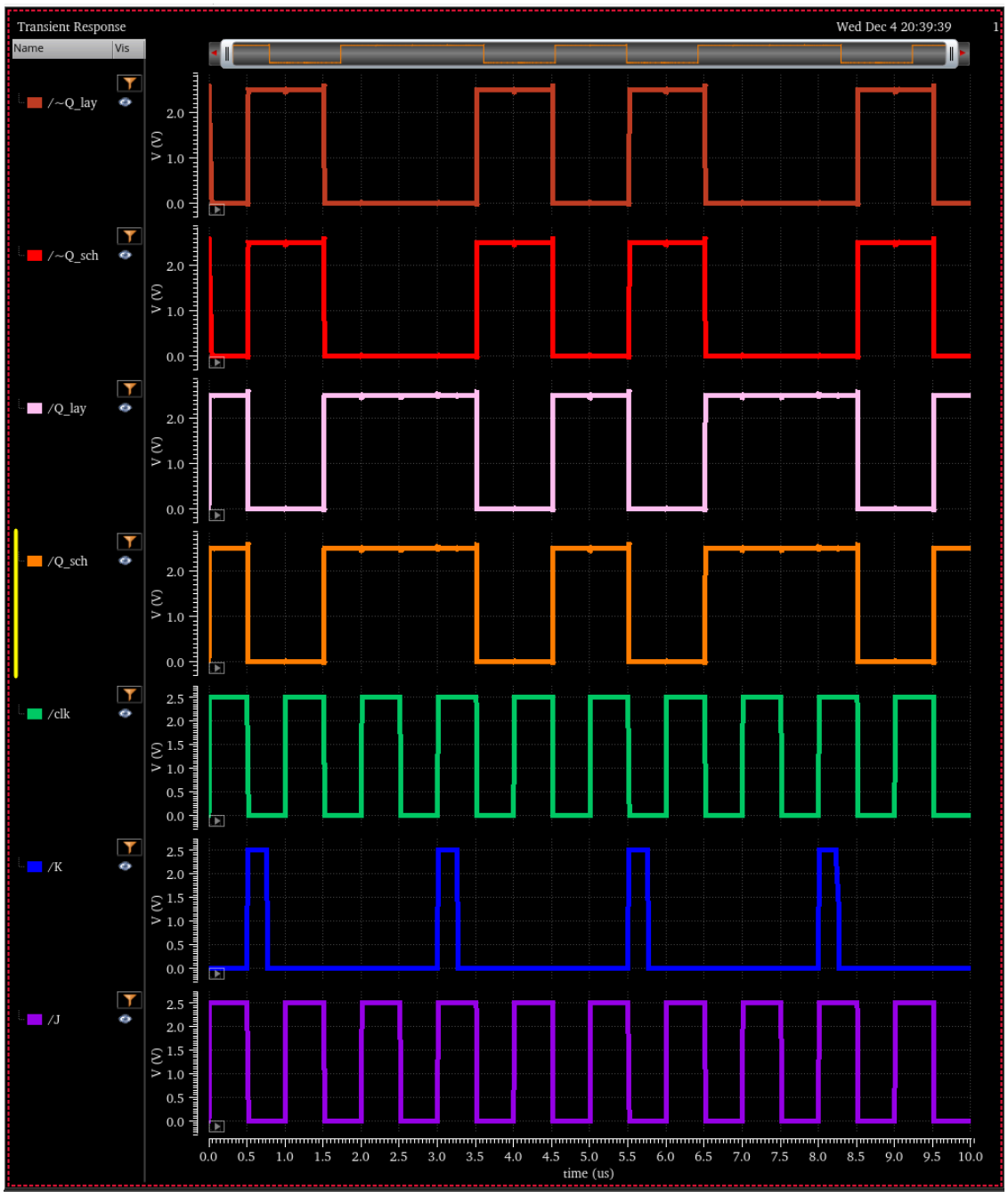
J-K Flip Flop Simulation Results

J-K Flip Flop Schematic Results



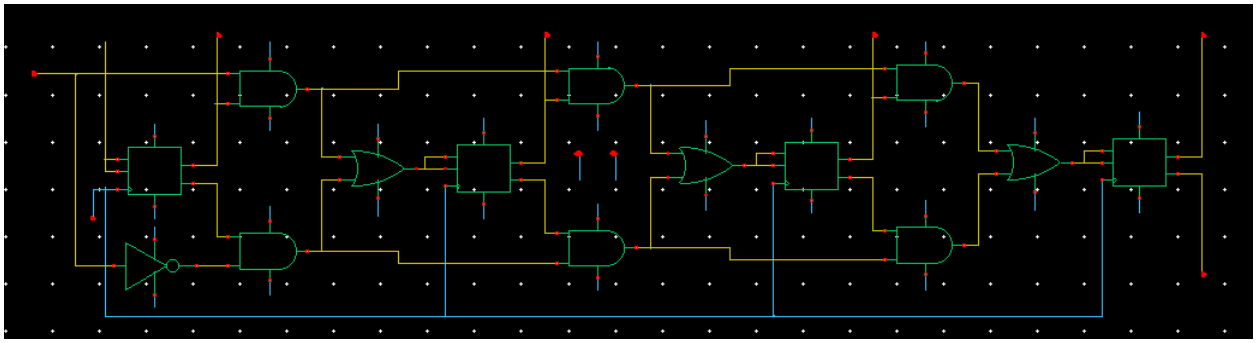
J-K Flip-Flop Layout Simulation Results


/~Q_lay
/~Q_sch
/Q_lay
/Q_sch
/clk
/K
/J

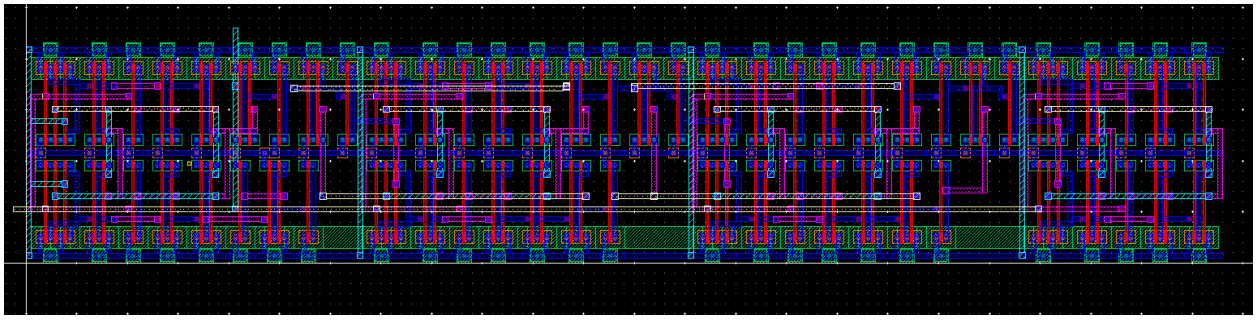

Transient Response
Wed Dec 4 20:39:39
Name
Vis
/~Q_lay
/~Q_sch
/Q_lay
/Q_sch
/clk
/K
/J
V (V)
time (us)
0.0 0.5 1.0 1.5 2.0 2.5 3.0 3.5 4.0 4.5 5.0 5.5 6.0 6.5 7.0 7.5 8.0 8.5 9.0 9.5 10.0

Binary Up/Down Counter Design

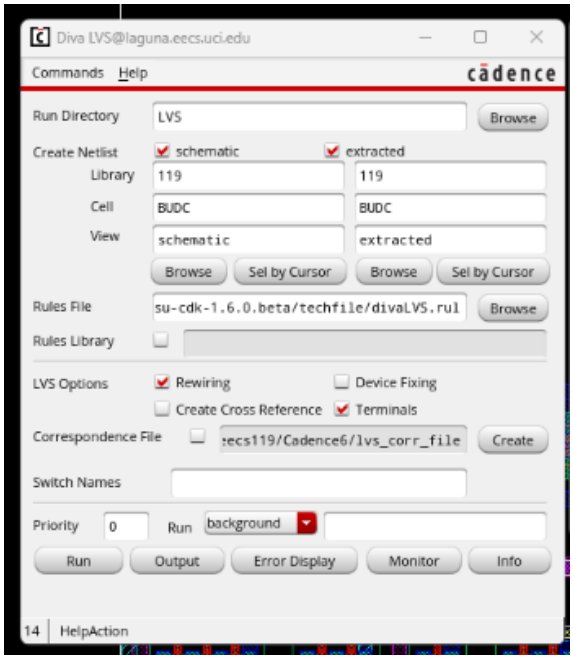
Binary Up/Down Counter Schematic

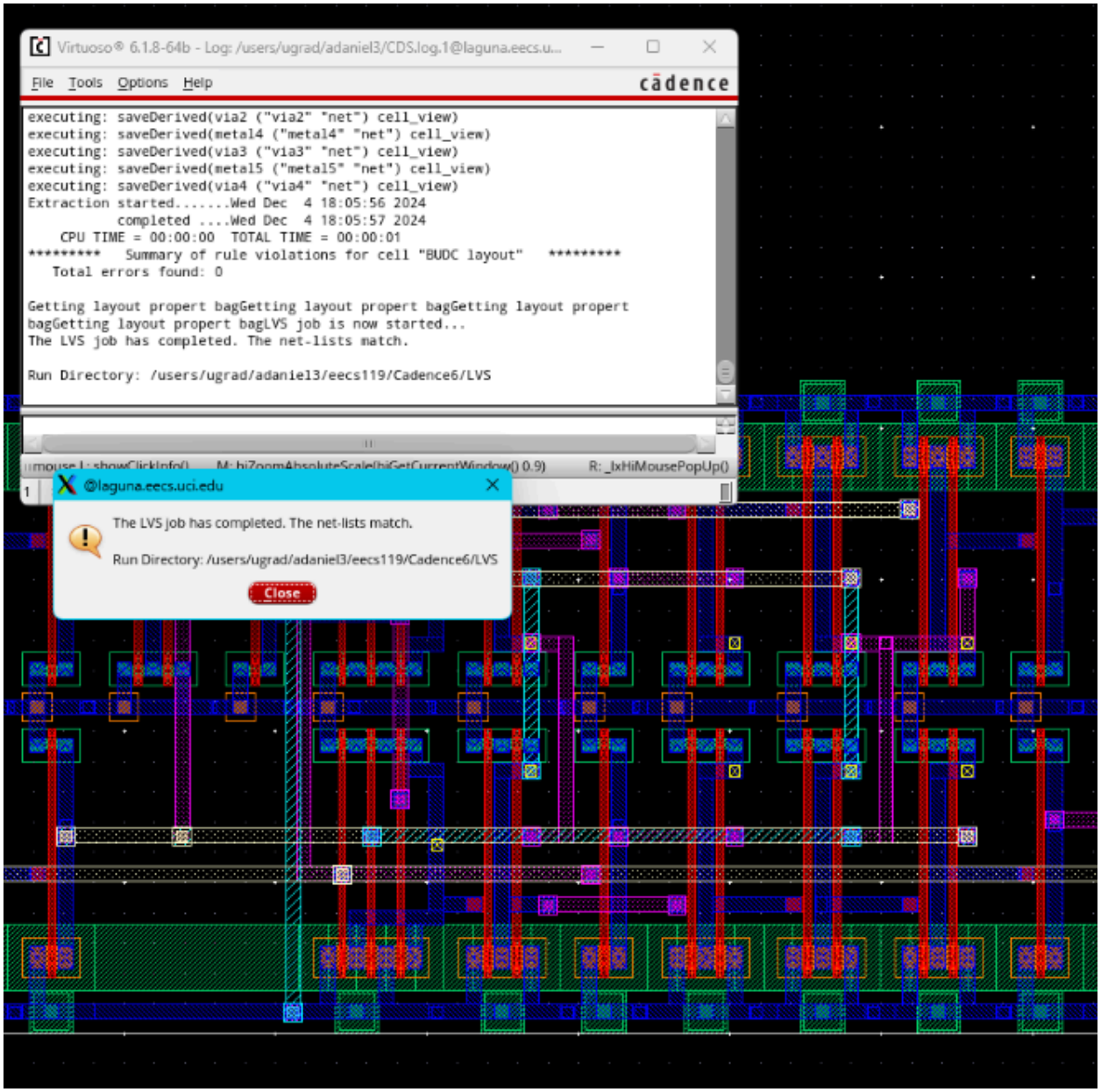


Binary Up/Down Counter Layout



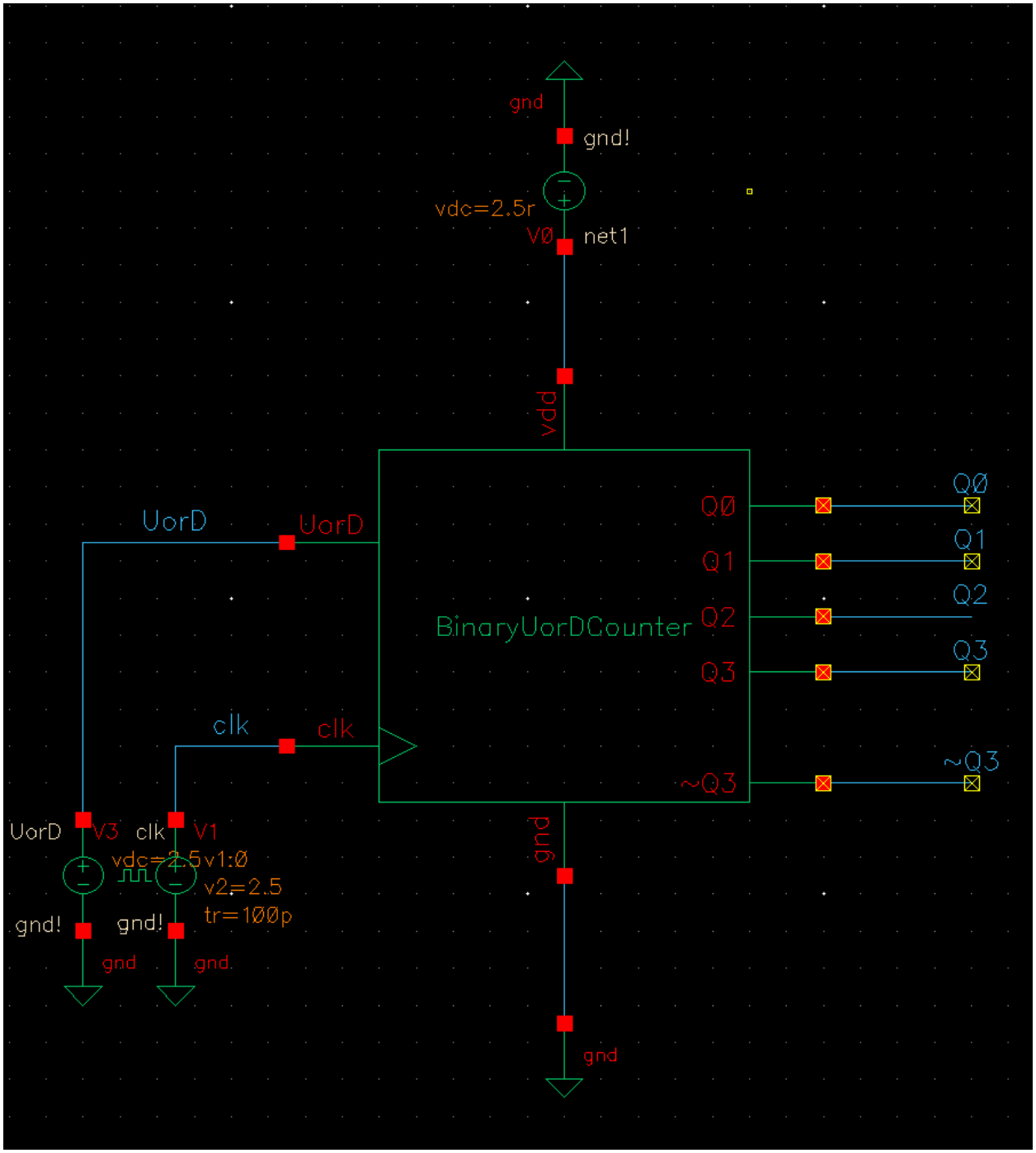
Binary Up/Down Counter: LVS and DRC Verification Passing ✅



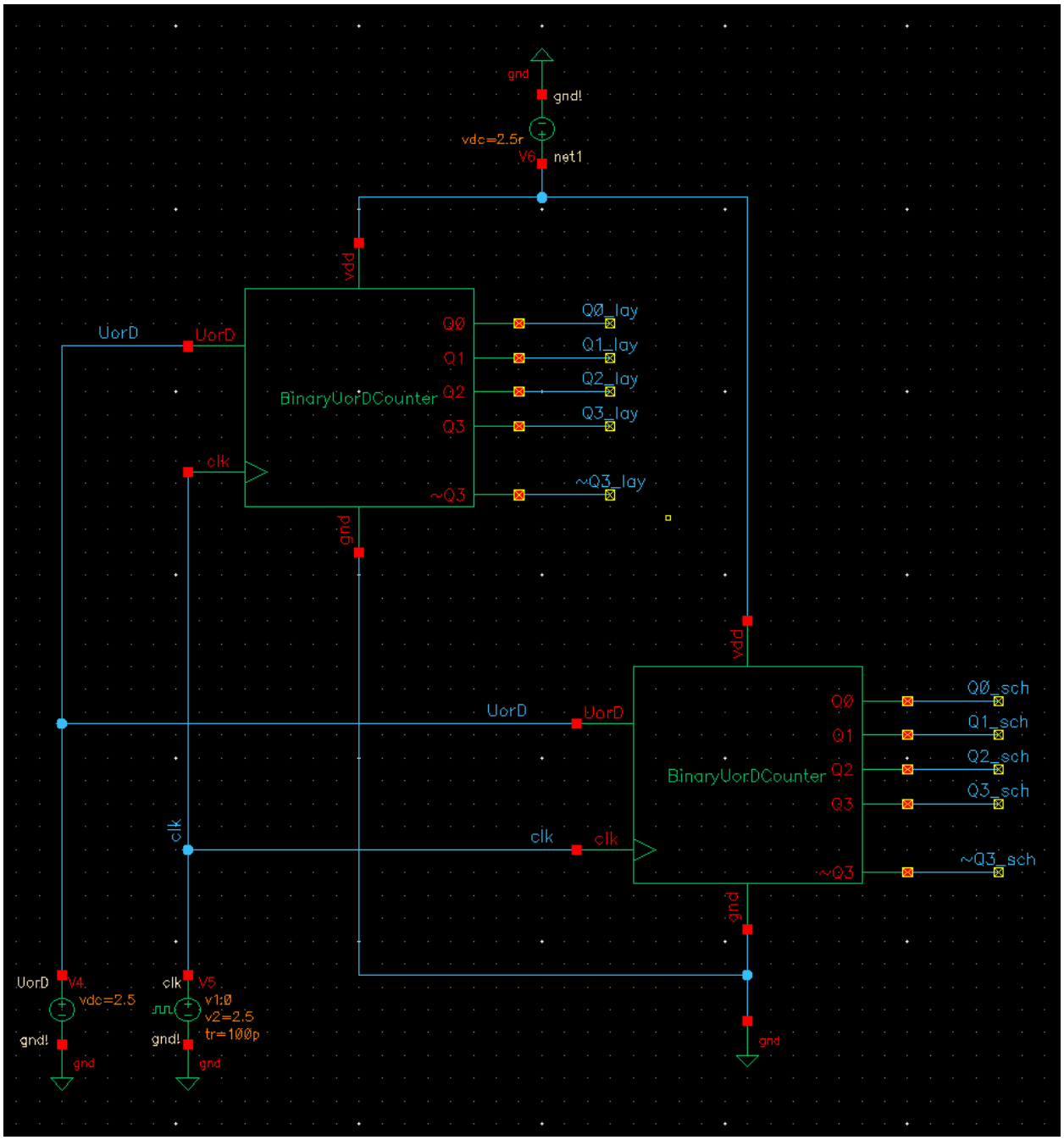


*DRC is listed in the console as having 0 total errors found

Binary Up/Down Counter Test Bench

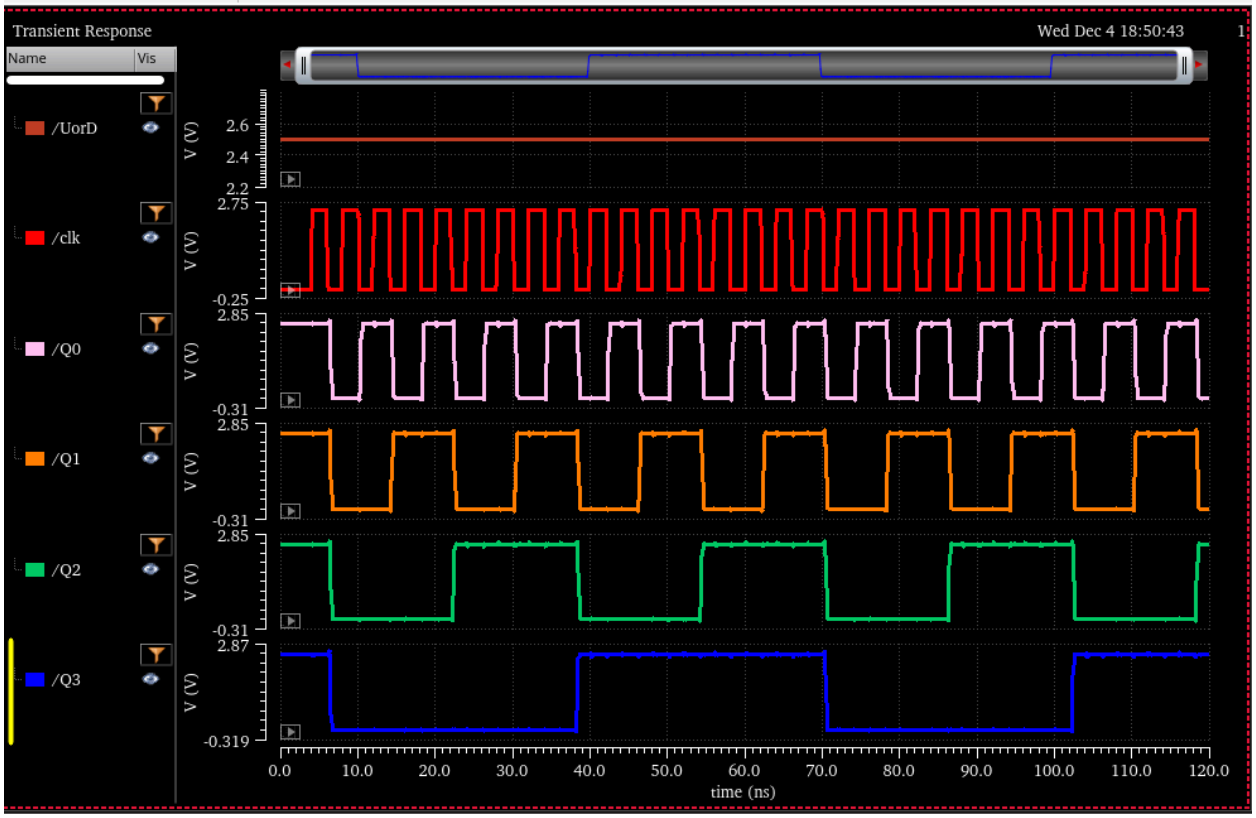


Binary Up/Down Counter Layout Schematic

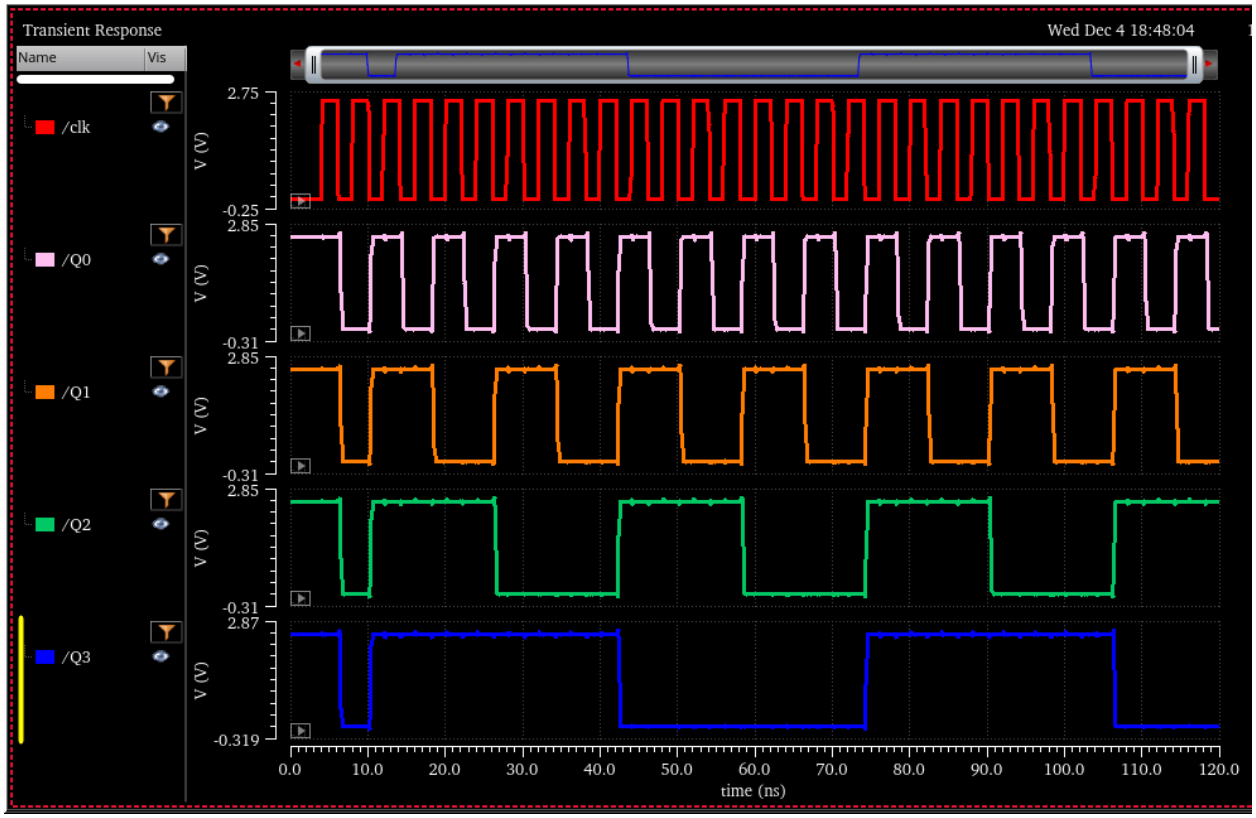


Binary Up/Down Counter Schematic Simulation

Binary Up/Down Counter: UorD at 2.5v Counting Up

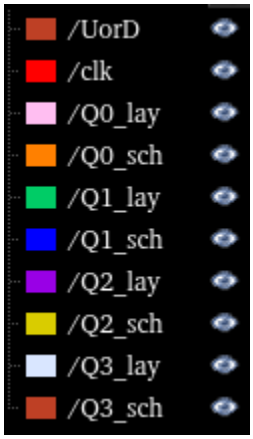


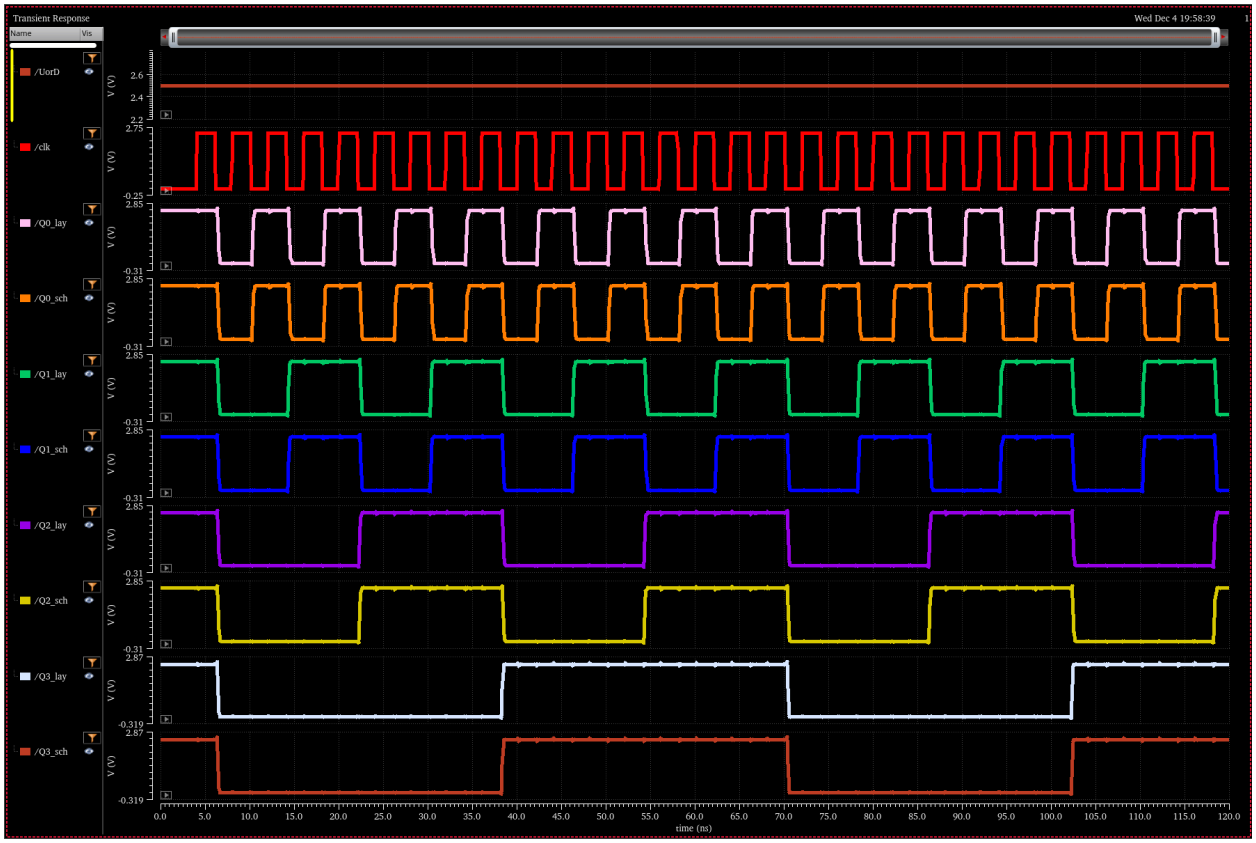
Binary Up/Down Counter: UorD at 0v Counting Down



Binary Up/Down Counter Layout Simulation

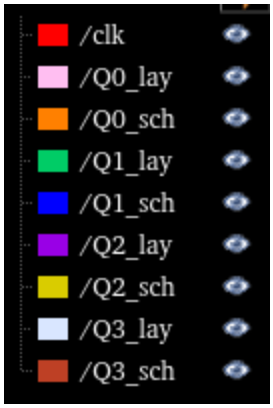
Binary Up/Down Counter Layout w/ Schematic comparison: UorD at 2.5v Counting Up

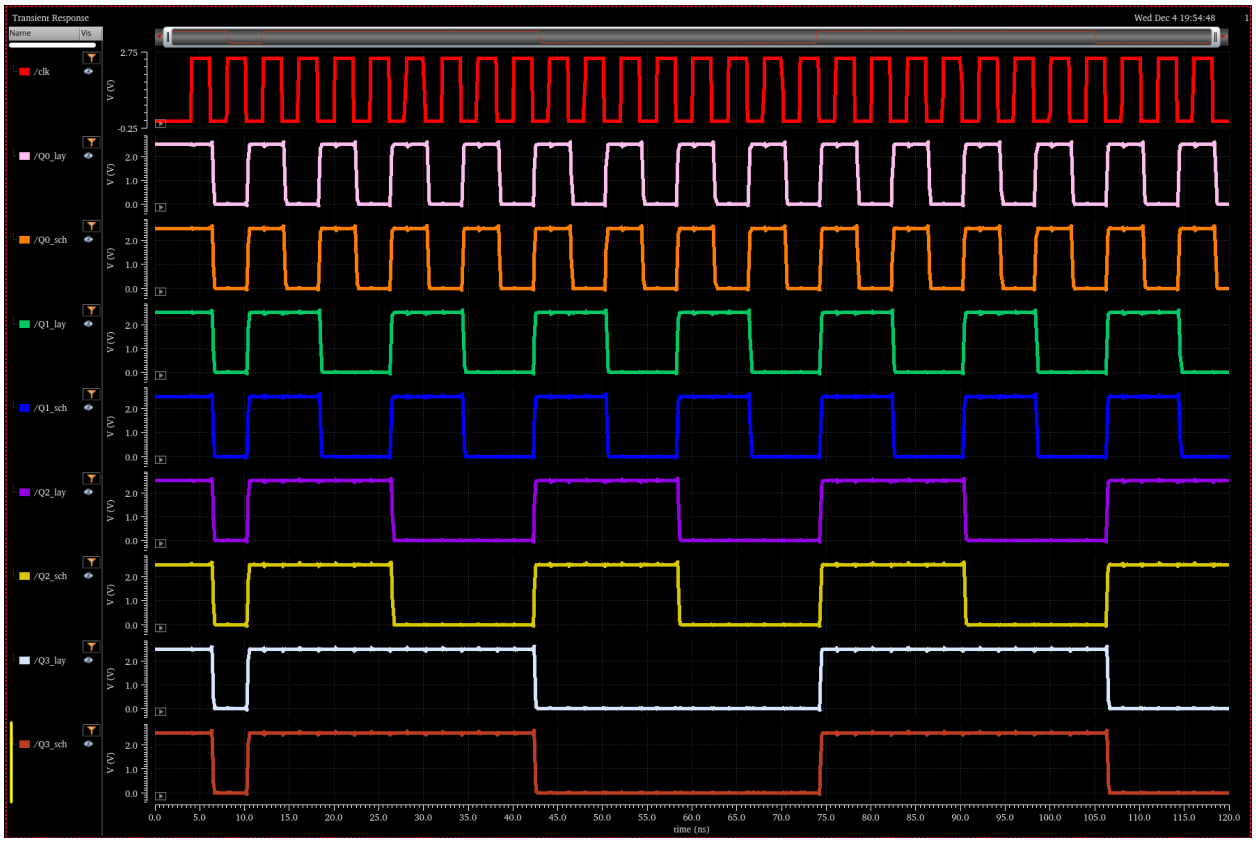




Layout and Schematics are staggered with schematic presented first from bottom to top (*sch then *_lay)

Binary Up/Down Counter Layout w/ Schematic comparison: UorD at 0v Counting Down





Layout and Schematics are staggered with schematic presented first from bottom to top (*_sch then *_lay)

***End of Cadence Screenshots**

Conclusion: In order to have a better understanding of VLSI design principles we designed a 4-bit Binary Up/Down Counter with functionality determined by a single input variable, UorD. Our successful implementation demonstrates the interplay between master-slave J-K flip-flops and logical gates to achieve reliable counting behavior in both up and down modes while adhering to design standards.