

- For $(N-1)$ philosophers → { wait (take fork (S.))
 (Philo left wala phis right wala) } wait (take fork (S+1) main)
- For N^{th} philosopher → { wait (take fork (S+1) main)
 (phile wo right fork) } wait (take fork (S));
 (other wala phis left)

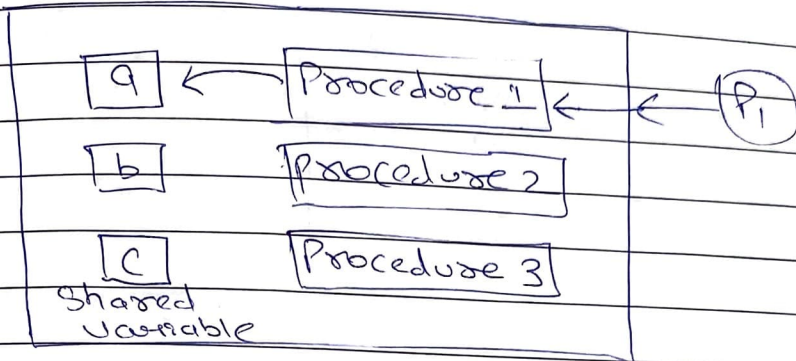
(Easy learning with nisha)

classmate

Date

Page

Monitors in Operating System



Monitor is a module that contains :-

- Shared data
- Procedure that operates on the shared data.

Syntax of monitor :-

monitor

{ Condition variables; → two operations
Variables;

Procedure 1

{ wait()
Signal() }

{

}

Procedure 2

{

}

}

End (100 k)

Practice Question on Binary Semaphore

Each process $P_i \{i = 1 \text{ to } 9\}$
Execute the following code -

Process P_0 executes the following code.

Diagram illustrating the execution flow of a semaphore:

- Entry Section** leads to **P(Mutex)**.
- P(Mutex)** leads to the **CS** (Critical Section).
- CS** leads to **V(Mutex)**.
- V(Mutex)** leads to **Exit Section**.
- The process then loops back to **Repeat** for every process.

```

do repeat
    V(mutex) ← Enter
    { CS }
    V(mutex) ← Exit
for all

```

What is maximum no. of processes that may present in CS at any point of time?

⇒ Index
 $\boxed{x} \neq x \neq x \neq x \neq x \neq x \dots$

→ P_1, P_2, P_3, P_4

CS | P_1 ~~P_2~~ P_3 ~~P_4~~
So on

In all the process
will come in C.S

max. $\Rightarrow 10$

If we change P_{10} ~~value~~ code \rightarrow

Mutex $\boxed{x} \neq 0$

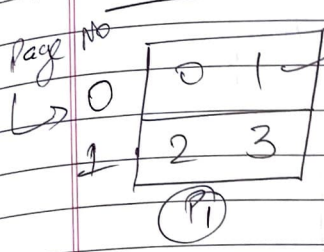
repeat
V(mutex) ← Enter
CS
P(mutex) ← Exit
forever

CS	$P_1 P_2$

now if P_0 execute will then
it pass through exit code which
decrease value of maxtex so it get blocked

max = 3

Paging



Bytes

frame no.

0	0	1
1	2	3
2	4	5
3	6	7
4	8	9
5	10	11
6	12	13
7	14	15

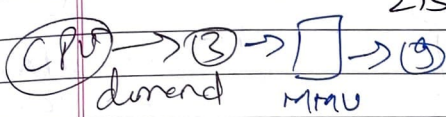
Process size = 4B
 Page size = 2B
 No. of Pages = $\frac{4B}{2B} = 2$

M/M

M/M size = 16B
 frame size = 2B

No. of frames = $\frac{16B}{2B}$

⇒ 8 frame



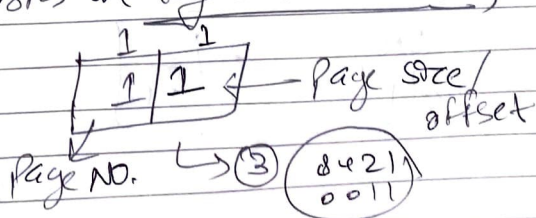
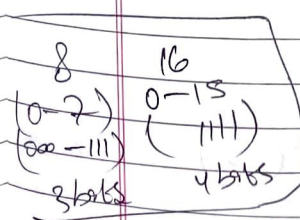
Page size = frame size

Page table of P₁

0	f ₂
1	f ₄

P₁

CPU always works on logical addresses,



2 bits → 4 2 no. ko dependent karne ke bye 1 bit

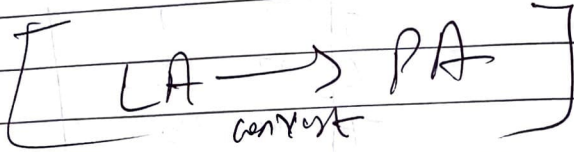
logical address



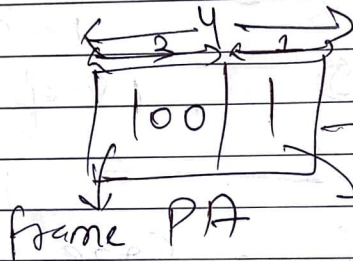
page no. m

Jana hai

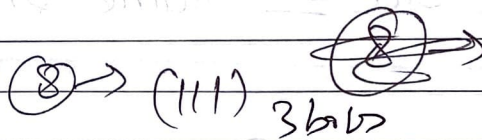
1st bit no accept karna hai.



Physical address directly related to Main memory.



no.

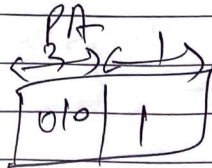
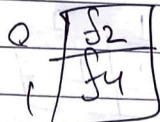
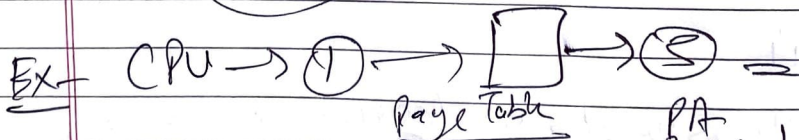


4 → 8421
0100

(16) → Ko represent kare ki logk 4 bits

This bit will be same as LA.

So (1001) → (9)



0101 → (5)