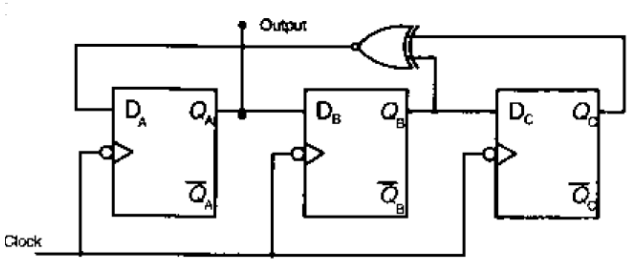
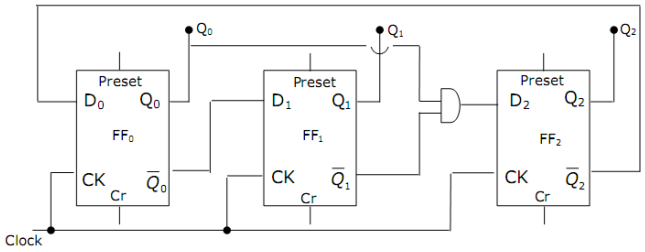
JAYPEE INSTITUTE OF INFORMATION TECHNOLOGY, NOIDA
Electronics and Communication Engg.
B.Tech. IInd year
Digital Systems (18B11EC213) Even Sem
Tutorial-4

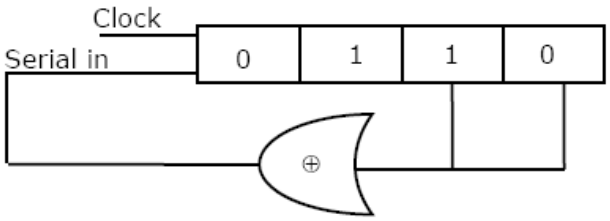
Q1. Assuming all the filp flop are in reset condition initially. The count sequence observes at Q_A will be: [CO3]



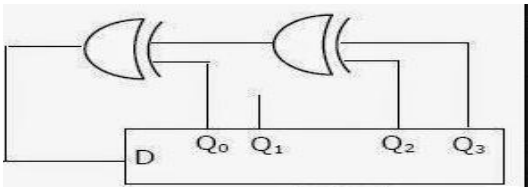
Q2: A sequence generator is shown in figure. The counter status ($Q_0Q_1Q_2$) is initialized to 010 using preset/clear input, the transition in clock pulse takes at rising clock edge. Find the sequence generated at counter till it repeats. [CO3]



Q3: The initial contents of the 4 bit serial in serial out, right shift, shift register are shown in figure, are 0110. After 3 clock pulses are applied, the content of shift register will be: [CO3]

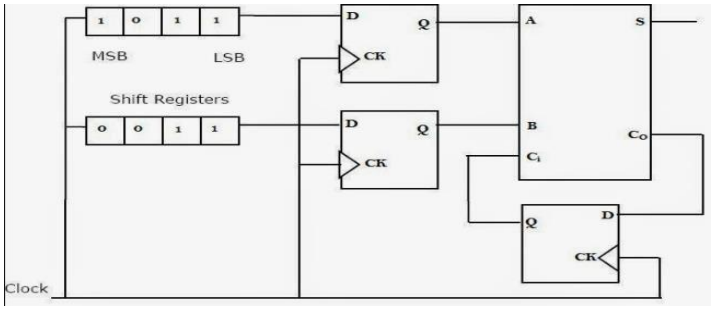


Q.4: A 4 bit shift register, which shift 1 bit to the right at every clock pulse is initialized to values 1000 for ($Q_0Q_1Q_2Q_3$). The D input is derived from Q_0, Q_2 and Q_3 through two XOR gates as shown in figure. [CO3]

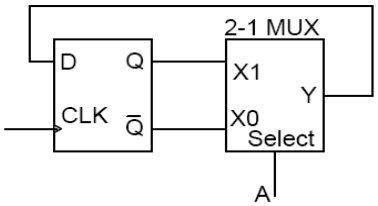


a) Write 4 bit values ($Q_0Q_1Q_2Q_3$) after each clock pulse till the pattern (1000) reappear on ($Q_0Q_1Q_2Q_3$)
b) To what values should the shift register be initialized so that pattern (1001) occurs after the first clock pulse?

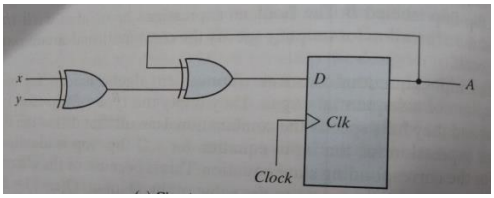
Q5: For the circuit shown, two 4-bit parallel in serial out shift registers loaded with the data shown are used to feed the data to a full adder. Initially all flip flop are at clear state. After applying two clock pulses, the output sum and carry of the full adder will be: [CO3]



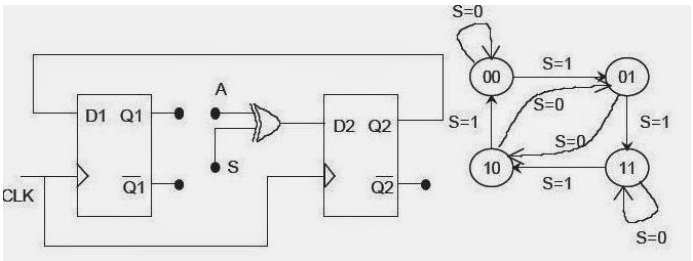
Q.6: Draw the state transition diagram for the given circuit: [CO3]



Q.7: For given circuit draw state table and state transition diagram. [CO3]



Q8: The digital logic shown in the figure satisfies the given state diagram when Q_1 is connected to input A of XOR gate. Suppose XOR is replaced by XNOR gate. Which one of the following options preserves the state diagram? [CO3]



a) Input A connected to $Q2$
b) Input A connected to Q2
c) Input A connected to $Q1$ and S is complemented.
d) Input A connected to $Q1$

Q9: Design Mod – 6 synchronous up/down counter. [CO3]