Interface two 4k×8 EPROM & two 4k×8 RAM chips with 8086:-

$4k = 2^{12} \Rightarrow$ 12 Address line

Chip		A_{19} A_{18} A_{17} A_{16}	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0	ADDRESS
RAM1	SA	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	00 000 H
	EA	0 0 0 0	0 0 0 1	1 1 1 1	1 1 1 1	1 1 1 0	01 FFEH
RAM2	SA	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 1	00001 H
	EA	0 0 0 0	0 0 0 1	0 0 0 0	0 0 0 0	0 0 0 1	01 FFFH
ROM1	SA	1 1 1 1	1 1 1 0	0 0 0 0	0 0 0 0	0 0 0 0	FE000
	EA	1 1 1 0	0 0 0 1	1 1 1 1	1 1 1 1	1 1 1 0	FFFFE
ROM2	SA	1 1 1 1	1 1 1 0	0 0 0 0	0 0 0 0	0 0 0 1	FE001
	EA	1 1 1 1	1 1 1 1	1 1 1 1	1 1 1 1	1 1 1 1	FFFFF H

$8k = 2^{13}$

$\Rightarrow$ 0000 0001 1111 1111 1111

   0 1 F F F

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  FFFFF
- 01FFF
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  FE000
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↑
Starting address of ROM