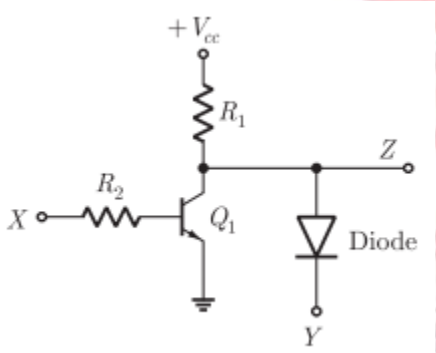
DIGITAL ELECTRONICS

1. In the circuit shown below, Q1 has negligible collector-to-emitter saturation voltage and the diode drops negligible voltage across it under forward bias. If Vcc is +5 V, X and Y are digital signals with 0 V as logic 0 and Vcc as logic 1, then the Boolean expression for Z is

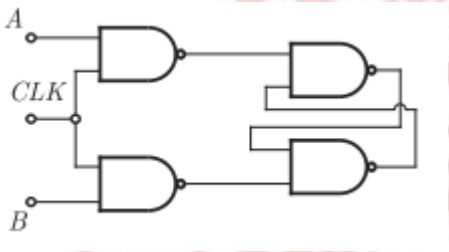


(A) XY (B) X'Y (C) XY ' (D) X'Y'

2. A bulb in a staircase has two switches, one switch being at the ground floor and the other one at the first floor. The bulb can be turned ON and also can be turned OFF by any one of the switches irrespective of the state of the other switch. The logic of switching of the bulb resembles

(A) AN AND gate (B) an OR gate **(C) an XOR gate** (D) a NAND gate

3. Consider the given circuit



In this circuit, the race around

(A) Does not occur

(B) Occur when CLK = 0

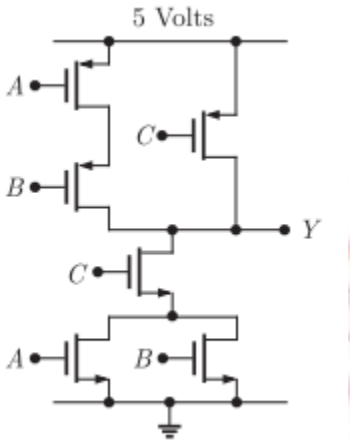
(C) Occur when CLK = 1 and A= B=1

(D) Occur when CLK =1 and A=B=0

4. The output Y of a 2-bit comparator is logic 1 whenever the 2-bit input A is greater than the 2-bit input B. The number of combinations for which the output is logic 1, is

(A) 4 (B) 6 (C) 8 (D) 10

5. In the circuit shown

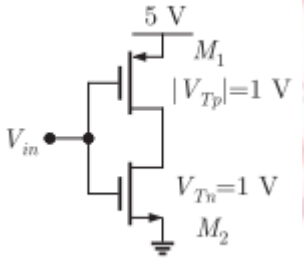


(A) **Y= A'B'+ C'** (B) Y= (A + B) C (C) Y=(A' + B ')C' (D) Y= AB+ C

6. In the sum of products function f(X,Y,Z) = ∑(2,3,4,5) the prime implicants are

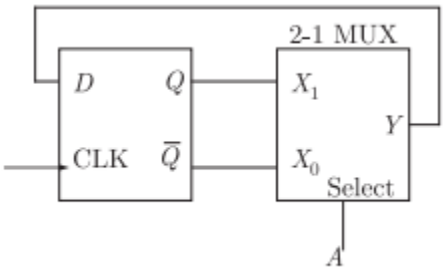
(A) X'Y, XY '(B) X'Y, X Y' Z', XY' Z (C) X'Y Z ',X'YZ, XY' (D) X'Y Z', X'YZ ,XY' Z', XY' Z

7. In the CMOS circuit shown, electron and hole mobilities are equal, and M_1 and M_2 are equally sized. The device M_1 is in the linear region if

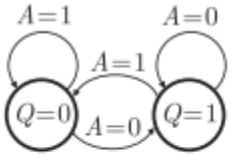


(A) **Vin < 1.875 V** (B) 1.875V<Vin< 3.125 V (C) Vin > 3.125 V (D) 0 < Vin<5V

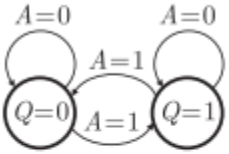
8. The state transition diagram for the logic circuit shown is



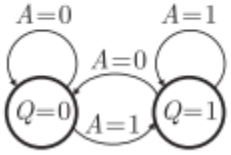
(A)



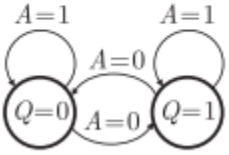
(B)



(C)

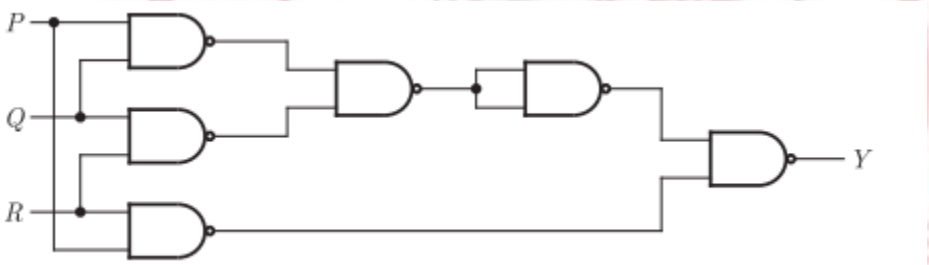


(B)



Ans: D

9. The output Y in the circuit below is always '1' when



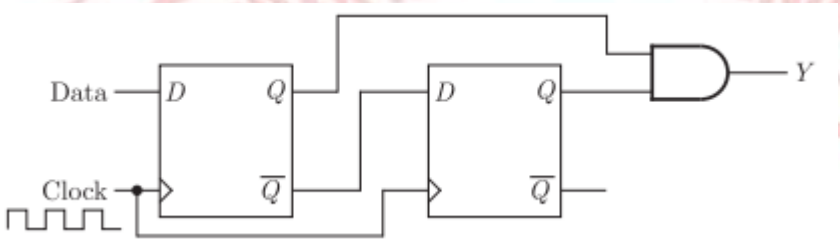
(A) Two or more of the inputs P Q, , R are '0'

(B) Two or more of the inputs P Q, , R are '1'

(C) Any odd number of the inputs P Q, , R is '0'

(D) Any odd number of the inputs P Q, , R is '1'

10. When the output Y in the circuit below is "1", it implies that data has



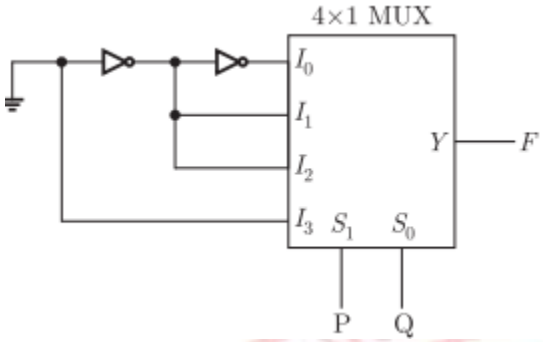
(A) Changed from "0" to "1"

(B) Changed from "1" to "0"

(C) Changed in either direction

(D) Not changed

11. The logic function implemented by the circuit below is (ground implies a logic “0”)



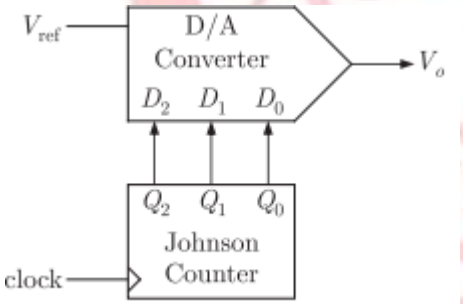
(A) F =AND (P, Q)

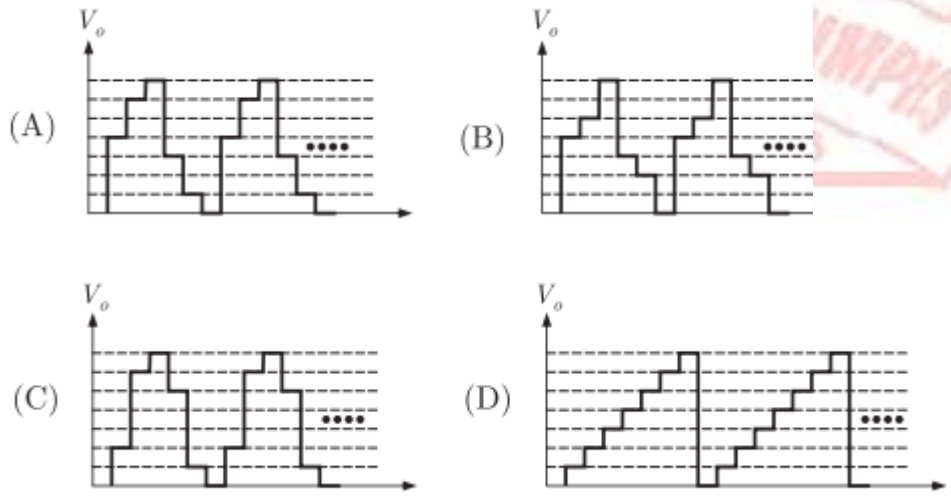
(B) F = OR (P, Q)

(C) F =XNOR (P, Q)

(D) F =XOR (P, Q)

12. The output of a 3-stage Johnson (twisted ring) counter is fed to a digital-to analog (D/A) converter as shown in the figure below. Assume all states of the counter to be unset initially. The waveform which represents the D/A converter output Vo is





Ans: A

13. Two D flip-flops are connected as a synchronous counter that goes through the following Q_B Q_A sequence00→11→01→10→ 00→….. The connections to the inputs D_A and D_B are

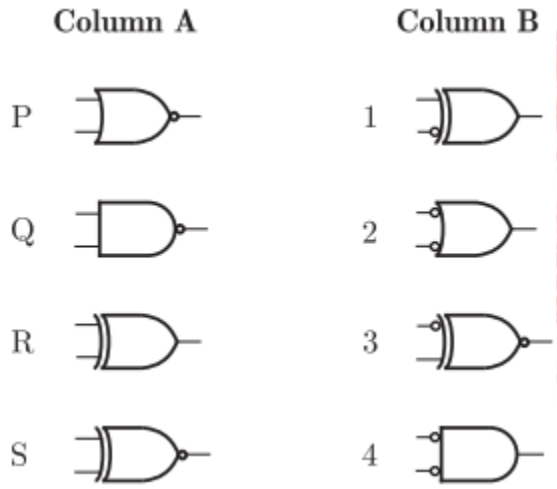
(A) $D_A = Q_B$, $D_B = Q_A$

(B)) $D_A = Q_A'$, $D_B = Q_B'$

(C)$D_A=(Q_A Q_B' + Q_A' Q_B)$,$D_B = Q_A$

(D) $D_A=(Q_A Q_B + Q_A' Q_B')$, $D_B = Q_B'$

14.Match the logic gates in Column A with their equivalents in Column B



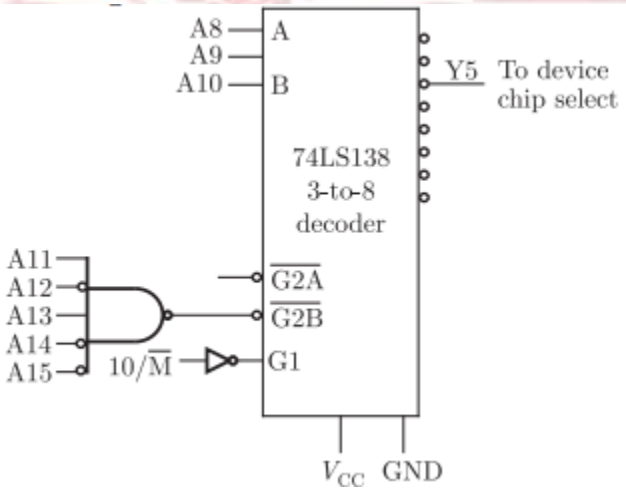
(A) P-2, Q-4, R-1, S-3

(B) P-4, Q-2, R-1, S-3

(C) P-2, Q-4, R-3, S-1

(D) P-4, Q-2, R-3, S-1

15. In the circuit shown, the device connected Y5 can have address in the range



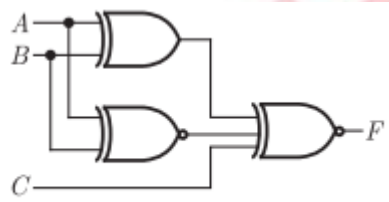
(A) 2000 - 20FF

(B) 2D00 - 2DFF

(C) 2E00 - 2EFF

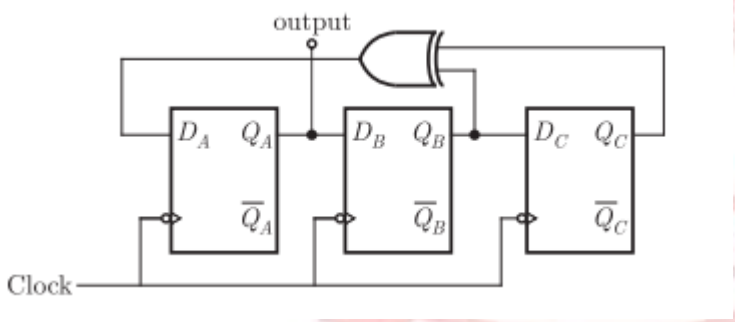
(D) FD00 – FDFF

16. For the output F to be 1 in the logic circuit shown, the input combination should be



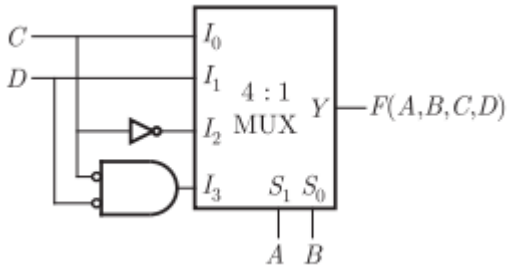
(A) **A =1,B =1, C=0 (B) A =1,B =0, C=0 (C)A =0,B =1, C=0** (D) A =0,B =0, C=1

17. Assuming that the flip-flop are in reset condition initially, the count sequence observed at QA, in the circuit shown is



(A) 0010111... (B) 0001011... (C) 0101111... **(D) 0110100....**

18. The Boolean function realized by the logic circuit shown is



(A) F=∑m (0,1, 3, 5, 9,10,14) (B) F =∑m (2 ,3 ,5 ,7 ,8 ,12 ,13) (C) F =∑m(1, 2, 4, 5, 11, 14, 15) **(D)F=∑m (2 ,3 ,5 ,7 ,8 ,9 ,12)**

19. The full form of the abbreviations TTL and CMOS in reference to logic families are

(A) Triple Transistor Logic and Chip Metal Oxide Semiconducto

(B) Tristate Transistor Logic and Chip Metal Oxide Semiconductor

(C) Transistor- Transistor Logic and Complementary Metal Oxide Semiconductor

(D) Tristate Transistor Logic and Complementary Metal Oxide

20. If X = 1in logic equation [X+Z{Y'+(Z'+XY')}] {X'+X'(X+Y)} =1 ,then

(A) Y= Z (B) Y =Z' (C) Z = 1 **(D) Z = 0**

21. What are the minimum number of 2- to -1 multiplexers required to generate a 2- input AND gate and a 2- input Ex-OR gate

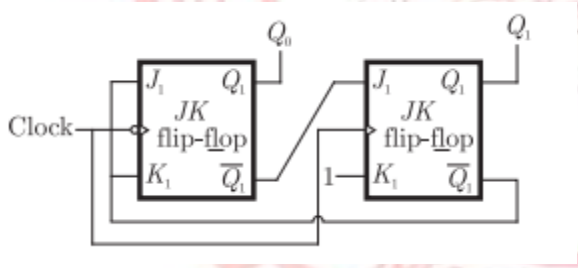
(A) 1 and 2

(B) 1 and 3

(C) 1 and 1

(D) 2 and 2

22. What are the counting states (Q_1 , Q_2)for the counter shown in the figure below



(A) 11, 10, 00 ,11, 10,...

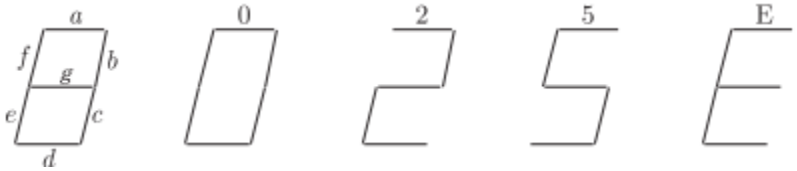
(B) 01, 10 ,11, 00, 01 ,…

(C) 00,11, 01, 10, 00,…

(D) 01,10, 00 ,01, 10,…

Statement for Linked Answer Question 23 &24 :

Two products are sold from a vending machine, which has two push buttons P1 and P2. When a buttons is pressed, the price of the corresponding product is displayed in a 7 - segment display. If no buttons are pressed, ' ' 0 is displayed signifying 'Rs 0'. If only P1 is pressed, '2' is displayed, signifying 'Rs. 2' If only P2 is pressed '5' is displayed, signifying 'Rs. 5' If both P1 and P2 are pressed, ' ' E is displayed, signifying 'Error' The names of the segments in the 7 - segment display, and the glow of the display for '0', '2', '5' and 'E' are shown below.



Consider

(1) Push buttons pressed/not pressed in equivalent to logic 1/0 respectively.

(2) A segment glowing/not glowing in the display is equivalent to logic 1/0 respectively.

23. If segments a to g are considered as functions of P1 and P2, then which of the following is correct

(A) g =P1'+P2 ,d=c+ e **(B) g =P1+P2 ,d=c+ e**(C) g =P1'+P2 ,d=b+c(D) g =P1+P2 ,d=b+c

24. What are the minimum numbers of NOT gates and 2 - input OR gates required to design the logic of the driver for this 7 - Segment display

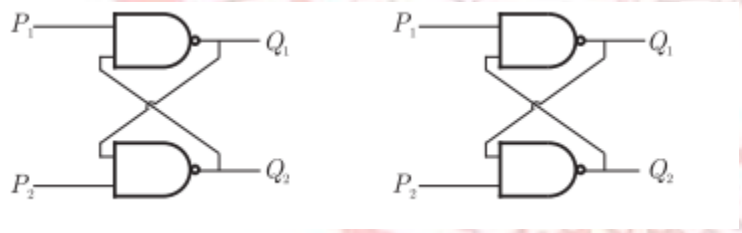
(A) 3 NOT and 4 OR

(B) 2 NOT and 4 OR

(C) 1 NOT and 3 OR

(D) 2 NOT and 3 OR

25. Refer to the NAND and NOR latches shown in the figure. The inputs (,) P P1 2 for both latches are first made (0, 1) and then, after a few seconds, made (1, 1). The corresponding stable outputs (,) Q Q1 2 are



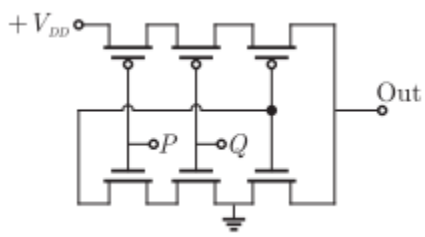
(A) NAND: first (0, 1) then (0, 1) NOR: first (1, 0) then (0, 0)

(B) NAND: first (1, 0) then (1, 0) NOR: first (1, 0) then (1, 0)

(C) NAND: first (1, 0) then (1, 0) NOR: first (1, 0) then (0, 0)

(D) NAND: first (1, 0) then (1, 1) NOR: first (0, 1) then (0, 1)

26. The logic function implemented by the following circuit at the terminal OUT is



(A) P NOR Q

(B) P NAND Q

(C) P OR Q

(D) P AND Q

27. The two numbers represented in signed 2's complement form are P = 11101101 and Q = 11100110. If Q is subtracted from P, the value obtained in signed 2's complement is

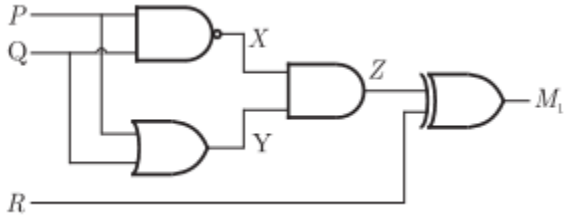
(A) 1000001111

(B) 00000111

(C) 11111001

(D) 111111001

28. Which of the following Boolean Expressions correctly represents therelation between ,, PQR and



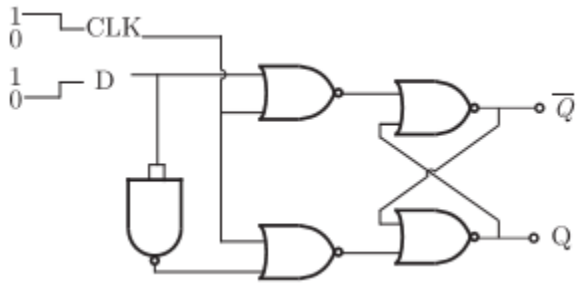
(A) M_1=(P OR Q) XOR R

(B) M_1=(P AND Q) XOR R

(C) M_1=(PNOR Q) XOR R

(D) M_1=(P XOR Q) XOR R

29. For the circuit shown in the figure, D has a transition from 0 to 1 after CLK changes from 1 to 0. Assume gate delays to be negligible Which of the following statements is true



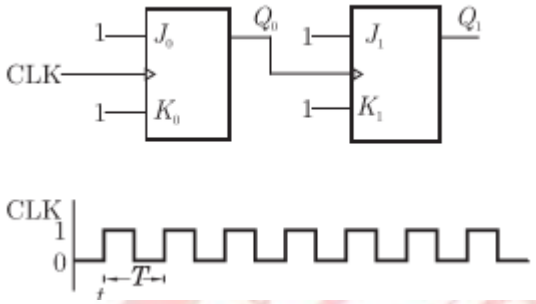
(A) Q goes to 1 at the CLK transition and stays at 1

(B) Q goes to 0 at the CLK transition and stays 0

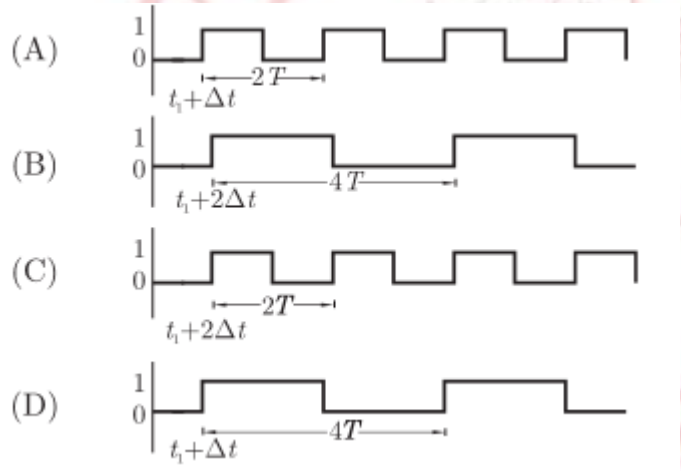
(C) Q goes to 1 at the CLK tradition and goes to 0 when D goes to 1

(D) Q goes to 0 at the CLK transition and goes to 1 when D goes to 1

30. For each of the positive edge-triggered JK - flip flop used in the following figure, the propagation delay is Æxt

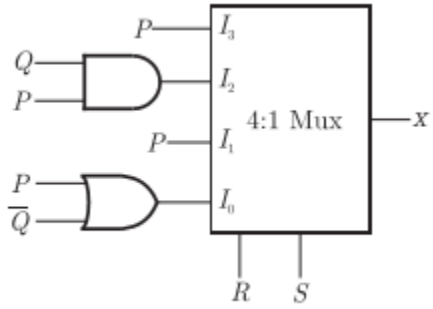


Which of the following wave forms correctly represents the output at Q1 ?



Ans: B

31.For the circuit shown in the following, II 03 - are inputs to the 4:1 multiplexers, R(MSB) and S are control bits. The output Z can be represented by



(A) PQ +PQ'S +(QRS)'

(B) PQ'+ PQR'+(PQS)'

(C) P(QR)'+ P'QR+ PARS+(QRS) '

(D) PQR'+PQRS'+P(QR)'S+(QRS)'

32. X =01110 and Y= 11001 are two 5-bit binary numbers represented in two's complement format. The sum of X and Y represented in two's complement format using 6 bits is

(A) 100111 (B) 0010000 **(C) 000111** (D) 101001

33. The Boolean function Y= AB+ CD is to be realized using only 2 - input NAND gates. The minimum number of gates required is

(A) 2 **(B) 3** (C) 4 (D) 5

34. The Boolean expression Y=(AB)'(CD)'+ A'BCD'+ A(BC)'D+ AB(CD)' can be minimized to

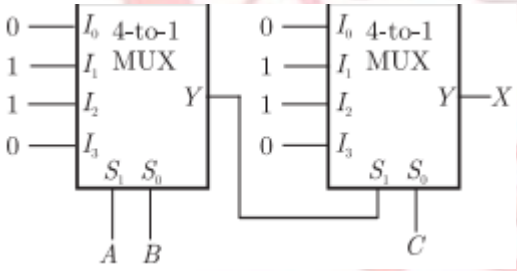
(A) Y=(AB)'C'D+ A'BC'+ AC'D

(B) Y=(ABC)'D +BCD '+AB'C'D

(C) Y =A'BCD'+(BC)'D+ A(BC)'D

(D) Y =A'BCD'+B'C'D+AB(CD)'

35. In the following circuit, X is given by



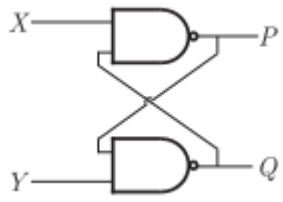
(A) X=A(BC)'+A'BC'+ A'B'C+ ABC

(B) X =A'BC+ AB'C+ ABC'+A'(BC)'

(C) X= AB +BC+ AC

(D) X =A'B'+ B'C'+ A'C'

36. The following binary values were applied to the X and Y inputs of NAND latch shown in the figure in the sequence indicated below : X=0,Y=1;X=0,Y=0; X=1, Y =1 The corresponding stable P,Q output will be.



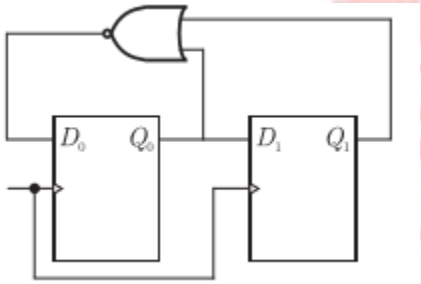
(A) P=1,Q=0; P=1, Q=0; P=1, Q=0 or P=0,Q=1

(B) P=1,Q=0; P=0, Q=1;or P=0, Q=1; P=0,Q=1

(C)) P=1,Q=0; P=1, Q=1;or P=1, Q=0;or P=0,Q=1

(D)P=1,Q=0; P=1, Q=1;P=1, Q=1.

37. For the circuit shown, the counter state (Q_1Q_0)follows the sequence



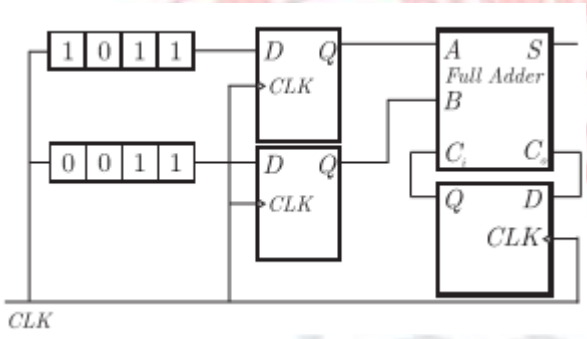
(A) **00, 01, 10, 11, 00** (B)00, 01 ,10, 00, 01 (C) 00, 01, 11, 00, 01 (D) 00,10,11,00,10

38. The number of product terms in the minimized sum-of-product expression obtained through the following K - map is (where, "d" denotes don't care states)

1	0	0	1
0	d	0	0
0	0	d	1
1	0	0	1

(A) **2** (B) 3 (C) 4 (D) 5

39. For the circuit shown in figures below, two 4 - bit parallel - in serial- out shift registers loaded with the data shown are used to feed the data to a full adder. Initially, all the flip - flops are in clear state. After applying two clock pulse, the output of the full-adder should be



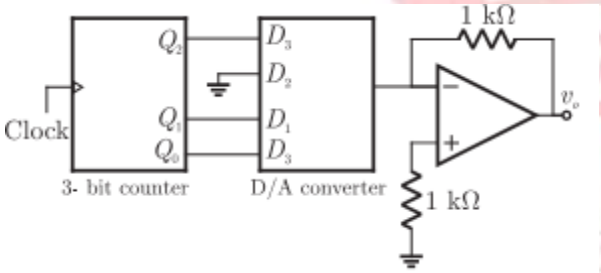
(A) S=0,C_0 =0 (B) S=0,C_0 =1 (C) S=1,C_0 =0 **(D) S=1,C_0 =1**

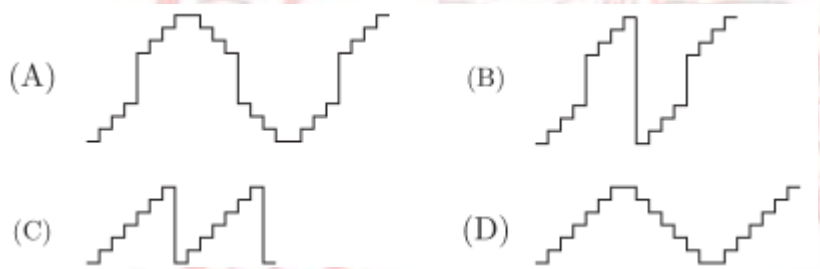
40. A new Binary Coded Pentary (BCP) number system is proposed in which every digit of a base-5 number is represented by its corresponding 3-bit binary code. For example, the base-5 number A new Binary Coded Pentary (BCP) number system is proposed in which every digit of a base-5 number is represented by its corresponding 3-bit binary code. For example, the base-5 number24 will be

represented by its BCP code 010100. In this numbering system, the BCP code 10001001101 corresponds of the following number is base-5 system

(A) 423 (B) 1324 (C) 2201 **(D) 4231**

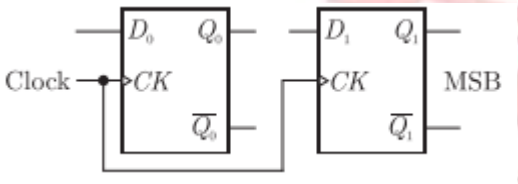
41. A 4 - bit D/A converter is connected to a free - running 3 - big UP counter, as shown in the following figure. Which of the following waveforms will be observed at V_0 ?





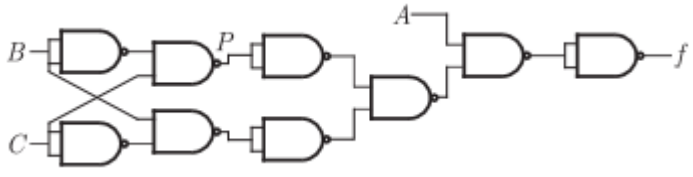
Ans: **B**

42. Two D - flip - flops, as shown below, are to be connected as a synchronous counter that goes through the following sequence 00 →01 →11 →10 →00.The inputs D_0 and D_1 respectively should be connected as,



(A)Q_1'and Q_0 (B) Q_0'and Q_1 (C) Q_1 'Q_0 andQ_1 'Q_0(D)Q_1 'Q_0'andQ_1 Q_0

43. The point P in the following figure is stuck at 1. The output f will be

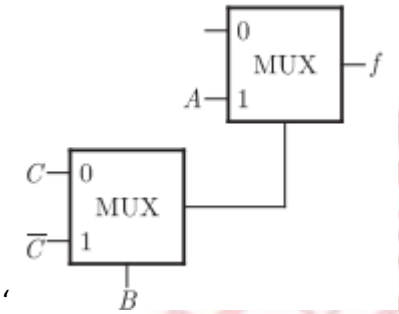


(A) ABC '(B) A' (C) ABC '**(D)A**

44. Decimal 43 in Hexadecimal and BCD number system is respectively

(A) B2, 0100 011 **(B) 2B, 0100 0011** (C) 2B, 0011 0100 (D) B2, 0100 0100

45. The Boolean function f implemented in the figure using two input multiplexes is



‘

(A) ABC’+ ABC’

(B) ABC +A(BC)’

(C) A’BC+(ABC)’

(D)(AB)’C+A’BC’

46. The Boolean expression for the truth table shown is

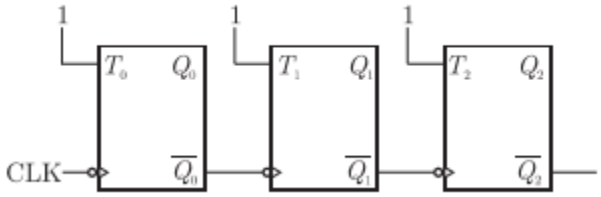
A	B	C	D
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	0

(A) **B(A+C)(A’+C’)** (B) B(A+C’)(A’+C) (C)B’(A+C’)(A’+C) (D) B’(A+C)(A’+C’)

47. The present output Q_n of an edge triggered JK flip-flop is logic 0. If J =1 , then Q_{n+1}

(A) Cannot be determined (B) Will be logic 0 **(C) Will be logic 1** (D) Will rave around

48. The given figure shows a ripple counter using positive edge triggered flip-flops. If the present state of the counter is $Q_2Q_1Q_0$ =001 then is next state $Q_2Q_1Q_0$ will be



(A) 010 (B) 111 **(C) 100** (D) 101

49. A master - slave flip flop has the characteristic that

(A) Change in the output immediately reflected in the output

(B) Change in the output occurs when the state of the master is affected

(C) Change in the output occurs when the state of the slave is affected

(D) Both the master and the slave states are affected at the same time

50. The range of signed decimal numbers that can be represented by 6-bits 1's complement number is **(A) -31 to +31** (B) -63 to +63 (C) -64 to +63 (D) -32 to +31

51. A digital system is required to amplify a binary-encoded audio signal. The user should be able to control the gain of the amplifier from minimum to a maximum in 100 increments. The minimum number of bits required to encode, in straight binary, is

(A) 8 (B) 6(C) 5 **(D) 7**

52. Choose the correct one from among the alternatives A,B,C,D after matching an item from Group 1 most appropriate item in Group 2.

Group 1	Group 2
P. Shift register	1. Frequency division
Q. Counter	2. Addressing in memory chips
R. Decoder	3. Serial to parallel data conversion

(A) P-3,Q-2,R-1 **(B) P-3,Q-1,R -2**(C) P-2,Q-1,R-3 (D) P-1,Q-2,R-2

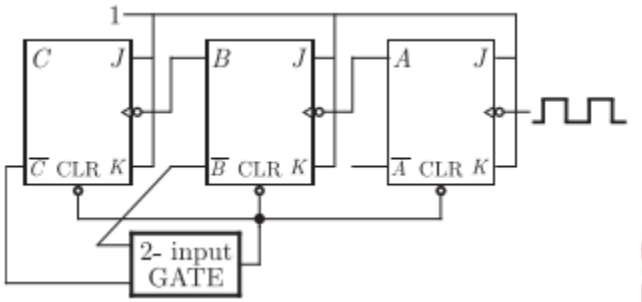
53. The figure the internal schematic of a TTL AND-OR-OR-Invert (AOI) gate. For the inputs shown in the figure, the output Y is

(A) **0** (B) 1 (C) AB (D)(AB)'

54. 11001, 1001, 111001 correspond to the 2's complement representation of which one of the following sets of number

(A) 25,9, and 57 respectively (B) -6, -6, and -6 respectively (C) **-7, -7 and -7 respectively** (D) -25, -9 and -57 respectively

55. In the modulo-6 ripple counter shown in figure, the output of the 2- input gate is used to clear the J-K flip-flop The 2-input gate is



(A) a NAND gate (B) a NOR gate **(C) an OR gate** (D) a AND gate

56. The minimum number of 2- to -1 multiplexers required to realize a 4- to -1 multiplexers is

(A) 1 (B) 2 **(C) 3** (D) 4

57. The Boolean expression AC+BC' is equivalent to

(A) A'C +BC'+ AC (B) B'C+ AC+ BC'+ A'CB' (C) AC +BC'+ B'C+ ABC **(D) ABC +A'BC'+ ABC'+ AB'C**

58. A Boolean function f of two variables x and y is defined as follows :f (0 ,0)=f (0 ,1)=f (1 ,1)=f (1 ,0)=0 Assuming complements of x and y are not available, a minimum cost solution for realizing f using only 2-input NOR gates and 2- input OR gates (each having unit cost) would have a total cost of

(A) 1 unit (B) 4 unit (C) 3 unit **(D) 2 unit**

59. The number of distinct Boolean expressions of 4 variables is

(A) 16 (B) 256 **(C) 1023** (D) 65536

60. Without any additional circuitry, an 8:1 MUX can be used to obtain

(A) Some but not all Boolean functions of 3 variables

(B) All functions of 3 variables but non of 4 variables

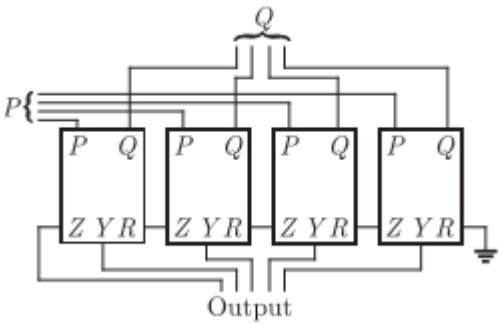
(C) All functions of 3 variables and some but not all of 4 variables

(D) All functions of 4 variables

61. A 0 to 6 counter consists of 3 flip flops and a combination circuit of 2 input gate (s). The common circuit consists of

(A) One AND gate (B) One OR gate (C) One AND gate and one OR gate **(D) Two AND gates**

62. The circuit in the figure has 4 boxes each described by inputs P,Q,R and outputs Y,Z with Y=P XOR Q XOR R and Z= RQ+ P'R+ QP'. The circuit acts as a



(A) 4 bit adder giving P+Q

(B) 4 bit Subtractor giving P-Q

(C) 4 bit Subtractor giving Q-P

(D) 4 bit adder giving P+Q+R

63.If the function W,X,Y and Z are as follows W =R+ P'Q +R'S ;X= PQ(RS)'+(PQRS)'+ P(QRS)' ; Y= RS+(PR+ PQ'+ P' Q')' ; Z= R+ S+ (PQ+ P 'Q 'R '+PQ' S')' .Then,

(A) W= Z ,X= Z' (B) W =Z ,X= Y (C) W= Y (D) W=Y=Z'

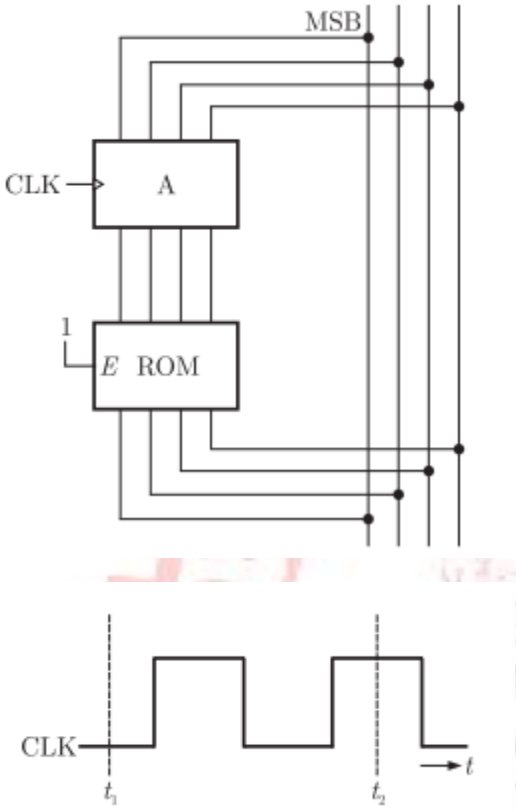
64. A 4 bit ripple counter and a bit synchronous counter are made using flip flops having a propagation delay of 10 ns each. If the worst case delay in the ripple counter and the synchronous counter be R and S respectively, then

(A) R = 10 ns, S = 40 ns **(B) R = 40 ns, S = 10 ns** (C) R = 10 ns ,S = 30 ns (D) R = 30 ns, S = 10 ns

65. In the circuit shown in the figure, A is parallel-in, parallel-out 4 bit register, which loads at the rising edge of the clock C. The input lines are connected to a 4 bit bus, W . Its output acts at input to a 16* 4 ROM whose output is floating when the input to a partial table of the contents of the ROM is as follows

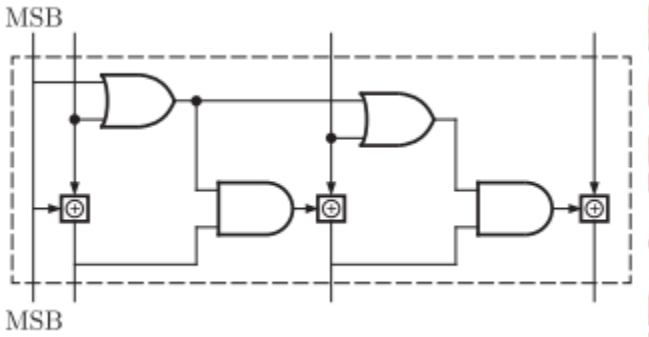
Data	0011	1111	0100	1010	1011	1000	0010	1000
Address	0	2	4	6	8	10	11	14

The clock to the register is shown, and the data on the W bus at time t_1 is 0110. The data on the bus at time t_2 is



(A) 1111 (B) 1011 **(C) 1000** (D) 0010

66.The circuit shown in figure converts



(A) BCD to binary code

(B) Binary to excess - 3 code

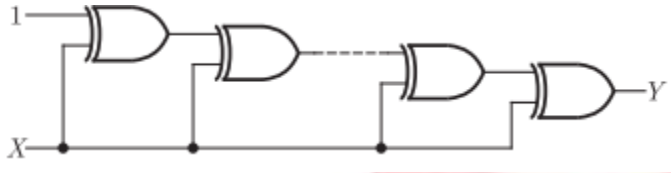
(C) Excess -3 to gray code

(D) Gray to Binary code

67.4 - bit 2's complement representation of a decimal number is 1000. The number is

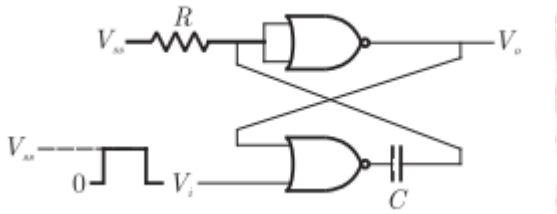
(A) +8 (B) 0 (C) -7 **(D) -8**

68. If the input to the digital circuit (in the figure) consisting of a cascade of 20 XOR - gates is X , then the output Y is equal to



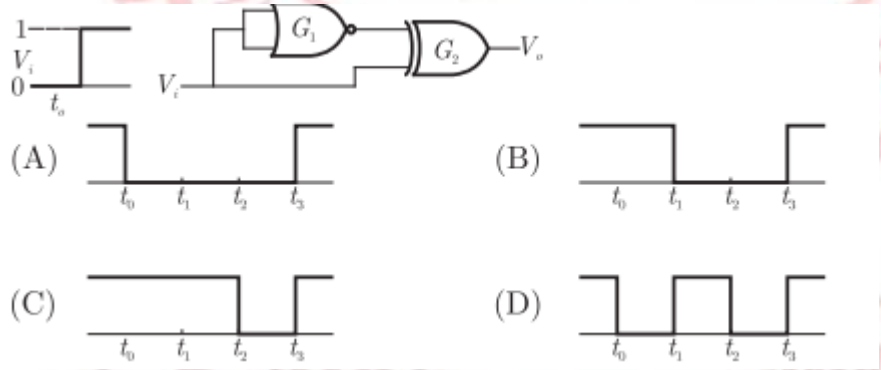
(A) 0 **(B) 1** (C) X' (D) X

69. The circuit in the figure has two CMOS NOR gates. This circuit functions as a:



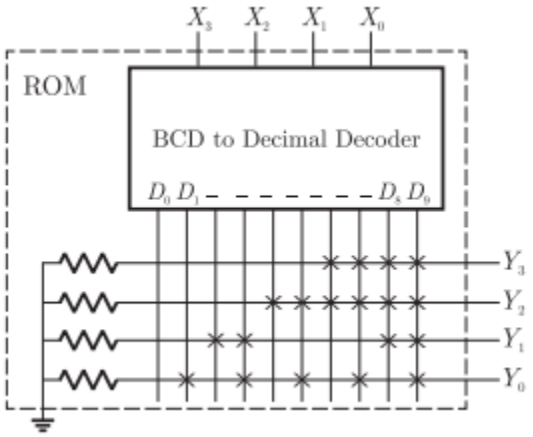
(A) flip-flop (B) Schmitt trigger **(C) Monostable multivibrator** (D) Astable multivibrator

70. The gates G_1 and G_2 in the figure have propagation delays of 10 ns and 20 ns respectively. If the input V_1, makes an output change from logic 0 to 1 at time $t = t_0$, then the output waveform V_0 is



Ans: B

71. If the input X_3,X_2, X_1 ,X_0 to the ROM in the figure are 8 4 2 1 BCD numbers, then the outputs Y_3 ,Y_2 Y_1 Y_0 are

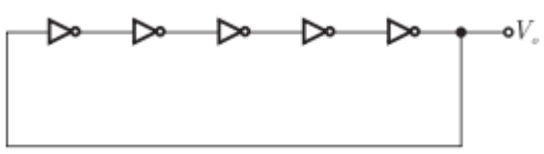


(A) Gray code numbers **(B) 2 4 2 1 BCD numbers** (C) Excess - 3 code numbers (D) None of the above

72. The 2's complement representation of -17 is

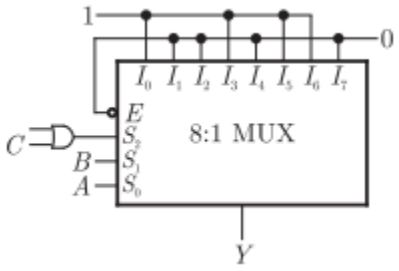
(A) 101110 **(B) 101111** (C) 111110 (D) 110001

73. For the ring oscillator shown in the figure, the propagation delay of each inverter is 100 pico sec. What is the fundamental frequency of the oscillator output



(A) 10 MHz (B) 100 MHz **(C) 1 GHz** (D) 2 GHz

74. In the TTL circuit in the figure, S_2 and S_0 are select lines and X_7 and X_0 are input lines. S_0 and X_0 are LSBs. The output Y is



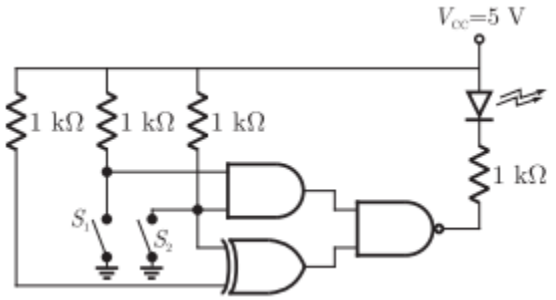
(A) indeterminate

(B) A EX-OR B

(C) (A EX-OR B)'

(D) C'(A EX-OR B)'+C(A EX-OR B)

75. In the figure, the LED



(A) Emits light when both S_1 and S_2 are closed

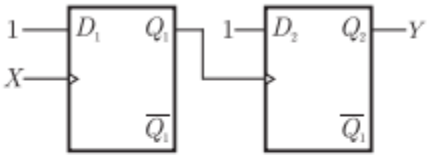
(B) Emits light when both S_1 and S_2 are open

(C) Emits light when only of S_1 and S_2 is closed

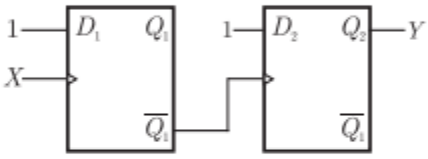
(D) Does not emit light, irrespective of the switch positions.

76. The digital block in the figure is realized using two positive edge triggered D-flip-flop. Assume that for t t<t_0 ,Q_1 =Q $_2$= 0. The circuit in the digital block is given by

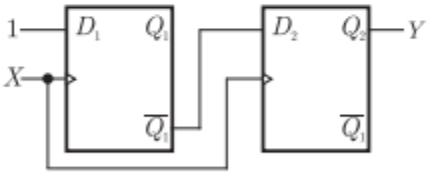
(A)



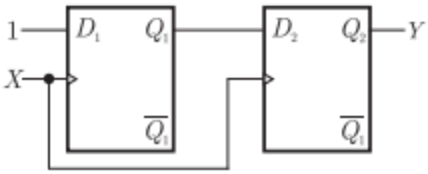
(B)



(C)

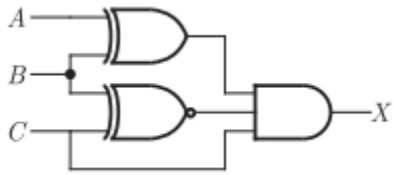


(D)



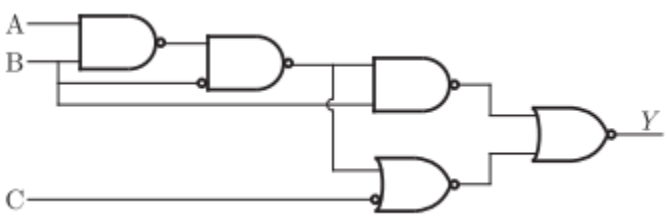
Ans: C

77.For the logic circuit shown in the figure, the required input condition (A,B,C) to make the output (X) = 1 is



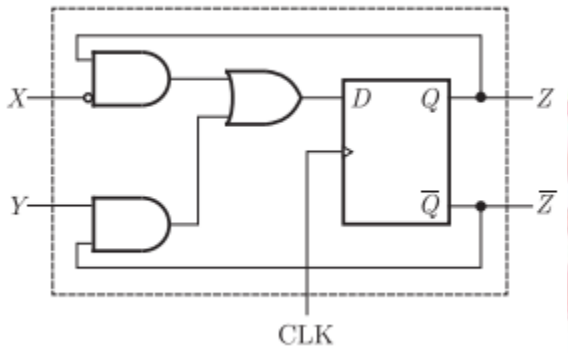
(A) 1,0,1 (B) 0,0,1 (C) 1,1,1 **(D) 0,1,1**

78. For the logic circuit shown in the figure, the simplified Boolean expression for the output Y is



(A) A+B+C (B) A **(C) B** (D) C

79. A sequential circuit using D flip-flop and logic gates is shown in the figure, where X and Y are the inputs and Z is the inputs. The circuit is



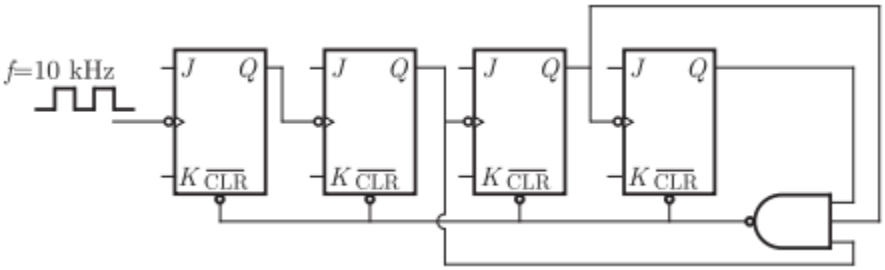
(A) S R - Flip-Flop with inputs X= R and Y= S

(B) S R - Flip-Flop with inputs X= S and Y= R

(C) J K - Flip-Flop with inputs X= J and Y= K

(D) J K - Flip-Flop with input X= K and Y= J

80. In the figure, the J and K inputs of all the four Flip-Flips are made high. The frequency of the signal at output Y is



(A) 0.833 kHz **(B) 1.0 kHz** (C) 0.91 kHz (D) 0.77 kHz

81. The logical expression y =A+ A'B is equivalent to

(A) y =AB (B) y= A'B (C) y= A'+B **(D) y =A+B**

82. The minimized form of the logical expression ('AB'C '+A'B C'+ A'BC+ ABC') is

(A) A'C'+ BC'+ A'B (B) AC'+ B'C+ A'B (C) A'C+ B'C+ A'B (D) AC'+ B'C+ AB'

83.For a binary half-Subtractor having two inputs A and B, the correct set of logical expressions for the outputs D(= A minus B) and X(= borrow) are

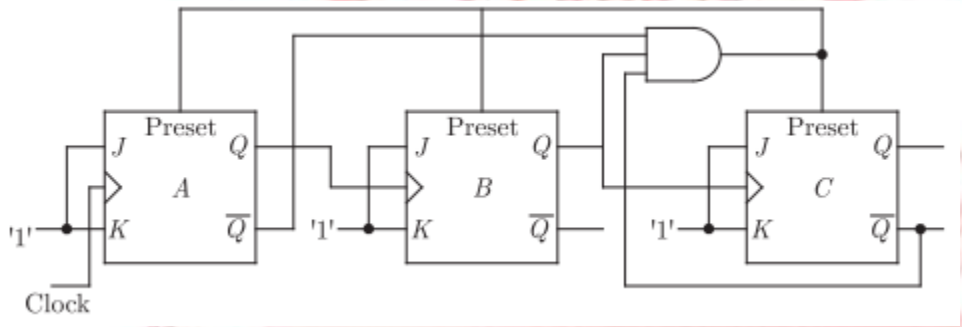
(A) D =A B +A'B ,X=A'B

(B)) D =A' B +AB '+AB',X=AB'

(C) D=A' B+ AB', X=A'B ,

(D) D =A B+ A'B', X= AB'

84. The ripple counter shown in the given figure is works as a

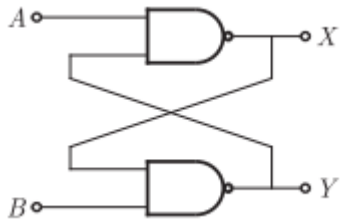


(A) mod-3 up counter (B) mod-5 up counter (C) mod-3 down counter **(D) mod-5 down counter**

85. The minimum number of 2-input NAND gates required to implement of Boolean function Z=AB'C , assuming that A, B and C are available, is

(A) Two (B) Three **(C) Five** (D) Six

86. In the figure is A = 1 and B = 1, the input B is now replaced by a sequence 101010....., the output x and y will be



(A) Fixed at 0 and 1, respectively

(B) x= 1010..... while Y=0101.....

(C) x= 1010.....and Y=1010.....

(D) Fixed at 1 and 0, respectively

87. An equivalent 2's complement representation of the 2's complement number 1101 is

(A) 110100 (B) 01101 (C) 110111 **(D) 111101**

88. Two 2's complement number having sign bits x and y are added and the sign bit of the result is z . Then, the occurrence of overflow is indicated by the Boolean function

(A) xyz (B) x'y'z' (C) x' y'z+ xyz' **(D) xy+ yz+ zx**

89. For the identity AB+ A'C+ BC= AB +A'C , the dual form is

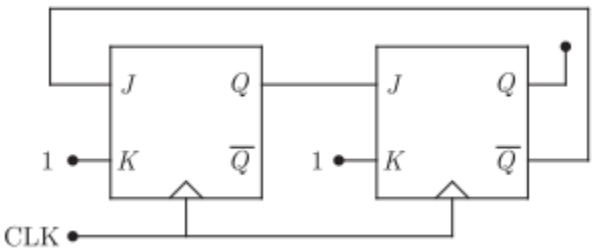
(A) (A+B)(A'+C)(B+C)=(A+B)(A'+C)

(B) (A'+B')(A+C')(B'+C'))=(A'+B')(A+C')

(C) (A+B)(A'+C)(B+C)=(A'+B')(A+C')

(D) A'B'+AC'+B'C'=A'B'+AC'

90. The figure is shows a mod-K counter, here K is equal to



(A) 1 (B) 2 **(C) 3** (D) 4

91. The K -map for a Boolean function is shown in the figure is the number of essential prime implicates for this function is

CD \ AB	00	01	11	10
00	1	1		1
01				1
11	1			
10	1			1

(A) **4** (B) 5 (C) 6 (D) 8

92. A 2 bit binary multiplier can be implemented using

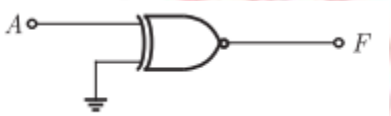
(A) 2 inputs ANSs only

(B) 2 input XORs and 4 input AND gates only

(C) Two 2 inputs NORs and one XNO gate

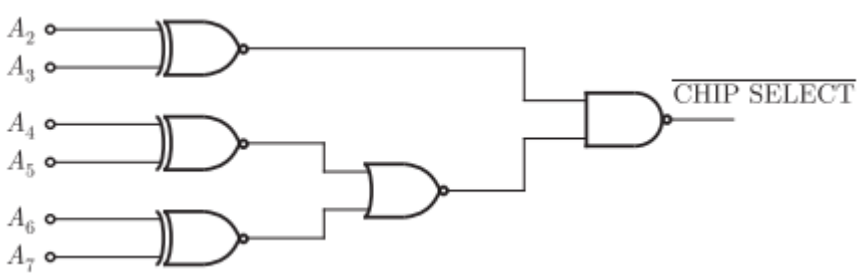
(D) XOR gates and shift registers

93. The output of the logic gate in the figure is



(A) **0** (B) 1 (C) A (D) F

94. The decoding circuit shown in the figure is has been used to generate the active low chip select signal for a microprocessor peripheral. (The address lines are designated as AO to A7 for I O/ address)



The peripheral will correspond to I O/ address in the range

(A) 60 H to 63 H

(B) A4 to A 7H

(C) 30 H to 33 H

(D) 70 H to 73 H

95. A signed integer has been stored in a byte using the 2's complement format. We wish to store the same integer in a 16 bit word. We should

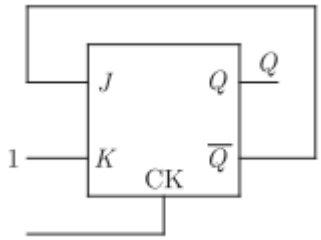
(A) Copy the original byte to the less significant byte of the word and fill the more significant with zeros

(B) Copy the original byte to the more significant byte of the word and fill the less significant byte with zeros

(C) Copy the original byte to the less significant byte of the word and make each fit of the more significant byte equal to the most significant bit of the original byte

(D) Copy the original byte to the less significant byte as well as the more significant byte of the word

96. In a J–K flip-flop we have J Q = and K = 1. Assuming the flip flop was initially cleared and then clocked for 6 pulses, the sequence at the Q output will be



(A) 010000 (B) 011001 (C) 010010 **(D) 010101**

97. The Boolean function A+BC is a reduced form of

(A) AB +BC

(B) (A+ B)(A+ C)

(C) A'B+ AB'C

(D) (A+ C) B

98. A pulse train can be delayed by a finite number of clock periods using

(A) A serial-in serial-out shift register

(B) A serial-in parallel-out shift register

(C) A parallel-in serial-out shift register

(D) A parallel-in parallel-out shift register

99. For an n-variable Boolean function, the maximum number of prime implicants is

(A) 2(n-1) (B) n/2 (C) 2^n (D) $2^{(n-1)}$

Answer: (D)

100. The number of bytes required to represent the decimal number 1856357 in packed BCD (Binary Coded Decimal) form is _____ .

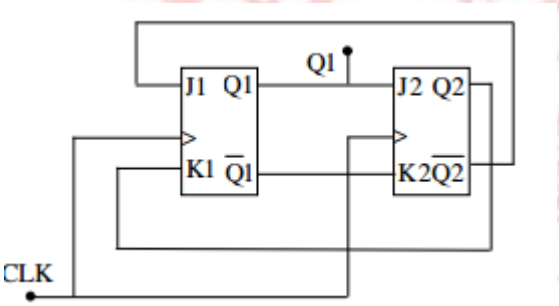
Answer: 4

101. In a half-Subtractor circuit with X and Y as inputs, the Borrow (M) and Difference (N = X - Y) are given by

(A) M= X XOR Y,N=XY (B) M= XY ,N=X XOR Y (C) M= X'Y ,N=X XOR Y (D) M= XY ,N=X XNOR Y

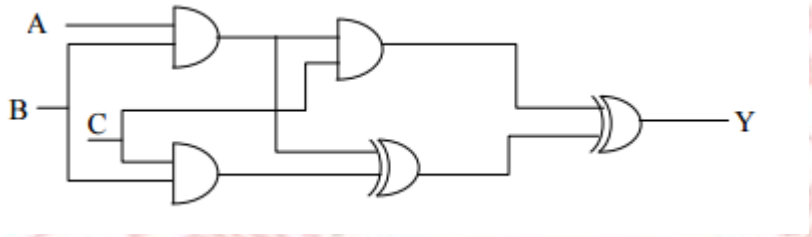
Answer: (C)

102. The outputs of the two flip-flops Q1, Q2 in the figure shown are initialized to 0,0. The sequence generated at Q1 upon application of clock signal is



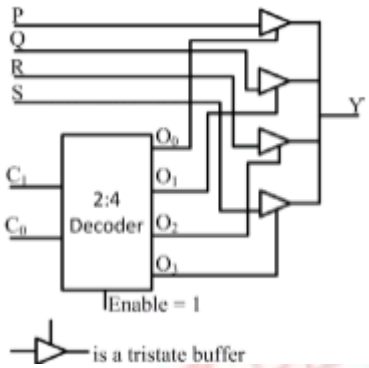
(A) 01110… (B) 01010… (C) 00110… (D) 01100…

103. The output of the combinational circuit given below is



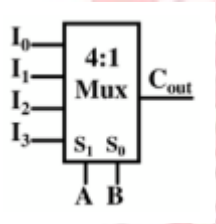
(A) A+B+C (B) A(B+C) (C) B(C+A) (D) C(A+B)

104. The functionality implemented by the circuit below is



(A) 2-to-1 multiplexer (B) 4-to-1 multiplexer (C) 7-to-1 multiplexer (D) 6-to-1 multiplexer

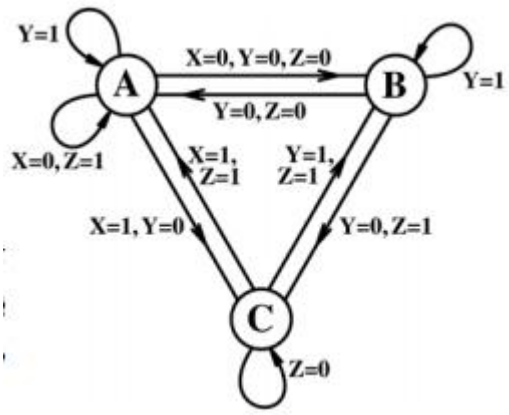
105. A 4:1 multiplexer is to be used for generating the output carry of a full adder. A and B are the bits to be added while Cin is the input carry and Cout is the output carry. A and B are to be used as the select bits with A being the more significant select bit.



106. Which one of the following statements correctly describes the choice of signals to be connected to the inputs I_0, I_1, I_2 and I_3 so that the output is C_{out}?

(A) I_0,=0 ,I_1 =C_{in}, I_2 = C_{in} and I_3=1
(B) I_0,=1 ,I_1 =C_{in}, I_2 = C_{in} and I_3=1
(C) I_0,=C_{in} ,I_1 =0, I_2 = 1and I_3= C_{in}
(D) I_0,=0,I_1 =, C_{in} ,I_2 = 1and I_3= C_{in}

107. The state transition diagram for a finite state machine with states A, B and C, and binary inputs X,Y and Z, is shown in the figure.



Which one of the following statements is correct?

(A) Transitions from State A are ambiguously defined

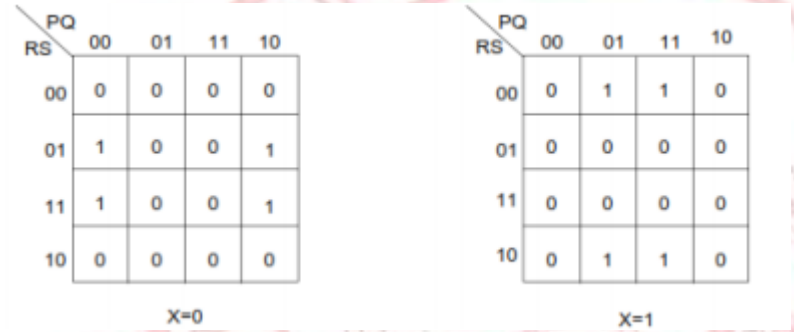
(B) Transitions from State B are ambiguously defined.

(C) Transitions from State Care ambiguously defined.

(D) All of the state transitions are defined unambiguously

Ans: C

108. Following is the K-map of a Boolean function of five variables P, Q, R, S and X. The minimum sumof-product (SOP) expression for the function is



RS \ PQ	00	01	11	10
00	0	0	0	0
01	1	0	0	1
11	1	0	0	1
10	0	0	0	0

X=0

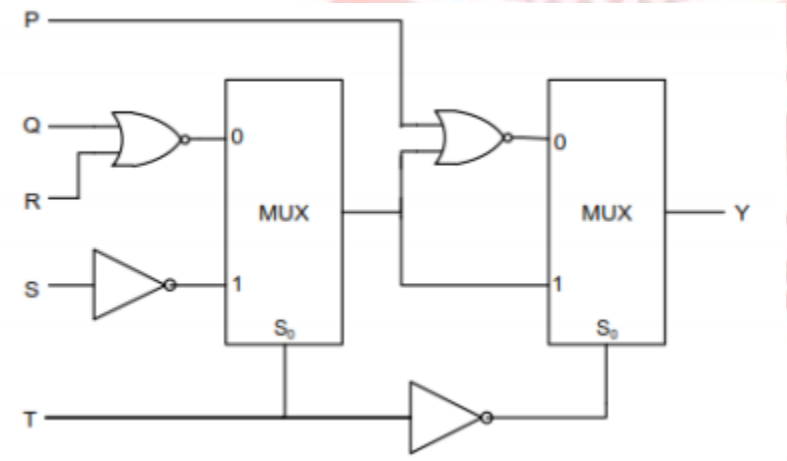
RS \ PQ	00	01	11	10
00	0	1	1	0
01	0	0	0	0
11	0	0	0	0
10	0	1	1	0

X=1

(A) P' Q'SX'+ P Q'SX'+ Q R 'S'X+ QRS'X (B) Q'SX'+ QS'X (C) Q'SX+ QS'X' (D) Q'S +QS'

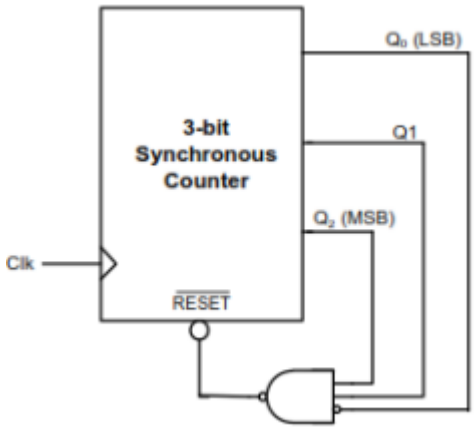
Key: (B)

109. For the circuit shown in the figure, the delays of NOR gates, multiplexers and inverters are 2 ns, 1.5 ns and 1 ns, respectively. If all the inputs P, Q, R, S and T are applied at the same time instant, the maximum propagation delay (in ns) of the circuit is _____.



Key: (6)

110. For the circuit shown in the figure, the delay of the bubbled NAND gate is 2 ns and that of the counter is assumed to be zero. If the clock (Clk) frequency is 1 GHz, then the counter behaves as a



(A) mod-5 counter (B) mod-6 counter (C) mod-7 counter (D) mod-8 counter

Key: (D)

111. Write the counting sequence of a 4 bit down synchronous counter. Design the same using negative edge triggered J–K Flip-Flops.

112. Perform the following operations on the given binary numbers as specified.
(a) 110.01 + 1.011
(b) Convert 11101.01 to decimal
(c) 11100.101 – 101.01 using 2's complement
(d) Convert 111000 to octal

113. State whether the following statement is True or False:
"All decimal fractions have exact binary equivalents."

114. Obtain the minimal SOP expression for Y(A, B, C, D) = Σm (2, 3, 5, 7, 8, 9,11, 12, 13, 14, 15) + d(2, 4) using K-map. Realize the expression using 2 input NAND gates only.

115. Design a mod-7 asynchronous up counter using JK flip-flops. Write the state diagram and the timing diagram for the same. The counter counts during positive edges of the clock.

105. Convert the following:
(i) Decimal number into octal $(5621.125)_{10}$
(ii) Hexadecimal number into octal and into binary $(5621)_{16}$.

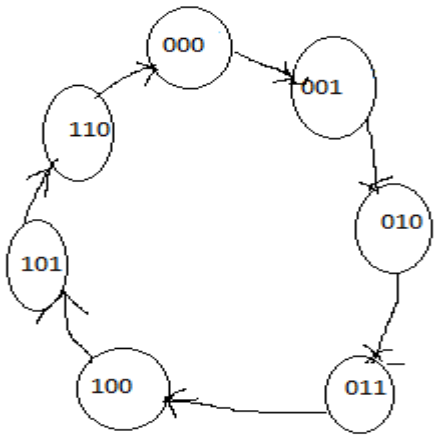
116. Write the counting sequence of a 4 bit down synchronous counter. Design the same using negative edge triggered J–K Flip-Flops.

117. Implement the following expressions using CMOS-AOI logic circuits. Verify the circuit operation with the help of truth table:
(i) $Y = A + BC$
(ii) $Y = (AB + CD)'$

118. Implement the function $f(A, B, C, D) = \Sigma(0, 1, 5, 7, 10, 14, 15)$ Using an appropriate multiplexer.

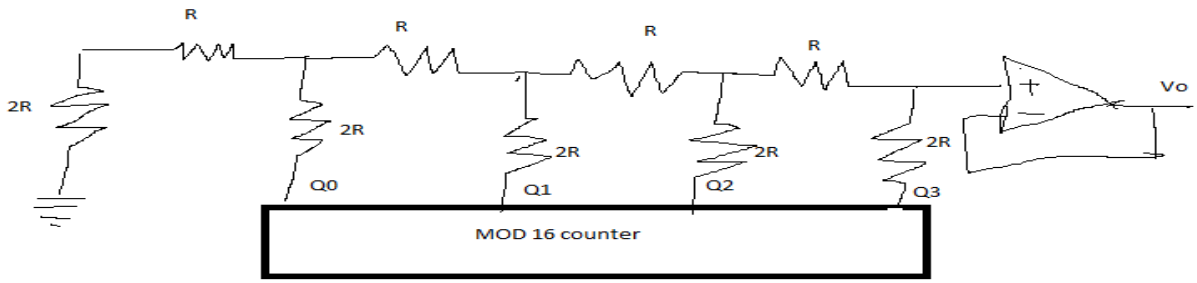
119. Design a combinational circuit that accepts a 3-bit number as input and generates an output binary number equal to square of the input number.

120. The state transition diagram of a synchronous counter is given below.Design the counter circuit using J – K flip-flops. Use the state table for the design.



121. Implement the following functions using static CMOS circuit:
i Y =A. B
ii Y= A+ B
iii Y= A XOR B
iv Y A XNOR B

122. For the given circuit shown below, the decimal inputs are given from a mod16 counter. Calculate the equivalent analog voltages when the counter outputs are 0011, 0111, 1011 and 1110. Also calculate the counter outputs when the analog voltages are 1.25V, 2.5 V, 3.75 V and 4.06 V. Assume that binary '1' =5V and '0' =0 V.



123. Assertion (A) : Asynchronous sequential circuits are difficult to design. Reason (R) : External clock is used for synchronization of asynchronous sequential circuits.
a. Both A and R are individually true and R is the correct explanation of A
b. Both A and R are individually true but R is not the correct explanation of A
c. A is true but R is false
d. A is false but R is true

124. Assertion (A) : The switching speed of ECL gate is very high. Reason

(R) : The devices in ECL gate operate in active region.

a. Both A and R are individually true and R is the correct explanation of A

b. Both A and R are individually true but R is not the correct explanation of A

c. A is true but R is false

d. A is false but R is true 1

125. The number of unused states in a 4-bit Johnson counter is

a. 2 b. 4 c. 8 d. 12

126. The characteristic equation for the next state (Qn+1) of a J-K flip-flop is

a. $Q_{n+1} = JQ_n + KQ_n$ '

b. $Q_{n+1} = J'Q_n$ '+ $K'Q_n$ '

c. $Q_{n+1} = JQ_n$ ' + $K'Q_n$ '

d. $Q_{n+1} = JQ_n + KQ_n$

127. Match List I (Digital Circuit) with List II (Circuit Type) and select the correct answer :

List I A. BCD to 7-segment Decoder B. 4- to -1 Multiplexer C. 4-bit Shift Register D. BCD Counter

List II 1. Sequential circuit 2. Combinational circuit 3. Neither sequential nor combinational circuit

	A	B	C	D
a.	2	1	2	1
b.	3	2	1	3
c.	2	2	1	1
d.	3	1	2	3

128. The output of a Moore sequential machine is a function of

a. All present states of the machine

b. All the inputs

c. A few combination of inputs and the, present state

d. All the combinations of inputs and the present state

128. Minimum number of J-K flip-flops needed to construct a BCD counter is

a. 2 b. 3 c. 4 d. 5

129. The minimum number of NAND gates required to implement the Boolean junction A + AB'+ AB'C is equal to

a. zero b. 1 c. 4 d. 7

130. The addition of two binary variables A and B results into a SUM and a CARRY output. Consider the following expressions for the SUM and CARRY outputs :

1. SUM = A . B + A '. B '

2. SUM = A. B'+ A'B

3. CARRY = A . B

4. CARRY = A + B

Which of these expressions are correct?

a. 1 and 3 b. 2 and 3 c. 2 and 4 d. 1 and 4

131. The Boolean expression (A'+B)(A+C')(B'+C')

a. (A+B)C' b . (A+B')C' c. (A'+B)C' d. (A'+B')C'