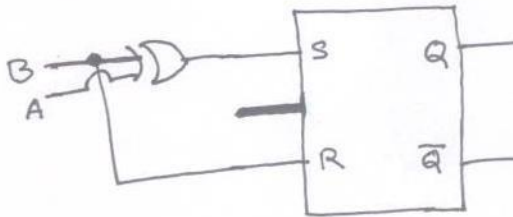


JAYPEE INSTITUTE OF INFORMATION TECHNOLOGY, NOIDA
Electronics and Communication Engineering
B.Tech 2nd Year
Digital System(18B11EC213) Even Sem
Tutorial-3

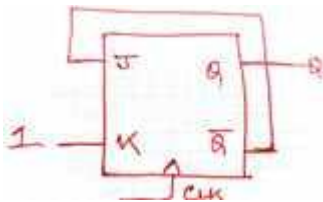
Q1. An AB Latch is constructed from an SR Latch as shown below

(i) Obtain the Expression for the next state $Q(t+1)$.

(ii) Find excitation table for the AB latch.

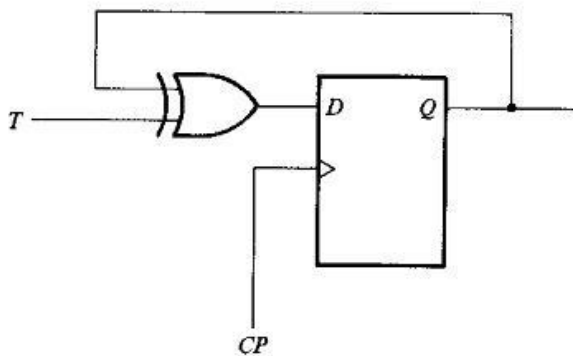


Q2. Consider the following J-K flip flop.

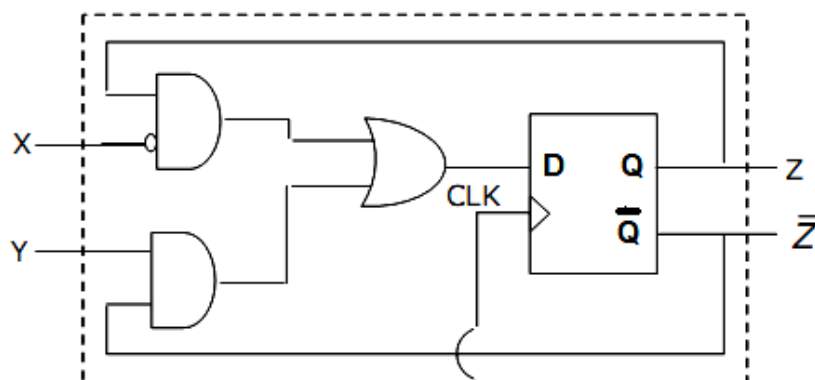


In the above J-K flip flop, $J=Q'$ and $K=1$. Assume that the flip flop was initially cleared and then clocked for 6 pulses. What is the sequence at the Q output?

Q3. Analyze the circuit of Fig. and prove that it is equivalent to a T flip-flop.



Q4. Show that following sequential circuit will work as a J K flip flop with input $X=K$ and $Y=J$.



Q5. A new clocked X-Y flip flop is define with two inputs, X and Y is in addition to the clock input. The flip flop functions as follows:
 If $XY = 00$, the flip flop changes state with clock pulse.
 If $XY = 01$, the flip flop state Q become '1' with the clock pulse
 If $XY = 10$, the flip flop state Q become '0' with the clock pulse
 If $XY = 11$, the change of state occurs with the clock pulse
 a) Write down truth table and excitation table for the XY flip flop.
 b) Implement X-Y flip flop using J-K flip flop.

Q6. The characteristic table of a new flip flop AB is given below.

a. Find the Excitation table

b. Realize it using T flip flop.

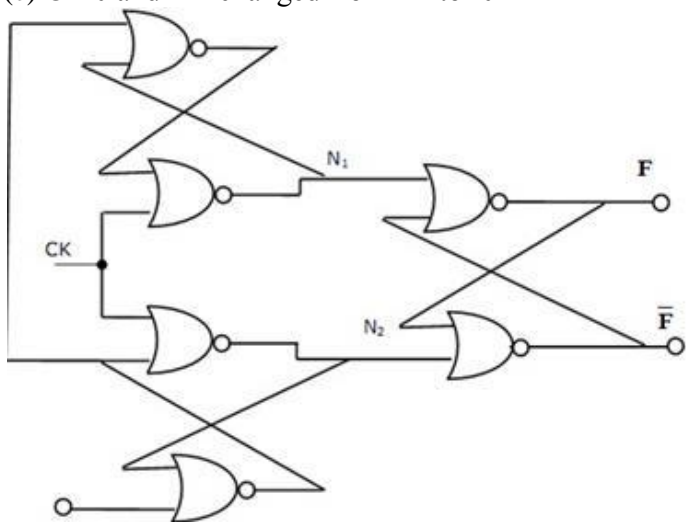
A	B	Q_{n+1}
0	0	Q_n'
0	1	1(Set)
1	0	0(Reset)
1	1	Q_n

Q7. For the digital circuit shown in the figure, explain what happen in node N1, N2, F and when

(a) $C_k = 1$ and 'A' changed from '0' to '1'.

(b) $A = 1$ and C_k changed from '1' to '0'

(c) $C_k = 0$ and 'A' changed from '1' to '0'



Q8. Draw the circuit diagram for MOD-13 ripple counter using T-flip flop and draw the waveforms at each flip flop output for 16 clock cycles.

Q9. Design a MOD-12 Asynchronous counter that counts from 0000 to 1011 using T Flip Flop.

Q10. Design a MOD-8 Up/Down Counter using J-K Flip Flop.

Q 11. Design a BCD counter with JK FLip-flop.