POSSESION OF MOBILES IN EXAM IS UFM PRACTICE

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Course Title: Computer Organization and Architecture — Max. Marks: 20
Course Code: 15B11CI313 — Max. Time: 1 Hour

Note: All questions are compulsory and use of Calculators is not allowed

Q.1 Answer the following short questions. **[1x5=5 Marks: CO1]**

a) Microprogrammed control is not suitable for RISC architecture. Justify with appropriate reasons
b) Identify the disadvantages of variable-length instructions?
c) What will be speed of the instruction with Direct Addressing Mode compare with respect to the Indirect Addressing Mode instructions? Justify with examples
d) How many bits of opcode is required to implement a CPU with 11 arithmetic and logical Instructions, 2 control instructions, and 4 data transfer instructions?
e) Calculate the number of address in the following instruction as well also recognize the type of addressing modes: STORE R1, 3030.

Q.2 (a) A benchmark program is run on a 200 MHz processor. The executed program consists of 2 million instruction executions, with the following instruction mix and clock cycle count:

Instruction Type	Instruction Count (%)	Cycles per Instruction
Arithmetic and logic	36	2
Load and store	11	4
Branch	44	2
Control transfer	9	1

Calculate the average CPI, MIPS rate, and execution time for this program. **[3 Marks: CO2]**

(b) The following table gives the opcode, frequency, cycles and % execution time of instruction in a program

Op	Freq	Cycles	% Time
ALU	30%	2	12%
Load	10%	3	40%
Store	20%	1	18%
Branch	40%	4	30%

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(i) If a CPU design enhancement improves the CPI of Branch instructions from 4 to 2, what is the overall speedup from this enhancement? **[2 Marks: CO2]**

(ii) If 20% of computation uses floating point processor and speedup of floating point processor is 10. What is the overall speedup achieved? **[1 Marks: CO2]**

(iii) Calculate overall speedup if we make 60% of a program run 30% faster.[**1 Marks: CO2]**

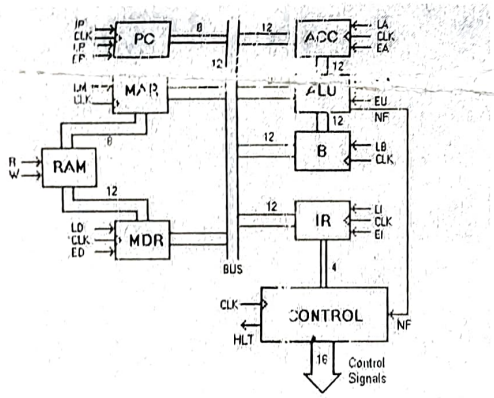
Q.3 (a) Translate the high-level assignment statements in a two address assembly code .

A = A - B;

A= A+ C;

Assume that A, B and C are 12 bit integer variables available in system RAM at locations M0, M1 and M2 respectively **[2 Marks: CO2]**

(b) In the following machine, these are instructions in its Instruction Set (LDA addr, STA addr, ADD, SUB, MBA, JMP addr, JN addr). Its hardware includes PC, IR, ALU, two registers – AC and B, MAR, MDR, and a Control Unit. The datapath control in the CPU is achieved through 16 different control signals connected to various hardware components



(i) Suppose you are the CPU design engineer, you have being instructed to modify the existing architecture by replacing the S control signal of ALU with C (2's complement). After modifying the control signals of ALU, Identify that the ISA of the JC-62 Machine is remain same or change. Justify your answer with valid reasons. **[CO-4, 3 Marks]**

(ii) Write the Microsteps for the **SUB** and **JMP addr** instructions for the modified machine above in **(i)**. **[CO-4, 3 Marks]**