JAYPEE INSTITUTE OF INFORMATION TECHNOLOGY, NOIDA

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

ELECTRICAL SCIENCE LAB-2

(15B17EC271)

Semester: Odd 2022 (3rd Semester)

Course Coordinator: Mr. Shivaji Tyagi

JAYPEE INSTITUTE OF INFORMATION AND TECHNOLOGY

VISION

To become a centre of excellence in the field of IT and related emerging areas of education, training and research comparable to the best in the world for producing professionals who shall be leaders in innovation, entrepreneurship, creativity and management.

MISSION

MISSION 1: To develop as a benchmark university in emerging technologies.

MISSION 2: To provide state-of-the-art teaching learning process and R&D environment.

MISSION 3: To harness human capital for sustainable competitive edge and social relevance.

Department Name: Electronics and Communication Engineering

VISION

To be a centre of excellence in education, training and research in Electronics and Communication Engineering to cultivate technically competent professionals for Industry, Academia and Society.

MISSION

MISSION 1: To impart education through contemporary, futuristic and flexible curricula with innovative teaching learning methods and hands on training with well equipped Labs.

MISSION 2: To carry out cutting edge research in different areas of Electronics and Communication Engineering.

MISSION 3: To inculcate technical and entrepreneurial skills in professionals to provide socially relevant and sustainable solutions.

Programme Name: B.Tech. in Electronics and Communication Engineering

Programme Educational Objectives:

PEO1: To provide strong foundation in Electronics and Communication Engineering to pursue professional career, entrepreneurship and higher studies.

PEO2: To develop capability to analyze, design and develop feasible solutions to real world problems.

PEO3: To inculcate professional ethics, managerial and communication skills to develop ingenious solutions for benefit of society and environment.

Programme Outcomes:

PO1: Engineering knowledge: Apply the knowledge of mathematics, science, engineering fundamentals, and an engineering specialization to the solution of complex engineering problems.

PO2: Problem analysis: Identify, formulate, research literature, and analyze complex engineering problems reaching substantiated conclusions using first principles of mathematics, natural sciences, and engineering sciences.

PO3: Design/development of solutions: Design solutions for complex engineering problems and design system components or processes that meet the specified needs with appropriate consideration for the public health and safety, and the cultural, societal, and environmental considerations.

PO4: Conduct investigations of complex problems: Use research-based knowledge and research methods including design of experiments, analysis and interpretation of data, and synthesis of the information to provide valid conclusions.

PO5: Modern tool usage: Create, select, and apply appropriate techniques, resources, and modern engineering and IT tools including prediction and modelling to complex engineering activities with an understanding of the limitations.

PO6: The engineer and society: Apply reasoning informed by the contextual knowledge to assess societal, health, safety, legal and cultural issues and the consequent responsibilities relevant to the professional engineering practice.

PO7: Environment and sustainability: Understand the impact of the professional engineering solutions in societal and environmental contexts, and demonstrate the knowledge of, and need for sustainable development.

PO8: Ethics: Apply ethical principles and commit to professional ethics and responsibilities and norms of the engineering practice.

PO9: Individual and team work: Function effectively as an individual, and as a member or leader in diverse teams, and in multidisciplinary settings.

PO10: Communication: Communicate effectively on complex engineering activities with the engineering community and with society at large, such as, being able to comprehend and write effective reports and design documentation, make effective presentations, and give and receive clear instructions.

PO11: Project management and finance: Demonstrate knowledge and understanding of the engineering and management principles and apply these to one's own work, as a member and leader in a team, to manage projects and in multidisciplinary environments.

PO12: Life-long learning: Recognize the need for, and have the preparation and ability to engage in independent and life-long learning in the broadest context of technological change.

Programme Specific Outcomes:

PSO 1: To identify the engineering problems and develop solutions in the area of communication, signal processing, VLSI and embedded systems.

PSO2: To demonstrate proficiency in utilisation of software and hardware tools along with analytical skills to arrive at appropriate solutions.

Course Description

Course Code	15B17EC271	**Semester -:** Odd (specify Odd/Even)	**Semester-:** Odd, **Session** 2022 -2023 **Month- : August- December**
Course Name	Electrical Science Lab-II		
Credits	1	**Contact Hours**	0-0-2

Faculty (Names)	**Coordinator(s)**	Dr. Abhishek Kashyap, Mr. Shivaji Tyagi
	Teacher(s)	Prof. Jitendra Mohan, Prof. Sajaiveer Singh, Dr. Bajrang Bansal, Dr. Yogesh Kumar, Dr. Abhishek Kashyap, Dr. Atul Kumar, Dr. Hemant Kumar, Dr. Kapil Dev Tyagi, Dr. Kaushal Nigam, Dr. Satyendra Kumar, Dr. Varun Goel, Mr. Vinay Tikkiwal, Mr. Shivaji Tyagi, Dr. Vijay Khare, Dr. Gaurav Khanna, Ms. K. Nisha, Dr. Ankur Bhardwaj, Mr. Atul Kumar Srivastava, Mr. Vishal Narain Saxena, Ms. Bhawna Gupta, Mr. Mandeep Narula, Mr. Ritesh Kumar Sharma, Dr. Garima Kapur, Dr. Ajay Kumar, Dr. Samriti Kalia, Mrs. Smriti Bhatnagar, Ms. Shradha Saxena,

COURSE OUTCOMES		**COGNITIVE LEVELS**
C204.1	Study and analyze time response of first order and second order passive circuits	Analyzing(C4)
C204.2	Understand two port resistive network parameters, operational amplifier applications and first order filter.	Understanding(C2)
C204.3	Understand the characteristics of pn junction diode and its applications	Understanding(C2)
C204.4	Understand the characteristics of Common emitter and common base configurations of BJT.	Understanding(C2)

Module No.	**Title of the Module**	**List of Experiments**	**COs**
1.	First and Second order passive circuits	Study the transient response of a series RC circuit and understand the time constant concept using pulse waveforms.	C204.1
		Study of Time Response of R-L-C Network	C204.1
2.	Two port resistive networks	To determine the Z-parameters of a 2- port resistive network.	C204.2
		To determine the h-parameters of a two-port resistive network.	C204.2

3.	Operational amplifier and its applications	To realize inverting and non inverting configurations using Op- Amp IC 741 amplifier.	C204.2
		To realize an adder and substractor circuits using Op- Amp IC 741 amplifier.	C204.2
4.	PN junction and Zener diodes	To study the forward and reverse bias (volt-ampere) characteristics of a simple p-n junction diode. Also determine the forward resistance of the diode.	C204.3
		To study the forward and reverse bias volt-ampere characteristics of a zener diode. Also determine the breakdown voltage, static and dynamic resistances.	C204.3
5.	Diode applications	To observe the output waveform of half/full wave rectifier and calculate its ripple factor and efficiency.	C204.3
		Realization of desired wave shapes using clipper and clamper circuits.	C204.3
		To study Zener voltage regulator and calculate percentage regulation for line regulation and load regulation.	C204.3
6.	Bipolar Junction Transistor	To plot input characteristics of a common emitter npn BJT.	C204.4
		To plot output characteristics of a common emitter npn BJT.	C204.4
		To plot input characteristic of a BJT in Common Base Configuration.	C204.4
		To plot output characteristic of a BJT in Common Base Configuration.	C204.4
7.	First order filters	To plot frequency and phase response of First order low pass and high pass filter.	C204.2

Evaluation Criteria

Components	**Maximum Marks**
Viva1	20
Viva2	20
Attendance, and D2D	60 (15+45)
Total	**100**

Project Based Learning: Students will learn about the transient response of first and second order passive circuits. Also, student will learn about Op-amp and its applications like adder and substractor circuits. This course also gives the understanding of semiconductor diodes and Bipolar Junction Transistor. These concepts are the required for Electronic circuit design.

Recommended Reading material: Author(s), Title, Edition, Publisher, Year of Publication etc. (Text books, Reference Books, Journals, Reports, Websites etc. in the IEEE format)

1.	R.C.Dorf, A. Svoboda, "Introduction to Electric Circuits",9th ed, John Wiley & Sons, 2013.
2.	D. Roy Choudhary and Shail B. Jain, " Linear Integrated Circuit," 2nd Edition, NAILP, 2003
3.	A.S .Sedra & K.C.Smith, Microelectronic Circuits Theory and Application, 6th Edition, Oxford University Press, 2015(Text Book)

Experiment No: 1

AIM:

Study the transient response of a series RC circuit and understand the time constant concept using pulse waveforms.

APPARATUS REQUIRED:

S.No	Apparatus	Specifications	Quantity
1.	CRO		
2.	Multimeter		
3.	Breadboard		
4.	Components		
5.	Connecting Wires		
6.	Function Generator		

COMPONENT REQUIRED:

S.No	Apparatus	Specifications	Quantity
1.	Resistor	2.2kΩ, 100kΩ	1 each
2.	Capacitor	0.1 µF, 0.01 µF	1 each

THEORY:

A capacitor has the ability to store an electrical charge and energy. The voltage across the capacitor is related to the charge by the equation V=Q/C for steady state values, or expressed as an instantaneous value dv=dq/C

We will study the transient response of the RC circuit, which is the response to a sudden change in voltage.

In this experiment, we apply a pulse waveform to the RC circuit to analyze the transient response of the circuit. The *pulse-width* relative to a circuit's *time constant* determines how it is affected by an RC circuit.

Time Constant **(τ)**: A measure of time required for certain changes in voltages and currents in RC and RL circuits. Generally, when the elapsed time exceeds five time constants (5τ) after switching has occurred, the currents and voltages have reached their final value, which is also called steady-state response.

The time constant of an RC circuit is the product of equivalent capacitance and the Thévenin resistance as viewed from the terminals of the equivalent capacitor.

$$\tau = RC \qquad \text{..... (1)}$$

A Pulse is a voltage or current that changes from one level to the other and back again. If a waveform's high time equals its low time, it is called a *square wave.* The length of each cycle of a pulse train is termed its *period* (**T**).

The *pulse width* (***t_p***) of an ideal square wave is equal to half the time period. The relation between pulse width and frequency is then given by,

$$f = \frac{1}{2\,t_p} \qquad \text{..... (2)}$$

A series RC circuit is shown in Figure1.

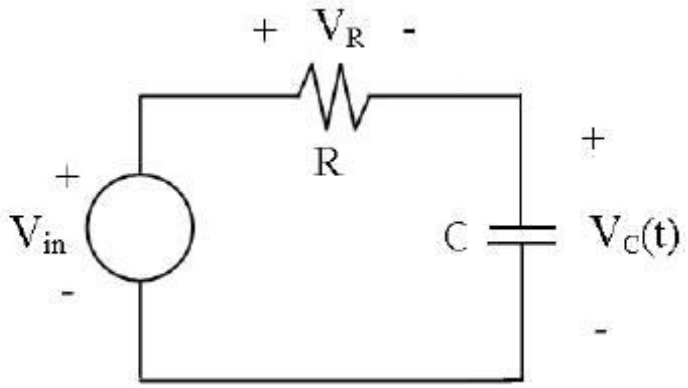


Figure 1.

From Kirchoff's laws, it can be shown that the charging voltage $\mathbf{V_C\,(t)}$ across the capacitor is given by:

$$V_C(t) = V(1 - e^{-t/RC}), \quad t \geq 0 \qquad \ldots\ldots\ldots(3)$$

Where, V is the applied source voltage to the circuit for $t \geq 0$. $\tau = RC$ is the time constant. The response curve, showing capacitor charging for Series RC circuit to a step input with time axis normalized by τ is shown in Figure 2.

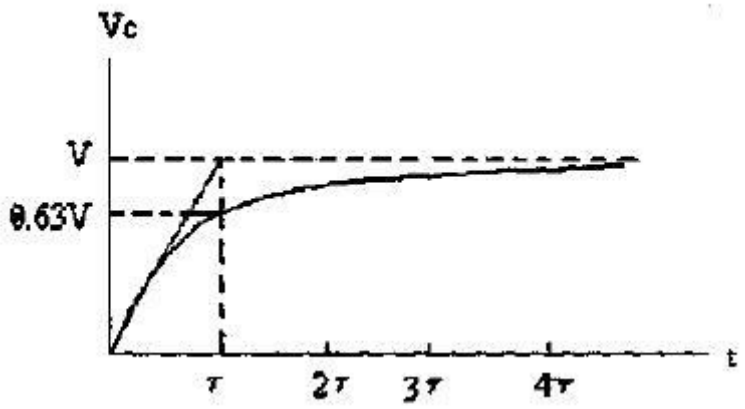
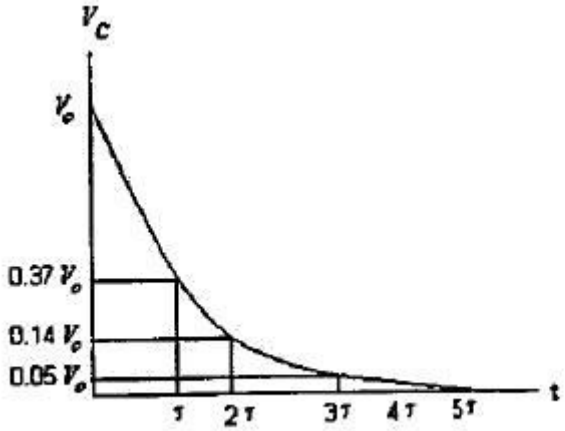


Figure 2.

The discharge voltage for the capacitor is given by:

$$V_C(t) = V_o e^{-t/RC}, \quad t \geq 0 \qquad \ldots\ldots(4)$$

Where V_O is the initial voltage stored in capacitor at t = 0, and τ=RC is time constant. The response curve is a decaying exponentials as shown in Figure 3.



t	$e^{-t/\tau}$
τ	0.37
2τ	0.14
3τ	0.05
4τ	0.02
5τ	0.01

Figure 3.

PROCEDURE:

1. Set up the circuit shown in Figure1 with the component values R = 2.2 kΩ and C =0.1 μF.

2. Set the Function Generator to generate a $4V_{p-p}$ square wave and apply as input voltage to the circuit.

3. Observe the input square wave on channel 1 and output, across the capacitor, on channel 2 of the CRO. Set the volt/div same for both the channels, as shown in Figure 4.

4. Observe the response of the circuit for the following three cases and record the results.

a. $t_p >> 5\tau$: Set the frequency of the function generator output such that the capacitor has enough time to fully charge and discharge during each cycle of the square wave. So Let $t_p = 15\tau$ and accordingly set the function generator frequency using equation (2). The value you have found should be approximately 150 Hz. Determine the time constant from the waveforms obtained on the CRO. (At $t= \tau$, V_c (t) =0.63V from equation (3)).

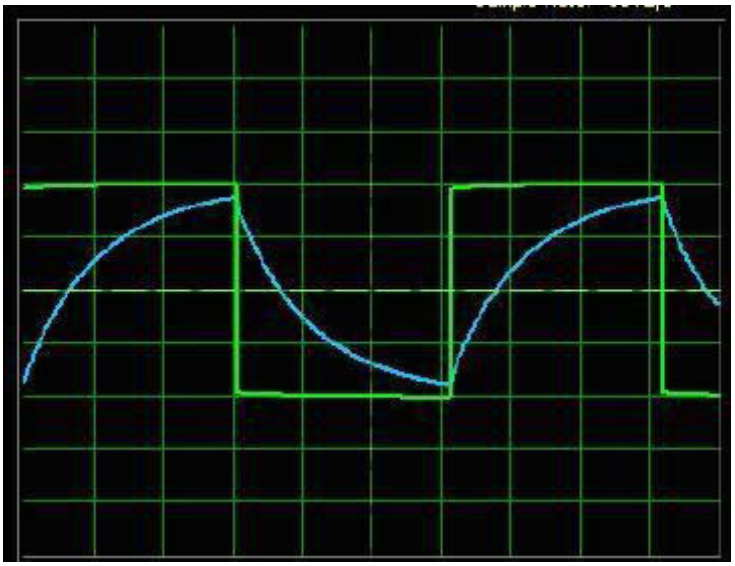


Figure 4.

b. $t_p = 5\tau$: Set the frequency such that $t_p = 5\tau$ (this should be 450 Hz)**.** Since the pulse width is exactly 5τ, the capacitor should just be able to fully charge and discharge during each pulse cycle. From the figure determine τ (see Figure 2 and Figure 5 below.)

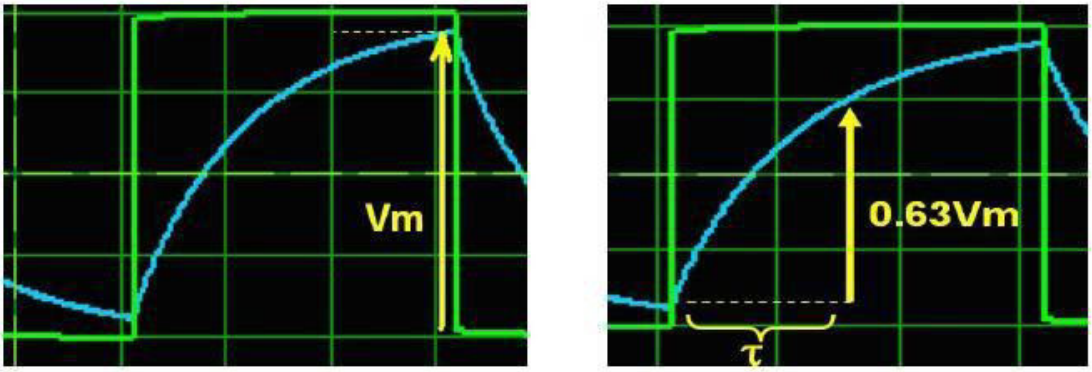


Figure 5.

c. $t_p << 5\tau$: In this case the capacitor does not have time to charge significantly before it is switched to discharge, and vice versa. Let $t_p = 0.5\tau$ in this case and set the frequency accordingly.

5. Repeat the procedure using R = 100 kΩ and C = 0.01 μF and record the measurements.

OBSERVATION TABLE:-

Value of R	Value of C	Time constant	
		Observed	Calculated

RESULT:-

PRECAUTIONS:

1. Care should be taken that low value resistances are not connected across the circuit
2. .Ammeter should be connected in series and voltmeter should be connected in parallel.
3. Take care to use the proper polarity when measuring voltage and current.

Experiment No: 2(a)

AIM:

To determine the Z-parameters of a 2- port resistive network

APPARATUS REQUIRED:

Sl.No	Apparatus	Specifications	Quantity
1. 2. 3.	Multi-meter Bread Board Power Supply		1 1 1

COMPONENT REQUIRED:

Sl.No	Apparatus	Specifications	Quantity
1. 2. 3.	Resistances Resistance Connecting Wires	1K 2.2K	2 1

THEORY:

A two -port network is an electrical circuit or device with two pairs of terminals. This makes possible the isolation of either a complete circuit or part of it. They are important in **modeling electronic devices** and system components.

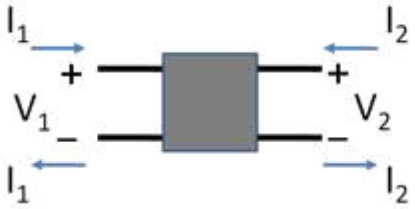


Figure1: Two Port Network

The Z parameters or the "Open Circuit" parameters relate to the output currents from the ports to their input voltages. It is called "Open Circuit" because it calculates, for example Z_{11}, we need to do open circuit of the output ($I_2 = 0$). The output voltages may be defined in terms of the Z-parameter matrix and the input currents by the following matrix equation:

$$\begin{pmatrix} V_1 \\ V_2 \end{pmatrix} \quad \begin{pmatrix} Z_{11} & Z_{12} \\ Z_{21} & Z_{22} \end{pmatrix} \begin{pmatrix} I_1 \\ I_2 \end{pmatrix}$$

Where,

$$Z_{11} = \left.\frac{V_1}{I_1}\right|_{I_2=0} \qquad Z_{12} = \left.\frac{V_1}{I_2}\right|_{I_1=0} \qquad \text{Eqn.-1}$$

$$Z_{21} = \left.\frac{V_2}{I_1}\right|_{I_2=0} \qquad Z_{22} = \left.\frac{V_2}{I_2}\right|_{I_1=0} \qquad \text{Eqn.-2}$$

All the Z-parameters have dimensions of ohms.

EXAMPLE:

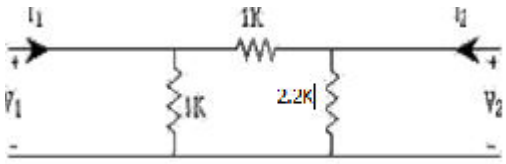


Figure2: Example Circuit of Two Port Network

SOLUTION:

Assemble the circuit. By applying appropriate sources of terminals of interest impedance parameter equations, the desired values can be found.

Step 1 Inspection of above matrix indicates that we can find Z_{11} and Z_{21} by open-circuit the right port (I_2=0), and injecting a current I_1 in the left port and determining the two voltages, Figure3.

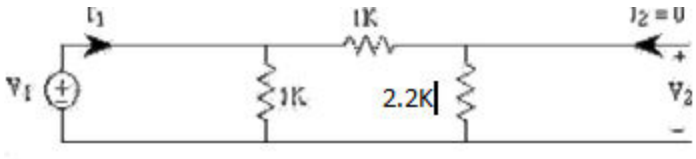


Figure3: Example Circuit for determining Z_{11} and Z_{21}

There will be no voltage drop across the 2.2 k resistor, and the current I_1 flows throughboth 1 k resistors.

According to Eqn.-1

$$V_1 = Z_{11}I_1$$
$$V_1 = Z_{12}I_2$$

According to Eqn.-2

$$V2=Z_{21}I1$$
$$V2=Z_{22}I2$$

According to Figure3

$$V_1 = I1(1k \| (1k+2.2k))$$

$$V_2 = \frac{2.2K}{1K+2.2K} V1$$

Therefore,

$$\mathbf{Z_{11} = 0.76k,\ Z_{21} = \frac{V2}{I1} = 0.52K}$$

Step 2

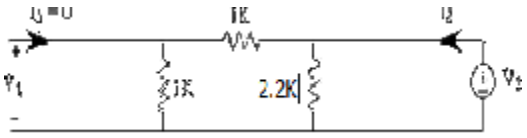


Figure 4: Example Circuit for determining Z_{12} and Z_{22}

According to Eqn.-1&2

$$V_1 = Z_{12} I_2$$

$$V_2 = Z_{22} I_2$$

According to Figure4

$$V1 = \frac{1K}{2K} V2 = 0.5V2$$

$$V2 = I2(2.2 \| (1K+1K))$$

Therefore,

$$\mathbf{Z_{22} = 1.047K,}$$

$$\mathbf{Z_{12} = V1/I2 = 0.524K}$$

OBSERVATION TABLE:

Table I – When Output Port is open Circuited, I_2 =0.

V_1(V)	I_1(A/mA)		V_2(V)		$Z_{11} = V_1/I_1$		$Z_{21} = V_2/I_1$	
Applied	**Exp.**	**The.**	**Exp.**	**The.**	**Exp.**	**The.**	**Exp.**	**The.**

Table II – When Input Port is Open Circuited, $I_1 = 0$.

V_2 (V)	V_1 (V)		I_2(A/mA)		$Z_{12} = V_1/I_2$		$Z_{22} = V_2/I_2$	
Applied	**Exp.**	**The.**	**Exp.**	**The.**	**Exp.**	**The.**	**Exp.**	**The.**

CALCULATION:

Parameters	Experimental	Theoretical
Z_{11}		
Z_{12}		
Z_{21}		
Z_{22}		
Calc Δ%		

- $\Delta\% = 100 \cdot [X_{exp} - X_{th}]/X_{exp}$
  - Where $X_j \equiv$ Z- Parameters

RESULT:-

PRECAUTIONS:

1. Care should be taken that low value resistances are not connected across the circuit
2. .Ammeter should be connected in series and voltmeter should be connected in parallel.
3. Take care to use the proper polarity when measuring voltage and current.

Experiment No: 2(b)

AIM:
To determine the h-parameters of a Two-port resistive network

APPARATUS REQUIRED:

Sl.No	Apparatus	Specifications	Quantity
1.	Multi-meter		1
2.	Bread Board		1
3.	Power Supply		1

COMPONENT REQUIRED:

SI.No	Apparatus	Specifications	Quantity
1.	Resistances	1K	2
2.	Resistance	2.2K	1
3.	Connecting Wires		

THEORY:

A two-port network is an electrical circuit or device with two pairs of terminals make it possible the isolation of either a complete circuit or part of it They are important in modeling electronic devices and system components.

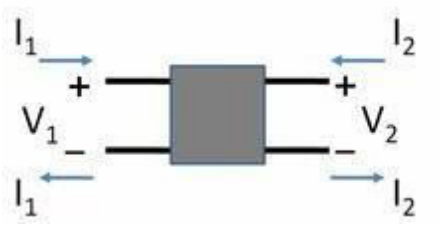


Figure1: Two Port Network

The h parameters use the input current at port 1 and the output voltage at port 2 as the independent variables. The output voltages may be defined in terms of the Z-parameter matrix and the input currents by the following matrix equation:

$$V_1 = h_{11} I_1 + h_{12} V_2 \qquad \text{Eqn.-1}$$

$$I_2 = h_{12} I_1 + h_{22} V_2 \qquad \text{Eqn.-2}$$

Where,

$h_{11} = [V_1 / I_1]$ with $V_2 = 0$

= Input Impedance with output port short circuited.

$h_{22} = [I_2 / V_2]$ with $I_1 = 0$

= Output admittance with input port open circuited.

$h_{12} = [V_1 / V_2]$ with $I_1 = 0$

= reverse voltage transfer ratio with input port open circuited.

$h_{21} = [I_2 / I_1]$ with $V_2 = 0$

= Forward current gain with output port short circuited.

Dimensions of h- Parameters are

h_{11} - Ω h_{22}– mhos

h_{12}, h_{21} – dimension less.

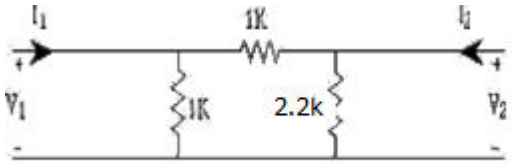


Figure2: Example Circuit of Two Port Network

SOLUTION:

Assemble the circuit, by applying appropriate sources of terminals of interest impedance parameter equations, the desired values can be found.

Step 1 As per Eqn.-1&2, we can find h_{11} and h_{21} by short circuiting the port-2, applying a voltage V_1 on port-1 (Figure 3) and determining V_1 and I_2.

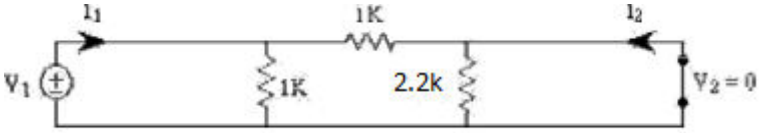


Figure 3: Example circuit for determining h11 and h21.

According to Eqn.-1&2 and fig 3 (@V_2=0)

$V_1=h_{11}I_1$

$I_2=h_{21}I_1$

$V_1=h_{11}I_1$

$V_1=I_1(1/2)=h_{11}=V_1/I_1=1/2k\Omega$

$I_2= -I_1/2$

$h_{21}=I_2/I_1= -1/2$

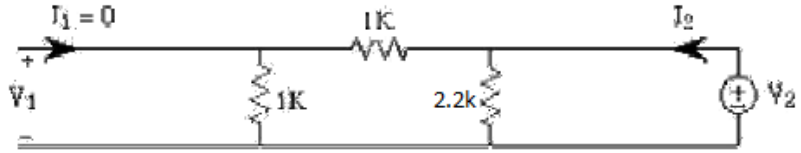


Figure 4: Example circuit for determining h_{12} and h_{22}.

From Eqn. 1&2 and fig 4 (@ $I_1=0$)

$$V_1=h_{12}V_2$$
$$I_2=h_{22}V_2$$

$$h_{12} = V_1/V_2 = \frac{1}{2}$$
$$V_2=I_2(2.2k\|2k)$$
$$h_{22}=I_2/V_2=0.95 \text{ m mho}$$

OBSERVATION TABLE:

Table I – When Output Port is short Circuited, $v_2=0$.

V_1(V)	I_1(A/mA)		I_2(A/mA)		$h_{11} = V_1/I_1$		$h_{21} = I_2/I_1$	
Applied	Exp.	The.	Exp.	The.	Exp.	The.	Exp.	The.

Table II – When Input Port is Open Circuited, $I_1= 0$.

V_2 (V)	V_1 (V)		I_2(A/mA)		$h_{12} = V_1/V_2$		$h_{22} = I_2/V_2$	
Applied	Exp.	The.	Exp.	The.	Exp.	The.	Exp.	The.

Parameters	Experimental	Theoretical
h_{11}		
h_{12}		
h_{21}		
h_{22}		
Calc Δ%		

- $\Delta\% = 100 \cdot [X_{exp} - X_{th}]/X_{exp}$
  - Where $X_j \equiv$ h- Parameters

RESULT:-

PRECAUTIONS:

1. Care should be taken that low value resistances are not connected across the circuit
2. .Ammeter should be connected in series and voltmeter should be connected in parallel.
3. Take care to use the proper polarity when measuring voltage and current.

EXPERIMENT: 3

AIM:

To observe inverting and Non inverting amplifier Configurations using Op-Amp IC741.

Appratus and component required:

S.No.	Apparatus and Components Required	Quantity
1.	Op Amp IC -741	1
2.	Resistors : 1k, 10k	1
3.	Function Generator	1
4.	DC Regulated Power Supply	1
5.	CRO	1
6.	Bread Board	1
7.	Connecting wires	

Pin Diagram of Op-Amp IC741:

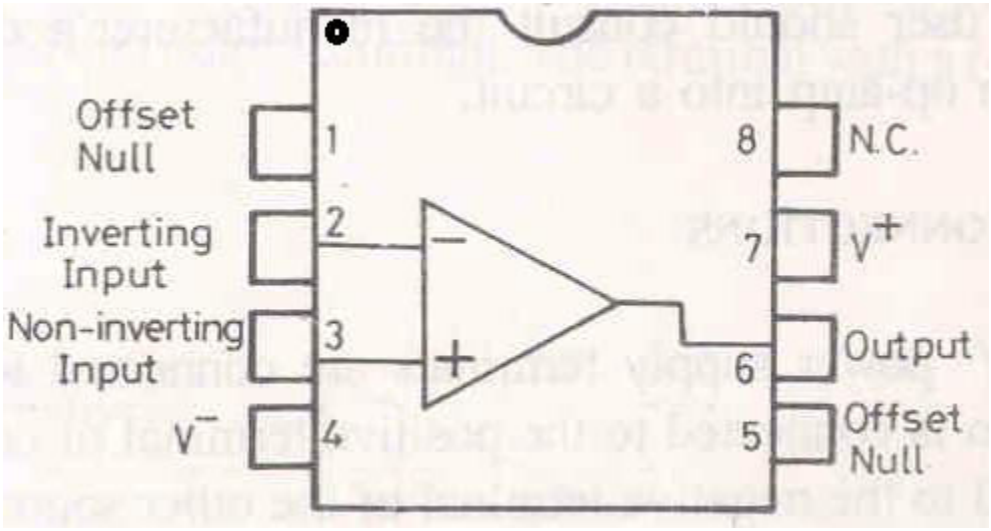


Fig. 1 Pin Diagram of Op-Amp741 IC

Inverting amplifier

THEORY:

Figure 2(a) shows a inverting amplifier. The output Voltage (V_o) is of the opposite polarity as the input voltage (V_{in}). The input signal is applied directly to the inverting (-ve) input terminal of the amplifier and the feedback resistance is also connected between the output terminal and inverting input terminal.

Closed –Loop Voltage Gain (A_F):

The closed-loop voltage gain A_F can be obtained by writing Kirchoff's Current equation at the input node 2 as follows:

$I_{in} = I_F + I_B$..... (1)

Since R_i is very large, the input bias current (I_B) is negligibly small. For instance,R_i = 2MΩ and I_B = 0.5μA for 741C. Therefore, $I_{in} \cong I_F$

Now, from circuit diagram shown in Fig. 2 (a)

$$\frac{V_{in} - V_2}{R_1} = \frac{V_2 - V_o}{R_F} \quad \text{.....(2)}$$

Using Virtual short concept $V_1 = V_2$

Since $V_2 = 0V$, Substituting this value of V_2 in Equation (2)

$$A_F = \frac{V_o}{V_{in}} = \frac{-R_F}{R_1} \quad \text{.....(3)}$$

Circuit Daigram & Waveform

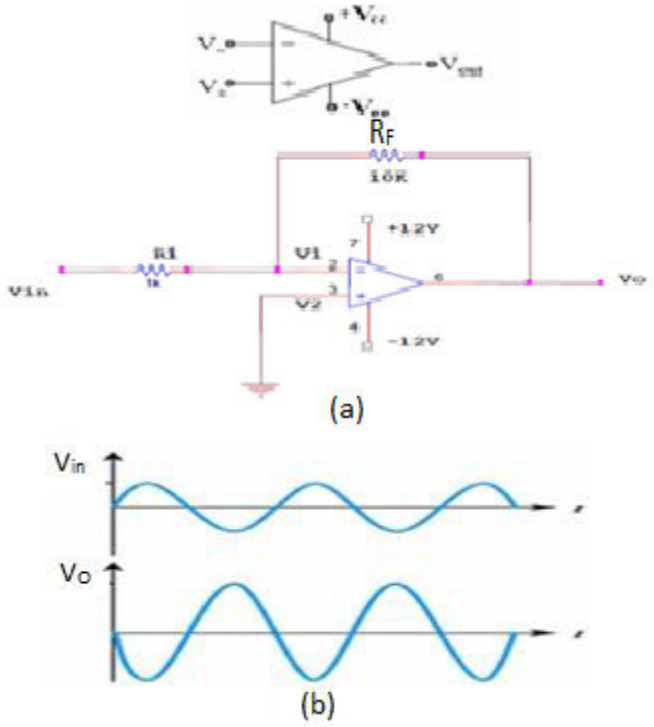


Fig. 2. Inverting Amplifier (a) Circuit diagram (b) Waveforms

Procedure:

1. Make the connections as per the circuit diagram.
2. Apply the input to the Inverting terminal and obtain the output on the CRO.
3. Take various readings by varying the input voltage and hence calculate the gain.
4. Calculate the gain using formula.

$A_F = - R_F / R_1$ (Theoretical)
$A_F = V_o/V_{in}$ (Practical)

Observation Table:

S. NO	V_{in}(volts	V_O(volts)	$A_{F=} - R_F/R_1$ (Theoretical	$A_F = V_O/V_{in}$ (Practical)
1				
2				
3				
4				

Non inverting amplifier

THEORY:

Figure shows a non-inverting amplifier. The output Voltage (V_o) is of the same polarity as the input voltage (V_{in}.) The input resistance of the non-inverting amplifier is very large (100MΩ) in this case. The input signal is applied directly to the non-inverting (+ve) input terminal of the amplifier and the feedback resistance are connected between the output terminal, the –ve input terminal and ground.

The Minimum Gain of the Non-Inverting Amplifier is 1

Closed –Loop Voltage Gain (A_F):

$A_F = V_o/V_{in}$ …….(4)

From the circuit diagram shown in Fig. 3 (a)

$V_1/ R_1 = (V_o - V_1)/ R_F$ ……..(5)

Using Virtual short concept $V_1=V_2=V_{in}$

Therefore, $V_{in} / R_1 = (V_o - V_{in})/ R_F$

➔ $A_F = V_0 / V_{in} = 1 + R_F / R_1$ …… (6)

Circuit Daigram & Waveform

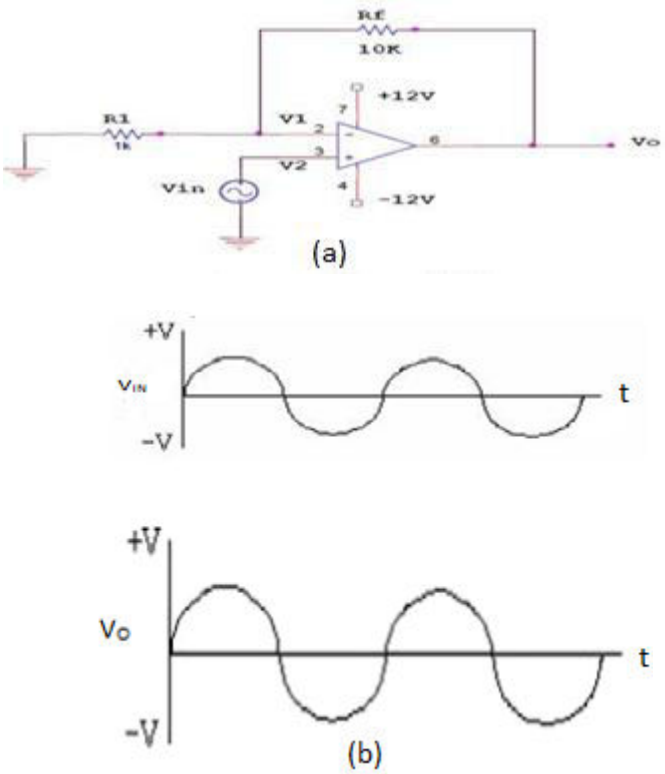


Fig. 3. Non-Inverting Amplifier (a) Circuit diagram (b) Waveforms

Procedure:

1. Make the connections as per the circuit diagram.
2. Apply the input to the Non-Inverting terminal and obtain the output on the CRO.
3. Take various readings by varying the input voltage and hence calculate the gain.
4. Calculate the gain using formula.

$$A_F = 1 + R_F / R_1$$

$$A_F = V_O / V_{in}$$

Observation table:

S. No.	V_{in} (Volts)	V_o(Volts)	$A_F=1+(R_F/R_1)$ (Theoretical)	$A_F=V_o/V_{in}$ (Practical)

Result:

Voltage gain of the Inverting/Non-inverting amplifiers depends on the value of R_F & R_1, whereas it is independent of the open loop gain 'A_o' of the op-amp. Theoretical and Practical values of the Gain are approximately same.

Learning outcome:

Experiment No. -4

Aim: To study the forward and reverse bias (volt-ampere) characteristics of a simple p-n junction diode. Also determine the forward resistance of the diode.

Apparatus and Components Required:

S. No.	Apparatus	Quantity
1.	DC power supply	1
2.	Multimeter	1
3.	Resistor 1K	1
4.	PN Diode IN4007	1

Theory: The diode is a semiconductor device formed from a junction of n-type and p-type semiconductor materials. The lead connected to p-type material is called as anode and the lead connected to n- type material is called cathode as shown in fig. 4.1.

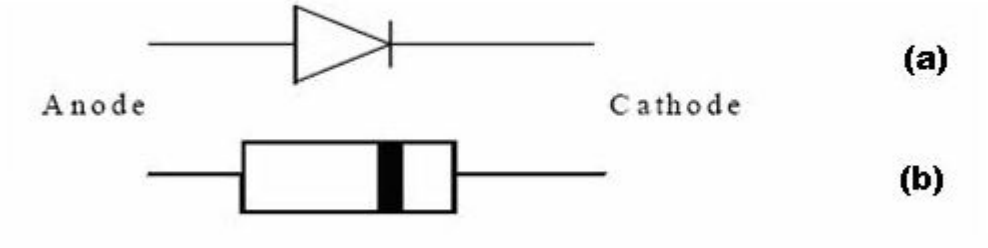


Figure 4.1: (a) Diode Symbol (b) Actual diode

When diode is in forward bias (higher potential is connected to the anode lead), current flows through it. As the voltage across diode increases, current also increases. It is observed that the rate of change in current increases with increase in the voltage across diode. After some potential drop across the diode, the rate of change in current increases rapidly. The potential drop after which current increases rapidly is called as **Cut in Voltage**. It is measured by drawing a tangent on the slope of the V-I Characteristics from where current increases drastically. For Germanium diode is it around 0.2-0.3V, while for Silicon diode it is 0.4-0.7V. When diode is in reverse bias (higher potential is connected to the cathode lead), ideally no current flows through it, practically a very small leakage current (in micro ampere) flows due to some impurity charge carriers. In the p-n junction diode the value of reverse breakdown voltage is very high (-600V for 1N4001). If this voltage is applied in the reverse bias, then very high value of current will flow and diode will get damaged. The characteristic curve for an ideal diode and practical diode is shown in Fig 4.2.

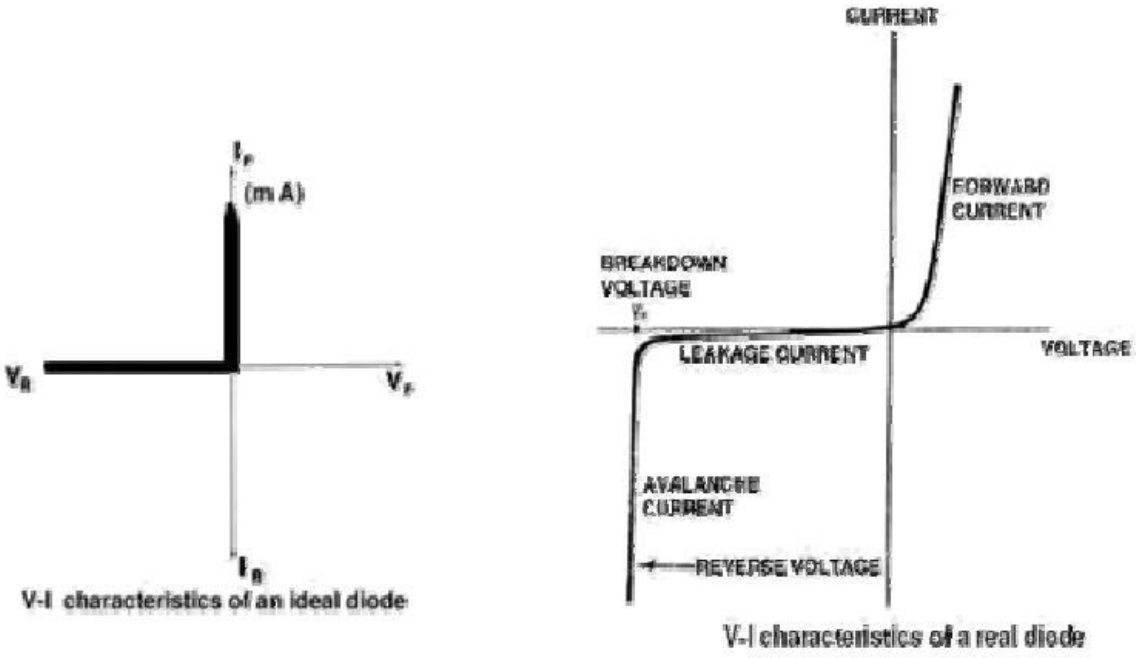


Figure 4.2: V-I characteristics of Ideal and Practical Diode

While analyzing circuits, the practical diode is usually replaced with a simpler model. In the simplest form, the ideal diode is modeled by a switch as shown in Fig 4.3. The switch is closed when the diode is forward biased and open when reverse biased. The real diode is modeled as shown in Fig 4.4. Rf and Rr are the resistances offered by the diode in the forward bias and reverse bias respectively. Vy is the cut-in voltage of the diode.

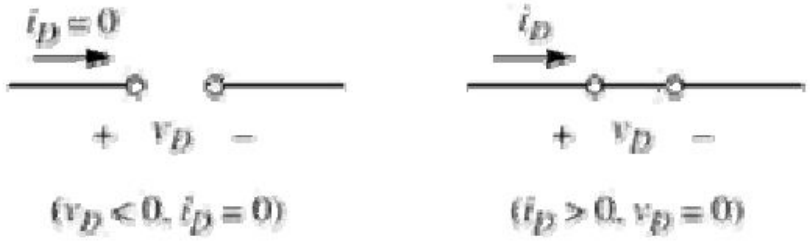


Figure 4.3: Equivalent model of ideal diode

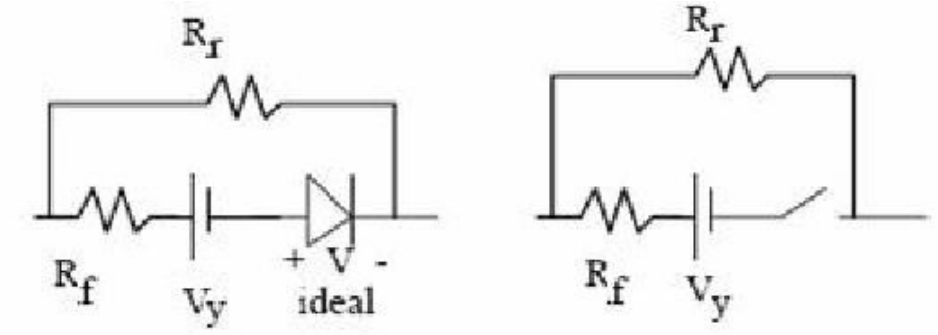


Figure 4.4: Equivalent model of practical diode

Circuit Diagram:

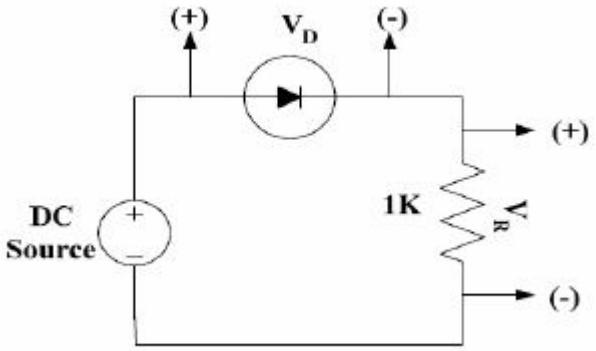


Figure 4.5: Circuit diagram

Procedure:

1. Study the characteristics of the diode in the data sheet. Copy all the specification for the diode in your final lab report.
2. Connect the circuit as shown in fig. 4.5.
3. Connect voltmeter across diode and resistor respectively.
4. Vary the input from DC source from -5 to 5 volt in the step of 0.1 volt and note down the reading across diode and resistor. Calculate the current flowing through the resistance.
5. Now plot the graph between the current flowing through the diode and potential across the diode.
6. From this graph, obtain the cut-in voltage(V_y) for the diode. From the point where current

   Increases sharply, draw a line to x-axis. The point where it intersects on the x-axis is called cut-in voltage.

7. Measure the slope of the curve to calculate the resistance offered by the diode in the forward bias. Forward bias resistance is named as R_f as shown in fig. 6.4.

Observation:

S. No.	**Resistor Voltage (V_r)**	**Current (I)=V_r/R**	**Diode Voltage (V_d)**

Result:

V_y=

R_f =

Learning Outcome:

Experiment No. - 5

Aim:

To study the forward and reverse bias volt-ampere characteristics of a zener diode. Also determine the breakdown voltage, static and dynamic resistances.

Apparatus and Components Required:

S. No.	Apparatus and Components Required	Quantity
1.	Zener Doide (V_Z=6.8v)	01
2.	Resistance 1K	01
3.	Bread Board	01
4.	DC Power Supply	01
5.	Multimeter	01
6.	Connecting wires	

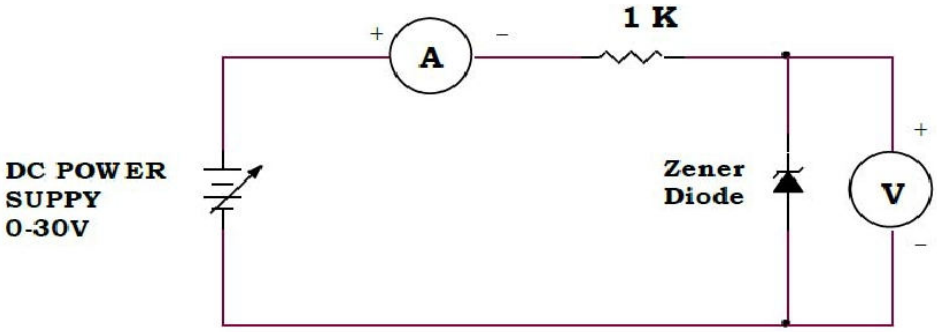
Theory:

The circuit diagram to plot the *VI* characteristics of a *zener* diode is shown. Zener diode is a special diode with increased amounts of doping. This is to compensate for the damage that occurs in the case of a *pn* junction diode when the reverse bias exceeds the breakdown voltage and thereby current increases at a rapid rate.

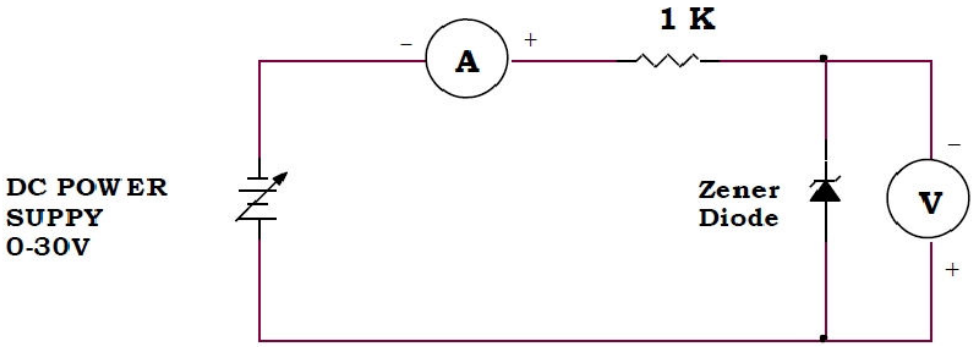
Applying a positive potential to the anode and a negative potential to the cathode of the zener diode establishes a forward bias condition. The forward characteristic of the zener diode is same as that of a *pn* junction diode i.e. as the applied potential increases the current increases exponentially. Applying a negative potential to the anode and positive potential to the cathode reverse biases the zener diode.

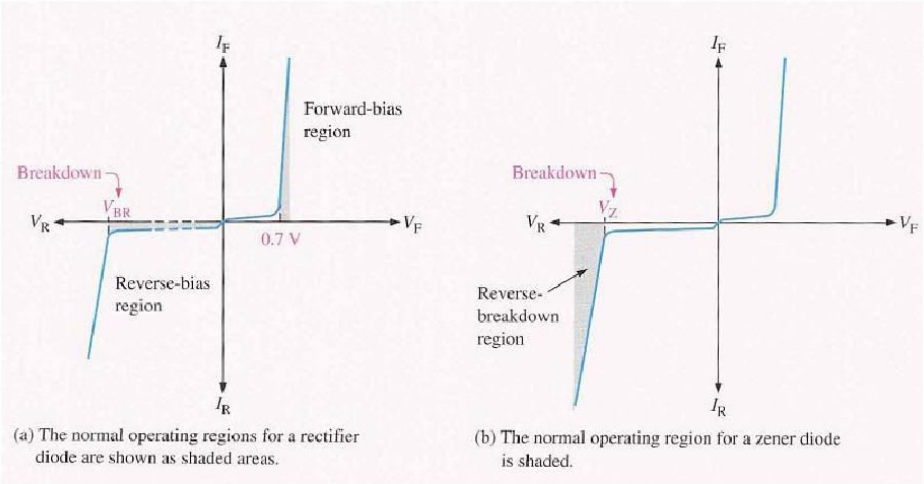
As the reverse bias increases the current increases rapidly in a direction opposite to that of the positive voltage region. Thus under reverse bias condition breakdown occurs. It occurs because there is a strong electric filed in the region of the junction that can disrupt the bonding forces within the atom and generate carriers. The breakdown voltage depends upon the amount of doping. For a heavily doped diode depletion layer will be thin and breakdown occurs at low reverse voltage and the breakdown voltage is sharp. Whereas a lightly doped diode has a higher breakdown voltage. This explains the zener diode characteristics in the reverse bias region. The maximum reverse bias potential that can be applied before entering the zener region is called the Peak Inverse Voltage referred to as PIV rating or the Peak Reverse Voltage Rating (PRV rating)

Circuit Diagram (REVERSE BIASE):



Circuit Diagram (FORWARD BIASE):





(a) The normal operating regions for a rectifier diode are shown as shaded areas.

(b) The normal operating region for a zener diode is shaded.

Procedure:

1. Connect the circuit as shown in figure.
2. Apply DC supply as shown in the figure.
3. Measure the value of V_Z and I_Z, V_R Reverse biased.
4. Reapeat the all step with opposite polarity of zener diode.
5. Measure the value of V_Z and I_Z, V_F Reverse biased.
6. Plot the curve between Voltage and current for forward and reverse biased zener diode.

Observation:

S. No.	Forward Bias			Reverse Bias		
	V_F	V_z	I_z	V_R	V_z	I_z
1.						
2.						
3.						

Result:

Plot for reverse biased and forward biased zener diode: Break down voltage value:
Static resistance = Vz/Iz

Dynamic resistance value: change in zener voltage/change in current through zener diode.

Learning Outcomes:

Experiment No. 6

Aim:

To observe the output waveforms of half wave and full wave rectifiers and calculate respective ripple factor and efficiency.

Apparatus and Components Required:

S. No.	Apparatus and Components Required	Quantity
1.	Transformer (12-0-12)	1
2.	Pin Diode	04
3.	Resistor 1 ∧K	1
4.	CRO	1
5.	Bread Board	1
6.	Connecting wires	

Theory:

Half wave and full wave bridge rectifier:

In half wave rectification, single diode act as a half wave rectifier. The A.C. supply to be rectified is applied in series with diode and load resistance RL. A.C. supply is given through a transformer. During positive half cycles of input A.C. voltage, this make diode forward biased and hence it conducts current. During negative half cycles, diode is reverse biased and it conducts no current. Therefore, current flow through the diode during positive half cycles of A.C. input voltage only. it is blocked during negative half cycles.

Full wave bridge rectifier, current flow through the load in the same direction for both half cycles of input A.C. it's contain four diode D1, D2, D3, D4 connected to form bridge. The A.C supply to be rectified is applied to the diagonally opposite end of the bridge trough the transformer. Between two other ends of the bridge, the load resistance RL is connected. During the positive half cycle of A.C. input voltage D1 & D3 forward biased while diode D2 &D4 are

reversed biased. Therefore only diode D1& D3 conduct. These two diode will be in series through the load. Current flow through load. During negative half cycles diodes D2&D4 becomes forward biased whereas D1 and D3 become reverse biased. Therefore only D2&D3 conduct .these diodes will be in series through the load RL. Current flow through lo

Circuit Diagram:

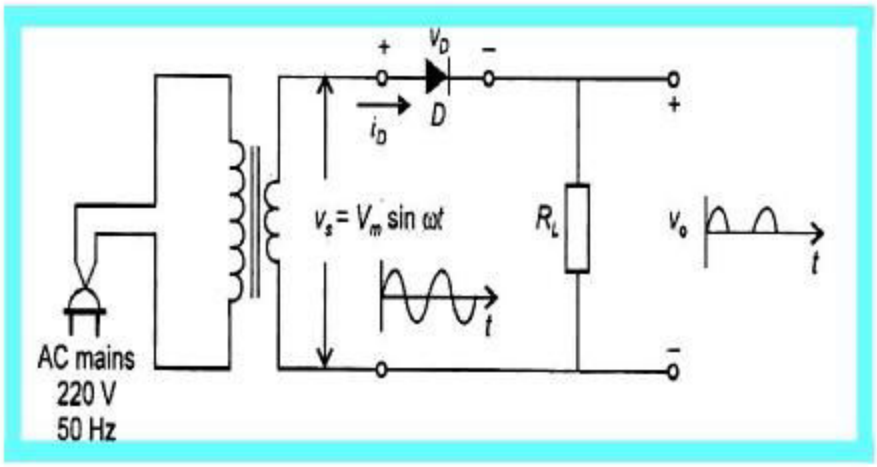


Figure 1: Half wave rectifier

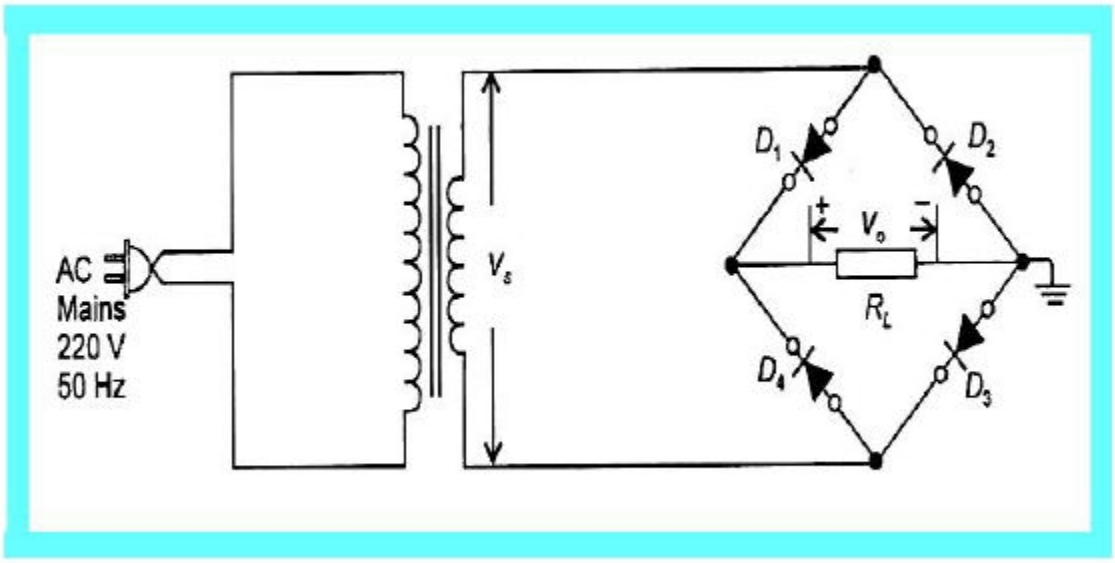


Figure 2 : Full wave bridge rectifier

Procedure:

1. Connect the circuit as shown in figure.

2. Apply A.C. supply through transformer; 3. Find the current through load resistance.
3. Observed voltage wave across the load on CRO.
4. Find the value of ripple factor and efficiency.

Calculation for Half Wave Rectifier:

Ripple factor

$$r = \frac{\text{rms value of the ac components of wave}}{\text{average or dc value}}$$

$$r = \sqrt{\left(\frac{I_{rms}}{I_{dc}}\right)^2 - 1} = \sqrt{\left(\frac{I_m/2}{I_m/\pi}\right)^2 - 1} = 1.21$$

Efficiency of half wave rectifier

Efficiency, is the ratio of the dc output power to ac input power

$$\eta = \frac{P_{dc}}{P_{ac}} = \frac{I_{dc}^2 R_L}{I_{rms}^2 (R_L + r_f)} = \left(\frac{I_{dc}}{I_{rms}}\right)^2 \frac{R_L}{R_L + r_f}$$

$$= \left(\frac{I_m/\pi}{I_m/2}\right)^2 \frac{R_L}{R_L + r_f} = 0.406 \frac{R_L}{R_L + r_f}$$

$$= \frac{40.6}{1 + r_f/R_L}\%$$

Calculation for Full Wave Bridge Rectifier:

Ripple Factor

The ripple factor for a Full Wave Rectifier is given by

$$r = \sqrt{\left(\frac{I_{rms}}{I_{dc}}\right)^2 - 1} = \sqrt{\left(\frac{I_m/\sqrt{2}}{2I_m/\pi}\right)^2 - 1} = \sqrt{\left(\frac{\pi}{2\sqrt{2}}\right)^2 - 1}$$

Efficiency

Efficiency, is the ratio of the dc output power to ac input power.

Results:

Voltage wave form across the load:

Ripple factor:

Efficiency:

Learning Outcomes:

Experiment No. -7

Aim:

Realization of desired wave shapes using clipper and clamper circuits

Apparatus and Components Required:

S. No.	Apparatus and Components Required	Quantity
1.	0.1 MFD capacitor	01
2.	100 K ohm resistance	01
3.	10 K ohm resistance	01
4.	1 K ohm resistance	01
5.	Diodes IN4007	02
6.	DC Power supply	01
7.	Breadboard	01
8.	Connecting wires	

Theory:

The circuit with which the waveform is shaped by removing (or clipping) a portion of the input signal without distorting the remaining part of the alternating waveform is called a *clipper*. Clipping circuits are also referred to as voltage (or current) limiters, amplitude selectors, or slicers. These circuits find extensive use in radars, digital computers, radio and television receivers etc.

In a clipping circuit, the output voltage will be proportional to the input voltage as long as the input lies between the specified reference levels. Outside this range, the output is clipped - it remains essentially constant, no longer dependent on the input. Clipping circuits find important uses in wave shaping and signal processing applications.

Often in the development of electronic circuits it is required that voltages be limited in some manner to avoid circuit damage. Furthermore, the limiting or clipping of voltages can be very useful in the development of wave-shaping circuits. A typical clipper circuit is shown in Figure 1. In this circuit the output voltage can never be greater than 3 V. The ideal diode becomes forward biased at Vo equal to 3 V and this ties the output directly to the 3 V supply. The waveform can be

clipped on the negative side by placing the series combination of a diode and power supply in parallel with the diode and power supply already shown.

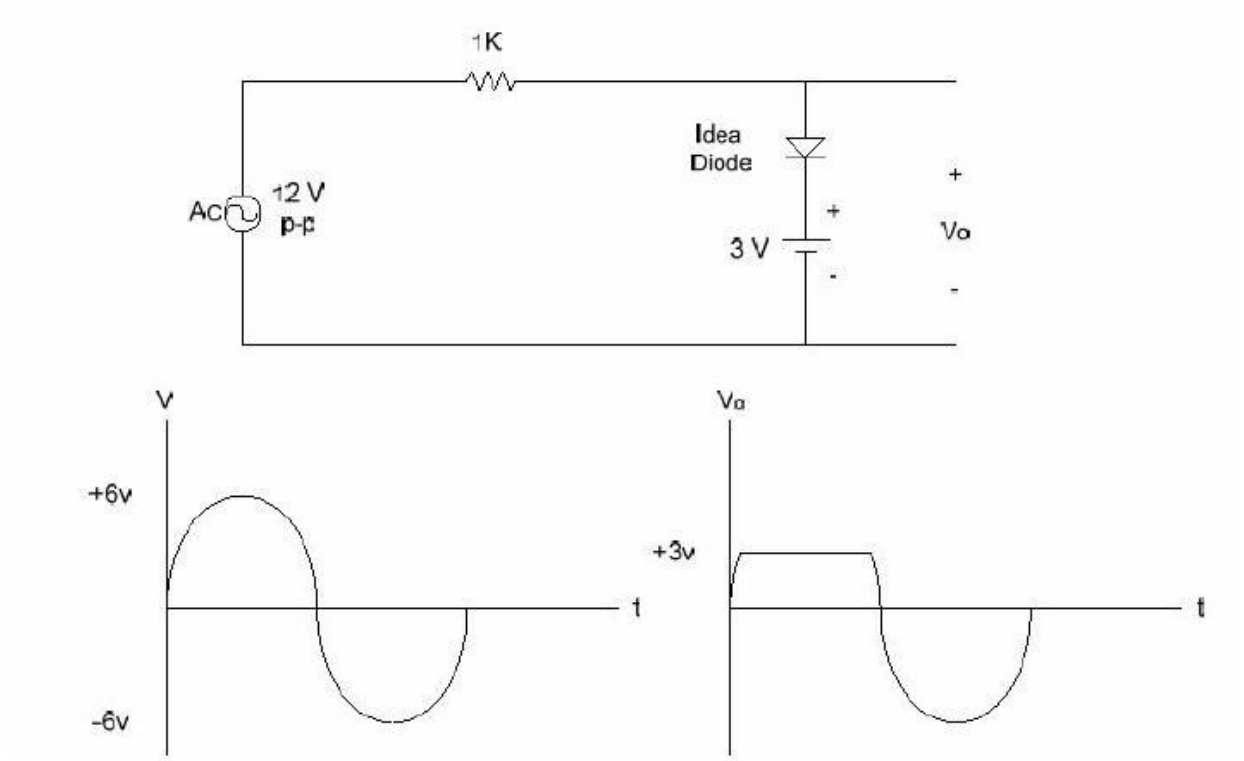


Figure 1: Diode clipping circuit showing input and output waveforms

While clipper circuits are concerned primarily with limiting or cutting off part of the waveform, clampers are used primarily to shift the DC level. For example, if we have a clock signal that swings between 0v and 5V but our application requires a clock signal from -5V to 0V, we can provide the proper DC offset with a passive clamper circuit. A typical clamper circuit is shown in Figure 2. For this circuit to work properly the pulse width needs to be much less than the RC time constant of 10 ms. The input square wave with a frequency of 1 KHz and a pulse width of 0.5 ms meets this requirement. The diode and power supply as shown will prevent the output voltage from exceeding 3 V (i.e., all of the region above 3 V can be viewed as a forbidden region for output voltage). Because of the time constant requirement the voltage across the capacitor cannot change significantly during the pulse width, and after a short transient period the voltage across the capacitor reached a steady state offset value. The output voltage is simply the input voltage shifted by this steady state offset. Also, observe that the peak-to-peat output voltage is equal to the peak-to-peak input voltage. This is true because the voltage across the capacitor cannot change instantaneously and the full change of voltage on the input side of the capacitor will likewise be seen on the output side of the capacitor.

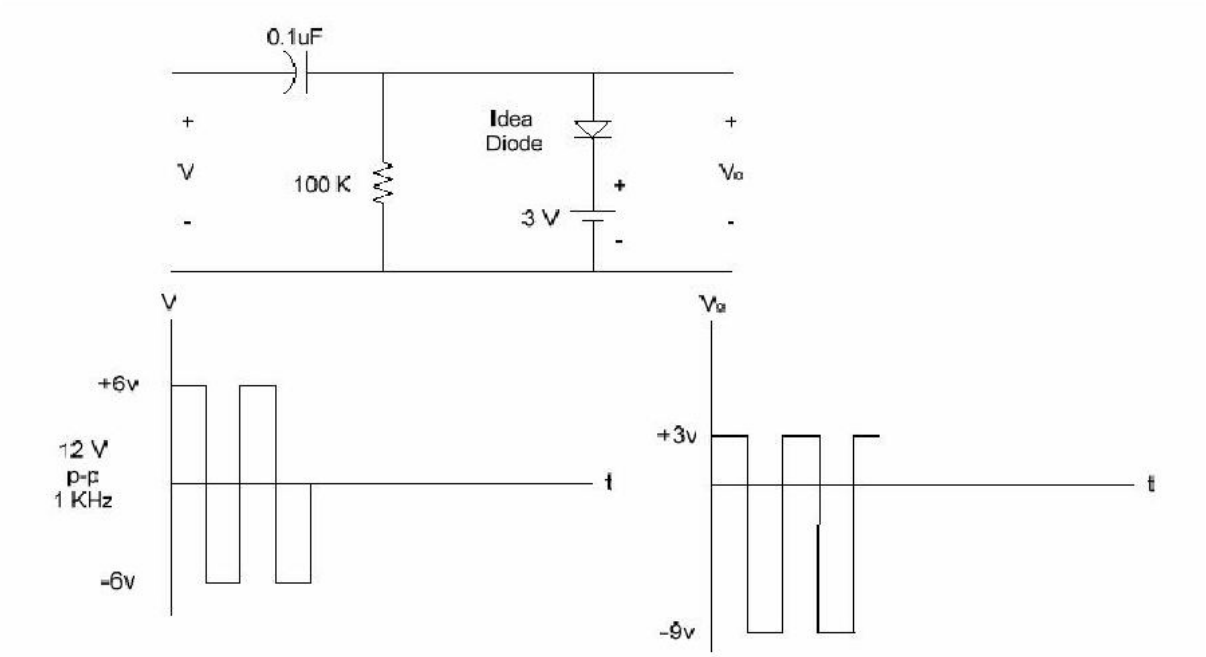


Figure 2: Diode clamper circuit showing input and output waveforms

Procedure:

A. Clipper Circuits:

1. Consider the clipper circuit in Fig.3, draw the input and output voltage waveforms in same plot vi(t)=10sin(200πt), R=1kΩ and RL=47kΩ.

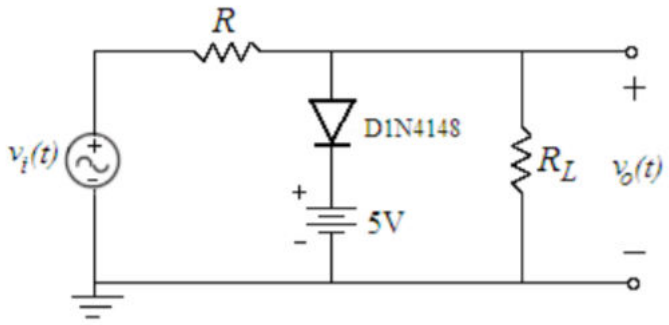


figure_3

2. Consider the clamper circuit in Fig.4, draw the input and output voltage waveforms, assume vi(t)=10sin(200πt) and C=47μF.

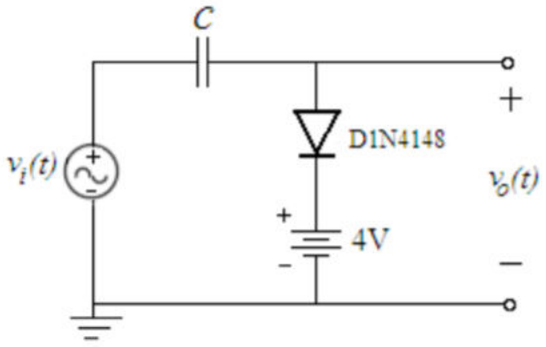


*figure_* **4**

Result

Learning Outcome

Experiment No.- 8

Aim:

To plot input characteristic of a BJT in Common Emitter configuration.

Apparatus and Components Required:

S. No.	Apparatus and Components Required	Quantity
1.	Transistor BC547	01each
2.	Resistors : 1K and 10K	01each
3.	DC power supply	01
4.	Digital multi-meters	01
5.	Breadboard	

Theory:

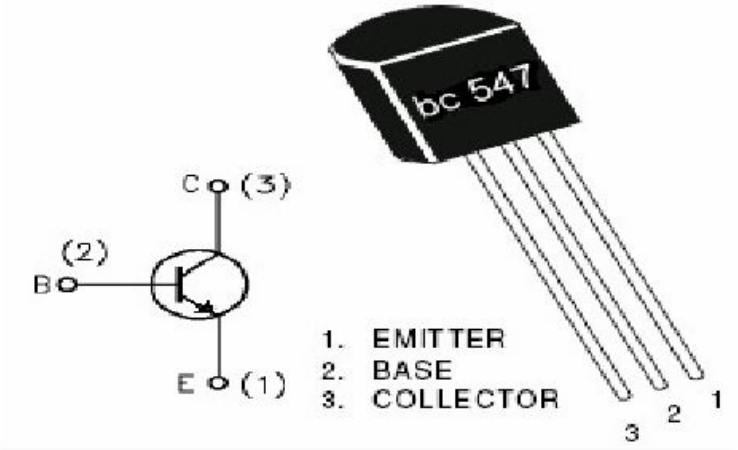
A transistor is a three terminal device. The terminals are emitter, base, collector. In common emitter configuration, input voltage is applied between base and emitter terminals and output is taken across the collector and emitter terminals. Therefore the emitter terminal is common to both input and output ports.

The input characteristic resembles that of a forward biased diode curve. This is expected since the Base-Emitter junction of the transistor is forward biased. As compared to CB arrangement IB increases less rapidly with VBE. Therefore input resistance of CE circuit is higher than that of CB circuit.

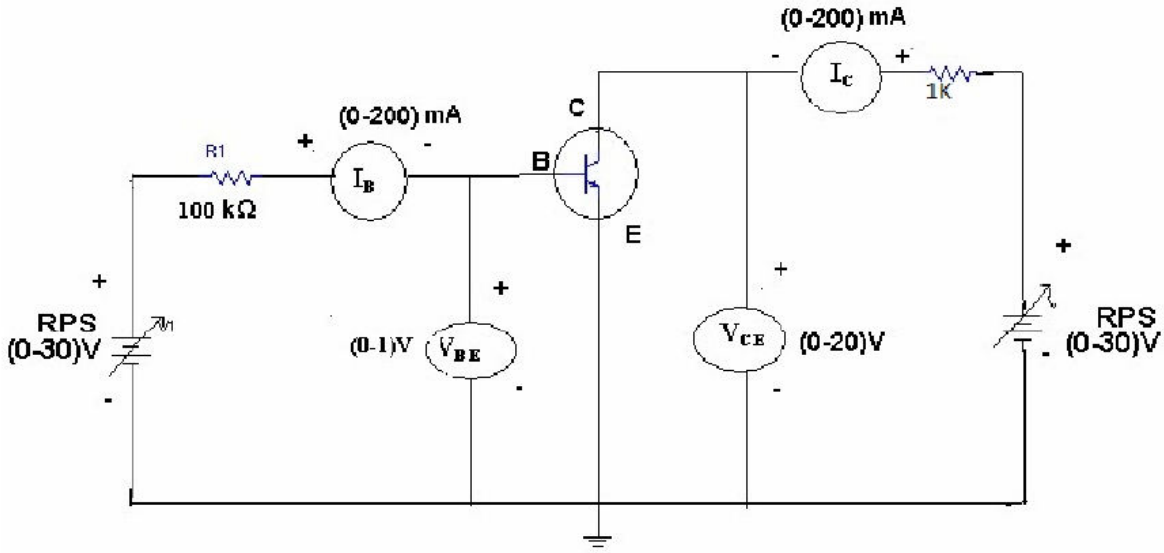
The output characteristics are drawn between Ic and VCE at constant IB. the collector current Ic varies with VCE upto few voltage only. After this the collector current becomes almost constant and independent of VCE. The value of VCE upto which the collector current changes with VCE is known as knee voltage. The transistor always operates in the region above knee voltage. Ic is always constant and is approximately equal to IB.

The current amplification factor of CE configuration is given by

$$\beta = \Delta I_C / \Delta I_B$$



Circuit Diagram:



INPUT CHARACTERISTIC

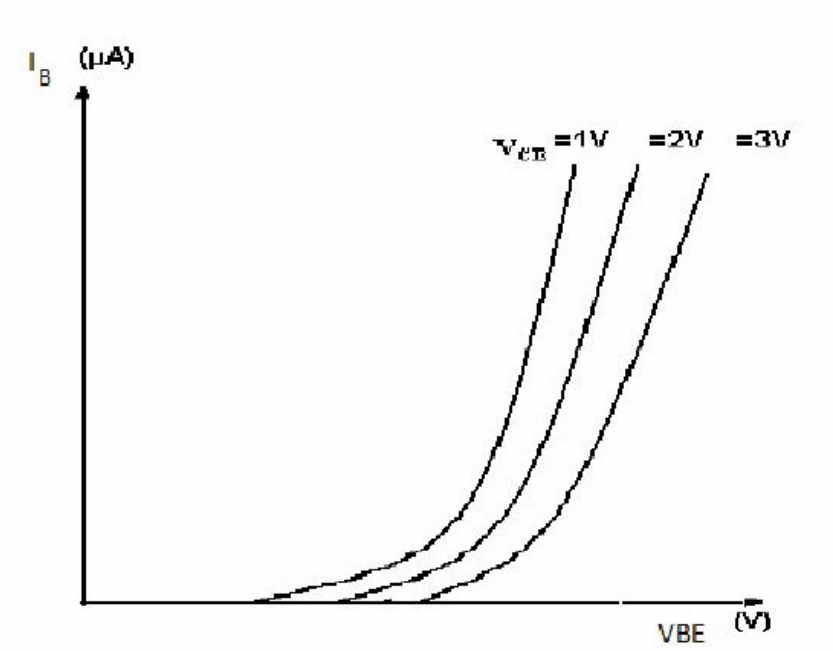
Procedure:

1) Connect the circuit as per the circuit diagram
2) For plotting the input characteristics the output voltage VCE is kept constant at 1V and for different values of V_{BE} . Note down the values of I_B
3) Repeat the above step by keeping V_{CE} at 2V and 4V.
4) Tabulate all the readings.
5) Plot the graph between VBE and IB for constant V_{CE}.

Observation Table:

S. No.	V_{CE}		V_{CE}		V_{CE}	
	V_{BE}	I_B	V_{BE}	I_B	V_{BE}	I_B

MODEL GRAPH



INPUT CHARACTERISTIC GRAPH

Procedure:

1) Connect the circuit as per the circuit diagram.
2) For plotting the output characteristics the input current IB is kept constant at 10μA and for different values of VCE note down the values of IC.
3) Repeat the above step by keeping IB at 20 μA 40 μA.

Result:

Learning Outcome:

Experiment No.- 9

Aim:

To plot output characteristic of a BJT in Common Emitter Configuration.

Apparatus and Components Required:

S. No.	Apparatus and Components Required	Quantity
1.	Transistor BC547	01each
2.	Resistors : 1K and 10K	01each
3.	DC power supply	01
4.	Digital multi-meters	01
5.	Breadboard	

Theory:

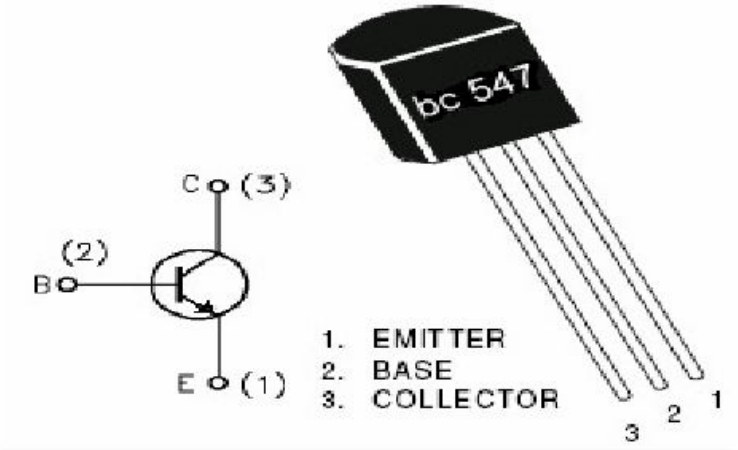
A transistor is a three terminal device. The terminals are emitter, base, collector. In common emitter configuration, input voltage is applied between base and emitter terminals and output is taken across the collector and emitter terminals. Therefore the emitter terminal is common to both input and output

The input characteristic resembles that of a forward biased diode curve. This is expected since the Base-Emitter junction of the transistor is forward biased. As compared to CB arrangement IB increases less rapidly with VBE. Therefore input resistance of CE circuit is higher than that of CB circuit.

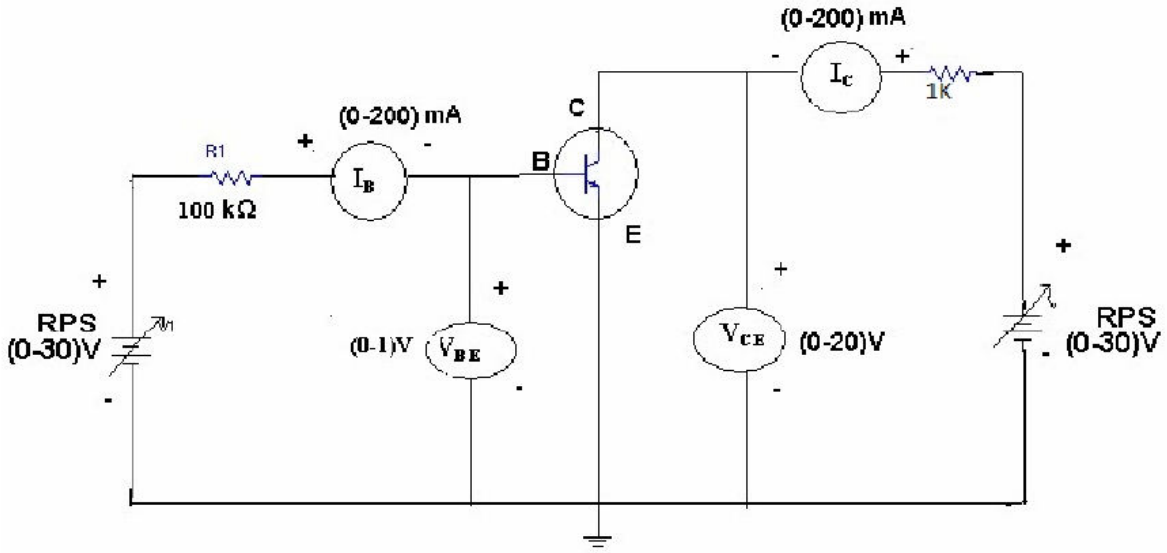
The output characteristics are drawn between Ic and VCE at constant IB. the collector current Ic varies with VCE upto few voltage only. After this the collector current becomes almost constant and independent of VCE. The value of VCE upto which the collector current changes with VCE is known as knee voltage. The transistor always operates in the region above knee voltage. Ic is always constant and is approximately equal to IB.

The current amplification factor of CE configuration is given by

$$\beta = \Delta I_C / \Delta I_B$$



Circuit Diagram:



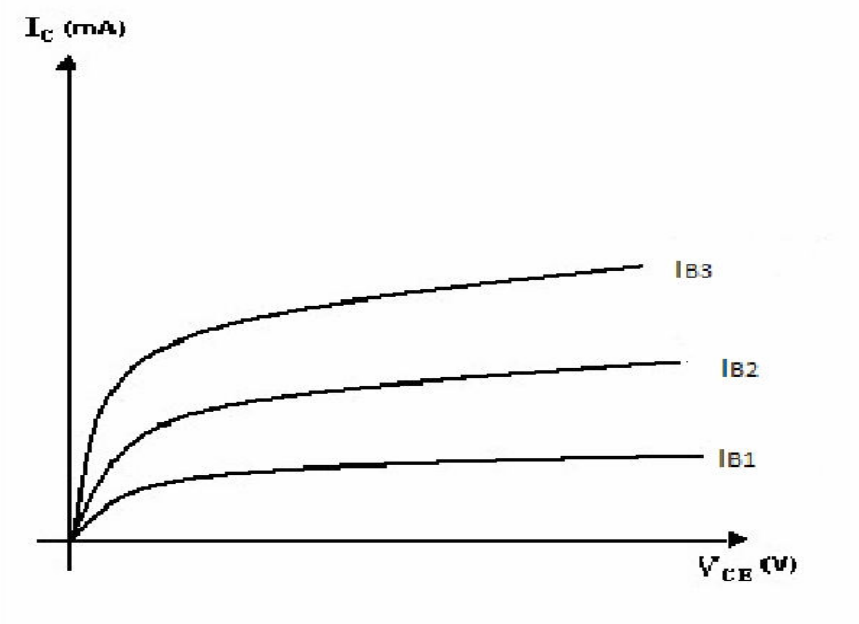
OUTPUT CHARACTERISTIC

Procedure:

1) Connect the circuit as per the circuit diagram.
2) For plotting the output characteristics the input current IB is kept constant at 10μA and for different values of VCE note down the values of IC.
3) Repeat the above step by keeping IB at 20 μA 40 μA.

S. No.	I_{B1}=10µA		I_{B2}=20µA		I_{B3}=40µA	
	VCE(mv)	**IC(mA)**	**VCE(mv)**	**IC(mA)**	**VCE(mv)**	**IC(mA)**
1.						
2.						

MODEL GRAPH



OUTPUT CHARACTERISTIC GRAPH

Result:

Learning Outcome:

EXPERIMENT NO: 10

AIM: **To plot input characteristic of a BJT in Common Base Configuration.**

Apparatus and Components Required:

S. No.	Apparatus and Components Required	Quantity
1.	Transistor	01
2.	Resistors : 1K	02
3.	DC power supply	01
4.	Digital multi-meters	01
5.	Breadboard	

Theory: Circuit Configurations: A transistor has three terminals hence when it is connected in a circuit one of its terminals in common to input and output parts of the circuits. Three circuits configurations in which a transistor can be connected are discussed below (discussion has been limited to NPN transistor):

Common Base Configuration:

The Common Base (CB) (Figure 14.1) circuit characteristics constitute a family of static characteristics plots of collector current versus collector-base voltage for several values of emitter current

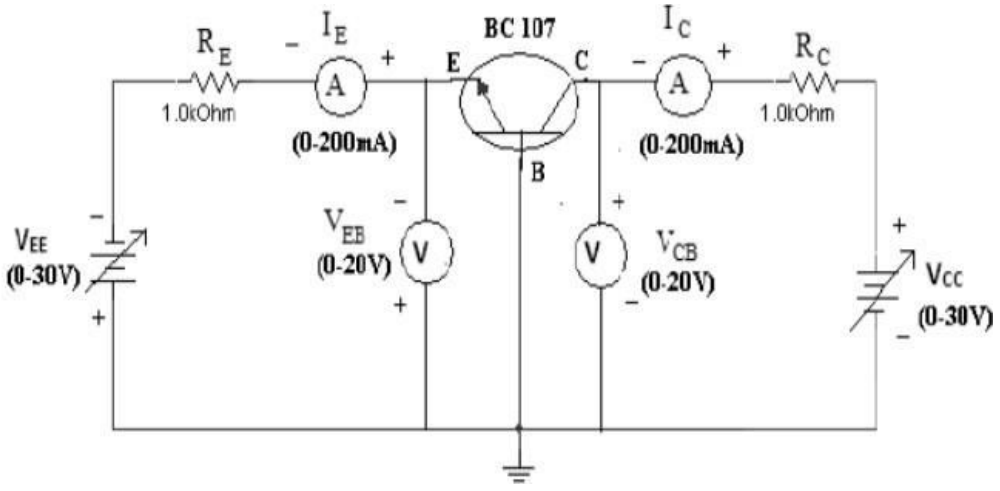


Fig: 13.1

Here the input is given between base and emitter and output is taken between collector and base as shown in fig13.1. Fig.13.1 shows the wiring diagram for practically determining the characteristics in the common base configuration.

Observation Table

13.1

Input Characteristics				
V_{EE} (Volts)	V_{CB} = 0V		V_{CB} = 4V	
	V_{EB} (Volts)	I_E (mA)	V_{EB} (Volts)	I_E (mA)

For input characteristics in the common base configuration the collector Vc is kept constant at a certain value. The emitter voltage V_e is varied and corresponding value of emitter current I_e are observed. Fig.13.2 shows the practical curves obtained for various transistors. From these curves we observe the following:

1. The curves start from zero.
2. The emitter current increases sharply at an emitter voltage which is about 0.2V for a Ge and about 0.6V for a Si transistor can be obtained as follows: $R_i = V_e/I_e$, for a certain of Vc.

Procedure: - Input Characteristics

1. Connect the circuit as shown in the circuit diagram.
2. Keep output voltage V_{CB} = 0V by varying V_{CC}.
3. Varying V_{EE} gradually, note down emitter current I_E and emitter-base voltage(V_{EE}).
4. Step size is not fixed because of nonlinear curve. Initially vary V_{EE} in steps of 0.1 V. Once the current starts increasing vary V_{EE} in steps of 1V up to 12V.
5. Repeat above procedure (step 3) for V_{CB} = 4V.

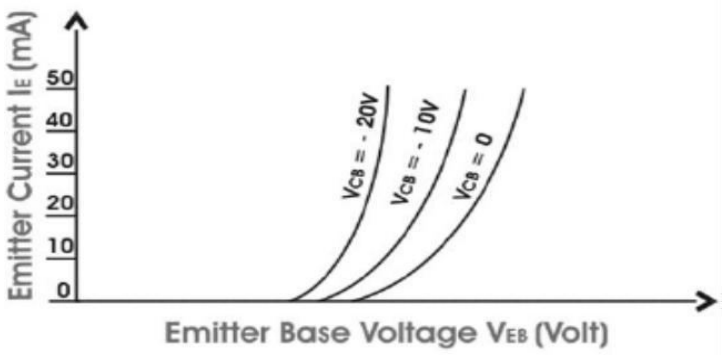


Fig: 13.2

RESULT:

LEARNING OUTCOMES:

PRECAUTION:

1. While performing the experiment do not exceed the ratings of the transistor. This may lead to damage the transistor.
2. Connect voltmeter and ammeter in correct polarities as shown in the circuit diagram.
3. Do not switch ON the power supply unless you have checked the circuit connections as per the circuit diagram.
4. Make sure while selecting the emitter, base and collector terminals of the transistor.

EXPERIMENT NO: 11

AIM: To plot output characteristic of a BJT in Common Base Configuration

Apparatus and Components Required

S. No.	Apparatus and Components Required	Quantity
1.	Transistor	01
2.	Resistors : 1K	02
3.	DC power supply	01
4.	Digital multi-meters	01
5.	Breadboard	

Theory: Circuit Configurations: A transistor has three terminals hence when it is connected in a circuit one of its terminals in common to input and output parts of the circuits. Three circuits configurations in which a transistor can be connected are discussed below (discussion has been limited to NPN transistor):

Common Base Configuration: The Common Base (CB) (Figure 15.1) circuit characteristics constitute a family of static characteristics plots of collector current versus collector-base voltage for several values of emitter current

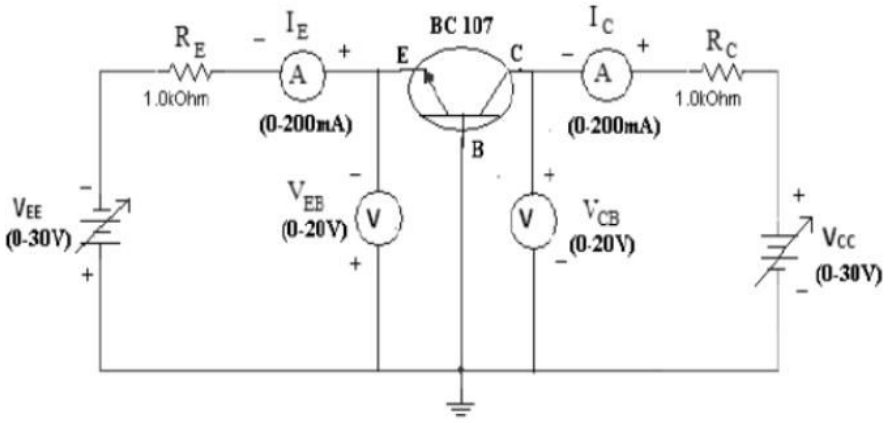


Fig: 14.1

Here the input is given between base and emitter and output is taken between collector and base as shown in fig 14.1. Fig.14.1 shows the wiring diagram for practically determining the characteristics in the common base configuration

Observation Table 14.1

Output Characteristics						
V_{CC} (Volts)	I_E = 0mA		I_E = 5 mA		IE = 10mA	
	V_{CB} (Volts)	I_C (mA)	V_{CB} (Volts)	I_C (mA)	V_{CB} (Volts)	I_C (mA)

For the output characteristics of a transistor in common base configuration, the emitter current Ie is kept constant at a certain value. The collector variations corresponding to variations of the collector voltages are observed. Fig. 14.2 shows the practical curves for various transistors. From the curves, we observe as follows:

1. The curves start from a point 0 instead of zero.

2. This point is about 0.2V for a Ge. Transistor and about 0.6V in case of a Si transistor.

3. Point 0 is of polarity to the usual polarity of collector voltage.

4. This point 0 is nearly same for all values of emitter current. This output resistance of a transistor in common base configuration can be determined as follows: $R_0 = V_c/I_c$, for a certain of I_e. The current gain can also be calculated as: $\alpha = I_c/I_e$, for a certain value of V_c.

Procedure: - Output Characteristics
1. Connect the circuit as shown in the circuit diagram.
2. Keep emitter current I_E = 5mA by varying V_{EE}.
3. Varying V_{CC} gradually in steps of 1V up to 12V and note down collector current I_C and collector-base voltage (V_{CB}). 4. Repeat above procedure (step 3) for I_E = 10mA.
Repeat above procedure (step 3) for I_E = 10mA.

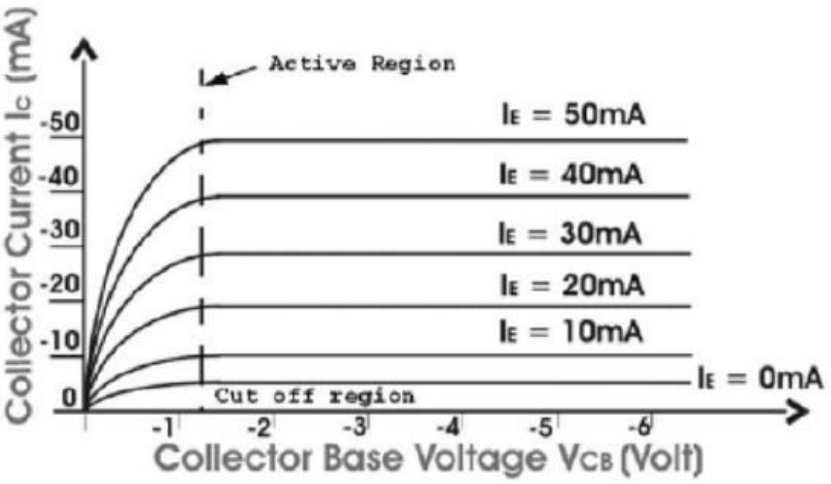


Fig. 14.2

RESULT:

LEARNING OUTCOMES

PRECAUTION:

1. While performing the experiment do not exceed the ratings of the transistor. This may lead to damage the transistor.

2. Connect voltmeter and ammeter in correct polarities as shown in the circuit diagram.

3. Do not switch ON the power supply unless you have checked the circuit connections as per the circuit diagram.

4. Make sure while selecting the emitter, base and collector terminals of the transistor

EXPERIMENT NO : 12

AIM:

To realize adder and subtractor circuits using Op-Amp IC 741.

APPARATUS AND COMPONENTS REQUIRED:

Sl. No.	Apparatus and Components	Specification	Quantity
1.	DC Regulated Power Supply	+/- 12 V Dual Supply, 0-5V, 0-10V	01
2.	Multimeter	Digital	01
3.	Bread Board	-	01
4.	Connecting Wires	-	-
5.	Op-Amp	IC741	01
6.	Resistance	1KΩ	04
7.	Resistance	10KΩ	01

THEORY:

ADDER:

Op-amp can be used to design a circuit whose output is the sum of several input signals. Such a circuit is called a summing amplifier or an adder. Summing amplifier can be classified as inverting and non-inverting summer depending on the inputs applied to inverting and non-inverting terminals respectively. Figure 1 shows a non-inverting adder with *n* inputs. Here the output will be the linear summation of input voltages. The circuit can also be used as summing amplifier, scaling amplifier, or as an averaging amplifier also.

From the circuit of adder, it can be noted that at pin3, $\mathbf{I_1+I_2+I_3+\ldots\ldots\ldots\ldots I_n=0}$

$$\frac{V_a - V_1}{R} + \frac{V_a - V_2}{R} + \frac{V_a - V_3}{R} \ldots\ldots\ldots\ldots \frac{V_a - V_n}{R} = 0$$

$$nV_a - \frac{(V_1 + V_2 + V_3 + \ldots\ldots\ldots + V_n)}{R} = 0$$

$$V_a = \frac{V_1 + V_2 + V_3 + \ldots\ldots\ldots\ldots + V_n}{R} = 0$$

$$V_O = \left(1 + \frac{R_f}{R_1}\right) V_a$$

$$V_O = \left(1 + \frac{R_f}{R_1}\right)\left(\frac{V_1 + V_2 + V_3 + \ldots\ldots\ldots\ldots + V_n}{n}\right)$$

$$= 1 + (n-1)\left(\frac{V_1 + V_2 + V_3 + \ldots\ldots\ldots\ldots + V_n}{n}\right)$$

$$= n\left(\frac{V_1 + V_2 + V_3 + \ldots\ldots\ldots\ldots + V_n}{n}\right)$$

$$V_O = V_1 + V_2 + V_3 + \ldots\ldots\ldots\ldots + V_n$$

The output voltage should be equal to the sum of all the input voltages.

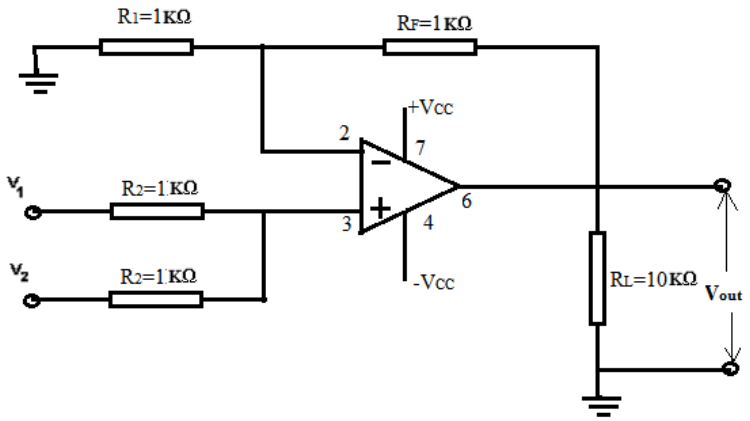


Figure 1: Adder circuit

PROCEDURE:

1. Connect the adder circuit as shown in Figure1.
2. Apply the input voltages V_1, V_2 from DC power supply (Negative of the power supply should be connected with the ground).
3. Biasing of the Op-amp should be done with correct polarity of Vcc(+/-12V).
4. Measure the output voltage across R_L with the help of DMM.

OBSERVATION TABLE:

	V_1 (V)	V_2 (V)	V_{out} (V)	V_1+V_2 (V)
Theoretical values				
Measured Values				

SUBTRACTOR:

A subtractor is a circuit that gives the difference of the two inputs, $V_o = V_2 - V_1$, where V_1 and V_2 are the inputs. By connecting one input voltage V_1 to inverting terminal and another input voltage V_2 to the non-inverting terminal, we get the resulting circuit as the Subtractor. This is also called as differential or difference amplifier using op-amps.

Output of a differential amplifier (subtractor) is given as

$$\mathbf{V_o = (-R_f/R_1)\ (V_1-V_2)}$$

If all external resistors are equal in value, then the gain of the amplifier is equal to -1. The output voltage of the differential amplifier with a gain of -1 is

$$\mathbf{V_o = (V_2-V_1)}$$

Thus the output voltage V_o is equal to the voltage V_2 applied to the non – inverting terminal minus the voltage V_1 applied to the inverting terminal.

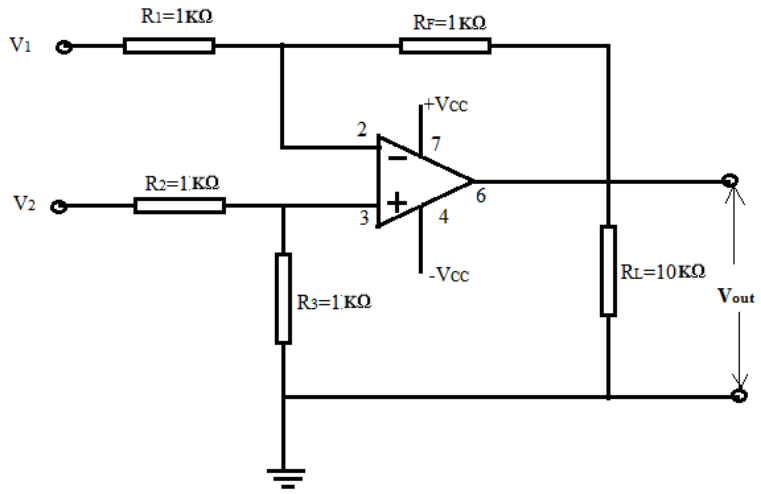


Figure 2: Subtractor circuit

PROCEDURE:

1. Connect the subtractor circuit as shown in Figure 2.
2. Apply the input voltages V_1, V_2 from DC power supply (Negative of the power supply should be connected with the ground).
3. Biasing of the Op-amp should be done with correct polarity of Vcc(+/-12V).
4. Measure the output voltage across R_L with the help of DMM.

OBSERVATION TABLE:

	V_1 (V)	V_2 (V)	V_{out} (V)	V_2-V_1 (V)
Theoretical values				
Measured Values				

RESULT:

LEARNING OUTCOMES:

Experiment No.- 13

Aim:

To study Zener voltage regulator and calculate percentage regulation for line regulation and load regulation

Apparatus and Components Required:

S. No.	Apparatus and Components Required	Quantity
1.	Zener Doide (V_Z=5.1 V)	01
2.	Variable regulated DC power supply	01
3.	Resistances (100 Ω / 0.5W for series resistance Rs)	01
4.	Variable resistance Pot (10K)	01
5.	Multimeter	01
6.	Connecting wires	

Theory:

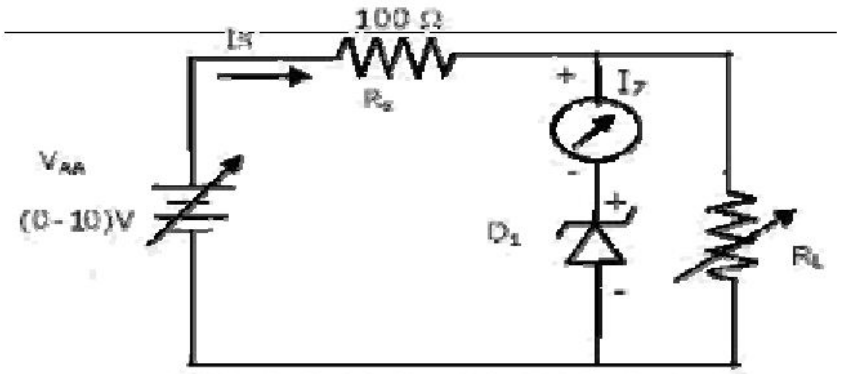
Voltage Regulator:

A voltage regulator circuit is required to maintain a constant dc Output voltage across the load terminals in spite of the variation:

- Variation in input mains voltage
- Change in the load current

The voltage regulator circuit can be designed using zener diode. For that purpose, zener diode is operated always in reverse biased condition. Here, zener is operated in breakdown region and is used to regulate the voltage across a load when there are variations in the supply voltage or load current.

The general circuit diagram for the zener voltage regulator is shown below



Zener Diode in Reverse Bias Condition

It consists of a current limiting resistor RS connected in series with the input voltage V_{AA} and zener diode is connected in parallel with the load RL in reverse biased condition. The output voltage is always selected with a breakdown voltage Vz of the diode.

The input source current, IS = IZ + IL…….. (1)

The drop across the series resistance, Rs = Vin - Vz …….. (2)
And current flowing through it, Is = (Vin - VZ) / RS …….. (3) From equation (1) and (2), we get, (Vin - Vz)/Rs = Iz +IL …… (4)

Regulation with a varying input voltage (line regulation): It is defined as the change in regulated voltage with respect to variation in line voltage. The minimum value of input after which regulation will start is given by the following formula.

$$\mathbf{R_L * Vin(Min)/(R_L + R_s) > V_Z.}$$

Once the zener enter into breakdown, the output voltage will be maintained at V_Z. Since loads resistance is constant so, the load current remains constant and as the input voltage increases, form equation (3) Is (current in series resistance) also varies accordingly. Therefore, zener current Iz will increase. The extra voltage is dropped across the Rs. Since, increased Iz will still have a constant Vz and Vz is equal to Vout. The output voltage will remain constant.
The maximum value of Vin is decide by the I_{Zmax} as as given below.

$$\mathbf{Vin(Max) - Vz = R_S(I_L + I_{Zmax})}$$
$$\mathbf{I_L = V_Z/R_L}$$

Regulation with the varying load (load regulation): It is defined as change in load voltage with respect to variations in load current. To calculate this regulation, input voltage is constant and

output voltage varies due to change in the load resistance value. The minimum value of load resistance after which regulation will start is given by the following formula.

$$R_{LMIN}*Vin/(R_{LMIN} + R_s) > V_Z.$$

The left side of the equation (4) is constant as input voltage Vin, IS and Rs is constant. As load current changes due to change in the value of resistance R_L, the zener current Iz will also change but in opposite way such that the sum of Iz and IL will remain constant. When Load resistance is

more then the R_{LMIN}, load current decreases since output voltage is Constant at V_Z. Due to this Zener current must increase in order to satisfy eq. 1. The maximum value of load resistance is decided by the Maximum current capability of the zener i.e. I_{ZMAX}

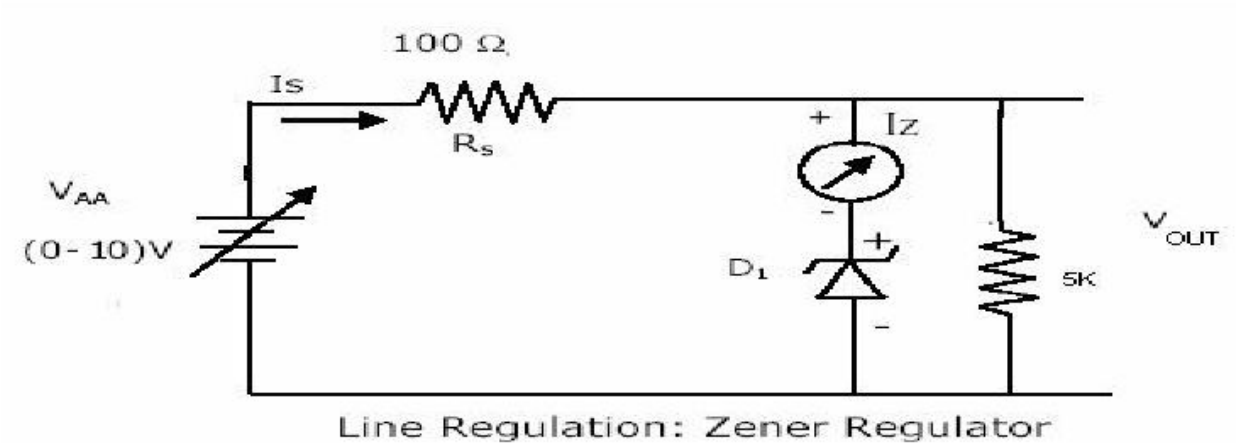
$$Vin- Vz = R_S(I_{LMin}+I_{Zmax})$$

$$I_{LMIN} = V_Z / R_{LMAX}$$

Procedure:

A) Line Regulation:

1. Make the connections as shown in figure below.



Line Regulation: Zener Regulator

1. Keep load resistance fixed value at 5K (By using variable resistance Pot); vary DC input voltage from 0V to 10V.
2. Note down output voltage and zener current.

Observation Table:

Vary input signal from 0 to 10 with step size of 1V and measure the output voltage and the current through the zener diode.

Then calculate the value of I_S and I_L using the formula given below and verify the equation 1.

S. No.	V_{AA} (Input Voltage)	V_{out} (Output voltage)	Zener Current (I_{Z-}) mA	I_L(mA)	I_s(mA)	%Regulation (use Eq. 5)

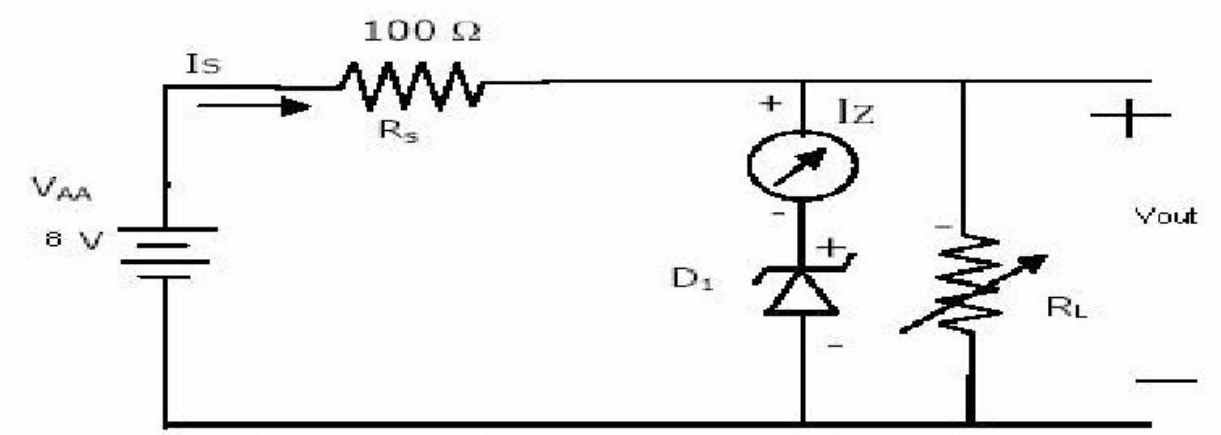
% Line Regulation: $\partial Vout/\partial V_{AA}$. (After the output is regulated) Eq. 5

$I_L=Vout/R_L$, $I_S=(V_{AA} - Vout)/R_s$,

Plot: Plot the Vout versus V_{AA} on graph sheet

B) Load Regulation:

1. For finding load regulation, make connections as shown in figure below.



2. Keep input voltage at 8V; vary load resistance value from minimum to Maximum

3. Note down output voltage and zener current

Observation Table:

Fixed the input voltage at 8V. Vary load resistance from Minimum to Maximum of the given 10K Pot, with step size of 50Ω in the range of (Minimum to 200 Ω), then with step of 100Ω till 5KΩ and measure the output voltage and the current through the zener diode.

S. No.	R_L (ohm)	V_o(output voltage)	Zener Current (I_z) mA	$I_L=(V_{out}/R_L)$	I_z+I_L	%Regulation (Use Eq. 6)

Calculate the $I_s= (8-5.1)/R_S$ Eq. 6

% Load Regulation = ∂Vout/∂I_L (After the output is regulated)

Plot: Plot the (a) Vout versus R_L and (b) Vout versus I_L on graph sheet.

Result:

Learning Outcomes: