Solar Cell Design Principles

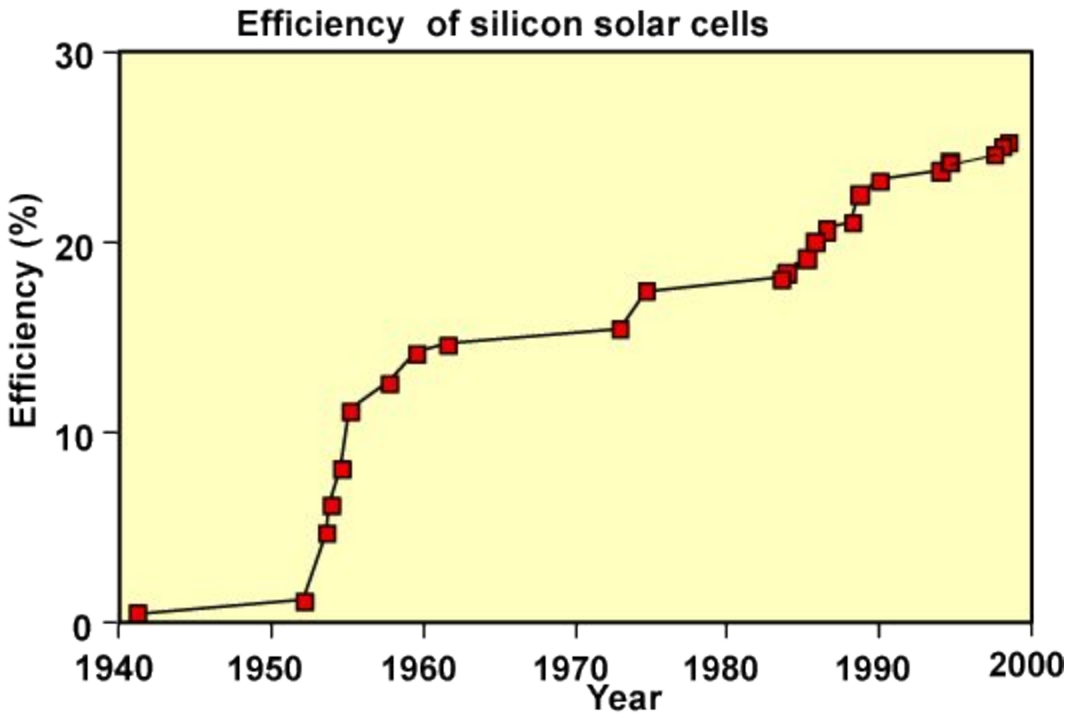
Solar Cell Design Principles

- Solar cell design involves specifying the parameters of a solar cell structure in order to maximize efficiency, given a certain set of constraints.

- These constraints are defined by the working environment in which solar cells are produced.

- In a commercial environment where the objective is to produce a competitively priced solar cell, the cost of fabricating a particular solar cell structure must be taken into consideration.

- In a research environment where the objective is to produce a highly efficient laboratory-type cell, maximizing efficiency rather than cost, is the main consideration.



The theoretical efficiency for photovoltaic conversion is in excess of 86.8%. However, the 86.8% figure uses detailed balance calculations and does not describe device implementation.

For silicon solar cells, a more realistic efficiency under one sun operation is about 29%. The maximum efficiency measured for a silicon solar cell is currently 24.7% under AM1.5G. The difference between the high theoretical efficiencies and the efficiencies measured from terrestrial solar cells is due mainly to two factors.

The first is that the theoretical maximum efficiency predictions assume that energy from each photon is optimally used, that there are no unabsorbed photons and that each photon is absorbed in a material which has a band gap equal to the photon energy. This is achieved in theory by modelling an infinite stack of solar cells of different band gap materials, each absorbing only the photons which correspond exactly to its band gap.

The second factor is that the high theoretical efficiency predictions assume a high concentration ratio. Assuming that temperature and resistive effects do not dominate in a concentrator solar cell, increasing the light intensity proportionally increases the short-circuit current.

Since the open-circuit voltage (V_{oc}) also depends on the short-circuit current, V_{oc} increases logarithmically with light level. Furthermore, since the maximum fill factor (FF) increases with V_{oc}, the maximum possible FF also increases with concentration. The extra V_{oc} and FF increase with concentration which allows concentrators to achieve higher efficiencies.

In designing such single junction solar cells, the principles for maximizing cell efficiency are:

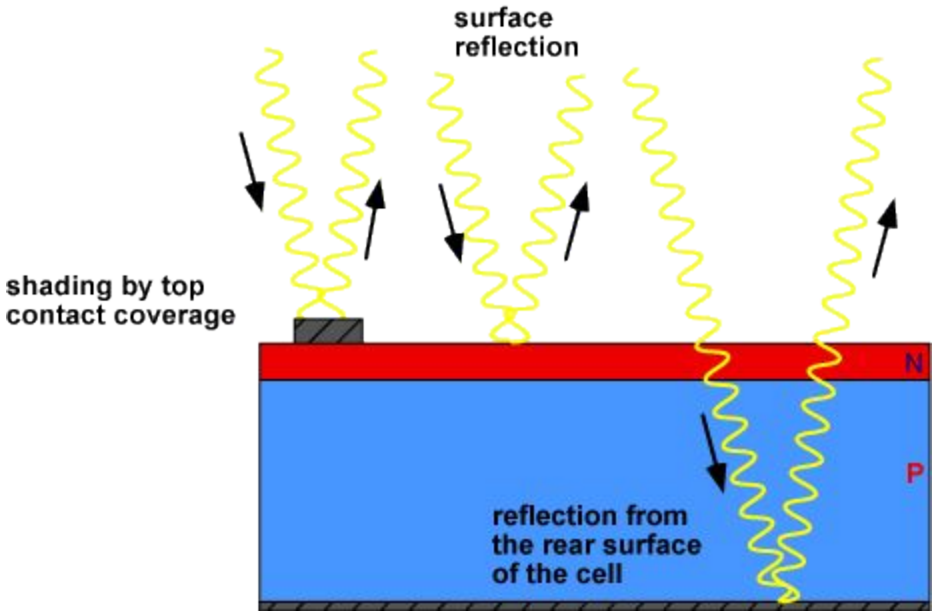
- increasing the amount of light collected by the cell that is turned into carriers;
- increasing the collection of light-generated carriers by the *p-n* junction;
- minimising the forward bias dark current;
- extracting the current from the cell without resistive losses.

Optical Losses

Optical losses mainly effect the power from a solar cell by lowering the short-circuit current.

Optical losses consist of light which could have generated an electron-hole pair, but does not, because the light is reflected from the front surface, or because it is not absorbed in the solar cell.

For the most common semiconductor solar cells, the entire visible spectrum (350 - 780 nm) has enough energy to create electron-hole pairs and therefore all visible light would ideally be absorbed.



Sources of optical loss in a solar cell.

There are a number of ways to reduce the optical losses:

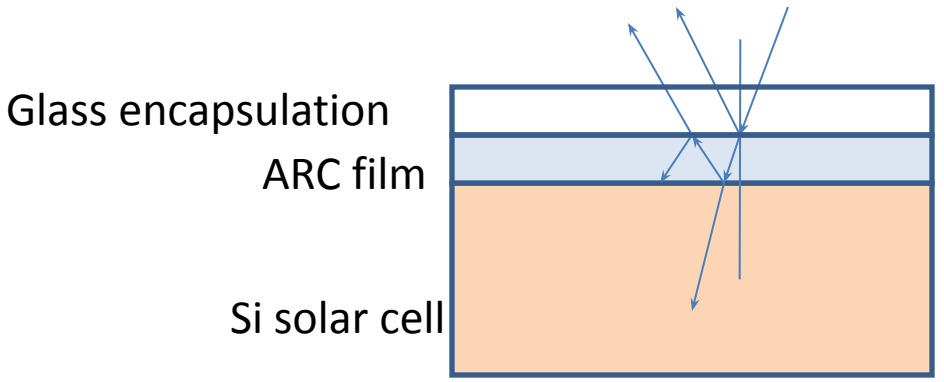
- Top contact coverage of the cell surface can be minimised (although this may result in increased series resistance);
- Anti-reflection coatings can be used on the top surface of the cell.
- Reflection can be reduced by surface texturing.
- The solar cell can be made thicker The solar cell can be made thicker to increase absorption (although light that is absorbed more than a diffusion length from the junction has a low collection probability and will not contribute to the short circuit current).
- The optical path length in the solar cell may be increased by a combination of surface texturing and light trapping.

The reflection of a silicon surface is over 30% due to its high refractive index. The reflectivity, R, between two materials of different refractive indices is determined by:

$$R = \left(\frac{n_0 - n_{Si}}{n_0 - n_{Si}}\right)^2$$

where n_0 is the refractive index of the surroundings and n_{Si} is the complex refractive index of silicon. For an unencapsulated cell $n_0 = 1$. For an encapsulated cell $n_0 = 1.5$. The refractive index of silicon changes with wavelength.

$$n_f = \sqrt{n_g n_{Si}}$$



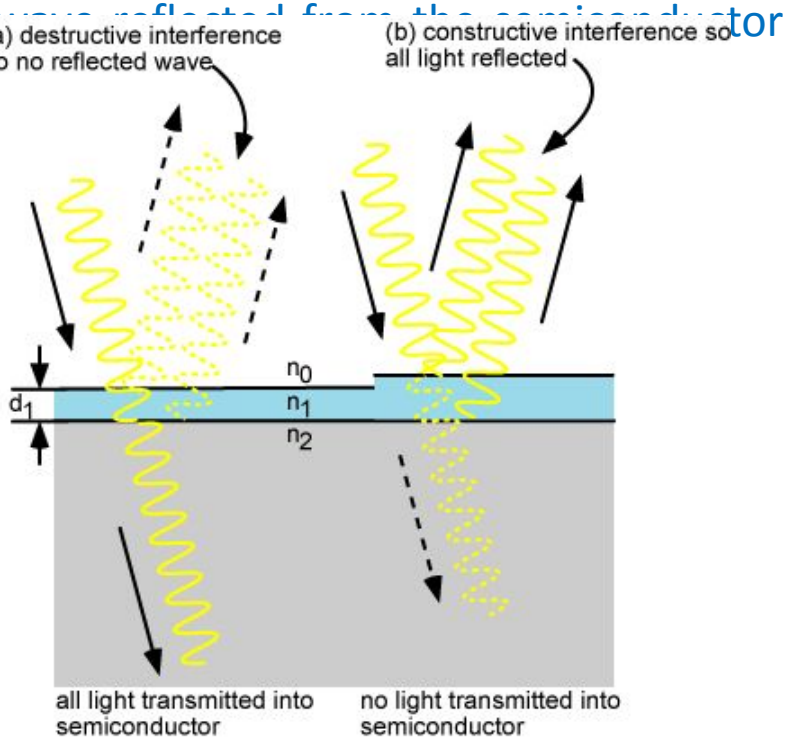
Anti-Reflection Coatings

- Bare silicon has a high surface reflection of over 30%. Bare silicon has a high surface reflection of over 30%. The reflection is reduced by texturing and by applying anti-reflection coatings (ARC) to the surface.

- Anti-reflection coatings on solar cells are similar to those used on other optical equipment such as camera lenses.

- They consist of a thin layer of dielectric material, with a specially chosen thickness so that interference effects in the coating cause the wave reflected from the anti-reflection coating top surface to be out of phase with the wave reflected from the semiconductor surfaces.

- These out-of-phase reflected waves destructively interfere with one another, resulting in zero net reflected energy. In addition to anti-reflection coatings, interference effects are also commonly encountered when a thin layer of oil on water produces rainbow-like bands of color.



The thickness of the anti-reflection coating is chosen so that the wavelength in the dielectric material is one quarter the wavelength of the incoming wave.

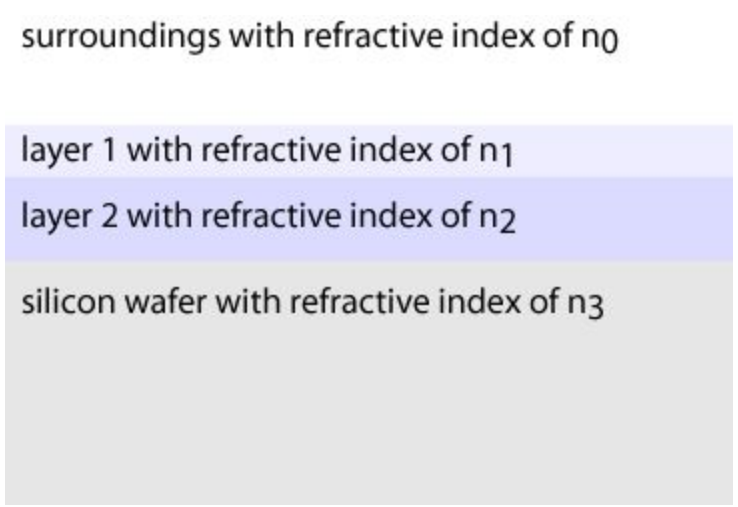
For a quarter wavelength anti-reflection coating of a transparent material with a refractive index n_1 and light incident on the coating with a free-space wavelength λ_0, the thickness d_1 which causes minimum reflection is calculated by:

$$d_1 = \frac{n_1}{4\lambda_0}$$

Four multicrystalline wafers covered with films of silicon nitride. The difference in color is solely due to the thickness of the film.

Double Layer Anti Reflection Coatings

A further reduction in reflectivity is achieved through a *double layer anti-reflection coating* (DLARC). Popular DLARC coatings are zinc sulfide (ZnS) with magnesium flouride (MgF) or layers of silicon nitride with varying refractive index. However, this is usually too expensive for most commercial solar cells.



Double layer anti-reflection film on silicon wafer. The layers are usually deposited on a textured substrate to decrease the reflectivity further.

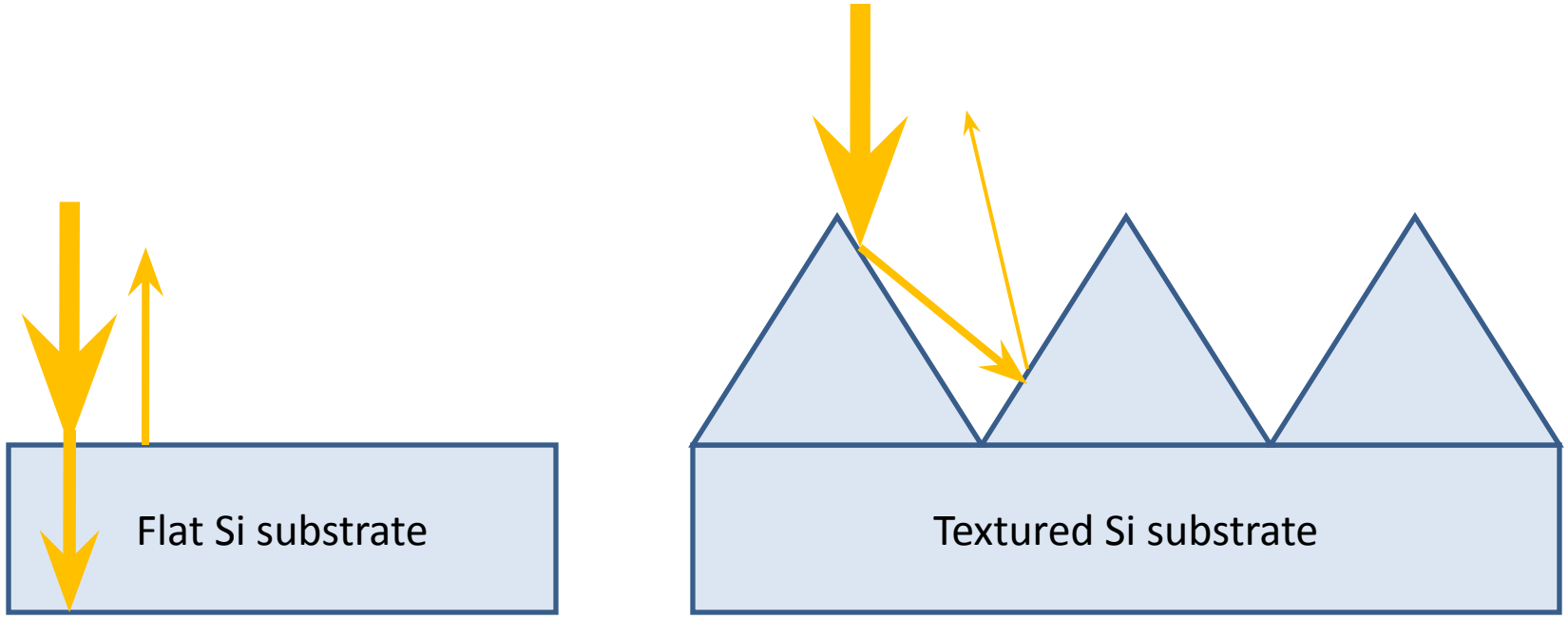
Question

Calculate the thickness required of the ARC film if the green wavelength (550 nm) is to be lest reflected from the surface of the Si (n_{Si}=3.8) solar cell.

Surface Texturing

Surface texturing, either in combination with an anti-reflection coating or by itself, can also be used to minimize reflection.

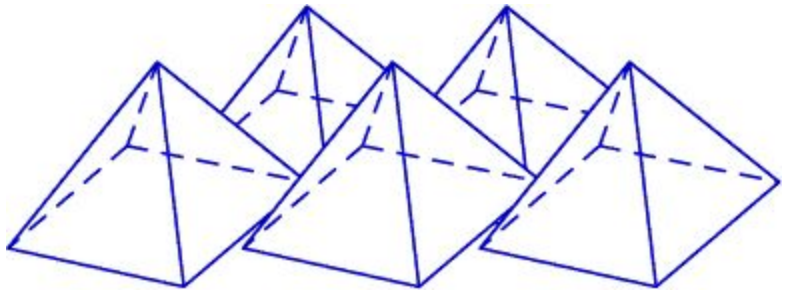
Any "roughening" of the surface reduces reflection by increasing the chances of reflected light bouncing back onto the surface, rather than out to the surrounding air.



Surface texturing can be accomplished in a number of ways.

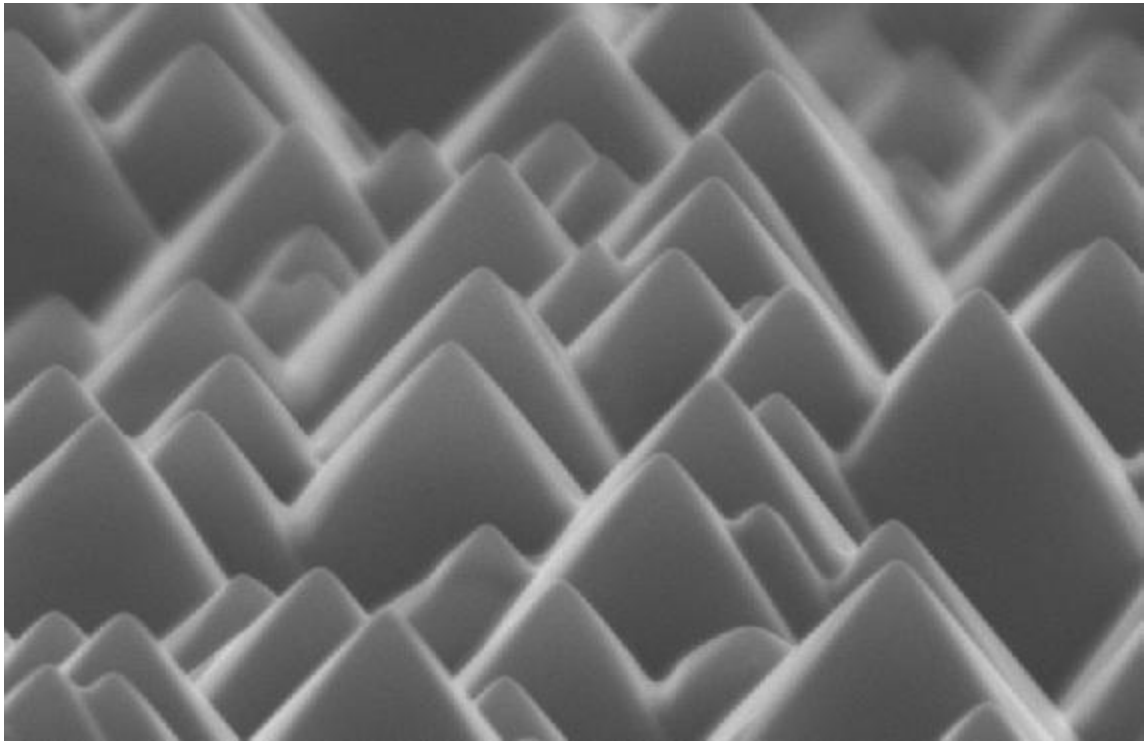
A single crystalline substrate can be textured by etching along the faces of the crystal planes. The crystalline structure of silicon results in a surface made up of pyramids if the surface is appropriately aligned with respect to the internal atoms.

One such pyramid is illustrated in the drawing below.



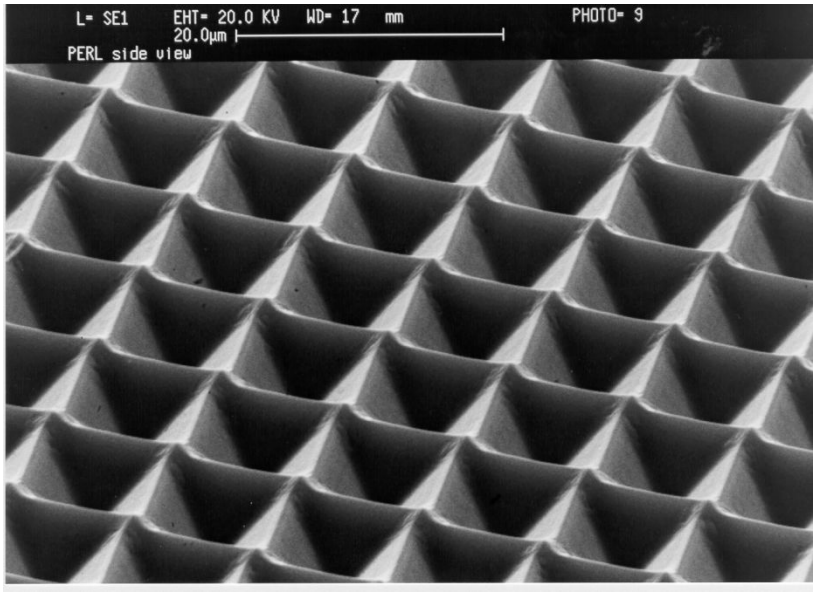
A square based pyramid which forms the surface of an appropriately textured crystalline silicon solar cell.

An electron microscope photograph of a textured silicon surface is shown in the photograph below. This type of texturing is called "random pyramid" texture, and is commonly used in industry for single crystalline wafers.



Scanning electron microscope photograph of a textured silicon surface. Image Courtesy of The School of Photovoltaic & Renewable Energy Engineering, University of New South Wales.

Another type of surface texturing used is known as "inverted pyramid" texturing. Using this texturing scheme, the pyramids are etched down into the silicon surface rather than etched pointing upwards from the surface. A photograph of such a textured surface is shown below.



Scanning electron microscope photograph of a textured silicon surface. Image Courtesy of The School of Photovoltaic & Renewable Energy Engineering, University of New South Wales.

Light Trapping

- The optimum device thickness is not controlled solely by the need to absorb all the light.

- For example, if the light is not absorbed within a diffusion length of the junction, then the light-generated carriers are lost to recombination.

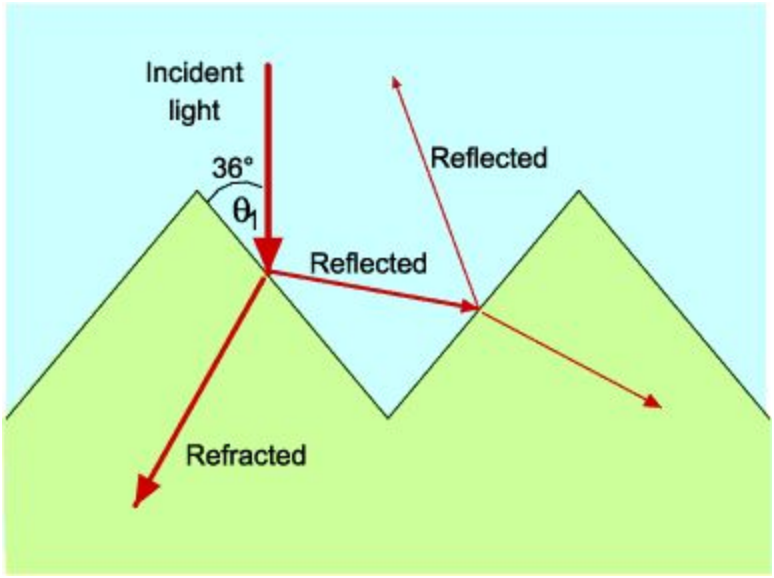
- In addition, as discussed in the Voltage Losses Due to Recombination, a thinner solar cell which retains the absorption of the thicker device may have a higher voltage. Consequently, an optimum solar cell structure will typically have "light trapping" in which the optical path length is several times the actual device thickness, where the optical path length of a device refers to the distance that an unabsorbed photon may travel within the device before it escapes out of the device. This is usually defined in terms of device thickness.

- For example, a solar cell with no light trapping features may have an optical path length of one device thickness, while a solar cell with good light trapping may have an optical path length of 50 times, indicating that light bounces back and forth within the cell many times.

Light trapping is usually achieved by changing the angle at which light travels in the solar cell by having it be incident on an angled surface. A textured surface will not only reduce reflection as previously described but will also couple light obliquely into the silicon, thus giving a longer optical path length than the physical device thickness. The angle at which light is refracted into the semiconductor material is, according to Snell's Law, as follows:

$$n_1 \sin\theta_1 = n_2 \sin\theta_2$$

In a textured single crystalline solar cell, the presence of crystallographic planes make the angle θ_1 equal to 36° as shown below.



Lambertian Rear Reflectors

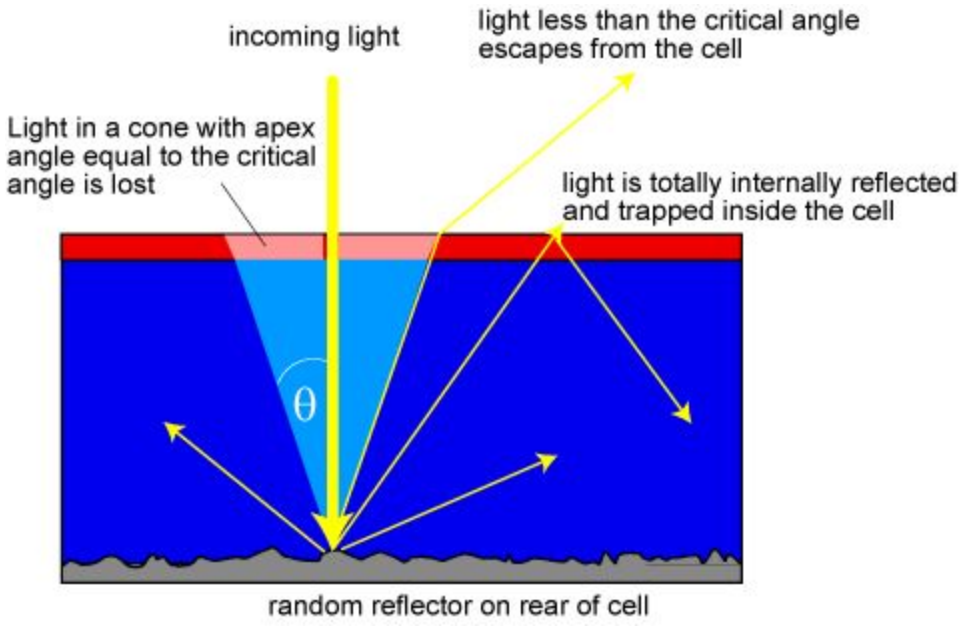
- A Lambertian back reflector is a special type of rear reflector which randomizes the direction of the reflected light.

- High reflection off the rear cell surface reduces absorption in the rear cell contacts or transmission from the rear, allowing the light to bounce back into the cell for possible absorption.

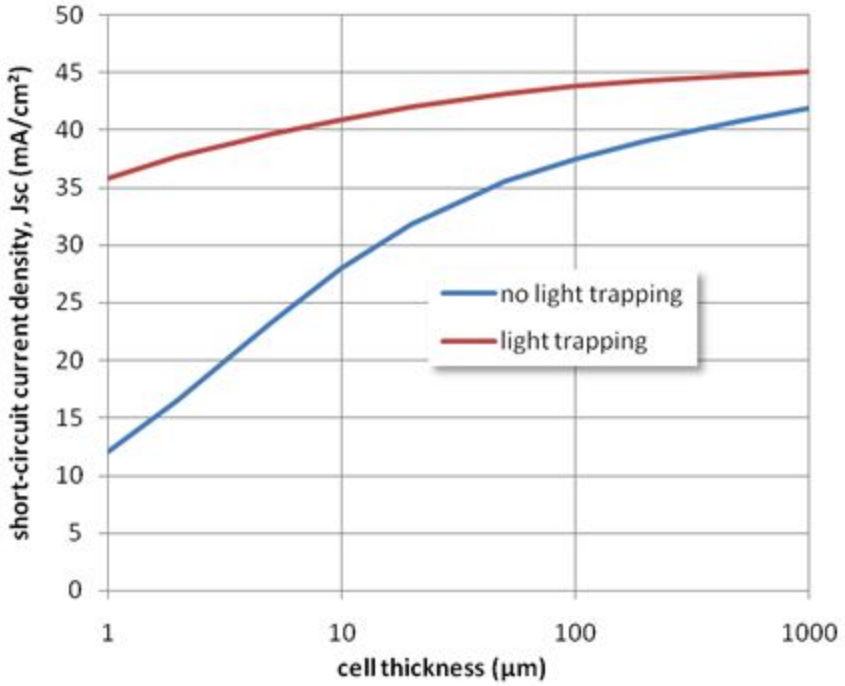
- Randomising the direction of light allows much of the reflected light to be totally internally reflected. Light reaching the top surface at an angle greater than the critical angle for total internal reflection is reflected again towards the back surface.

- Light absorption can be dramatically increased in this way, since the pathlength of the incident light can be enhanced by a factor up to $4n^2$ where n is the index of refraction for the semiconductor.

This allows an optical path length of approximately 50 ($4 \times 3.5^2 \approx 50$) times the physical devices thickness and thus is an effective light trapping scheme. A Lambertian rear surface is illustrated in the figure below.



Light trapping using a randomised reflector on the rear of the cell. Light less than the critical angle escapes the cell but light greater than the critical angle is totally internally reflected inside the cell. In actual devices, the front surface is also textured using schemes such as the random pyramids mentioned earlier.



Light trapping increases the short-circuit current (J_{SC}) of the solar cell - particularly for thin devices.

Recombination Losses

Recombination losses effect both the current collection (and therefore the short-circuit current) as well as the forward bias injection current (and therefore the open-circuit voltage).

Recombination is frequently classified according to the region of the cell in which it occurs.

Typically, recombination at the surface (surface recombination) or in the bulk of the solar cell (bulk recombination) are the main areas of recombination. The depletion region is another area in which recombination can occur (depletion region recombination).

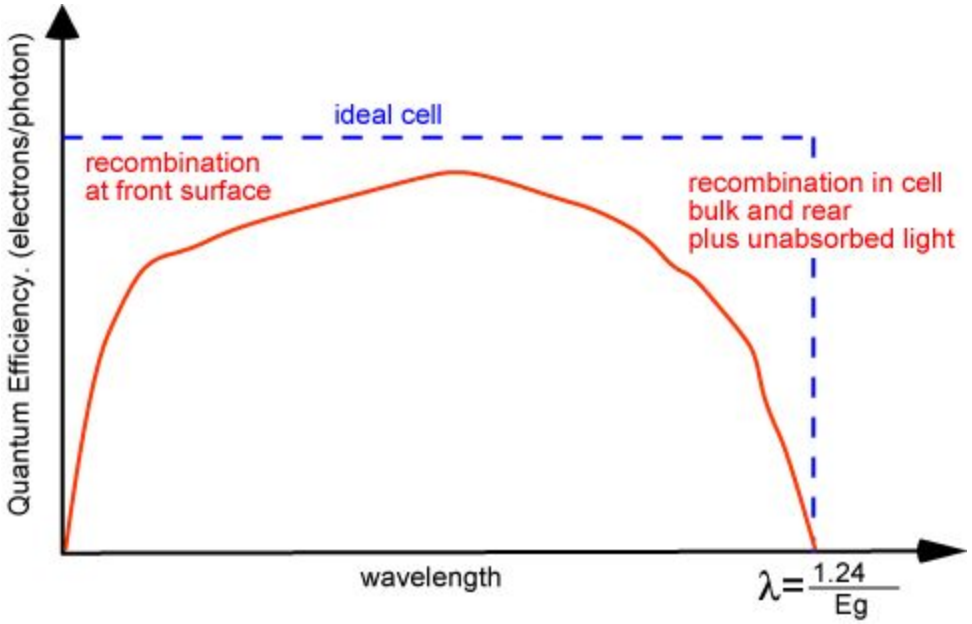
Current Losses Due to Recombination

In order for the *p*-*n* junction to be able to collect all of the light-generated carriers, both surface and bulk recombination must be minimised. In silicon solar cells, the two conditions commonly required for such current collection are:

- the carrier must be generated within a diffusion length of the junction, so that it will be able to diffuse to the junction before recombining; and

- in the case of a localized high recombination site (such as at an unpassivated surface or at a grain boundary in multicrystalline devices), the carrier must be generated closer to the junction than to the recombination site.

- For less severe localised recombination sites, (such as a passivated surface), carriers can be generated closer to the recombination site while still being able to diffuse to the junction and be collected without recombining.



Typical quantum efficiency in an ideal and actual solar cell, illustrating the impact of optical and recombination losses.

Voltage Losses due to Recombination

The open-circuit voltage is the voltage at which the forward bias diffusion current is exactly equal to the short circuit current. The forward bias diffusion current is dependent on the amount recombination in a *p-n* junction and increasing the recombination increases the forward bias current. Consequently, high recombination increases the forward bias diffusion current, which in turn reduces the open-circuit voltage.

The material parameter which gives the recombination in forward bias is the diode saturation current. The recombination is controlled by the number of minority carriers at the junction edge, how fast they move away from the junction and how quickly they recombine. Consequently, the dark forward bias current, and hence the open-circuit voltage is affected by the following parameters:

- the number of minority carriers at the junction edge. The number of minority carriers injected from the other side is simply the number of minority carriers in equilibrium multiplied by an exponential factor which depends on the voltage and the temperature. Therefore, minimising the equilibrium minority carrier concentration reduces recombination. Minimizing the equilibrium carrier concentration is achieved by **increasing the doping**;

- the diffusion length in the material. A low diffusion length means that minority carriers disappear from the junction edge quickly due to recombination, thus allowing more carriers to cross and increasing the forward bias current. Consequently, to minimise recombination and achieve a high voltage, a **high diffusion length is required.**

  The diffusion length depends on the types of material, the processing history of the wafer and the doping in the wafer. High doping reduces the diffusion length, thus introducing a trade-off between maintaining a high diffusion length (which affects both the current and voltage) and achieving a high voltage;

- the presence of localised recombination sources within a diffusion length of the junction. A high recombination source close to the junction (usually a surface or a grain boundary) will allow carriers to move to this recombination source very quickly and recombine, thus dramatically increasing the recombination current. The impact of surface recombination is reduced by **passivating the surfaces**.

Surface Recombination

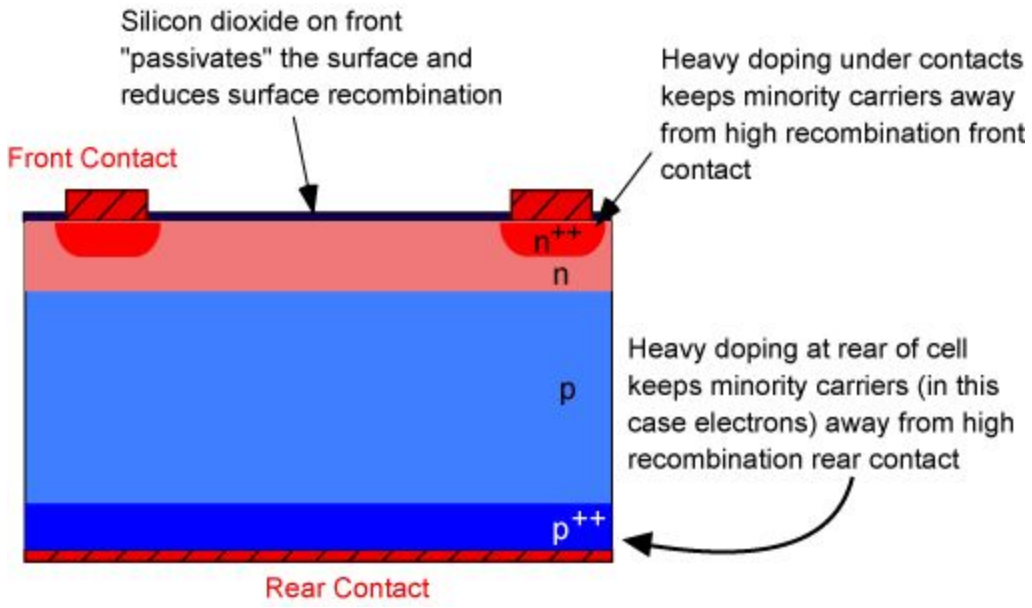
Surface recombination can have a major impact both on the short-circuit current and on the open-circuit voltage. High recombination rates at the top surface have a particularly detrimental impact on the short-circuit current since top surface also corresponds to the highest generation region of carriers in the solar cell.

Lowering the high top surface recombination is typically accomplished by reducing the number of dangling silicon bonds at the top surface by using "passivating" layer on the top surface. The majority of the electronics industry relies on the use of a thermally grown silicon dioxide layer to passivate the surface due to the low defect states at the interface. For commercial solar cells, dielectric layers such as silicon nitride are commonly used.

Since the passivating layer for silicon solar cells is usually an insulator, any region which has an ohmic metal contact cannot be passivated using silicon dioxide.

Instead, under the top contacts the effect of the surface recombination can be minimised by increasing the doping. While typically such a high doping severely degrades the diffusion length, the contact regions do not participate in carrier generation and hence the impact on carrier collection is unimportant.

In addition, in cases where a high recombination surface is close to the junction, the lowest recombination option is to increase the doping as high as possible.



Techniques for reducing the impact of surface recombination.

Back Surface Field

A similar effect is employed at the rear surface to minimise the impact of rear surface recombination velocity on voltage and current if the rear surface is closer than a diffusion length to the junction.

A "back surface field" (BSF) consists of a higher doped region at the rear surface of the solar cell.

The interface between the high and low doped region behaves like a *p*-*n* junction and an electric field forms at the interface which introduces a barrier to minority carrier flow to the rear surface.

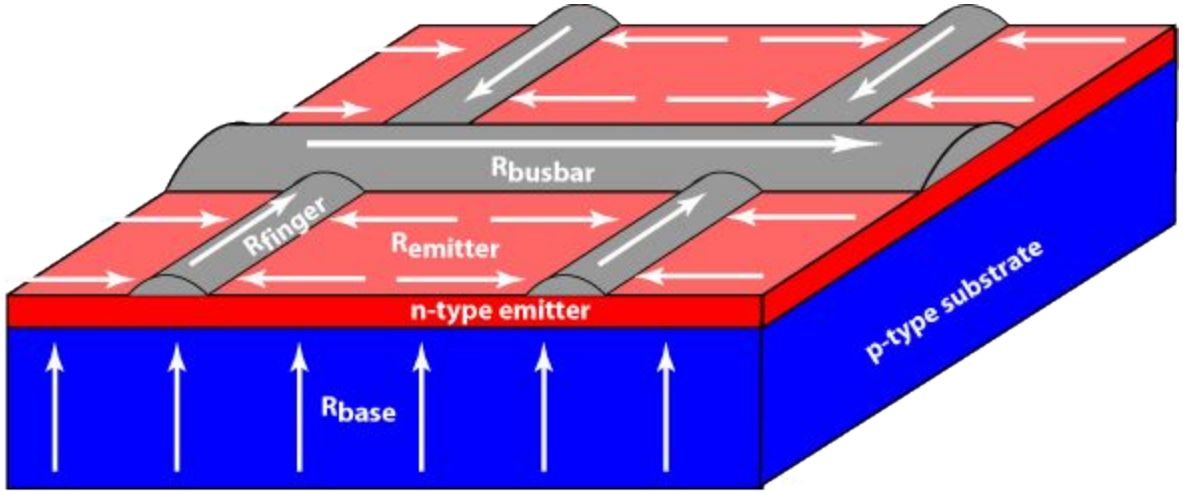
The minority carrier concentration is thus maintained at higher levels in the bulk of the device and the BSF has a net effect of passivating the rear surface.

Top Contact Design

Series Resistance

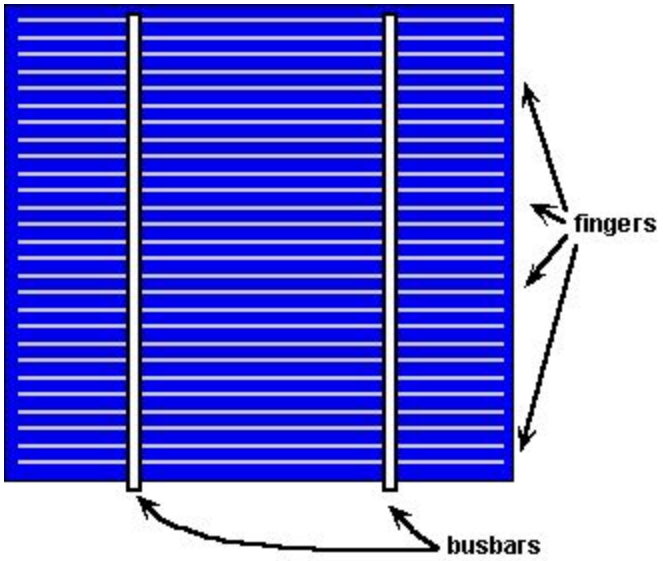
In addition to maximizing absorption and minimizing recombination, the final condition necessary to design a high efficiency solar cell is to minimise parasitic resistive losses. Both shunt and series resistance losses decrease the fill factor and efficiency of a solar cell. A detrimentally low shunt resistance is a processing defect rather than a design parameter. However, the series resistance, controlled by the top contact design and emitter resistance, needs to be carefully designed for each type and size of solar cell structure in order to optimise solar cell efficiency.

The series resistance of a solar cell consists of several components as shown in the diagram. Of these components, the emitter and top grid (consisting of the finger and busbar resistance) dominate the overall series resistance and are therefore most heavily optimised in solar cell design.



Resistive components and current flows in a solar cell.

The metallic top contacts are necessary to collect the current generated by a solar cell. "Busbars" are connected directly to the external leads, while "fingers" are finer areas of metalization which collect current for delivery to the busbars. The key design trade-off in top contact design is the balance between the increased resistive losses associated with a widely spaced grid and the increased reflection caused by a high fraction of metal coverage of the top surface.



Top contact design in a solar cell. The busbars connect the fingers together and pass the generated current to the external electrical contacts.

Base Resistance

Generated current typically flows perpendicular to the cell surface from the bulk of the cell and then laterally through the top doped layer until it is collected at a top surface contact.

The resistance and current of the base is assumed to be constant. The resistance to the current of the bulk component of the cell, or the "bulk resistance", R_b, is defined as:

$$R_b = \frac{\rho l}{A} = \frac{\rho_b W}{A}$$

taking into account the thickness of the material. Where:
l = length of conducting (resistive) path
ρ_b = "bulk resistivity" (inverse of conductivity) of the bulk cell material (0.5 - 5.0 Ω cm for a typical silicon solar cell)
A = cell area, and
w = width of bulk region of cell.

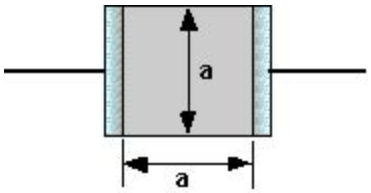
Emitter/Sheet Resistivity

For the emitter layer, the resistivity as well as the thickness of the layer will often be unknown, making the resistance of the top layer difficult to calculate from the resistivity and thickness. However, a value known as the "sheet resistivity", which depends on both the resistivity and the thickness, can be readily measured for the top surface *n*-type layer. For a uniformly doped layer, the sheet resistivity is defined as:

$$\rho_{\square} = \rho_{sh} = \frac{\rho}{W_e} = \frac{1}{q\mu_n(x)N_d(x)W_e}$$

Where ρ is the resistivity of the layer; and W_e is the thickness of the layer. The sheet resistivity is normally expressed as ohms/square or Ω/□.

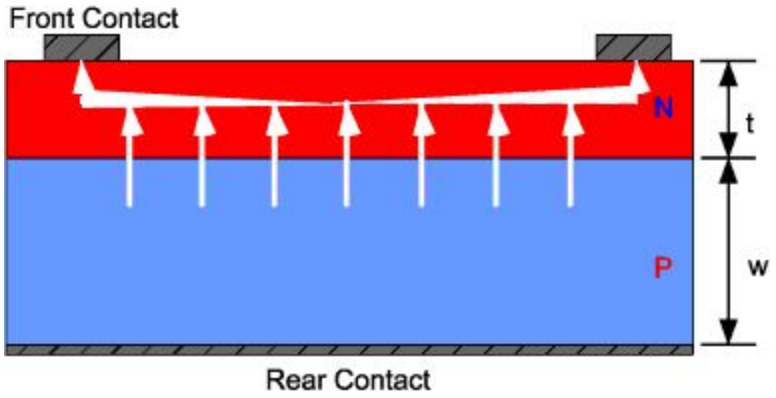
$$R_e = \frac{\rho l}{A} = \frac{\rho a}{W_e a} = \frac{\rho_{sh} a}{a} = \rho_{sh} \quad for \quad square \quad sheet$$



The resistance of a square conductive sheet is the same no matter what size it is so long as it remains a square.

Emitter Resistance

Based on the sheet resistivity, the power loss due to the emitter resistance can be calculated as a function of finger spacing in the top contact. However, the distance that current flows in the emitter is not constant. Current can be collected from the base close to the finger and therefore has only a short distance to flow to the finger or, alternatively, if the current enters the emitter between the fingers, then the length of the resistive path seen by such a carrier is half the grid spacing.



Idealised current flow from point of generation to external contact in a solar cell. The emitter is typically much thinner than shown in the diagram.

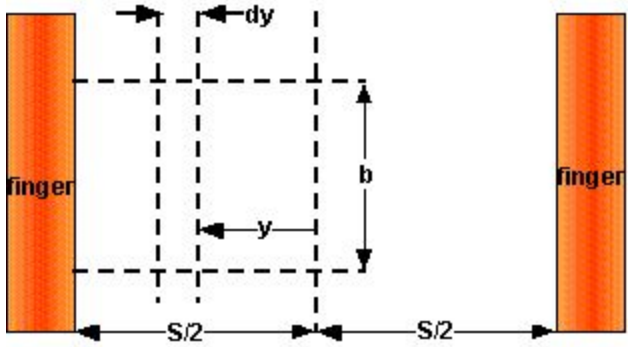
The incremental power loss in the section *dy* is given by:

$$dP_{loss} = I^2 dR$$

The differential resistance is given by: $dR = \frac{\rho}{b} dy$

$$dR = \frac{\rho}{A} dy = \frac{\rho}{W_e b} dy = \frac{\rho_{sh}}{b} dy$$

where
ρ is the sheet resistivity in Ω/sqr
b is the distance along the finger; and
y the distance between two grid fingers as shown below.



Dimensions needed for calculating power loss due to the lateral resistance of the top layer.

The current also depends on y and I(y) is the lateral current flow, which is zero at the midpoint between grating lines and increases linearly to its maximum at the grating line, under uniform illumination. The equation for the current is:

$$I(y) = Jby$$

where
J is the current density;
b is the distance along the finger; and
y the distance between two grid fingers as shown in fig.
The total power loss is therefore:

$$P_{loss} = \int I(y)^2 dR = \int_0^{S/2} \frac{J^2 b^2 y^2 \rho_{\square} dy}{b} = \frac{J^2 b \rho_{\square} S^3}{24}$$

Where *S* is the spacing between grid lines.

At the maximum power point, the generated power is:

$$P_{gen} = J_{MP} b \frac{S}{2} V_{MP}$$

The fractional power loss is given by:

$$P_{\%lost} = \frac{P_{loss}}{P_{gen}} = \frac{\rho_{\square} S^2 J_{MP}}{12 V_{MP}}$$

Claculate finger spacing for a typical silicon solar cell where ρ= 40 Ω/sq, J_{mp} = 30 mA/cm^2, V_{mp} = 450 mV, to have a power loss in the emitter of less than 4%.

Hence, the minimum spacing for the top contact grid can be calculated. For example, for a typical silicon solar cell where ρ= 40 Ω/sq, J_{mp} = 30 mA/cm^2, V_{mp} = 450 mV, to have a power loss in the emitter of less than 4% the finger spacing should be less than 4 mm.

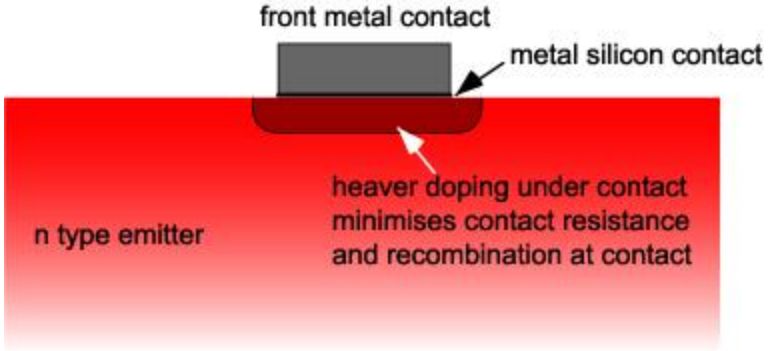
Contact resistance

Contact resistance losses occur at the interface between the silicon solar cell and the metal contact.

To keep top contact losses low, the top N^+ layer must be as heavily doped as possible. However, a high doping level creates other problems.

If a high level of phosphorus is diffused into silicon, the excess phosphorus lies at the surface of the cell, creating a "dead layer", where light generated carriers have little chance of being collected.

Many commercial cells have a poor "blue" response due to this "dead layer". Therefore, the region under the contacts should be heavily doped, while the doping of the emitter is controlled by the trade-offs between achieving a low saturation current in the emitter and maintaining a high emitter diffusion length.



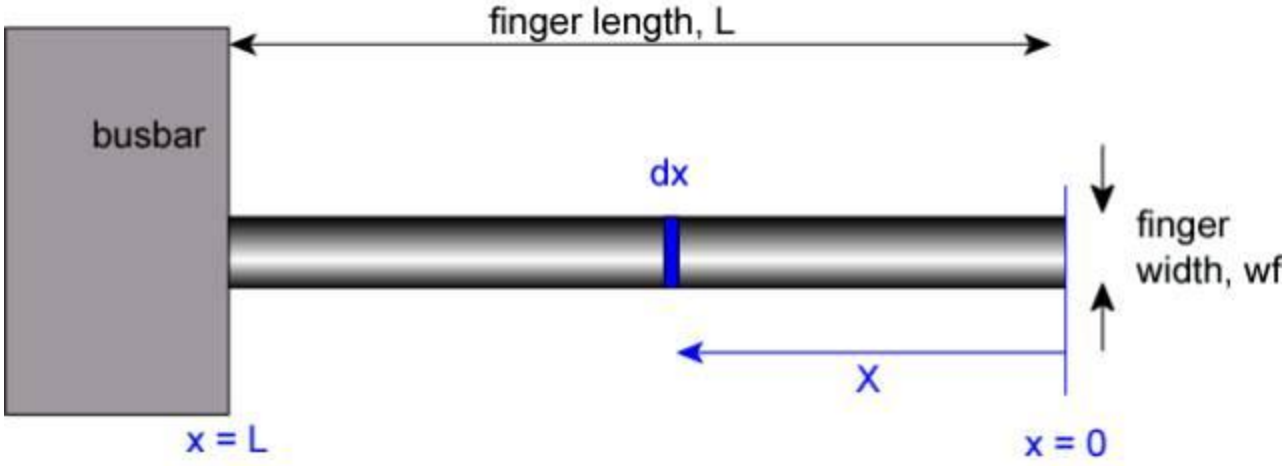
Points of contact resistance losses at interface between grid lines and semiconductor.

In commercial screen printed solar cells the contact resistance varies across the wafer. The physics of silver paste firing are quite complicated so small differences in surface topology and local heating cause large variations in the quality of the silver-silicon bond.

Finger Resistance

To provide higher conductivity, the top of a cell has a series of regularly spaced finger. While tapered fingers theoretically provide lower losses technology limitations mean that fingers are usually uniform in width. The resistive loss in a finger is calculated as below.

Calculation of Power Loss in the Fingers



Calculation of the power loss in a single finger. The width is assumed constant and it is assumed that the current is uniformly generated and that it flows perpendicularly into the finger, i.e., no current flow directly into the busbar.

Consider an element dx at a distance x from the end of the finger.

The current through the element dx is: $xJ_{MP}S_f$

where J_{mp} is the current at maximum power point and S_f is the finger spacing.

The resistance of the element dx is: $\frac{dx\rho_f}{w_f d_f}$

where w_f is the finger width, d_f is the finger depth (or height) and ρ_f is the effective resistivity of the metal.

The power loss in the element dx is: $I^2R = \frac{dx\rho_f}{w_f d_f}\left(xJ_{MP}S_f\right)^2$

Integrating x from 0 to L gives the power loss in the finger:

$$\int_0^L \frac{\left(xJ_{MP}S_f\right)^2 \rho_f}{w_f d_f} dx = \frac{1}{3} L^3 J_{MP}^2 S_f^2 \frac{\rho_f}{w_f d_f}$$

Optimization of Finger Spacing

Combining the equations for resistive losses allows use to determine the total power loss in the top contact grid.

For a typical cell type, say a screen printed cell, the metal resistivity will be fixed and the finger width is controlled by the screen size.

Typical values for the specific resistivity of silver are 3×10^{-8} Ω m.

For non-rectangular fingers the width is set to the actual width and an equivalent height is used to get the correct cross sectional area.

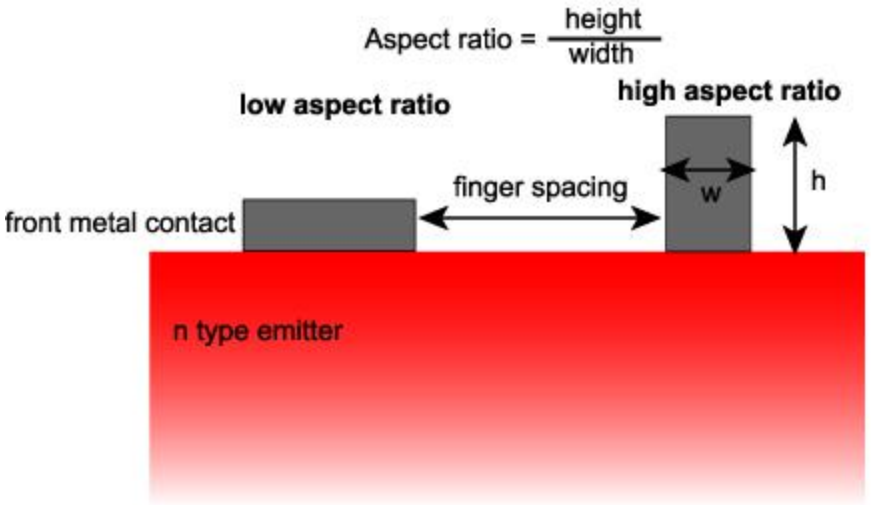
Metal Grid Pattern

The design of the top contact involves not only the minimization of the finger and busbar resistance, but the overall reduction of losses associated with the top contact.

These include resistive losses in the emitter, resistive losses in the metal top contact and shading losses.

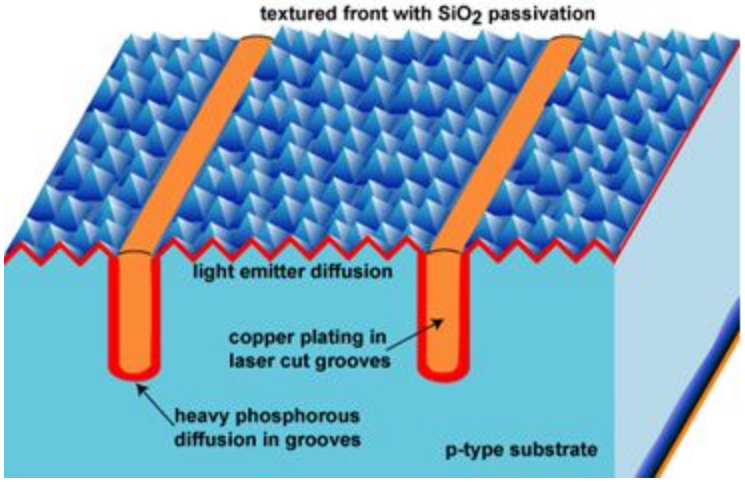
The critical features of the top contact design which determine how the magnitude of these losses are:

- the finger and busbar spacing,
- the metal height-to-width aspect ratio,



Key features of a top surface contacting scheme.

- the minimum metal line width and
- the resistivity of the metal.



Buried contacts. Differential n^+ doping in the contact grooves reduces series resistance.

Impact of Finger Spacing on Emitter Resistance

An important factor in top contact design is that of resistive losses in the emitter. As discussed in the Emitter Resistance section:

- the power loss from the emitter depends on the cube of the line spacing, and
- therefore a short distance between the fingers is desirable for a low emitter resistance.

Grid Resistance

The grid resistance is determined by:

- the resistivity of the metal used to make the metal contact,
- the pattern of the metallization and
- on the aspect ratio of the metallization scheme.

A low resistivity and a high metal height-to-width aspect ratio are desirable in solar cells, but in practice are limited by the fabrication technology used to make the solar cell.

Shading Losses

Shading losses are caused by the presence of metal on the top surface of the solar cell which prevents light from entering the solar cell.

The shading losses are determined by the transparency of the top surface, which, for a planar top surface, is defined as the fraction of the top surface covered by metal.

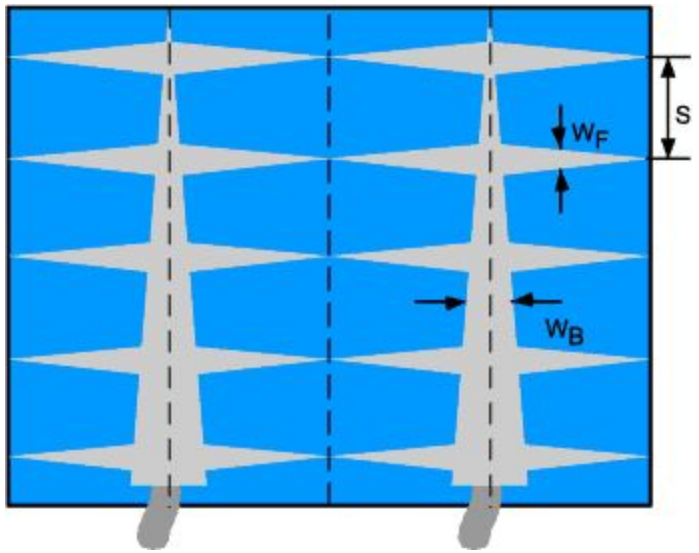
The transparency is determined by the width of the metal lines on the surface and on the spacing of the metal lines.

An important practical limitation is the minimum line width associated with a particular metallization technology. For identical transparencies, a narrow line-width technology can have closer finger spacing, thus reducing the emitter resistance losses.

Design Rules

While a multitude of top contacting schemes exist, for practical reasons most top surface metalization patterns are relatively simple and highly symmetrical. A symmetrical contacting scheme can be broken down into unit cells and several broad design rules can be determined. It can be shown that:

- the optimum width of the busbar, W_B, occurs when the resistive loss in the busbar equals its shadowing loss;
- a tapered busbar has lower losses than a busbar of constant width; and
- the smaller the unit cell, the smaller finger width, W_F , and the smaller the finger spacings, S, the lower the losses.



Schematic of a top contact design showing busbars and fingers