SEG APPLICATION PROJECT

UltraFLEX Digital: I8243 Module

STUDENT GUIDE

SUBJECT

The FPGA virtual device contains many IP modules that can be seen on digital devices. Simulated I8243 is one of them. The subject of this mini project is:

1. Cover UltraFLEX basic digital training mini project 1

TERADYNE LINK

LEARNING
INFORMATION
NETWORKING
KNOWLEDGE

Table of Contents

Change History

Version #	Date	Author	Comments
1.0	Jun 2019	Amanda Nie	First Revision
2.0	Jun 2023	Pradeep Sellamuthu	Fine tune test plan

Background Knowledge

I8243 is a model device used as the first mini project of IGXL family digital programing basic training. The FPGA training kit could be set to I8243 mode, to simulate the function of this device. So, users could do I8243 mini project on this platform if the standard lab hardware setup is not available.

Please note to use I8243 function, training kit hardware need to be connected to configuration server and use the configuration GUI to configure it to I8243.

Feature and Description

I8243 is an Intel device. It is an input/output expander designed specifically to provide a low cost means of I/O expansion for the MCS-48 family of single chip microcomputers. It consists of four 4 bits bidirectional static I/O ports which serve as an interface to the MCS-48 Microcomputers. The 4 bits interface requires that only 4 I/O lines of the 8048 be used for I/O expansion and allows multiple 8243s to be added to the same bus.

The I/O ports of the 8243 serve as a direct extension of the resident I/O facilities of the MCS-48 microcomputers and accessed by their own MOV, ANL and ORL instructions.

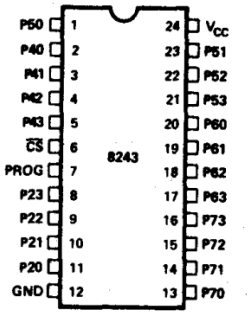


Figure 2. 8243 Pin Configuration

Table 1. Pin Description

Symbol	Pin No.	Function
PROG	7	**CLOCK INPUT.** A high to low transition on PROG signifies that address and control are available on P20–P23, and a low to high transition signifies that data is available on P20–P23.
$\overline{CS}$	6	**CHIP SELECT INPUT.** A high on CS inhibits any change of output or internal status.
P20–P23	11–8	Four (4) bit bi-directional port contains the address and control bits on a high to low transition of PROG. During a low to high transition, contains the data for a selected output port if a write operation, or the data from a selected port before the low to high transition if a read operation.
GND	12	0 volt supply.
P40–P43 P50–P53 P60–P63 P70–P73	2–5 1, 23–21 20–17 13–16	Four (4) bit bi-directional I/O ports. May be programmed to be input (during read), low impedance latched output (after write), or a tri-state (after read). Data on pins P20–P23 may be directly written, ANDed or ORed with previous data.
V_{CC}	24	+5 volt supply.

P21	P20	Address Code	P23	P22	Instruction Code
0	0	Port 4	0	0	Read
0	1	Port 5	0	1	Write
1	0	Port 6	1	0	ORLD
1	1	Port 7	1	1	ANLD

The functionality of this simulated device is the same as Intel 8243, refer to the datasheet for more details. The only difference is as below:

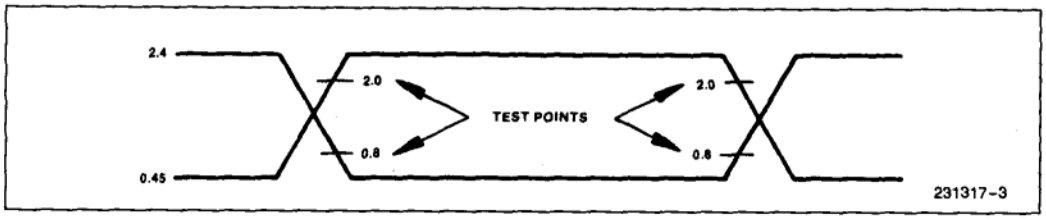
1. Intel 8243 only has one 5V power. This simulated Intel 8243 need VCC = 1.8V and VCCIO = 3.3V.
2. Intel 8243 digital level is 0-VCC(5V). This simulated Intel 8243 digital level is LVCMOS33.

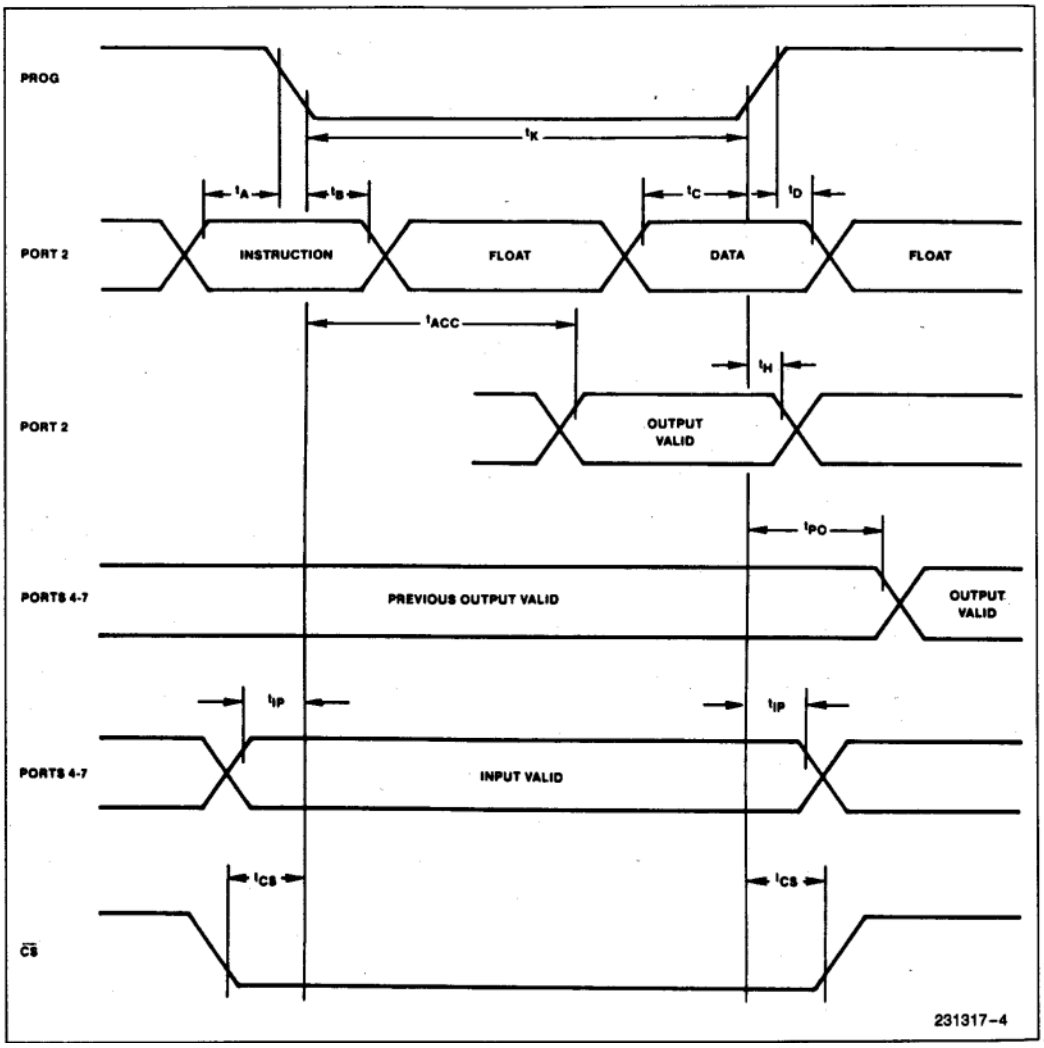
	I/O Standard	VIL		VIH		VOL	VOH	IOL	IOH
		Min, V	Max, V	Min, V	Max, V	Max, V	Min, V	mA	mA
I8243	LVCMOS33	-0.300	0.8	2.000	3.450	0.400	Vcco-0.400 (2.9)	1	-1
TI245									
SPI									
PLL									

3. Timing performance is different with Intel 8243. But the timing parameter tests are not tested in standard mini project. Below attached Intel 8243 timing diagram and AC parameter spec for your reference.

A.C. CHARACTERISTICS T_A = 0°C to 70°C, V_{CC} = 5V ±10%

Symbol	Parameter	Min	Max	Units	Test Conditions
t_A	Code Valid Before PROG	100		ns	80 pF Load
t_B	Code Valid After PROG	60		ns	20 pF Load
t_C	Data Valid Before PROG	200		ns	80 pF Load
t_D	Data Valid After PROG	20		ns	20 pF Load
t_H	Floating After PROG	0	150	ns	20 pF Load
t_K	PROG Negative Pulse Width	700		ns	
t_{CS}	CS Valid Before/After PROG	50		ns	
t_{PO}	Ports 4–7 Valid After PROG		700	ns	100 pF Load
t_{LP1}	Ports 4–7 Valid Before/After PROG	100		ns	
t_{ACC}	Port 2 Valid After PROG		650	ns	80 pF Load





4. Power on Initialization (same with Intel 8243)

Initial application of power to the device forces input/outputs 4,5,6 and 7 to the tri-state and port 2 to the input mode. The PROG pin may be either high or low when power is applied. The first high to low transition of PROG causes the device to exit power on mode. The power on sequence is initialed if VCC drops below 1.65V or VCCIO drops below 3.1V.

5. Write Modes (same with Intel 8243)

The device has three write modes.

MOVD: directly writes new data into the selected port and old data is lost.

ORLD: takes new data, OR it with the old data and then writes it to the selected port.

ANLD: takes new data, AND it with the old data and then write it to the selected port.

Operation code and the port address are latched from the input port 2 on the high to low transition of the PROG pin. On the low to high transition of PROG, data on port 2 is transferred to the logic block of the specified output port.

After the logic manipulations are performed, the data is latched in and out. The old data remains latched until new valid outputs are entered.

6. Read mode

The device has one read mode. The operation code and port address are latched from the input port 2 on the high to low transition of the PROG pin. As soon as the read operation and port address are decoded, the appropriate outputs are tri-stated. And the input buffer is switched on. The read operation is terminated by a low to high transition of the PROG pin. The port (4,5,6,7) that was selected is switched to the tri-stated mode while port 2 is returned to the input mode.

Normally, a port (4,5,6,7) will be in an output (write mode) or input (read mode). If modes are changed during operation, the first read following a write should be ignored. All following reads are valid. This is to allow the external driver on the port to settle after the first read instruction removes the low impedance drive from the 8243 outputs. A read of any port will leave that port in a high impedance state.

Pin Configuration

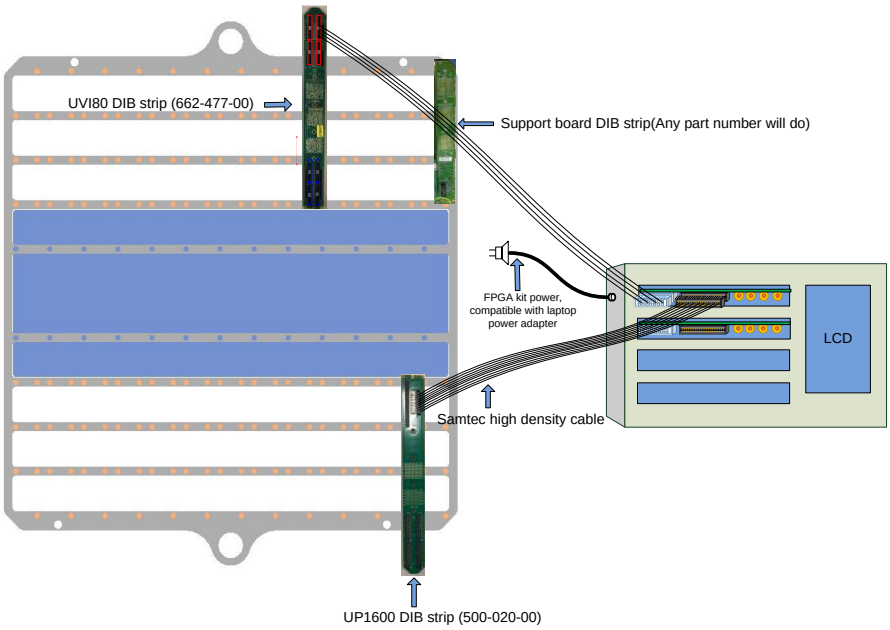
FPGA is connected with UP1600/UP2200 by 40 digital channels. I8243 channel Map is as below:

1. If you are using UltraFLEX DIB strip hardware, please use this channel map.

Pin Name	UltraFLEX
8243_p5[0]	CH005
8243_p4[0]	CH006
8243_p4[1]	CH007
8243_p4[2]	CH008
8243_p4[3]	CH009
8243_cs	CH010
8243_prog	CH011
8243_p2[3]	CH012
8243_p2[2]	CH013
8243_p2[1]	CH014
8243_p2[0]	CH015
8243_p7[0]	CH033
8243_p7[1]	CH129
8243_p7[2]	CH130
8243_p7[3]	CH131
8243_p6[3]	CH132
8243_p6[2]	CH133
8243_p6[1]	CH134
8243_p6[0]	CH135
8243_p5[3]	CH136
8243_p5[2]	CH137
8243_p5[1]	CH138

Note: For UltraFLEX setup, each DIB strip only supports one site. So, the channel number for all sites are the same, but the UP1600 slot number is different for each site according to tester configuration. Please make sure tester configuration – DIB strip installation location – channel map slot number could match.

For UltraFLEX hardware connection, please follow below figure:



Note: UP1600 and UVI80 slot numbers can be adjusted based on tester actual configuration.

Could support up to 4 sites. Same connection for each site.

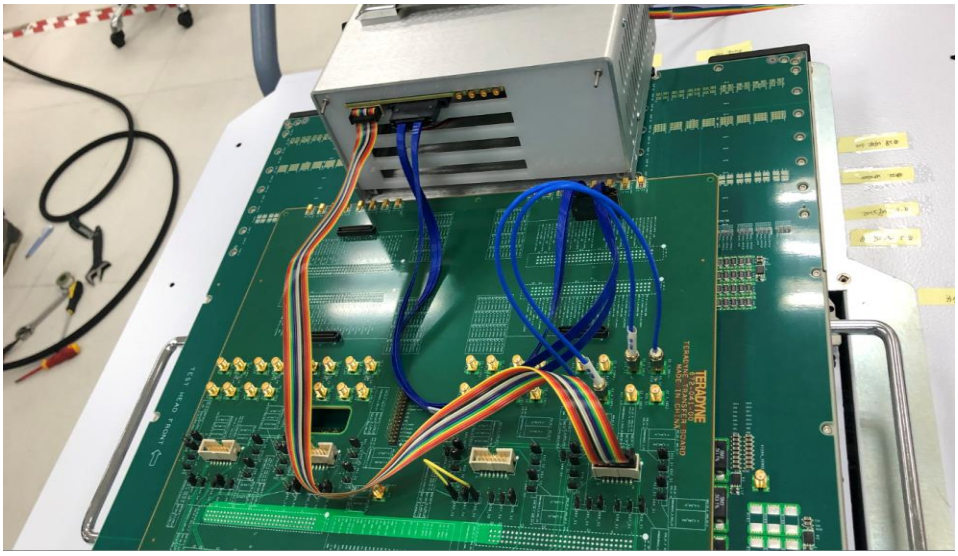
2. If you are using UltraFLEXplus mother board hardware, please use this channel map.

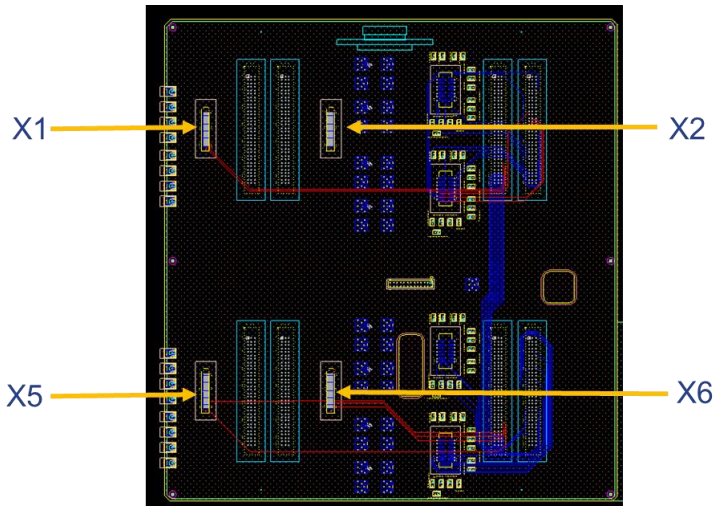
Mother board PN: 655-094-00
Adaptor board PN: 672-041-00

Pin Name	UltraFLEXplus			
	Site 0 (Cable to X1)	Site 1 (Cable to X2)	Site 2 (Cable to X5)	Site 3 (Cable to X6)
8243_p5[0]	22.3ch36	22.3ch05	22.1ch21	22.1ch04
8243_p4[0]	22.3ch38	22.3ch06	22.1ch22	22.1ch05
8243_p4[1]	22.3ch39	22.3ch07	22.1ch23	22.1ch06
8243_p4[2]	22.3ch40	22.3ch08	22.1ch24	22.1ch07
8243_p4[3]	22.3ch41	22.3ch09	22.1ch25	22.1ch08
8243_cs	22.3ch42	22.3ch10	22.1ch26	22.1ch09
8243_prog	22.3ch43	22.3ch11	22.1ch27	22.1ch10
8243_p2[3]	22.3ch44	22.3ch12	22.1ch28	22.1ch11
8243_p2[2]	22.3ch45	22.3ch13	22.1ch29	22.1ch12
8243_p2[1]	22.3ch46	22.3ch14	22.1ch30	22.1ch13
8243_p2[0]	22.3ch48	22.3ch16	22.1ch31	22.1ch47
8243_p7[0]	22.3ch50	22.3ch18	22.1ch33	22.1ch49
8243_p7[1]	22.3ch51	22.3ch19	22.1ch34	22.1ch50
8243_p7[2]	22.3ch52	22.3ch20	22.1ch35	22.1ch51

8243_p7[3]	22.3ch53	22.3ch21	22.1ch36	22.1ch52
8243_p6[3]	22.3ch54	22.3ch22	22.1ch37	22.1ch53
8243_p6[2]	22.3ch55	22.3ch23	22.1ch38	22.1ch54
8243_p6[1]	22.3ch56	22.3ch24	22.1ch39	22.1ch55
8243_p6[0]	22.3ch57	22.3ch25	22.1ch40	22.1ch56
8243_p5[3]	22.3ch58	22.3ch82	22.1ch98	22.1ch57
8243_p5[2]	22.3ch59	22.3ch83	22.1ch99	22.1ch58
8243_p5[1]	22.3ch60	22.3ch26	22.1ch100	22.1ch59

For UltraFLEXplus mother board hardware connection, please follow below figure:





3. If you are using UltraFLEXplus DIB strip hardware, please use this channel map.

Below DIB strips are needed to use this setup:

675-133-00 (UltraFLEXplus UP2200 DIB strip 1pc)

675-134-00(UltraFLEXplus UVS256HP DIB strip 1pc)

659-406-20 (UltraFLEXplus stiffener 1pc)

608-200-00(UltraFLEXplus DSI DIB strip 1pc)

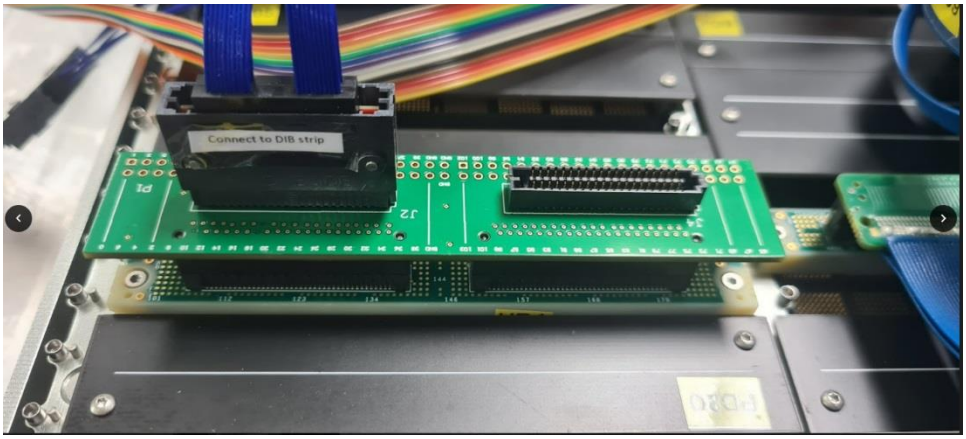
600-001-01 (UP2200 UltraFLEXplus DIB strip adaptor board 1pc)

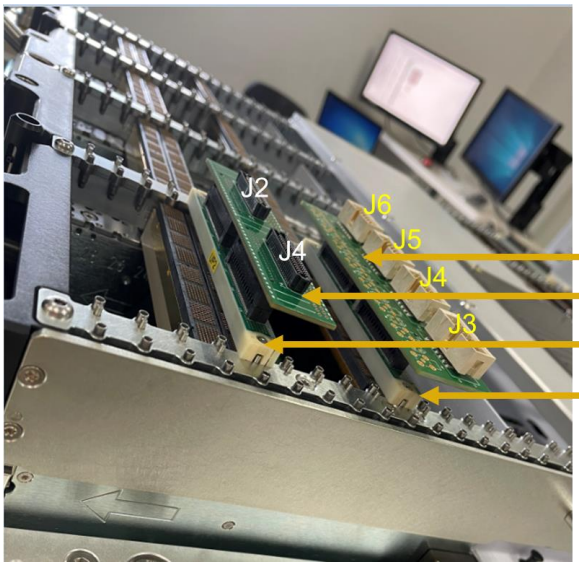
600-002-02(UVS256HP UltraFLEXplus DIB strip adaptor board 1pc)

I8243 Pin Name	DIB strip UP2200 channel (Install on BLK100)		DIB strip UP2200 channel (Install on BLK200)		DIB strip UP2200 channel (Install on BLK300)		DIB strip UP2200 channel (Install on BLK400)	
	J2	J4	J2	J4	J2	J4	J2	J4
8243_p5[0]	3_CH21	4_CH82	3_CH85	4_CH18	1_CH21	2_CH82	1_CH85	2_CH18
8243_p4[0]	3_CH23	4_CH78	3_CH87	4_CH14	1_CH23	2_CH78	1_CH87	2_CH14
8243_p4[1]	3_CH29	4_CH74	3_CH93	4_CH10	1_CH29	2_CH74	1_CH93	2_CH10
8243_p4[2]	3_CH33	4_CH70	3_CH97	4_CH6	1_CH33	2_CH70	1_CH97	2_CH6
8243_p4[3]	3_CH37	4_CH66	3_CH101	4_CH2	1_CH37	2_CH66	1_CH101	2_CH2
8243_cs	3_CH4	4_CH99	3_CH68	4_CH35	1_CH4	2_CH99	1_CH68	2_CH35
8243_prog	3_CH16	4_CH95	3_CH80	4_CH31	1_CH16	2_CH95	1_CH80	2_CH31
8243_p2[3]	3_CH17	4_CH90	3_CH81	4_CH26	1_CH17	2_CH90	1_CH81	2_CH26
8243_p2[2]	3_CH19	4_CH94	3_CH83	4_CH30	1_CH19	2_CH94	1_CH83	2_CH30
8243_p2[1]	3_CH18	4_CH91	3_CH82	4_CH27	1_CH18	2_CH91	1_CH82	2_CH27
8243_p2[0]	3_CH20	4_CH83	3_CH84	4_CH19	1_CH20	2_CH83	1_CH84	2_CH19
8243_p7[0]	3_CH28	4_CH75	3_CH92	4_CH11	1_CH28	2_CH75	1_CH92	2_CH11
8243_p7[1]	3_CH32	4_CH71	3_CH96	4_CH7	1_CH32	2_CH71	1_CH96	2_CH7
8243_p7[2]	3_CH3	4_CH100	3_CH67	4_CH36	1_CH3	2_CH100	1_CH67	2_CH36
8243_p7[3]	3_CH7	4_CH96	3_CH71	4_CH32	1_CH7	2_CH96	1_CH71	2_CH32
8243_p6[3]	3_CH1	4_CH103	3_CH65	4_CH39	1_CH1	2_CH103	1_CH65	2_CH39
8243_p6[2]	3_CH0	4_CH101	3_CH64	4_CH37	1_CH0	2_CH101	1_CH64	2_CH37
8243_p6[1]	3_CH2	4_CH97	3_CH66	4_CH33	1_CH2	2_CH97	1_CH66	2_CH33
8243_p6[0]	3_CH22	4_CH81	3_CH86	4_CH17	1_CH22	2_CH81	1_CH86	2_CH17
8243_p5[3]	3_CH25	4_CH77	3_CH89	4_CH13	1_CH25	2_CH77	1_CH89	2_CH13
8243_p5[2]	3_CH27	4_CH76	3_CH91	4_CH12	1_CH27	2_CH76	1_CH91	2_CH12
8243_p5[1]	3_CH34	4_CH69	3_CH98	4_CH5	1_CH34	2_CH69	1_CH98	2_CH5

Note: For UltraFLEXplus DIB strip setup, each DIB strip supports 2 sites. Which column of the above table should be used depends on where the DIB strip is installed (Block 100/200/300/400). Please make sure tester configuration – DIB strip installation location – channel map slot number could match.

For UltraFLEXplus DIB strip hardware connection, please follow below figure:


Connect to DIB strip

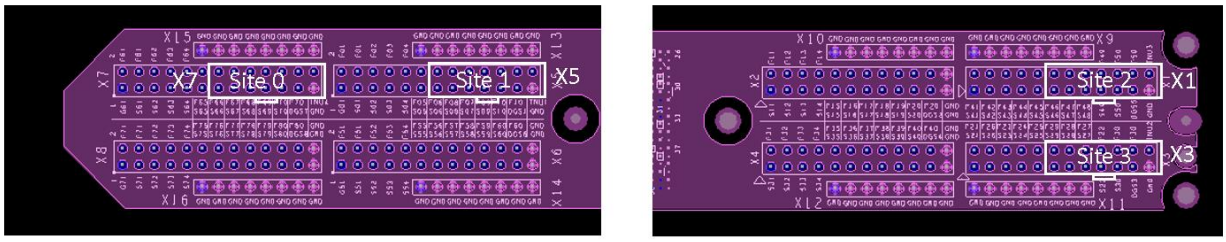

J2
J6
J5
J4
J4
J3
600-002-02
600-001-01
675-133-00
675-134-00

Power up Requirement

A separate power system is designed to support this kit. The power is distributed to FPGA core board by this power system. Take note on below item:

A. Do not source any voltage on this system before turning on the power supply.
B. Follow the DC voltage level to setup, to avoid damage.
C. Correct operating sequence should be.
   a. Plug in the 19V power and turn on the kit system power switch on the cable.
   b. Supply 1.8V to VCC pin
   c. Supply 3.3V to VCCIO pin

1. If you are using UltraFLEX DIB strip hardware, please use this channel map.



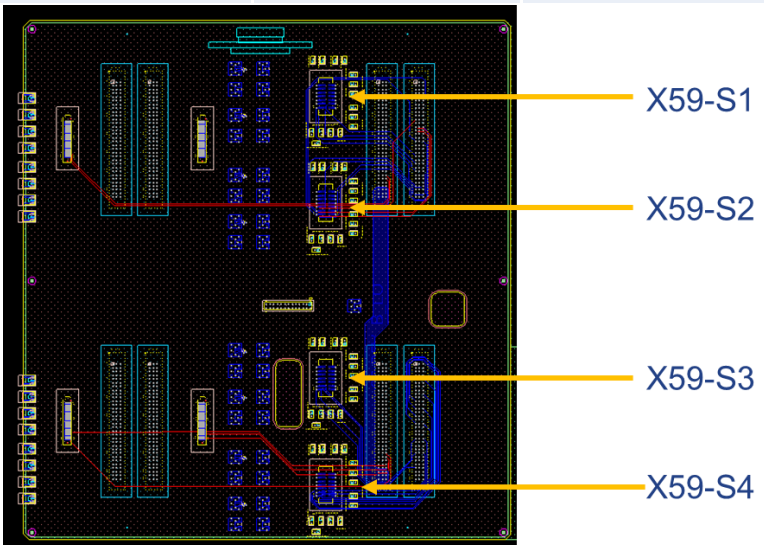
UltraFLEX Setup				
Pin Name	**Site 0**	**Site 1**	**Site 2**	**Site 3**
VCC	F/S 69	F/S 09	F/S 49	F/S 22
VCCIO	F/S 66	F/S 06	F/S 46	F/S 29

2. If you are using UltraFLEXplus mother board hardware, please use this channel map.

IMPORTANT: Please note there are 150-ohm resistors connect the channel to ground for xx.3Sense01, and xx.3Sense13, so you might see high current when using site 0 (X59-S1). If you want to avoid this issue, please use other connectors/sites.

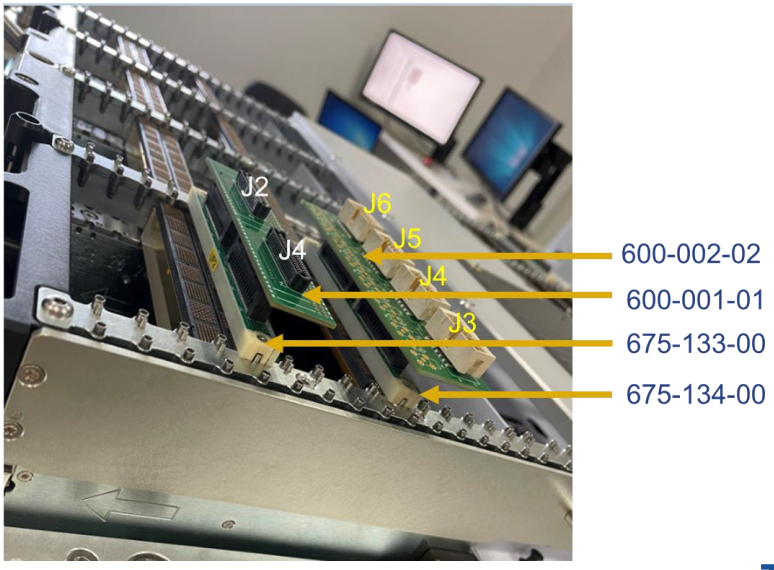
UltraFLEXplus Setup

Pin Name	Site 0 (X59-S1)	Site 1 (X59-S2)	Site 2(X59-S3)	Site 3(X59-S4)
VCC	12.3Sense01	12.3Sense17	12.1Sense11	12.1Sense26
VCCIO	12.3Sense13	12.3Sense10	12.1Sense12	12.1Sense22



3. **If you are using UltraFLEXplus DIB strip hardware, please use this channel map**

Pin Information		Block100				Block200				Block300				Block400			
Name	Type	J3(X1)	J4(X1)	J5(X2)	J6(X2)	J3(X1)	J4(X1)	J5(X2)	J6(X2)	J3(X1)	J4(X1)	J5(X2)	J6(X2)	J3(X1)	J4(X1)	J5(X2)	J6(X2)
VCC	Power	4_HS40	4_HF47	3_HS06	3_HS01	4_HS08	4_HF15	3_HS38	3_HS33	2_HS40	2_HF47	1_HS06	1_HS01	2_HS08	2_HF15	1_HS38	1_HS33
VCCIO	Power	4_HF43	4_HS48	3_HS09	3_HS11	4_HF11	4_HS16	3_HS41	3_HS43	2_HF43	2_HS48	1_HS09	1_HS11	2_HF11	2_HS16	1_HS41	1_HS43



Test Plan

Please develop your test program following this chapter.

1. Shorts Test Using Dynamic Loads

The Opens/Shorts test grounds all pins (including VDD), and program dynamic loads to -400uA, test Port2 & Port4-7.

This test can test shorts defects of VSS diodes, and pin to pin shorts.

- ♣ Ground all pins (including VDD) with pattern.
- ♣ Set the test pin to Hiz state one by one using pattern.

- ♣ Program dynamic loads to -100uA, test output voltage. If the resultant voltage is GT -0.3V, it fails.

If the above test is passed, means: VSS diodes are ok without shorts. Note, this test open test shorts if there is an open, this test should pass. Some of the customers require open and short defects fall into different bin numbers.

2. Opens Test Using Dynamic Loads

The opens test uses dynamic loads to ground all pins (including VDD), and program dynamic loads to -400uA, to test VSS diodes for open defects.

- ♣ Ground all pins (including VDD) with pattern.
- ♣ Set the test pin to Hiz state one by one using pattern.
- ♣ Program dynamic loads to -100uA, to test VSS diodes for open defects. If the resultant voltage is LT -1.0v or, it fails.

3. Parametric Continuity Test

This test will test both VDD diodes and VSS diodes by using PPMU to force current and measure voltage.

Test Pins: PROG, CS, Port2 and Port 4-7

Test method:

1) Force 0 V on VCC and VCCIO
2) Set PPMU clamp voltage at +/-3V. Use PPMU to force 100uA on each pin and measure voltage, while force 0V on other pins. Test each pin serially.
3) Data log results.
4) Set PPMU clamp voltage at +/-3V. Use PPMU to force -100uA on each pin and measure voltage, while force 0V on other pins. Test each pin serially.
5) Data log results.

Limit:

VDD diode: Hlimit = 1.5V, Llimit = 0.3V
VSS diode: Hlimit = -0.3V, Llimit = -1.5V

4. Full Functional Test

WRITE “1010” to port4-7, AND “1110” with the existing data on port4-7, OR “0011” with the existing data on port4-7.

Test Pins: PROG, CS, Port2 and Port 4-7

Test method:

1) Apply power.
2) Apply level and timing; (Create the time sets based on the datasheet parameters and waveforms)

3) Run pattern.
4) Data log results.

Level:

	VIL	VIH	VOL	VOH	IOL	IOH
All Digital Pins	0V	3.3V	0.35V	1.65V	100uA	-100uA

Timing: (Example)

Time Sets (Basic) TERADYNE

Timing Mode: Single Master Timeset Name:
Time Domain: Strobe Ref Setup Name:

	Cycle	Pin/Group			Data		Drive				Compare				Edge Resolution	
Time Set	Period	Name	Clock Period	Setup	Src	Fmt	On	Data	Return	Off	Mode	Open	Close	Ref Offset	Mode	C
rw_inst	1.E-06	I8243_ports		i/o	PAT	NR		0		0	edge	900.E-09			Auto	
rw_inst	1.E-06	I8243_cs		i/o	PAT	NR				0	off				Auto	
rw_inst	1.E-06	I8243_prog		i/o	PAT	RL		0	500.E-09	0	off				Auto	
rw_data	1.E-06	I8243_ports		i/o	PAT	nr		0		0	edge	900.E-09			Auto	
rw_data	1.E-06	I8243_cs		i/o	PAT	nr		0		0	Off				Auto	
rw_data	1.E-06	I8243_prog		i/o	PAT	rh		0	500.E-09	0	Off				Auto	

Pattern: I8243_Func.pat (Create by yourself)

5. Input Leakage

Description: Port 2 and PROG, CS pins are set to input mode at power on. Force VSS/VCCMAX on them and measure the current using PPMU. This test should be done by serial while force opposite voltage on other input pins.

Test Pins: Port 2, CS, PROG

Test method:

1) Apply power.
2) Apply level and timing.
3) Set PPMU current clamp to 20uA. Force 0V on each pin and measure current with PPMU, while force 3.3V on other input pins. Test each pin serially.
4) Datalog the results.
5) Set PPMU current clamp to 20uA. Force 3.3V on each pin and measure current with PPMU, while force 0V on other input pins. Test each pin serially.
6) Datalog the results.

Limit:

Hlimit = 10uA, Llimit = -10uA

6. Output tristate leakage

The output tristate leakage test measured current from ports 4-7 when the output is preconditioned to its tristate state. Force VSS/VCCMAX on them and measure the current using PPMU. This test should be done by serial while force opposite voltage on other input pins.

Test Pins: Port 4-7

Test method:

1) Apply power.
2) Apply level and timing.
3) Run Pre-condition pattern to set port 4-7 to tri-state mode.
4) Set PPMU current clamp to 20uA. Force 0V on each pin and measure current with PPMU, while force 3.3V on other input pins. Test each pin serially.
5) Datalog the results.
6) Set PPMU current clamp to 20uA. Force 3.3V on each pin and measure current with PPMU, while force 0V on other input pins. Test each pin serially.
7) Datalog the results.

Limit:

Hlimit = 10uA, Llimit = -10uA

7. Static ICC

Set the DUT to static states and measure the current on VCC/VCCIO pins using DCVI.

Test Pins: VCC, VCCIO

Test method:

1) Apply power.
2) Apply level and timing.
3) Set all input pins to specific state.
4) Measure the current on VCC and VCCIO
7) Datalog the results.

Limit:

Hlimit = 500 uA, Llimit = 100 uA

8. Dynamic ICC

Set the DUT to dynamic states and measure the current on VCC/VCCIO pins using DCVI.

Test Pins: VCC, VCCIO

Test method:

1) Apply power.
2) Apply level and timing.
3) Loop functional pattern at full speed

4) Measure the current on VCC and VCCIO
7) Datalog the results.

Limit:

Hlimit = 500 uA, Llimit = 100 uA

9. Frequency Counter

Create state transition on pin P40 and measure the transition frequency with frequency counter.

Test Pins: Port 2, P40, CS, PROG

Test method:

1) Apply power.
2) Apply level and timing.
3) Run a functional pattern to create multiple transitions on P40
4) Open the window for 80ms and read back the counts
7) calculate the frequency and datalog the results.

10. Rise fall time

Measure the rise time at P50 and fall time at P53 pin using characterization.

Test Pins: Port 2, P50, P53, CS, PROG

Test method:

1) Apply power.
2) Apply level and timing.
3) Run a functional pattern to set P50 to output H/L state. Measure the VOH and VOL on P50.
4) Run a functional pattern to create low to high transitions on P50
5) Find the 10%(VOH-VOL) voltage time, and the 10%(VOH-VOL) voltage time of the rising edge.
6) Calculate the rise time and datalog the results.
7) Run a functional pattern to set P53 to output H/L state. Measure the VOH and VOL on P53.
8) Run a functional pattern to create high to low transitions on P53
9) Find the 90%(VOH-VOL) voltage time, and the 10%(VOH-VOL) voltage time of the falling edge.
10) Calculate the fall time and datalog the results.

Appendix