SEG APPLICATION PROJECT

UltraFLEX Digital: I8243 MCS-48 Input Output Expander

STUDENT GUIDE

TERADYNE LINK

LEARNING
INFORMATION
NETWORKING
KNOWLEDGE

Change History

Version #	Date	Author	Comments
0.1	July 2018	Ann Yong	First Revision
1.0	Sep 2018	Jane Wang	Second Revision
2.0	Oct 2018	Ruth Ann Avila/ Sardiah Mae Mocorro	• Removed Task Guidelines and combined it under Recommended Project Work Plan • Fixed Table of Contents • Standardized Text Formatting • Additional items on appendix

Table of Contents

I. PROJECT INFORMATION

Project Objectives

1. To provide training to accelerate the learning curve as a test engineer
2. To provide turnkey project exposure including hardware design, test plan creation, coding to correlation
3. Enable jump step learning to the common tests in digital device
    - This project content focus on developing Student's device test technique and identify the tests which are commonly used in most of digital devices.
    - This project provides the Student an opportunity to develop a test program using I8243 on UltraFLEX System and develop their confidence when they extend the knowledge to a more complex digital device.
4. To develop the Student's programming and debugging skills on UltraFLEX instrument

Project Pre-requisites

Before starting this project, the Student should have:

- Completed the 1-week UltraFLEX Programming Fundamentals Class
- Knowledge on Project Management Process
- Knowledge on ATE Fundamental

Project Learning Outcomes

At the end of the assignment, the engineer should have an understanding of following learning outcomes

Basic project management

Fundamental test lists of typical digital devices
Tester resource assignment
Simple schematic design
Essential quality check and basic repeatability/ correlation

Project Duration

This program is conducted over 2-3 weeks[1] to meet the minimum requirement of the training objectives.

Provided Materials

The following materials will be provided, at the beginning of program:

- Student Handbook
- Device datasheet, PDF
- Test Plan Template, Spreadsheet file
- Sample Project Management documentation (PMP, SOW) [2]
- Other reference materials and information on the tester configuration

Once the Student completes his/her draft schematics and discussed with Mentor, the following materials will be provided:

- Recommended solution of test circuitry schematics based on actual DIB Board
- Actual DUTs (I8243 devices)
- Actual DIB Board hardware

[1] Suggested duration, assuming Student's full-time commitment
[2] PMP = Project Management Plan; SOW = Statement of Work

II. Project Terms and Conditions

The Student is required to complete the basic development Test program within a stipulated date and time agreed by the Student as well as the project supervisor.

a) Technical Mentor

A Mentor will be assigned to you during the duration of this project. His/her role is to assist the Student in the development the Student's skill in the basics of test development on the system.

The Mentor is a full-time applications engineer. The Mentor will have his/her timely commitment to this project as well.

The Student is supposed to make meeting appointments with his/her Mentor for their assistances. The Mentor's assistance will be kept to certain level since the Student is expected to be the one responsible driving the project.

b) The Student

The Student is to deliver to Mentor the deliverables as mentioned above. The Student is expected to drive the project to completion in the stipulated timeframe. The Student is expected to work closely with his/her Mentor over a certain number of contact hours.

The Student is required to meet with the Mentor (at least) once per week to update on the project progress. Also, during the coding phase of the project, the Student is advised to hold a code review session together with the Mentor once per week.

The two meetings mentioned above can either be in same or separate meeting sessions subject to the availability of both the Student and the Mentor.

The Student shall set up the meeting and send invitation to the Mentor for said meeting, preferably through IBM Notes. Clarification on issues pertaining to this project should be directed to the Teradyne Project Supervisor or the Student's Mentor.

III. Project Deliverables

Project Management Documentations

- PMP (project schedule) and SoW[3] must be created and displayed to the project supervisor prior to project work, and any schedule alterations should be immediately forwarded to your supervisor and/or Mentor.
- During the course of the project, PMP file must also be updated (at least once per week) to reflect the progress of the project, and shown to project supervisor and/or Mentor regularly (twice a week is recommended, subject to Student/Mentor's availabilities).

Test Schematics

A schematic for the device testing must be created, delivered and approved by your Mentor before the start of any coding.

Schematic Design Requirements:

1. Device pin with its corresponding tester instrument allocation
2. Include additional circuitry or components (if needed) depending on the device and test requirements
3. Able to explain the reason for assigning that tester instrument to the device pins and other additional components (if any)

Test Program

The test program must comply with the following requirements:

1. IG-XL version to be used (preferably v8.30.xx or later)
2. Written with good structure, sufficient comments, correct binning info, error handling and any other codes deemed necessary to make it a production-worthy test program.
3. Prior to its online debug phase, in offline simulation environment, run and produce offline datalog with no errors/warnings.

[3] Optional

4. Compare offline datalog and sample reference datalog[4] (if any) to ensure test limits/test names/test numbers are correct.

Data Collection

This includes the following items once the program is debugged and fine-tuned to its best status.

Quality Check/Correlation Items:

a) Test Flow Check

   Test program check on test name, test number, limits and binning

b) Open Socket Check

   - DC Test – measurement should FAIL. If PASS need to explain why.
   - Functional Test – result should FAIL. If PASS need to explain why.

c) Repeatability Data (50 loops)

   - All tests should pass during the 50 loop runs.
   - Cp/Cpk > = 2

d) Waveform and Shmoo Captures

   - Waveform - must match the device datasheet timing diagram
   - Shmoo - to identify device functional passing margin

Wrap-Up Presentation

As the last phase of the program, the Student is to give presentation to Mentor/supervisor to share things learned and to give feedback on the program. Refer to "Project Presentation Template"[5]for a recommended presentation agenda.

[4] Refer to Appendix
[5] Refer to Appendix

IV. Project Details

Test List of I8243

1. Shorts Test Using Dynamic Loads
2. Opens Test Using Dynamic Loads
3. Parametric Continuity Test
4. Static Icc Test
5. Dynamic Icc Test
6. Input Low Leakage Test on port2 and control pins
7. Output tristate leakage on port4-7
8. Full Functional Test
   - At Vccnom
   - At Vccmin
   - At Vccmax

   Pattern should:

   - do a write of pattern 1010 to port 4-7

   - do an 'and' of 1110 port 4-7

   - do an 'or' of 0011 to port 4-7
9. Rise/Fall time tests
   - Rise/Fall time tests using characterization method
   - Modify the patterns and workbook to perform a rise time and a fall time test
   - Modify the following sheets:
     - Levels sheet
     - Timing sheet
     - Test Instances
     - Characterization
     - Flow Table
   - To perform:

- A rise time measurement for pin p50
- A fall time measurement for pin p53

Rise time measurement for pin p50

- Do a level adjust characterization to find actual VOL and VOH values
- Overlay the actual values of VOL and VOH using rise time pattern containing a 'L' to 'M' search for pin P50.
- Find 10% and 90% points on rising edge
- Write an interpose function to calculate the rise time

Fall Time measurement for pin p53

- Modify rise time pattern to include a vector searching for Midband ('M') from a 'H' for pin p53
- Use the same level adjust characterization to find VOH and VOL values
- Overlay the new actual values of VOH and VOL
- Find 90% and 10% points on falling edge
- Write an interpose function to calculate the fall time

10. Frequency Counter Test[6]

- Modify the pattern and workbook to setup the frequency counter mode for pins p40 and p41.
- Create 2 frequency counter tests with the following criteria:
  a. Create/Measure in pin p40
     - Vector period = 1us. Result = 2.5kHz.
  b. Create/Measure in pin p41.
     - Vector period = 1us. Result is 1.25kHz.

11. Scan Test[7]

- Create a scan pattern that uses pins (p20,p21 & p23) as the scan in pins and pins(p40, p51 & p53) as the scan out pins.
- The scan pattern should do the following
  - scan in pin : p23 pattern is 0101 (1 bit and using symbol)
  - scan out pin : p43 pattern is LHLH (1 bit and using symbol)
  - scan in pin : p20 pattern is C9A (1 bit and using Hex)

[6] Optional
[7] Optional

- scan out pin : p40 pattern is XXXXXX (2 bit and using Hex)
- scan in pin : p21 pattern is 0101 (1 bit and using symbol)
- scan out pin : p51 pattern is LHLH (1 bit and using symbol)
- scan in pin : p23 pattern is C9A (1 bit and using Hex)
- scan out pin : p53 pattern is XXXXXX (2 bit and using Hex)

Recommended Project Work Plan

PRE-WORK

1. Go through the Student Handbook.
2. Complete Skills Assessment Form (Before) in Handbook excel document.
3. Setup SVN/Oasis for revision control of test program.[8]
4. Complete the Test Plan on the excel Spreadsheet.
5. Understand the project objectives and review materials.
   - Device Datasheet
   - Create test Plan using the Test Plan Template provided
   - Complete Instruments Estimation Table (IET) and review with Mentor
6. Produce a scope of work (SOW)[9] and project schedule (PMP) for all planned activities
7. Book tester time for the debugging activities.

MAIN WORK

8. Design test schematic for this project. The IET completed in Pre-Work phase will be a good reference.

   The following procedures are:

   - Submit draft schematics to Mentor for review
   - Implement necessary changes on the schematic based on Mentor's feedback (if any)

[8] Refer to Test Program Requirements under Project Deliverables section
[9] Optional

- After approval from Mentor, official schematics (based on actual DIB Board) will be released to you. Compare this with own version and prepare to start the test program coding.

9. Develop test program[10]
10. Weekly progress updates / code review session with Mentor and/or supervisor
11. Online debug Test Program till achieve Bin 1
    - Hints if tests still FAIL:
        - Add settling time or wait time for experiment
        - Add longer period for functional tests to check stability
        - Re-check waveform diagram compare to device timing diagram
        - Use external tool (example multimeter, oscilloscope to counter verify the program settings)
        - Check power up sequence if any
12. Collect datalog
13. Perform necessary quality check and correlation items[11]
14. Show all the works done to Mentor and review result.

POST- WORK

15. Prepare for Wrap-Up Presentation with Mentor and/or supervisor[12]
16. Complete "Skill Self-Assessment Form (**After** Project)"
17. Submit final test program and all deliverables to Mentor and/or supervisor
18. Upload to SVN

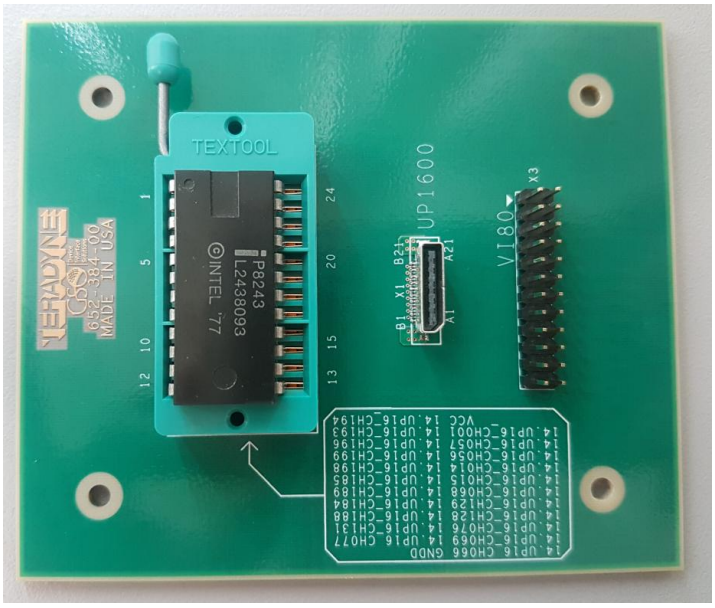
[10] Refer to Test Program Requirements under Project Deliverables section
[11] Refer to Data Collection details under Project Deliverables section
[12] Refer to Project Presentation Template under Appendix

V. APPENDIX

Device Datasheet

Student package\Project References\Datasheet

I8243 Single Site Daughter Board



Simulated Config

- Used for offline coding

Student package\ Project References \Simulated Config

Reference Datalog

Student package\ Project References \Teradyne_IG-XL_DataCollect_9328 (Digital)

Project Presentation Template

Student package\Project Presentation Template

Sample SVN/Oasis Structure