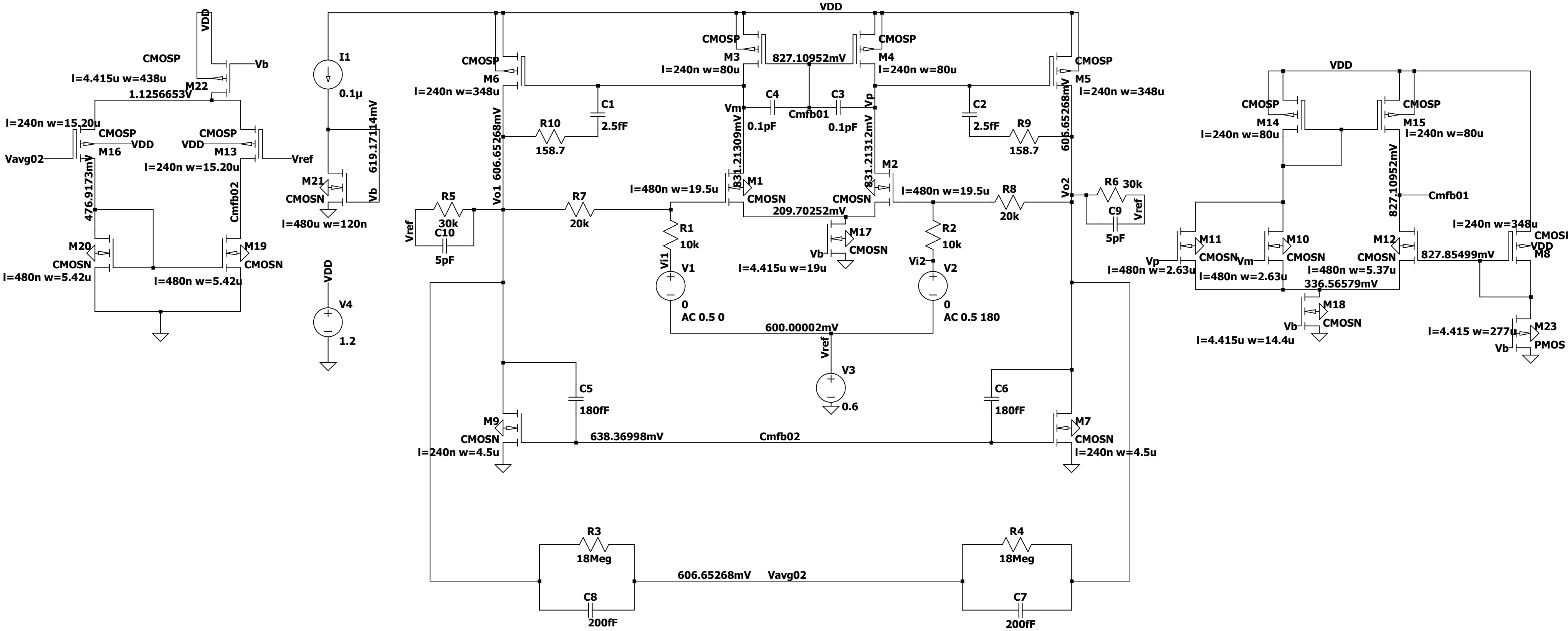


VDD
CMOSP
Vb
l=4.415u w=438u
M22
1.1256653V
l=240n w=15.20u
CMOSP
CMOSP
M16
VDD
VDD
M13
Vref
Vavg02
l=240n w=15.20u
476.9173mV
Cmfb02
M20
M19
CMOSN
CMOSN
l=480n w=5.42u
l=480n w=5.42u
I1
0.1µ
619.17114mV
M21
CMOSN
Vb
l=480u w=120n
VDD
V4
1.2
CMOSP
M6
l=240n w=348u
C1
2.5fF
R10
158.7
Vo1 606.65268mV
R5
30k
Vref
C10
5pF
R7
20k
CMOSP
M3
l=240n w=80u
827.10952mV
CMOSP
M4
l=240n w=80u
Vm
C4
0.1pF
Cmfb01
C3
0.1pF
Vp
831.21309mV
831.21312mV
M1
M2
l=480n w=19.5u
CMOSN
CMOSN
l=480n w=19.5u
209.70252mV
M17
Vb
CMOSN
l=4.415u w=19u
R1
10k
Vi1
V1
0
AC 0.5 0
R2
10k
Vi2
V2
0
AC 0.5 180
600.00002mV
Vref
V3
0.6
CMOSP
M5
l=240n w=348u
C2
2.5fF
R9
158.7
606.65268mV
R8
20k
Vo2
R6
30k
C9
5pF
Vref
C5
180fF
M9
CMOSN
l=240n w=4.5u
638.36998mV
Cmfb02
C6
180fF
M7
CMOSN
l=240n w=4.5u
R3
18Meg
C8
200fF
606.65268mV
Vavg02
R4
18Meg
C7
200fF
VDD
CMOSP
M14
l=240n w=80u
CMOSP
M15
l=240n w=80u
827.10952mV
Cmfb01
l=240n w=348u
CMOSP
VDD
M8
M11
M10
M12
Vp
CMOSN
Vm
CMOSN
CMOSN
l=480n w=2.63u
l=480n w=2.63u
l=480n w=5.37u
827.85499mV
336.56579mV
M18
Vb
CMOSN
l=4.415u w=14.4u
l=4.415 w=277u
M23
Vb
PMOS

(c)

As in project 1 I used gm/Id Methodology to Size of transistor and currents:
Same Methodology I used here and I used Same transistor size for Differential State and for CMFB1

⇒ for transistor characterisation
I calculate $\frac{gm}{gds}$ vs $\frac{gm}{Id}$, $\frac{gm}{Id}$ vs $\frac{I_D}{W}$ for differnt different length (lmin, 2×lmin. 3lmin ...) at different biasing for both PMOS and NMOS and then curve fit and interpolation.

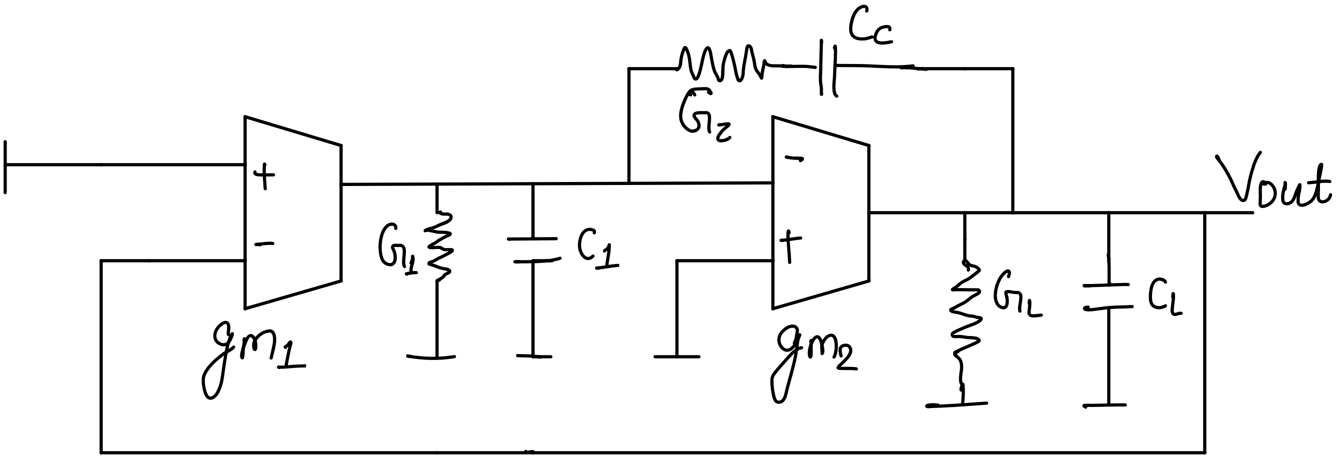
⇒ for NO peaking I assume PM > 60°

⇒ for Steady State error less < 1% take gain > 40dB (as shown in next page)

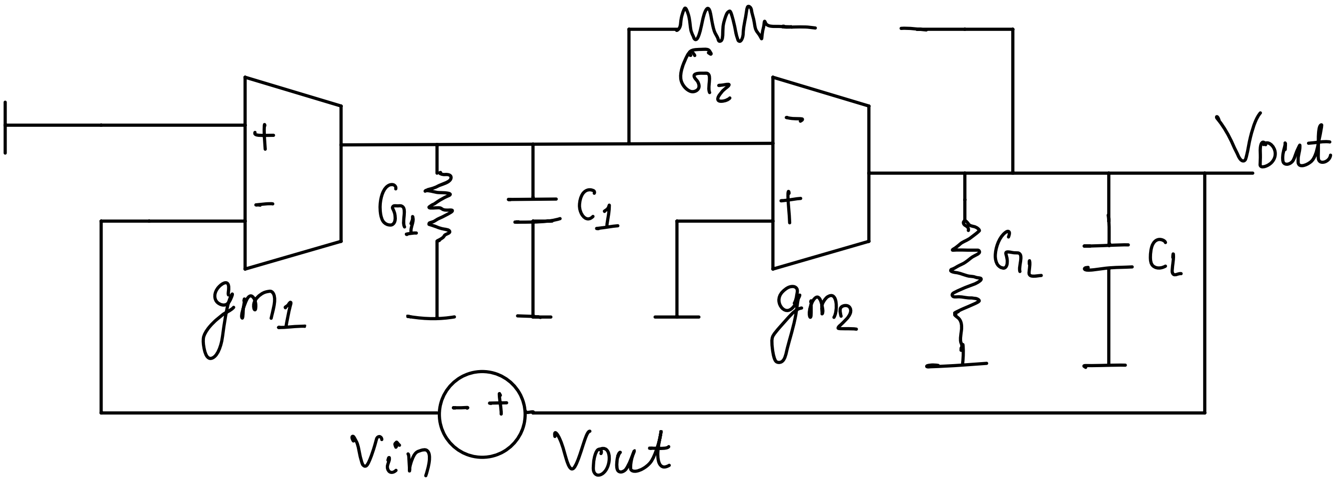
Steady State error < 1%

$$\frac{1}{|\text{DC loop gain}|} \leq \frac{1}{100}$$

$$\text{DC loop gain} > 100 \Rightarrow \text{loop gain} \geq 40\,\text{dB}$$



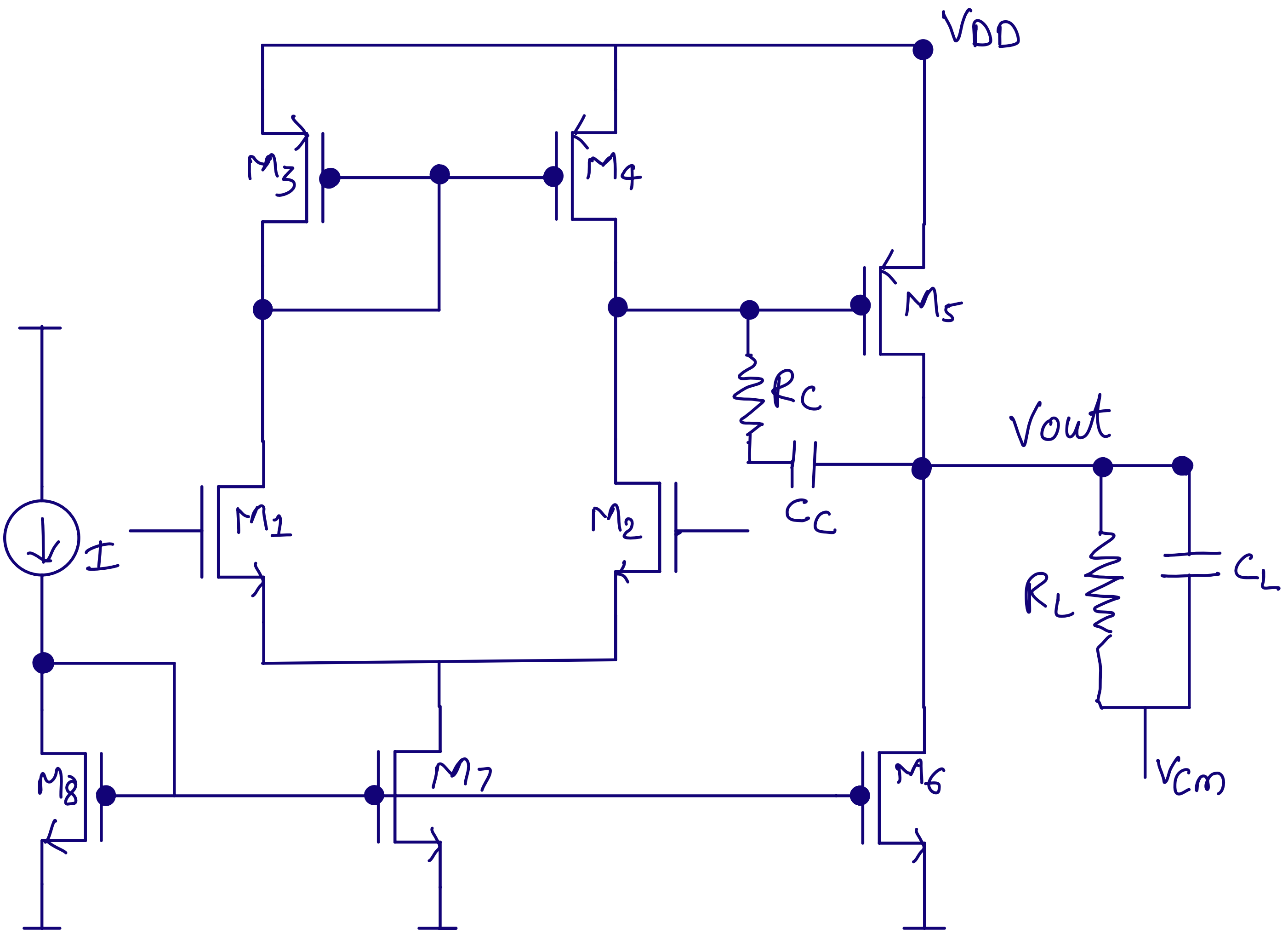
Block Diagram



Block Diagram for DC loop gain

$$A_0 = \frac{g_{m_1} g_{m_2}}{G_1 \cdot G_L} = \text{DC loop gain}$$

$$\text{loop gain} = \frac{g_{m_1}}{g_{ds_2} + g_{ds_4}} \times \frac{g_{m_2}}{(g_{ds_5} + g_{ds_6} + G_L)}$$



Assume Phase Margin > 60° So that there is no peaking

Take PM = 76° (with margin) and taking $\omega_u = 50MHz$

$$\Rightarrow \quad PM = 90° - \tan^{-1}\left(\frac{\omega}{P_2}\right)$$

$$76° = 90° - \tan^{-1}\left(\frac{\omega}{P_2}\right)$$

$$\frac{\omega_u}{P_2} = \tan(14°) = 0.2493$$

$$\Rightarrow \quad P_2 = 1260.165 \times 10^6 \text{ rad/sec}$$

$$P_2 = \frac{g_{m_2}}{C_L} \Rightarrow g_{m_2} = 1260.165 \times 10^6 \times 5 \times 10^{-12}$$

$$= 6.3 \text{ m/s}$$

$\Rightarrow$ assume C_c some % of C_L = 3PF

$\Rightarrow$ $g_{m1} = \omega_u \times C_c = 100\pi \times 3 \times 10^{-12} = 0.942\ m/s$

From g_m/g_{ds} Vs $\frac{g_m}{I_d}$ / for $L = 480n$

assume $g_{ds1} = g_{ds2}$
$= 12.4\mu/s$

$\frac{g_{m1}}{g_{ds1}} = 75.8$

Corresponding $g_m/I_d = 11.7 \Rightarrow I_d = 80.55\ \mu A$

and from $\frac{g_m}{I_d}$ Vs $\frac{I_d}{W}$

$\frac{I_d}{W} = 15 \Rightarrow W = 5.37\ \mu m$

$\Rightarrow$ for Second Stage at $L = 240nm$

from $\frac{g_{m2}}{g_{ds2}} = 36.9 \Rightarrow g_{ds2} = 1.7 \times 10^{-4}/s$

Corresponding $\frac{g_{m2}}{I_d} = 18.1$

$\Rightarrow I_d = 348\mu A$

Corresponding $\frac{I_D}{W}$ ($\frac{g_{m2}}{I_d}$ Vs $\frac{I_D}{W}$)

$\frac{I_D}{W} = 1 \Rightarrow W = 348\ \mu m$

$$A_0 = \frac{g_{m1}\ g_{m2}}{2g_{ds1}(g_{ds5} + G_L)}$$

$\left\{ g_{ds} + G_L = 1.7 \times 10^{-4} + 10 \times 10^{-3} \right.$

$$= \frac{0.946 \times 10^{-3} \times 6.3 \times 10^{-3}}{2 \times 12.4 \times 10^{-6} \times 2.7 \times 10^{-4}}$$

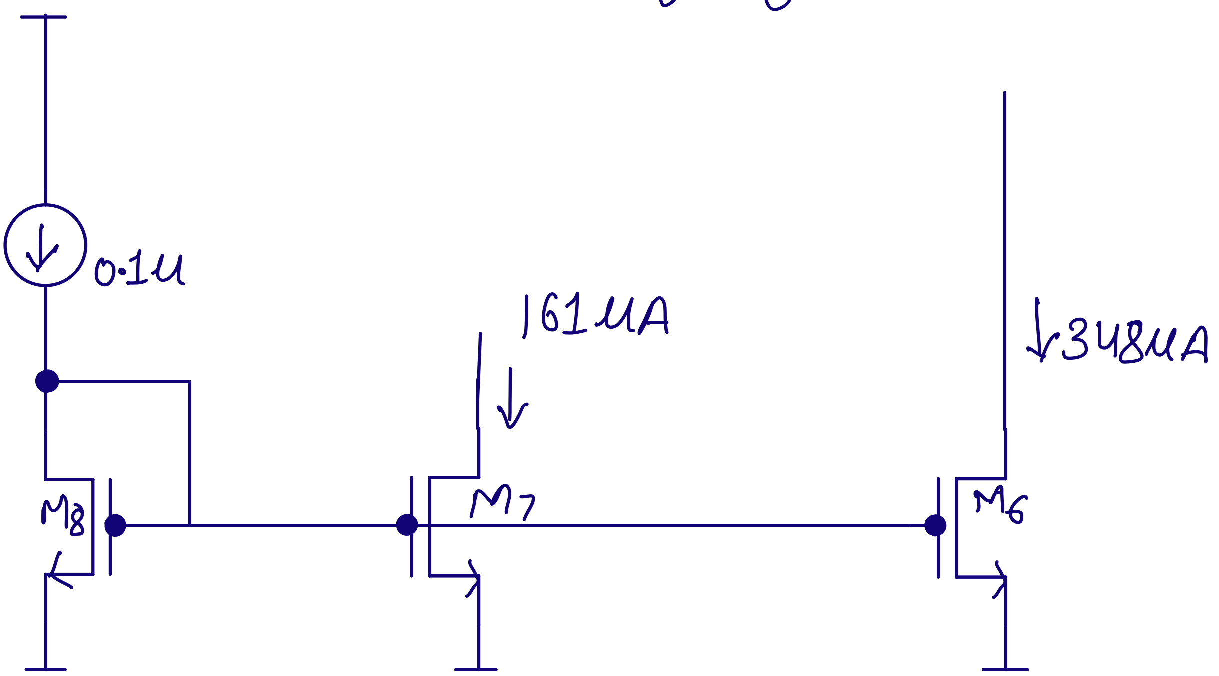
$A_o = 886.29$

$$\Rightarrow \left(\frac{I_d}{W}\right)_5 = \left(\frac{I_d}{W}\right)_{3,4}$$ So that no DC offset

$$1 = \left(\frac{80\,uA}{W}\right)$$

$\Rightarrow W = 80\,um$

Now biasing and Sizing of Tail Transistors



Choose the W.L So that it mirror in proper way

$\Rightarrow$ for CMFB2

I design P-Mos input 2 stage Miller amplifier. Similar fashion I design the sizes of transister and Calculation are below

$\Rightarrow$ assume PM = 70°

$$70 = 90° - \tan^{-1}\left(\frac{\omega_u}{P_2}\right)$$

$$\frac{\omega_u}{P_2} = 0.3639 \Rightarrow P_2 = \frac{\omega_u}{0.3639}$$

$$P_2 = \frac{g_{m2}}{C_L} = \frac{\omega_u}{0.3639}$$

$$g_{m_2} = 4.57 \text{ mS}$$

$$\omega_u = \frac{g_{m_1}}{C_c} \quad (C_c = 3\text{pF}$$

$$g_{m_1} = 0.999 \text{mS}$$

from g_m/g_{ds} Vs $\frac{g_m}{I_d}$ for L=240nm

$$\frac{g_{m_1}}{g_{ds}} = 34.88 \quad \text{Corresponding } \frac{g_{m_1}}{I_d} = 9.12$$

$$\Rightarrow I_d = 109.54 \, \mu A$$

$$\Rightarrow \frac{I_D}{W} = 7.2 \Rightarrow W = 15.20 \, \mu m$$

for second stage (L=480

$$\frac{g_{m2}}{g_{ds}} = 70.17 \Rightarrow \frac{g_{m_2}}{I_d} = 9.687$$

$\Rightarrow I_d = 472.104 \mu A$ Corresponding $\frac{I_d}{W} = 20.188$

$\frac{I_d}{W} = 20.188 \Rightarrow W = 23.394 \mu m$

$$\left(\frac{I_d}{W}\right)_{\text{first Stage}} = \left(\frac{I_d}{W}\right)_{\text{second Stage}}$$

$$20.188 = \frac{I_d}{W} \Rightarrow W = \frac{109.54 \mu A}{20.188}$$

$$\boxed{W = 5.42 \mu m}$$

But the gain for 1st stage was not as required value so I tweek the size of transistor and C_c capacitor for PM and W_u.

ⓓ Block level design

	Gm	Rc(Ω)	Cc	G_1
First stage	0.942 m/s	158.7	2.5PF	24.8 uS
Second stage	6.3 m/s			.27 uS
CMFB 1	0.942 m/s	—	0.1PF	—
CMFB 2	0.999 m/s	18 MΩ	200PF	—

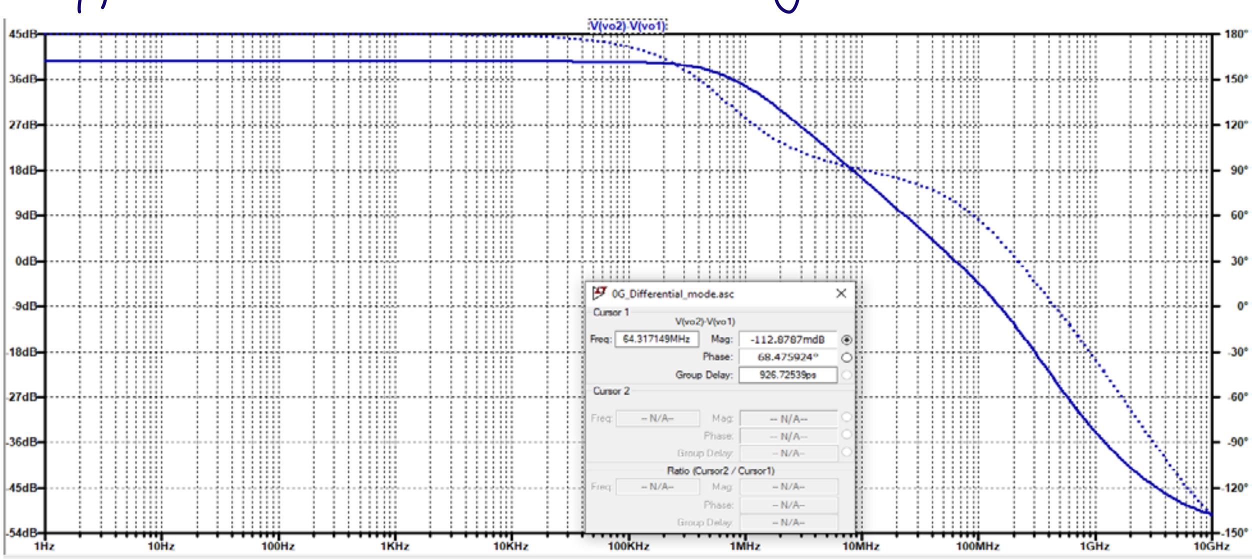
(e) Transistor level design

Transistor	width(um)	length(um)
M_1	19.5	0.480
M_2	19.5	0.480
M_3	80	0.240
M_4	80	0.240
M_5	348	0.240
M_6	348	0.240
M_7	4.5	0.240
M_8	348	0.240
M_9	4.5	.240
M_{10}	2.63	0.480
M_{11}	2.63	0.480
M_{12}	5.37	0.480
M_{13}	15.20	0.240
M_{14}	80	0.240
M_{15}	80	0.240
M_{16}	15.20	0.240
M_{17}	19	4.415
M_{18}	14.44	4.415
M_{19}	5.42	0.480
M_{20}	5.42	0.480
M_{21}	0.120	480
M_{22}	438	4.415

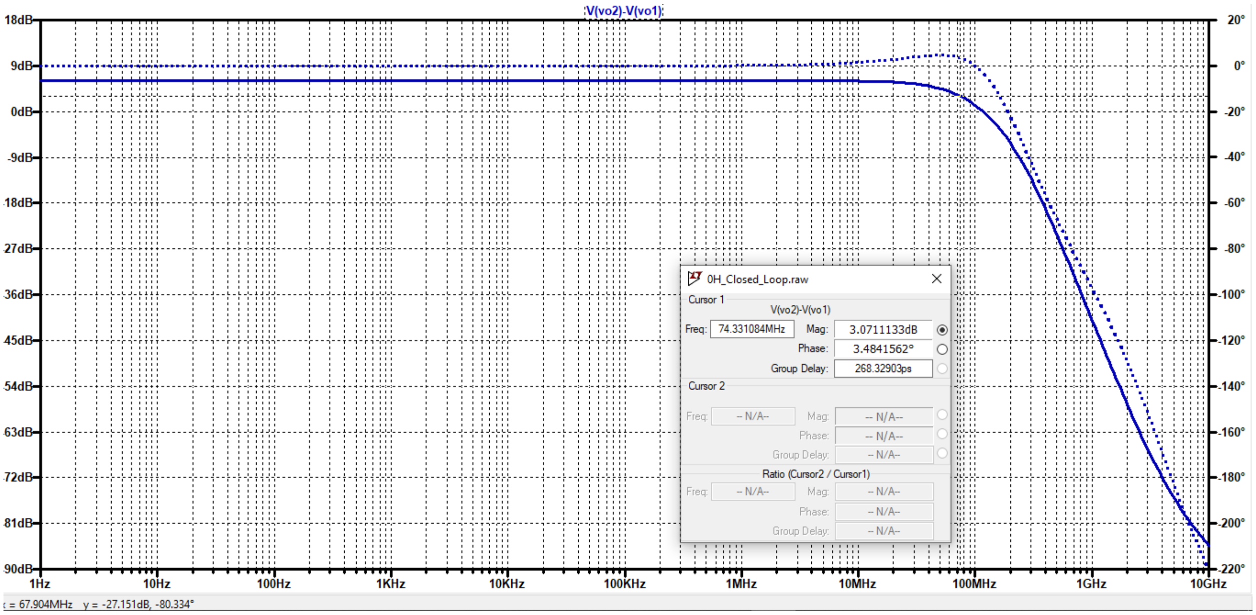
f

Name:	m1	m2	m3	m4	m5	m6	m7	m9
Model:	cmosn	cmosn	cmosp	cmosp	cmosp	cmosp	cmosn	cmosn
Id:	8.05E-05	8.05E-05	-8.05E-05	-8.05E-05	-3.63E-04	-3.63E-04	3.63E-04	3.63E-04
Vgs:	3.93E-01	3.93E-01	-3.73E-01	-3.73E-01	-3.69E-01	-3.69E-01	6.38E-01	6.38E-01
Vds:	6.22E-01	6.22E-01	-3.69E-01	-3.69E-01	-5.93E-01	-5.93E-01	6.07E-01	6.07E-01
Vbs:	-2.10E-01	-2.10E-01	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00
Vth:	2.61E-01	2.61E-01	-3.30E-01	-3.30E-01	-3.25E-01	-3.25E-01	2.88E-01	2.88E-01
Vdsat:	9.47E-02	9.47E-02	-8.80E-02	-8.80E-02	-8.89E-02	-8.89E-02	2.04E-01	2.04E-01
Gm:	1.60E-03	1.60E-03	1.55E-03	1.55E-03	6.96E-03	6.96E-03	1.81E-03	1.81E-03
Gds:	1.08E-05	1.08E-05	4.01E-05	4.01E-05	1.75E-04	1.75E-04	5.32E-05	5.32E-05
Gmb	1.92E-04	1.92E-04	2.15E-04	2.15E-04	9.54E-04	9.54E-04	2.12E-03	2.12E-03
Cbd:	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00
Cbs:	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00
Cgsov:	7.86E-15	7.86E-15	3.10E-14	3.10E-14	1.35E-13	1.35E-13	1.80E-15	1.80E-15
Cgdov:	7.86E-15	7.86E-15	3.10E-14	3.10E-14	1.35E-13	1.35E-13	1.80E-15	1.80E-15
Cgbov:	4.59E-17	4.59E-17	2.25E-17	2.25E-17	2.25E-17	2.25E-17	2.19E-17	2.19E-17
dQgdVgb:	9.30E-14	9.30E-14	1.95E-13	1.95E-13	8.47E-13	8.47E-13	1.26E-14	1.26E-14
dQgdVdb:	-7.87E-15	-7.87E-15	-2.88E-14	-2.88E-14	-1.25E-13	-1.25E-13	-1.79E-15	-1.79E-15
dQgdVsb:	-8.12E-14	-8.12E-14	-1.56E-13	-1.56E-13	-6.80E-13	-6.80E-13	-1.73E-14	-1.73E-14
dQddVgb:	-3.94E-14	-3.94E-14	-8.20E-14	-8.20E-14	-3.57E-13	-3.57E-13	-5.34E-15	-5.34E-15
dQddVdb:	7.88E-15	7.88E-15	3.00E-14	3.00E-14	1.30E-13	1.30E-13	1.80E-15	1.80E-15
dQddVsb:	3.59E-14	3.59E-14	5.92E-14	5.92E-14	2.58E-13	2.58E-13	7.36E-15	7.36E-15
dQbdVgb:	-1.41E-14	-1.41E-14	-3.06E-14	-3.06E-14	-1.33E-13	-1.33E-13	-1.90E-15	-1.90E-15
dQbdVdb:	-1.50E-17	-1.50E-17	-1.71E-16	-1.71E-16	-5.79E-16	-5.79E-16	-1.05E-17	-1.05E-17
dQbdVsb:	1.55E-15	1.55E-15	6.90E-15	6.90E-15	2.93E-14	2.93E-14	7.79E-16	7.79E-16

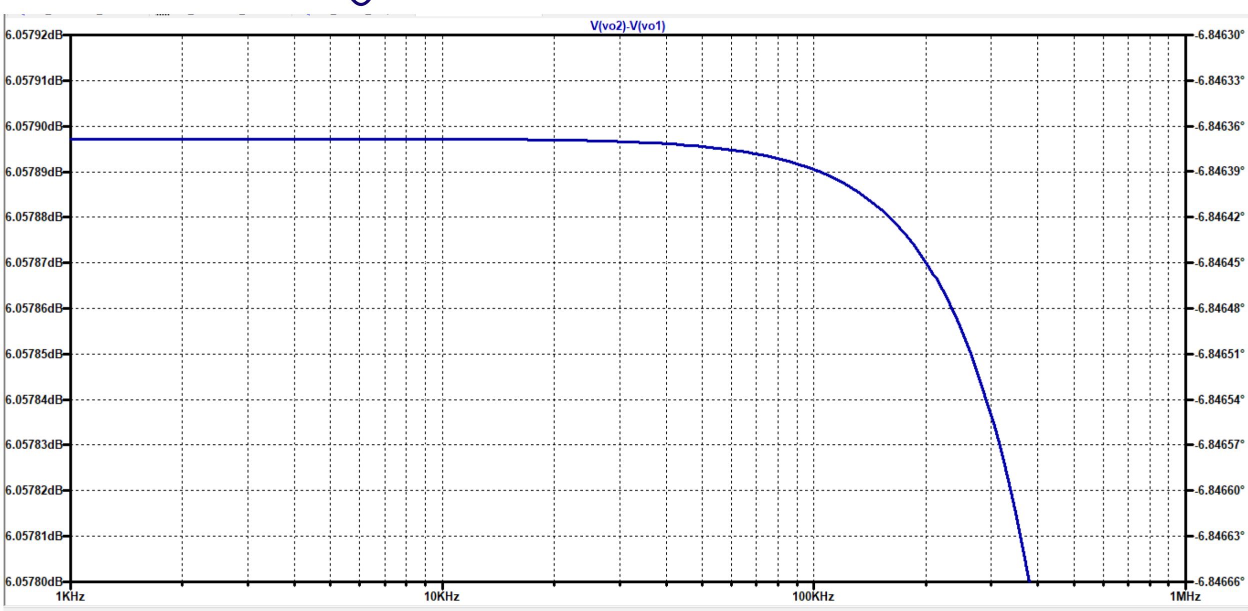
G Differential Mode loop gain



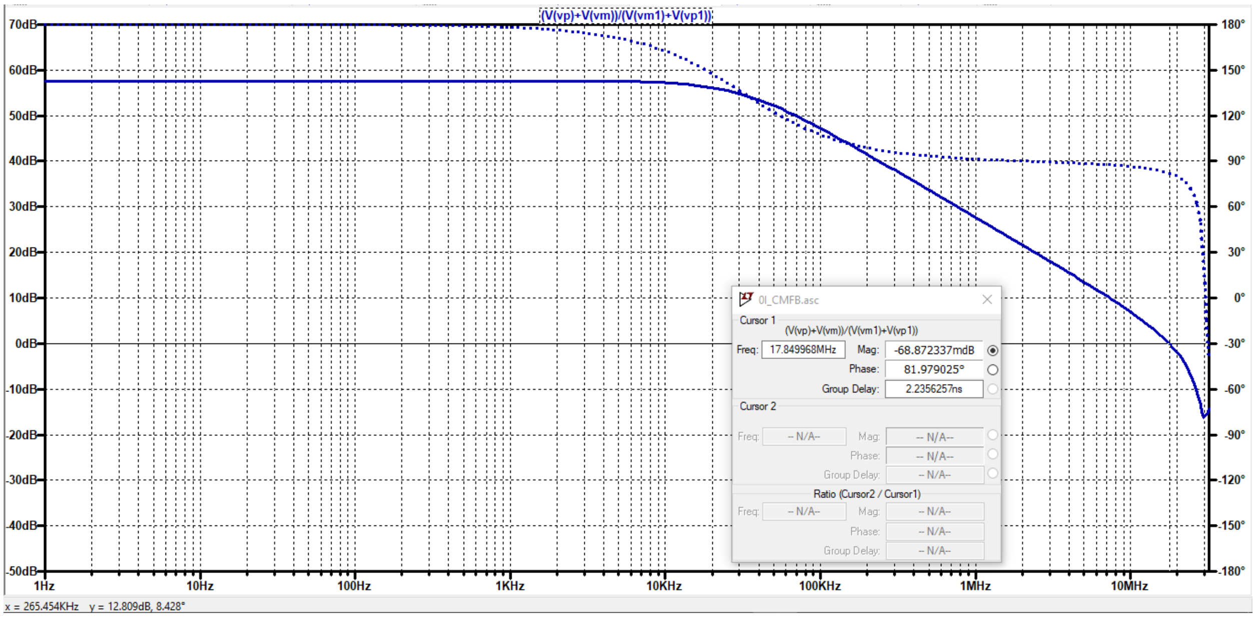
(h) closed loop frequency response



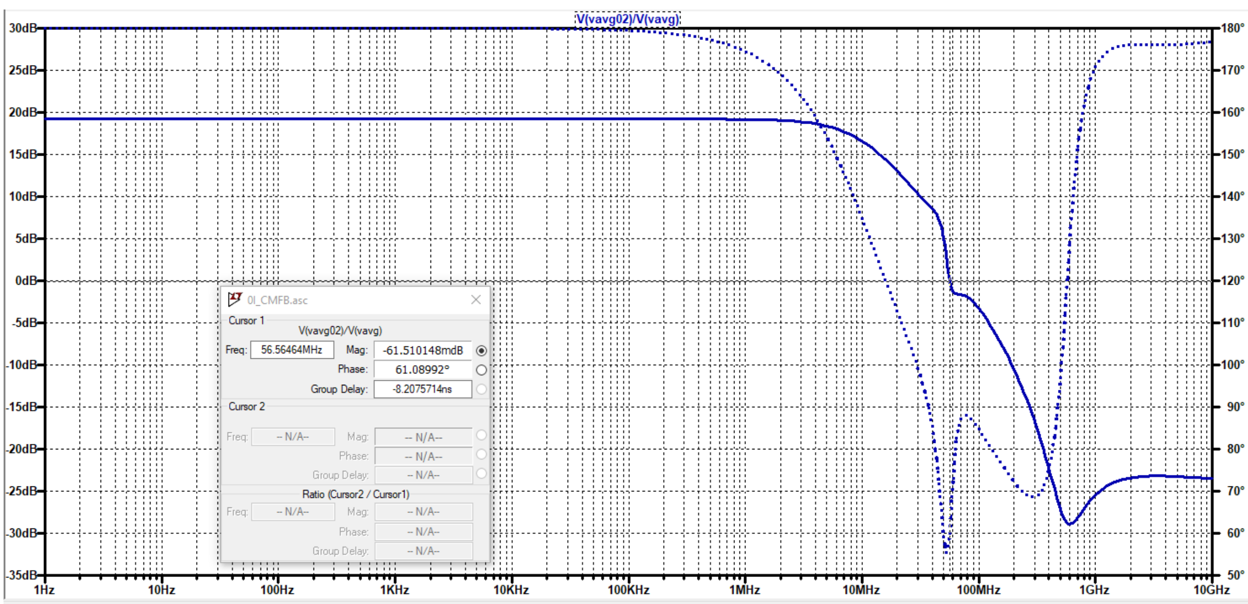
Zoomed version of above for no peaking



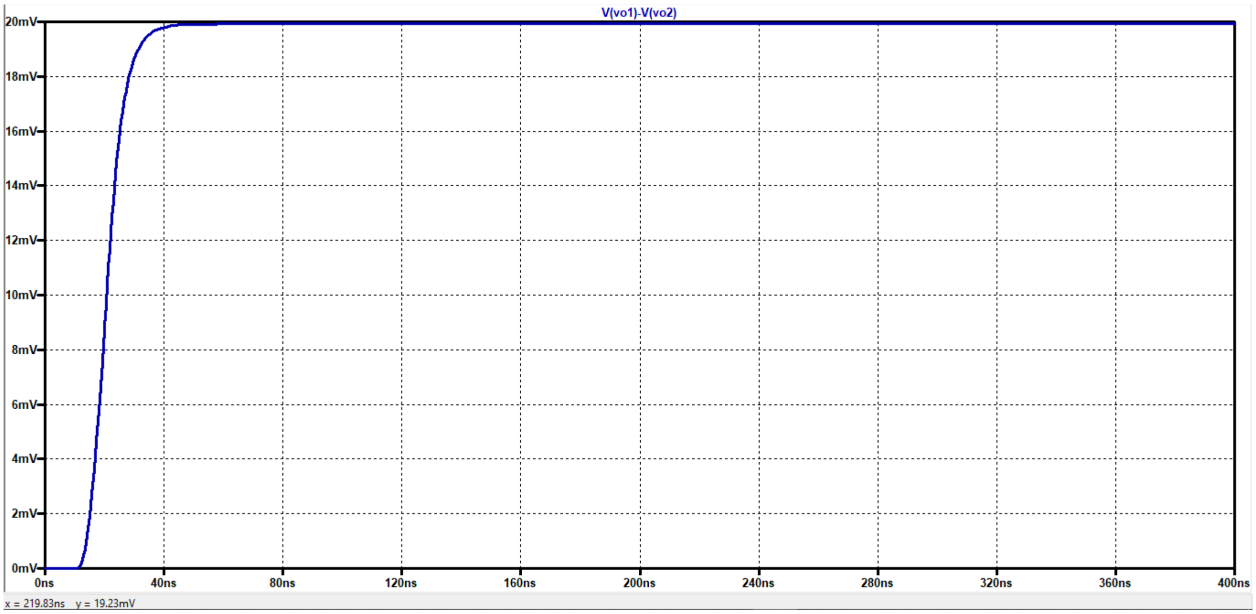
① CMFB1 loop gain



CMFB2 loop gain



(j) Differential Step



(k) Common mode step