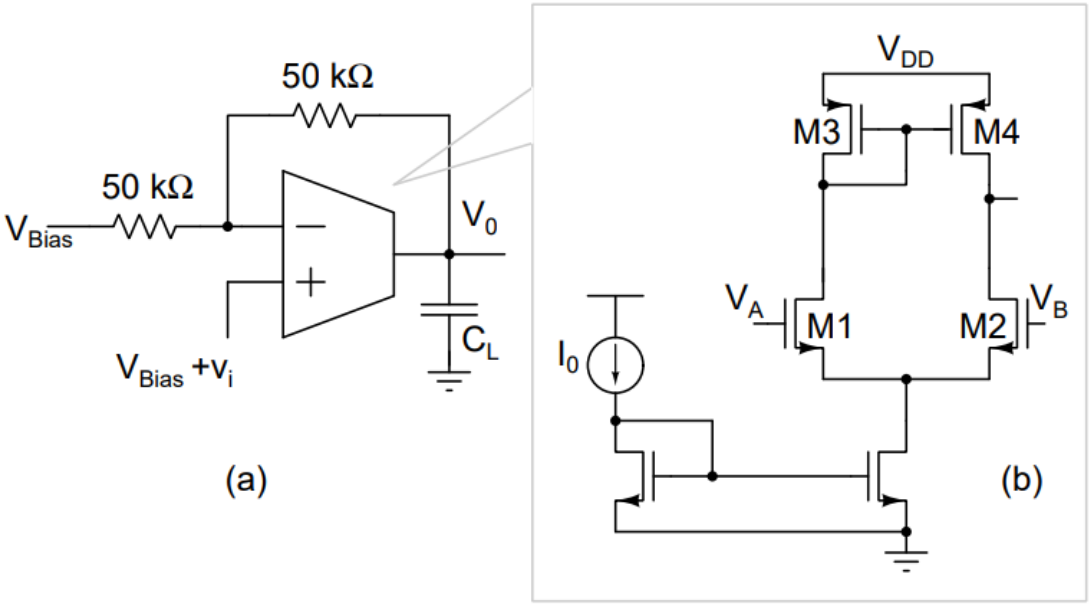
EE610A: Analog VLSI Circuits
Project / Simulation Assignment

Submitted by : Rahul Kumar Gupta
(21204408)

Specifications:

Input stage	VDD	CL	Loop gain (min)	–3dB Bandwidth of V0/Vi (min)	CMRR(@dc)
NMOS	1.8V	10pF	40 dB	100MHz	80dB



*Given prototype

Fig. 1. (a) Top level of the opamp. (b) Prototype internal schematic (without zero cancelling resistor). (c) CMFB of first stage. (d) CMFB of second stage.

DESIGN METHODOLOGY

1. At first, I designed and tried to achieve the specifications by a simple Differential Amplifier structure as provided in the prototype schematic.

2. With theoretical calculations, the prototype circuit had the $w_{u,loop}$ at $g_m/2*pi*C_L$ ie. 100MHz(as per the specs)
   C_L = 10pF(fixed)
   g_m= 2*pi mS

3. Since the specifications were not met with that design(even after bringing g_m to the desired value), I switched to telescopic cascode structure to increase R_{out} in order to achieve a high gain.

4. Also I used the below mentioned three relations to tweak the circuit and achieve the mentioned specifications.

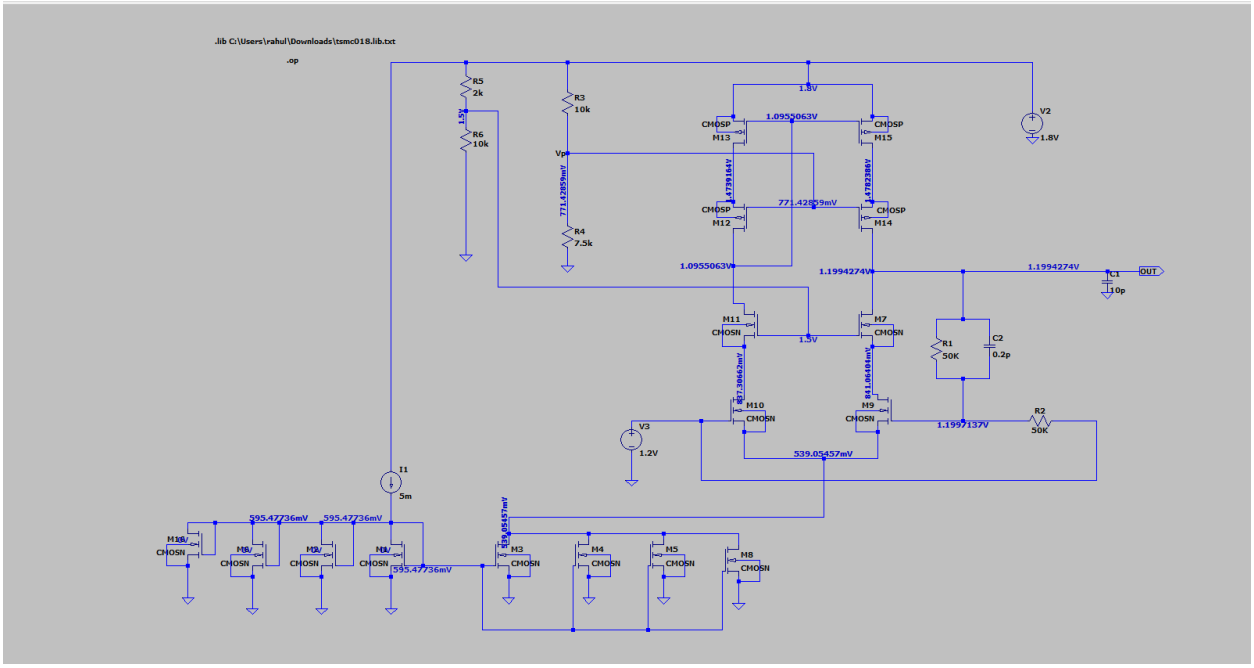
$$g_m = \sqrt{2\mu_n C_{ox} \frac{W}{L} I}$$

$$\frac{g_m}{g_{DS}} \propto \sqrt{\frac{WL}{I}}$$

$$V_{OV} = \sqrt{\frac{2I}{\mu_n C_{ox} \frac{W}{L}}}$$

5. At first I tried to achieve the desired g_m value using the first relation and then I tried to get a high gain while keeping the gm almost constant.

Design



6. I also had to make two changes:

   i) In the current mirror pulling down current, I had to increase the W/L of the transistors in order to match their Drain and Gate voltages → for better current mirroring.
   In order to keep the NMOS transistors all the same , I added more NMOS transistors and connected them in parallel.

   ii) In the feedback path, I added a Capacitor to introduce a pole.
   It was done to **cancel** the zero which affected the V_o/V_i plot at high frequencies.
   The value of the capacitor was determined by approximate analysis and simulations.

Name:	m15	m14	m13	m12	m16
Model:	cmosp	cmosp	cmosp	cmosp	cmosn
Id:	-2.48e-03	-2.48e-03	-2.48e-03	-2.48e-03	1.25e-03
Vgs:	-7.04e-01	-7.07e-01	-7.04e-01	-7.02e-01	5.95e-01
Vds:	-3.22e-01	-2.79e-01	-3.26e-01	-3.78e-01	5.95e-01
Vbs:	0.00e+00	0.00e+00	0.00e+00	0.00e+00	0.00e+00
Vth:	-4.56e-01	-4.56e-01	-4.56e-01	-4.56e-01	4.64e-01
Vdsat:	-2.02e-01	-2.04e-01	-2.02e-01	-2.01e-01	1.10e-01
Gm:	1.81e-02	1.77e-02	1.81e-02	1.84e-02	1.68e-02
Gds:	8.23e-04	1.15e-03	8.02e-04	6.15e-04	1.99e-04
Gmb	5.61e-03	5.51e-03	5.62e-03	5.69e-03	4.58e-03
Cbd:	0.00e+00	0.00e+00	0.00e+00	0.00e+00	0.00e+00
Cbs:	0.00e+00	0.00e+00	0.00e+00	0.00e+00	0.00e+00
Cgsov:	2.70e-13	2.70e-13	2.70e-13	2.70e-13	1.48e-13
Cgdov:	2.70e-13	2.70e-13	2.70e-13	2.70e-13	1.48e-13
Cgbov:	3.01e-19	3.01e-19	3.01e-19	3.01e-19	3.26e-19

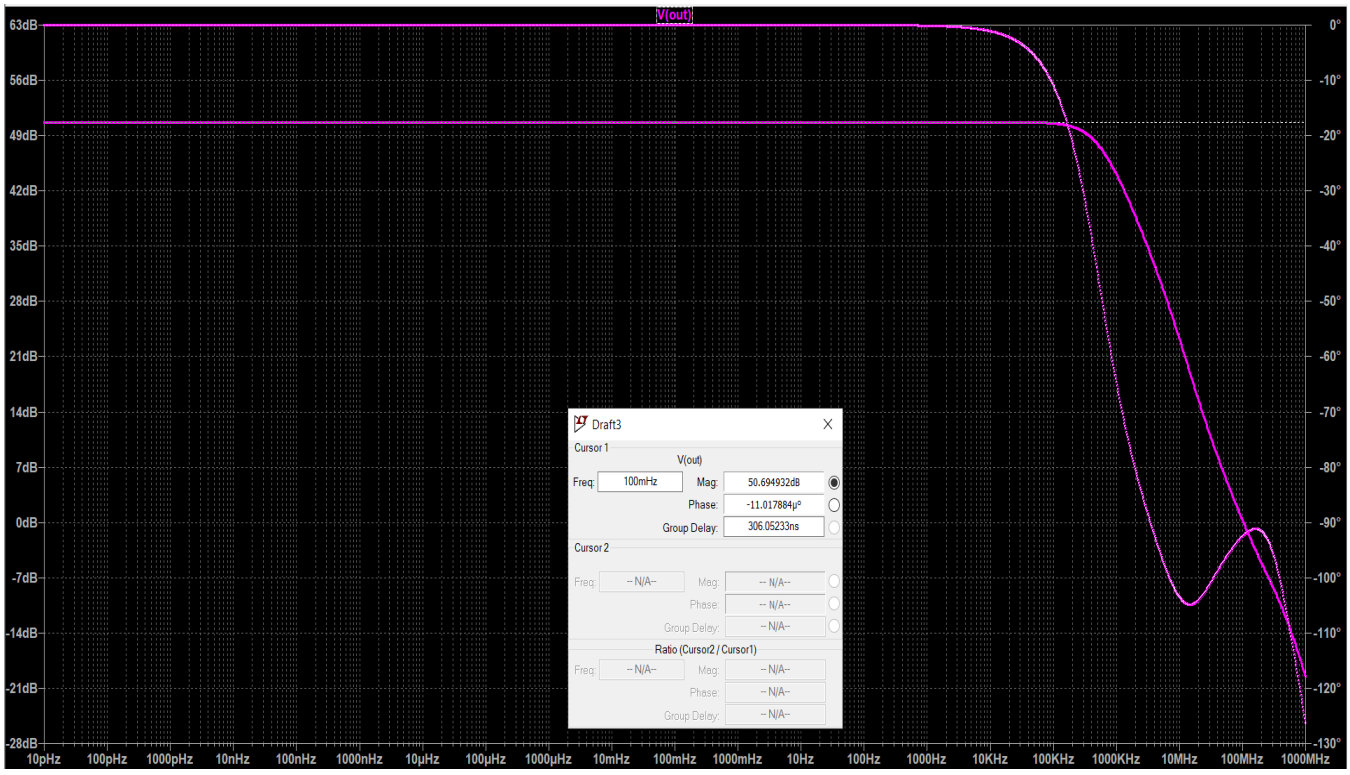
Name:	m11	m10	m9	m7	m3
Model:	cmosn	cmosn	cmosn	cmosn	cmosn
Id:	2.48e-03	2.48e-03	2.48e-03	2.48e-03	1.24e-03
Vgs:	6.63e-01	6.61e-01	6.61e-01	6.59e-01	5.95e-01
Vds:	2.58e-01	2.98e-01	3.02e-01	3.58e-01	5.39e-01
Vbs:	0.00e+00	0.00e+00	0.00e+00	0.00e+00	0.00e+00
Vth:	4.66e-01	4.66e-01	4.66e-01	4.65e-01	4.64e-01
Vdsat:	1.48e-01	1.47e-01	1.47e-01	1.46e-01	1.10e-01
Gm:	2.32e-02	2.36e-02	2.36e-02	2.39e-02	1.67e-02
Gds:	1.20e-03	8.76e-04	8.53e-04	6.25e-04	2.10e-04
Gmb	6.28e-03	6.38e-03	6.38e-03	6.46e-03	4.55e-03
Cbd:	0.00e+00	0.00e+00	0.00e+00	0.00e+00	0.00e+00
Cbs:	0.00e+00	0.00e+00	0.00e+00	0.00e+00	0.00e+00
Cgsov:	1.48e-13	1.48e-13	1.48e-13	1.48e-13	1.48e-13
Cgdov:	1.48e-13	1.48e-13	1.48e-13	1.48e-13	1.48e-13
Cgbov:	3.26e-19	3.26e-19	3.26e-19	3.26e-19	3.26e-19

Name:	m1
Model:	cmosn
Id:	1.25e-03
Vgs:	5.95e-01
Vds:	5.95e-01
Vbs:	0.00e+00
Vth:	4.64e-01
Vdsat:	1.10e-01
Gm:	1.68e-02
Gds:	1.99e-04
Gmb	4.58e-03
Cbd:	0.00e+00
Cbs:	0.00e+00
Cgsov:	1.48e-13
Cgdov:	1.48e-13
Cgbov:	3.26e-19

Name:	m8	m6	m5	m4	m2
Model:	cmosn	cmosn	cmosn	cmosn	cmosn
Id:	1.24e-03	1.25e-03	1.24e-03	1.24e-03	1.25e-03
Vgs:	5.95e-01	5.95e-01	5.95e-01	5.95e-01	5.95e-01
Vds:	5.39e-01	5.95e-01	5.39e-01	5.39e-01	5.95e-01
Vbs:	0.00e+00	0.00e+00	0.00e+00	0.00e+00	0.00e+00
Vth:	4.64e-01	4.64e-01	4.64e-01	4.64e-01	4.64e-01
Vdsat:	1.10e-01	1.10e-01	1.10e-01	1.10e-01	1.10e-01
Gm:	1.67e-02	1.68e-02	1.67e-02	1.67e-02	1.68e-02
Gds:	2.10e-04	1.99e-04	2.10e-04	2.10e-04	1.99e-04
Gmb	4.55e-03	4.58e-03	4.55e-03	4.55e-03	4.58e-03
Cbd:	0.00e+00	0.00e+00	0.00e+00	0.00e+00	0.00e+00
Cbs:	0.00e+00	0.00e+00	0.00e+00	0.00e+00	0.00e+00
Cgsov:	1.48e-13	1.48e-13	1.48e-13	1.48e-13	1.48e-13
Cgdov:	1.48e-13	1.48e-13	1.48e-13	1.48e-13	1.48e-13
Cgbov:	3.26e-19	3.26e-19	3.26e-19	3.26e-19	3.26e-19

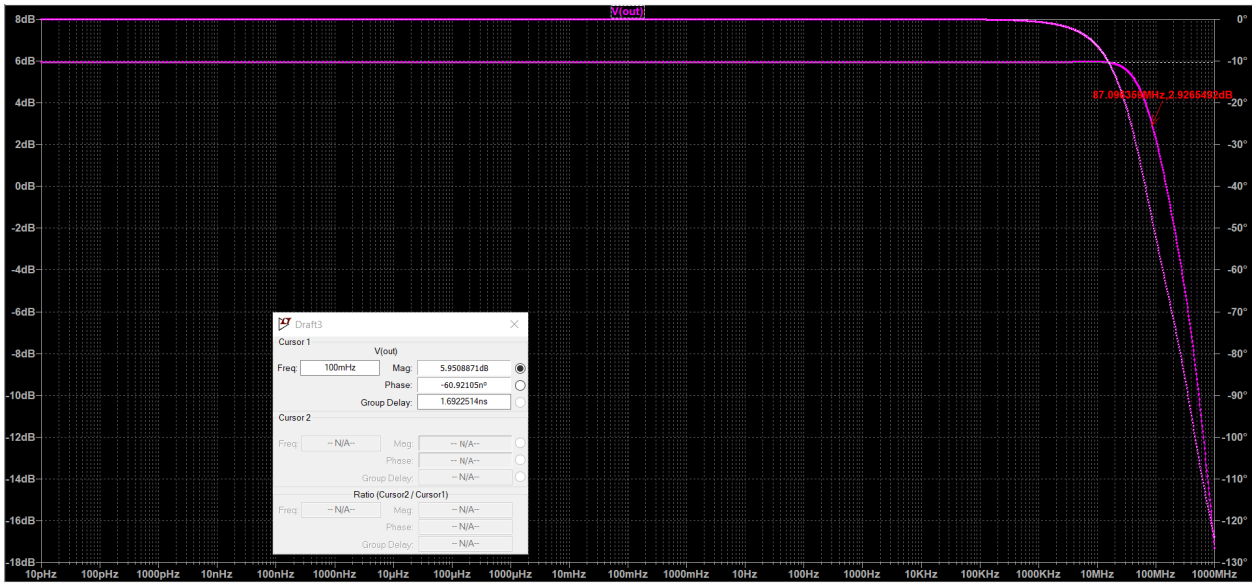
Following are the plots obtained at room temp.

1. Open Loop Gain and Phase



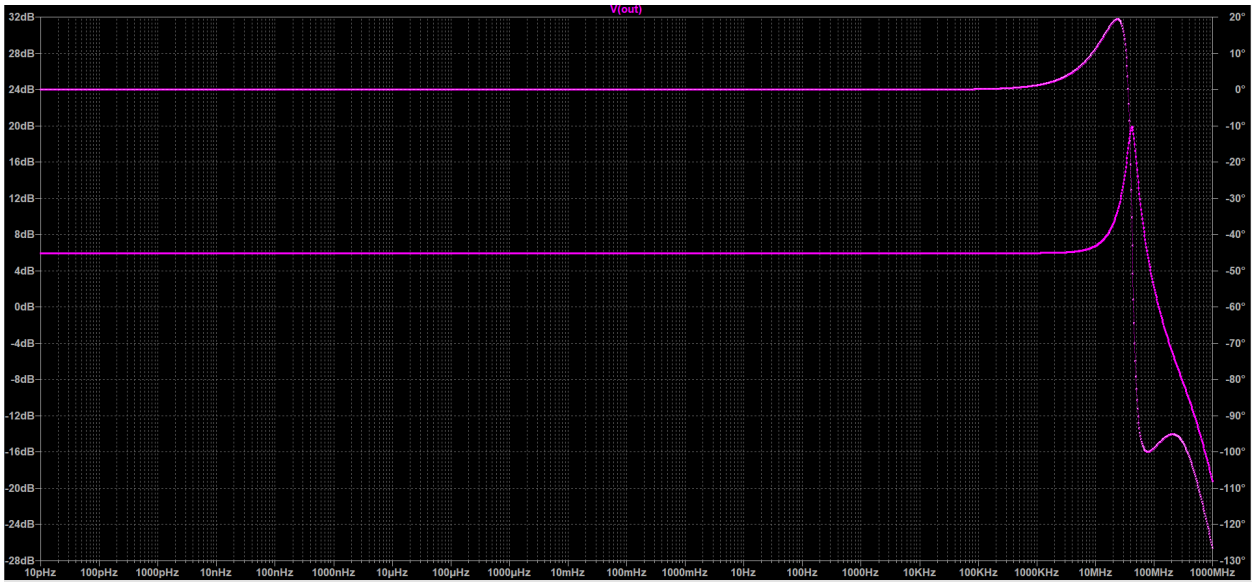
- **Open Loop Gain obtained = 50.69 dB**

2. Closed Loop Gain and Phase
   →Vo/Vi plot



- **Closed Loop Gain obtained = 5.95 dB**
- **-3dB bandwidth = 87.09MHz**

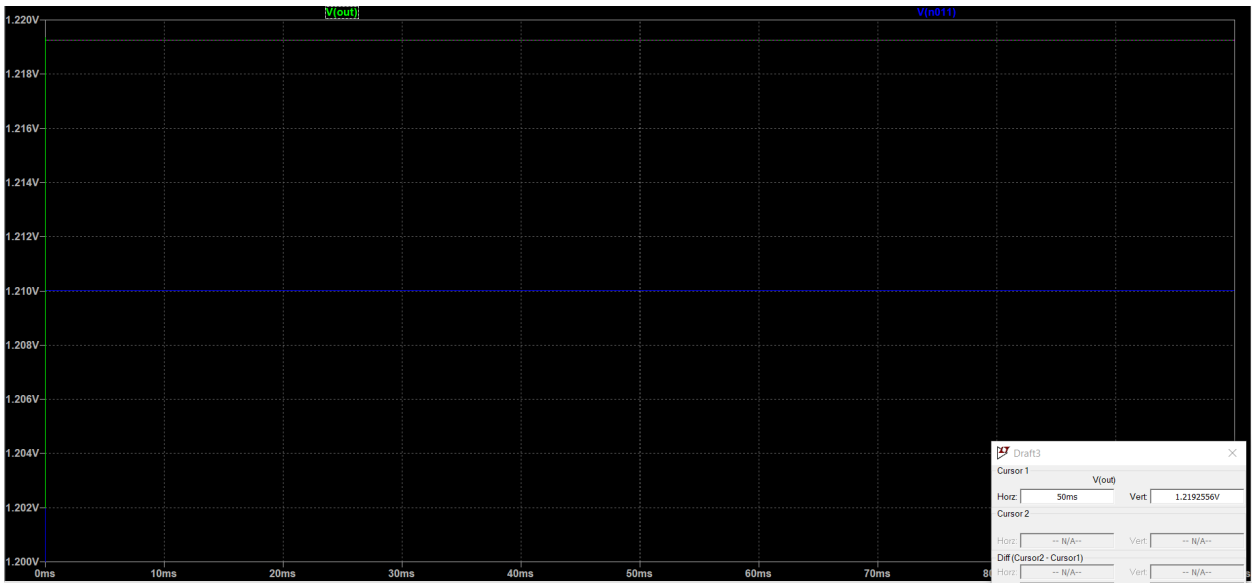
  -3dB bandwidth is reduced in my design due to the addition of a pole.I added that pole(with cap. C2 in the circuit) in order to cancel the effect of a zero showing up at higher frequencies.



The above curve shows Vo/Vi without adding a pole.

- Loop Gain = Open Loop Gain - Closed Loop Gain (in dB)
- Therefore, **Loop Gain = 44.7 dB** (verified by “Big inductor” method in LTspice)

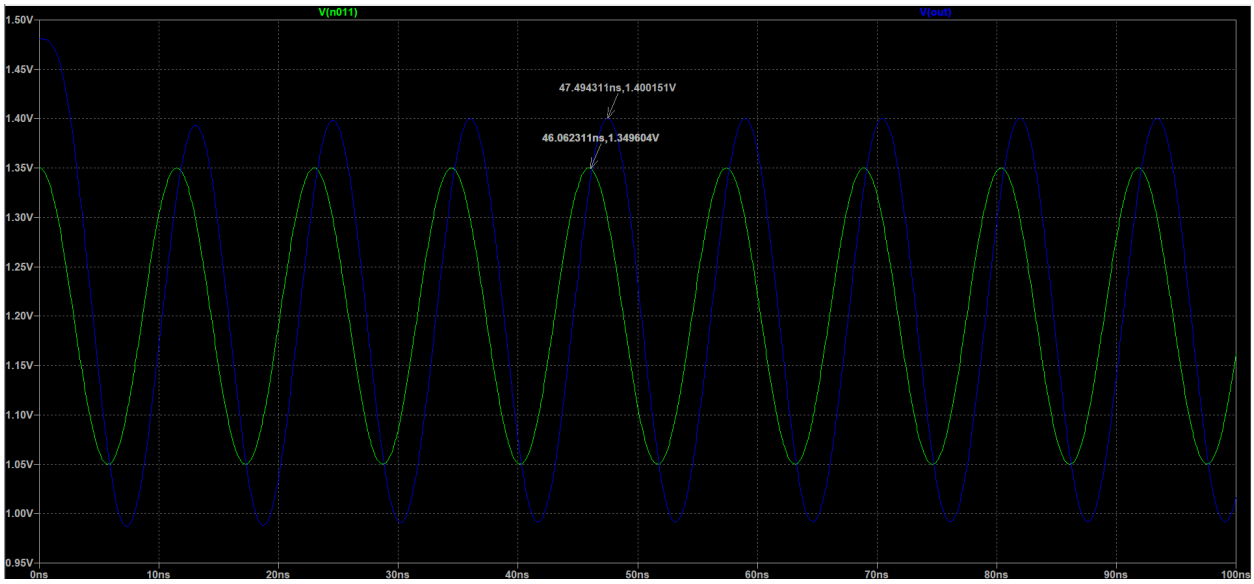
3. Transient response of the non inverting amplifier with a 0.01 step input at v_i.



Vout reaches 1.219V at steady state.
Ideal Vout = 1.2 + 2*0.01 V = 1.22V
e_{ss} = 1.22 - 1.219
e_{ss} = 0.001 V

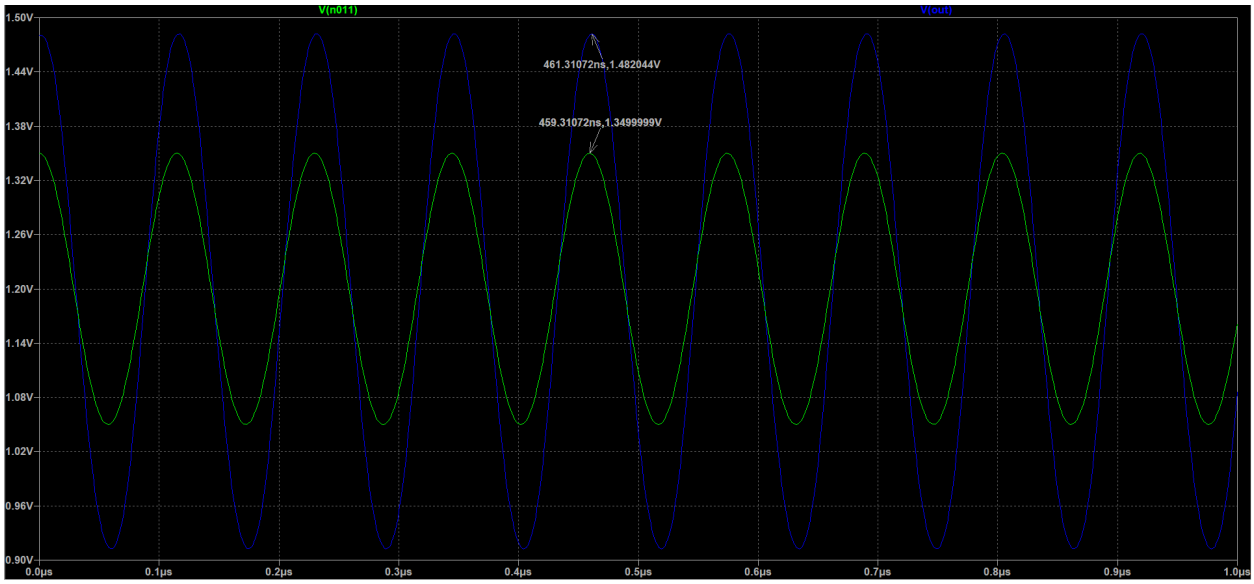
4. Transient response of the non inverting amplifier with v_i = 150mV(cos(w_{3dB}t))

As per my design w_{3dB} = 87.09MHz



Green→ input Blue→output

5. Transient response of the non inverting amplifier with v_i = 150mV(cos(w_{3dB}t/10))

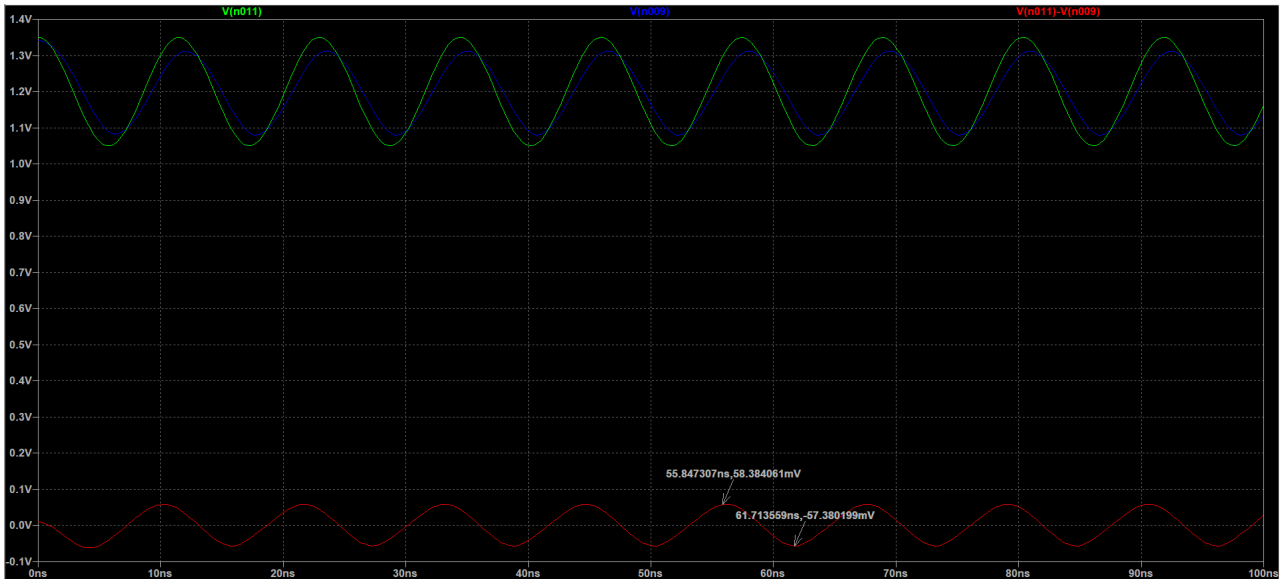


Green→ input Blue→output

6. Difference between input voltages for $v_i = 150mV(\cos(w_{3dB}t))$

→ V1-V2 = 58 mV (approx)

→ V1-V2 = 0 mV due to virtual short (theoretically)

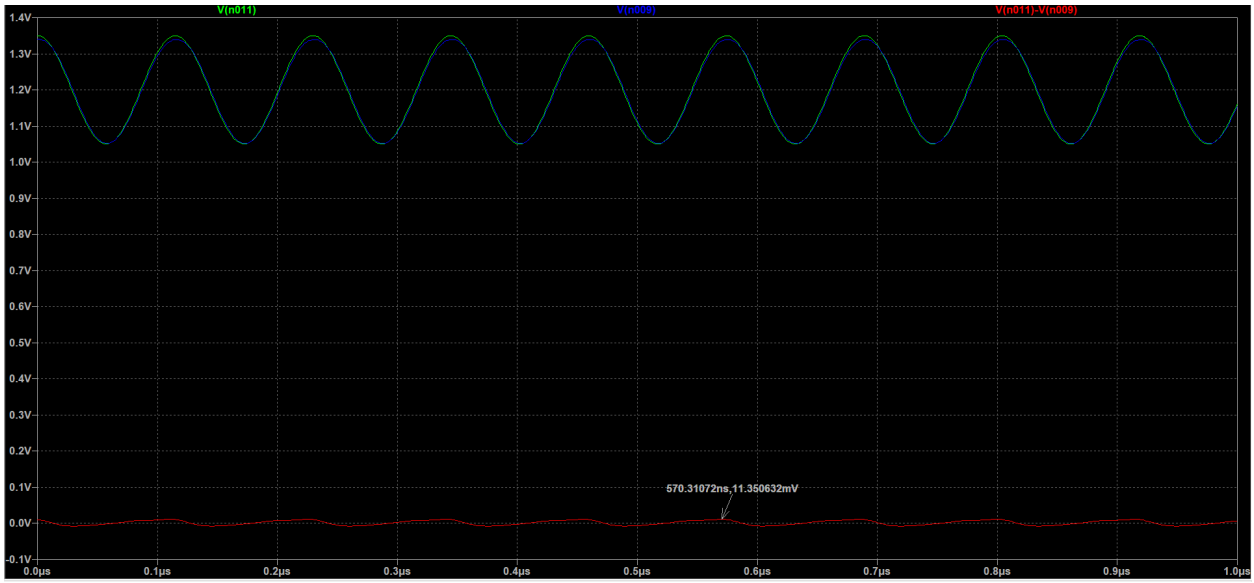


*Difference is shown by the red curve

7. Difference between input voltages for $v_i = 150mV(\cos(w_{3dB}t/10))$

→ V1-V2 = 11.35mV(max)

→V1-V2 = 0 mV(theoretically)

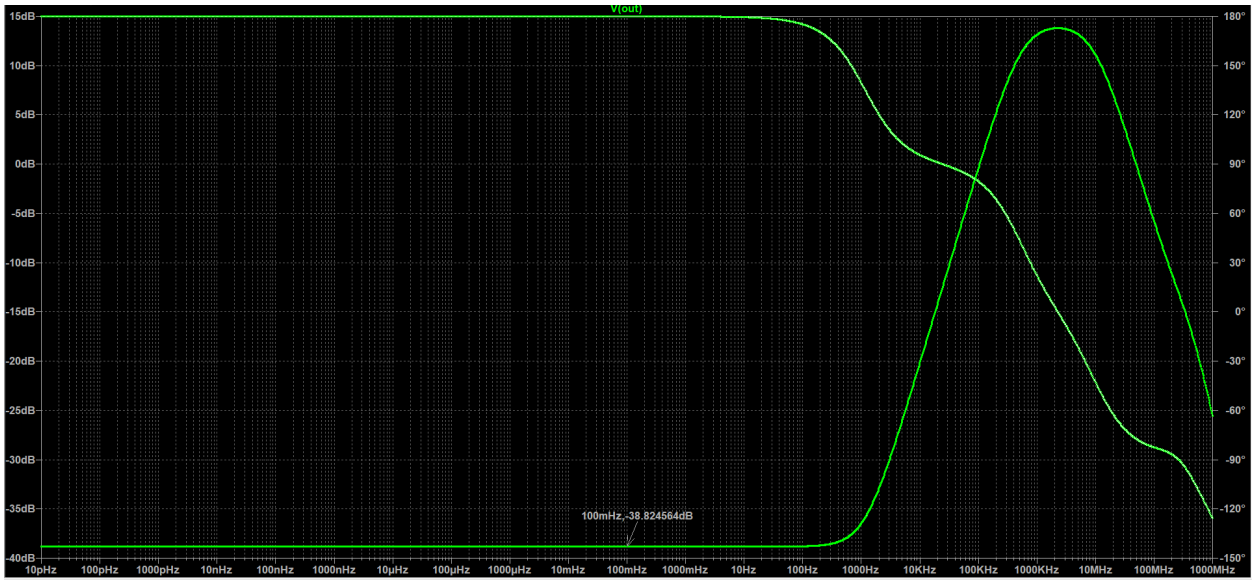


*Difference is shown by the red curve

8. Common Mode Rejection Ratio

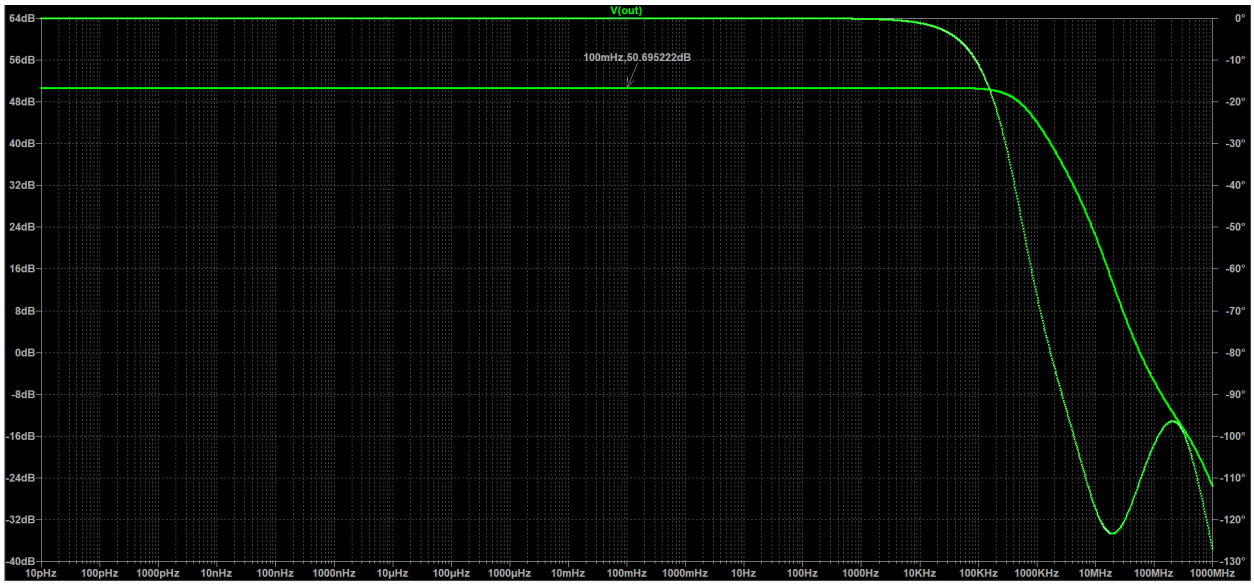
→ Plotting Common Mode Gain

Acm = -38.82 dB



→Plotting Differential Gain

Ad = 50.69 dB



CMRR = A_d- A_{CM} = 89.51 dB

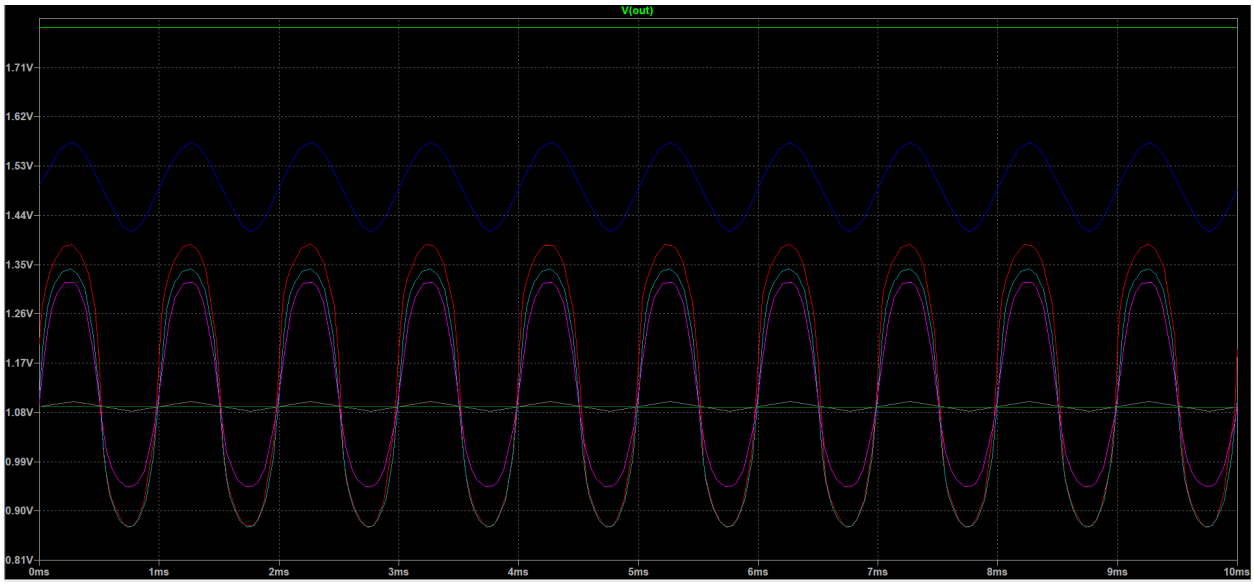
9. ICMR calculation

The design approach for ICMR is as follows: -

1) Run a low frequency analysis on the Diff Amp circuit with different V_{CM} values.

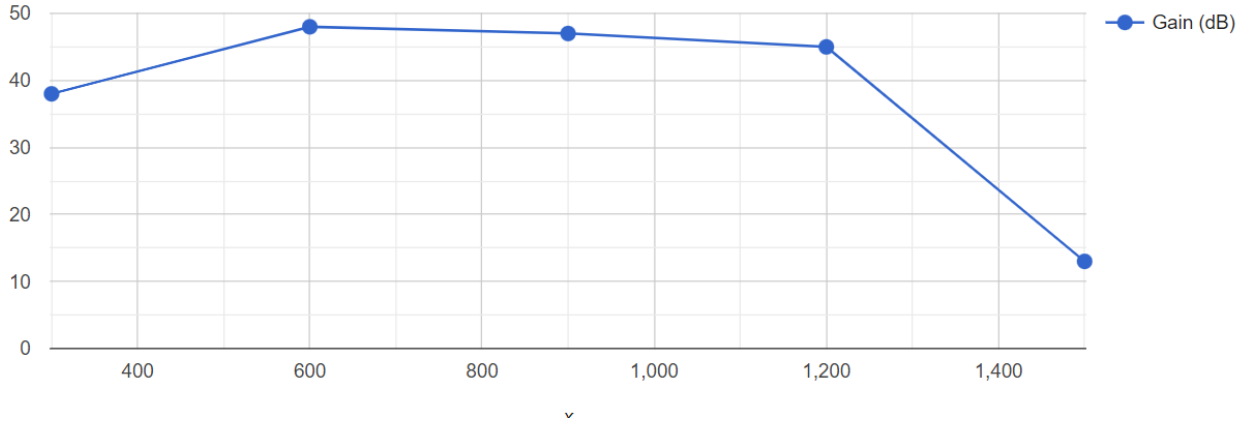
2) Using parametric analysis, the values of V_{CM} will be varied in steps of 0.3V ranging from 0 to 1.8V.

Using transient analysis, observe the gain for various V_{CM} values and calculate $ICMR^{+}$ and $ICMR^{-}$ from a plot of Gain vs Vcm.



*V_{out} plots for different values of $V_{CM.}$

Plot of Gain (dB) vs V_{CM} (mV)



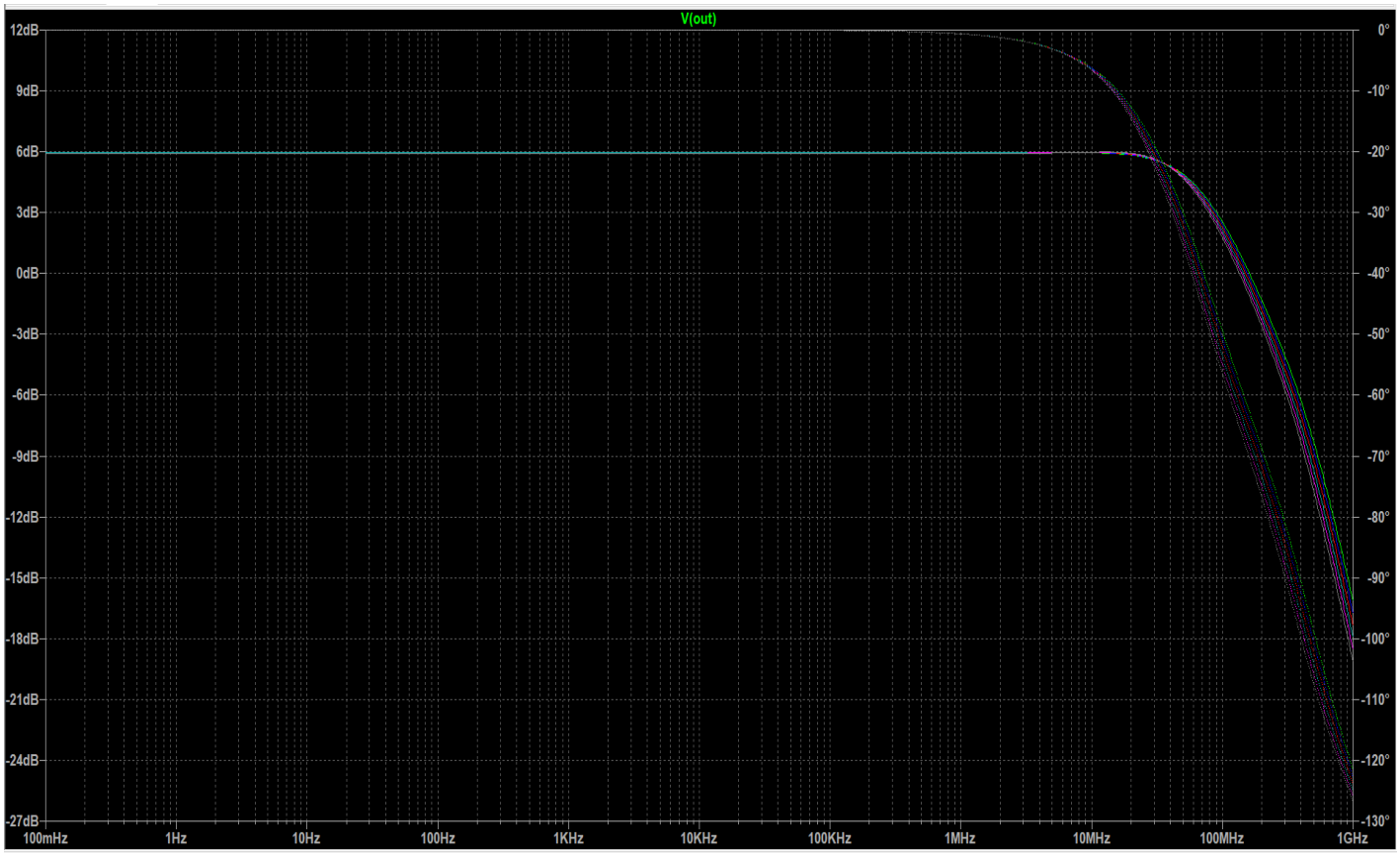
- In the above plot it can be seen that Gain is almost constant between 600mV and 1.2V.
- Therefore, an estimate of ICMR can be determined

  $ICMR^{+}$ = 1.2V

  $ICMR^{-}$ = 0.6V

10. Below are the plots for different temperature values

10.1 Closed Loop Gain and Phase



10.2 Open Loop Gain and Phase