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LNCT UNIVERSITY, BHOPAL

EnrolmentNo..

CS-203UC

B.TECH (CS/AIML) -I &II SEMESTER EXAMINATION [JUNE-2024]

DIGITAL CIRCUITS &EMBEDDED SYSTEMS

Maximum Marks: 70 **TimeAllowed:3 Hours**

Note:-Attempt all questions internal choice are given.

(SECTION –A)

1. Short Answer Type Questions(Attempt Any Five) [5x6=30]

i. Obtain the minimal SOP expression for the following Boolean function using K-map and Implement the minimal SOP obtained using only NAND gates.
$F(w,x,y,z) = \Sigma m(0,1,5,9,13,14,15) + \Sigma_d(3,4,7,10,11)$

ii. Design a full adder using Multiplexer

iii. Write the characteristic, excitation tables for JK, RS, T and D flip-flops.

iv. Design 4 bit PISO Shift Register.

v. What is critical and non-critical races in asynchronous circuits? How to avoid races?

vi. Explain about analysis procedure in sequential circuits in detail.

vii. Explain the Interrupt Structure with the associated register in 8051 microcontroller.

viii. Explain the Interfacing of Keyboard/Display with 8051 microcontroller.

(SECTION –B)

2 Long Answer Type Questions (Attempt Any Four) [04x10=40]

i. Design a 4 bit parallel adder using Full adder modules.

ii. Explain the term Race around condition. How is it satisfied by Master-slaveFlip-Flops?

iii. Using D-Flip flops and waveforms, explain the working of a 4-bit SISO shift register.

iv. Implement the switching function
$F = \sum m\ (1, 3, 5, 7, 8, 9, 14, 15)$ by a static hazard free two level AND- OR network.

v. Explain the data transfer instructions of timer unit in 8051 microcontroller.

vi. Convert SR flip flop to T flip flop.
