PED

EXPERIMENT - 2

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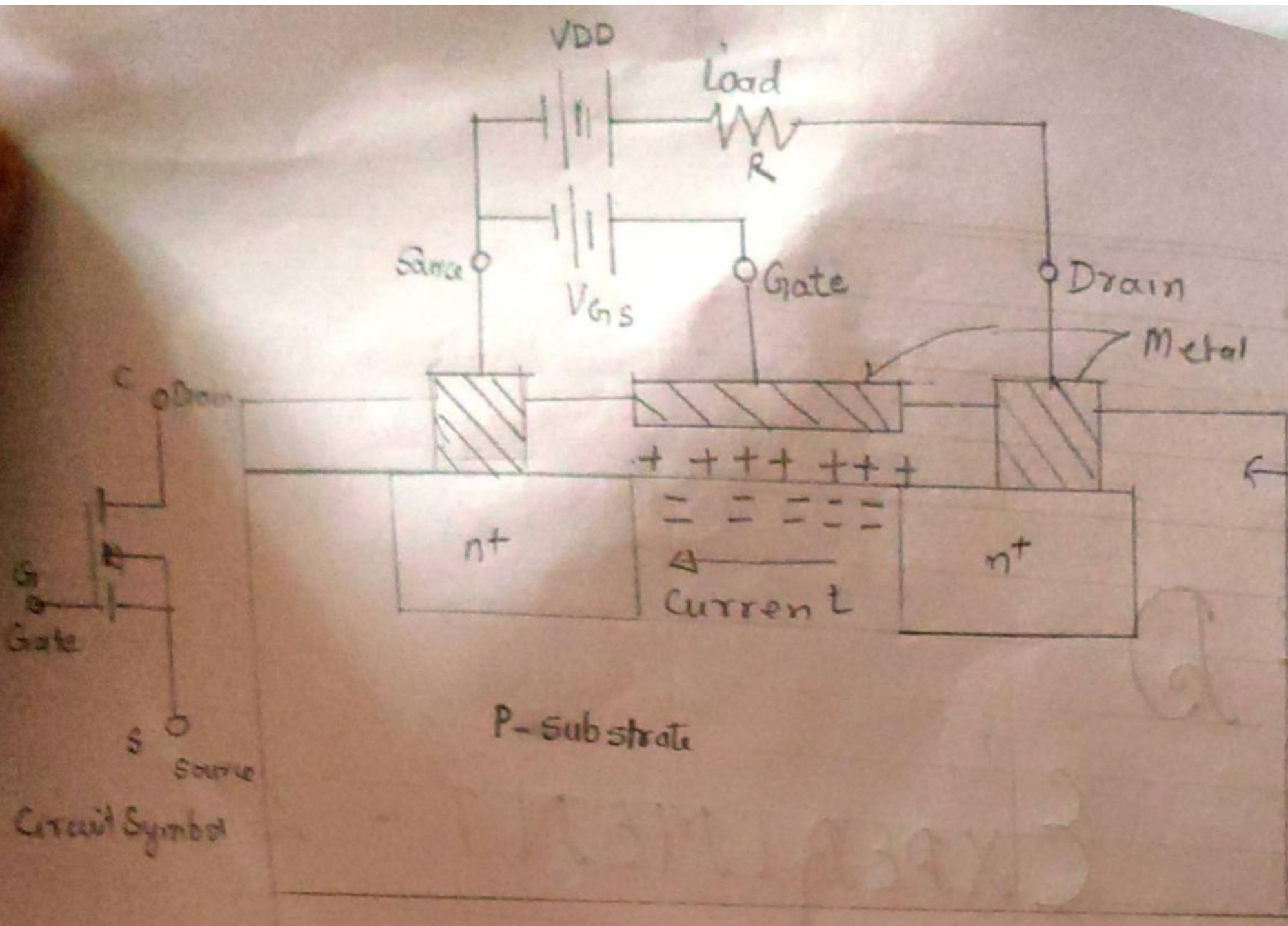
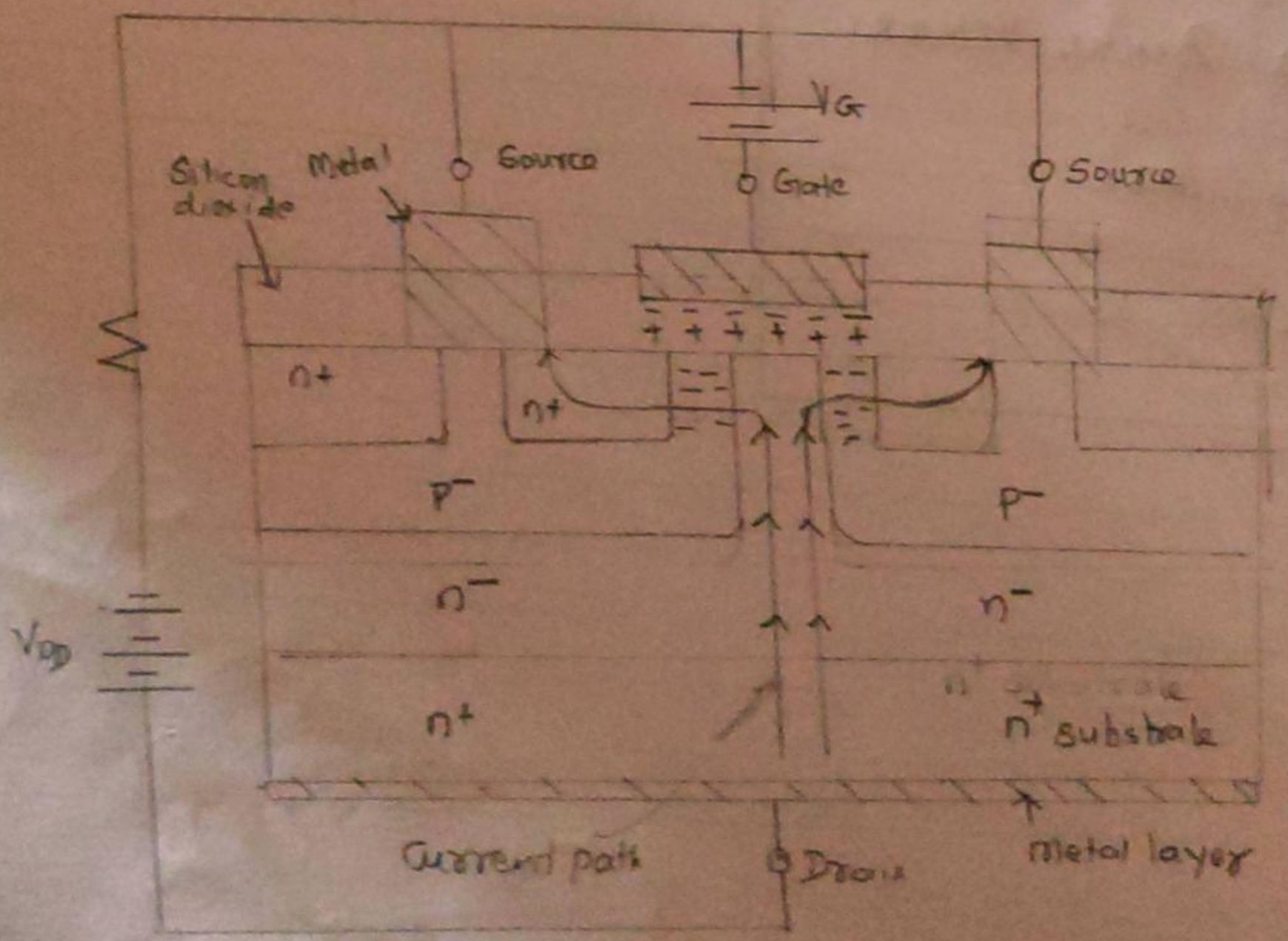


fig a) N-Channel enhancement power MOSFET



Fg b Structur of n^1 channel DMOS Power MOSFET

AIM: Simulate & plot characteristics of power MOSFET & IGBT.

Software Used: MultiSim.

Theory:

Power MOSFETS

A metal oxide semiconductor field-effect transistors (MOSFET) is a recent device developed by combining the areas of field-effect connect & MOS Technology.

A power MOSFET has 3 terminals called drain, source & gate in place of the corresponding 3 terminals collector, emitter & base for BJT In circuit symbol of power MOSFET arrow indicates the direction of electron flow. A BJT is a current controlled device whereas a power MOSFET is a voltage controlled devices. As its operation depends upon the flow of majority carriers only. MOSFET is a unipolar device The control signal (or gate current) required in a MOSFET is a unipolar device. The control signal or base current in BJT is much larger than the (gate current). This is because of the fact that the gate circuit impedance in MOSFET gate to be driven directly from microelectrons circuits. BJT satisfies from 2nd breakdown voltage whereas MOSFET is free from this problem. Power MOSFETs are now finding increasing applications in low-power high frequency converters Power MOSFETs are of 2 types, n-channel enhancement MOSFET & p-channed enhancement MOSFET Out of these 2-types n-channel enhancement MOSFET is more common because of higher mobility

of electrons. As such only the type of MOSFET is studied.

A simplified structure of n-channel planar MOSFET of low power rating is showing on p-substrate, 2 heavily doped, n regions are diffused as shown. An insulating layer of silicon dioxide (SiO_2) is developed on the surface. Now this insulating layer is etched in order to embed metallic source & drain terminals. A layer of metal is deposited on SiO_2 layer so as to form gate of MOSFET.

When gate circuit is open no current flows from drain to source & load because of one reverse-biased n-p junction. When gate is made positive with respect to source an electric field is established. Eventually induced negative charges in the p-substrate below SiO_2 layer are formed. These -ve charges called electrons from n-channel & current can flow from drain to source as shown by the arrow. If V_{GS} is made more +ve, n-channel becomes more deep & therefore more current flows from D to S. This shows that drain current I_D is enhanced by the gradual increase of gate voltage, hence the name enhancement MOSFET.

The main disadvantage of n-channel planar MOSFET is that conducting n-channel is between drain & source gives large on state resistance. This leads to high power dissipation in n-channel. This shows that planar MOSFET construction is feasible only for low-power MOSFETs.

Diffussed metal-oxide-semiconductor (DMOS) structured for n-channel which is quite common for power MOSFETs. On n^+ substrate high resistivity n-layer is epitaxially grown. The thickness of n^- layer determined the voltage blocking capability of the device. On the other side of n^+ substrate, a metal layer is desposited to form the drain terminal. Now p^- regions are diffused in the epitaxially grown n^- layer. determines n^+ layer region are diffused in p^- regions.

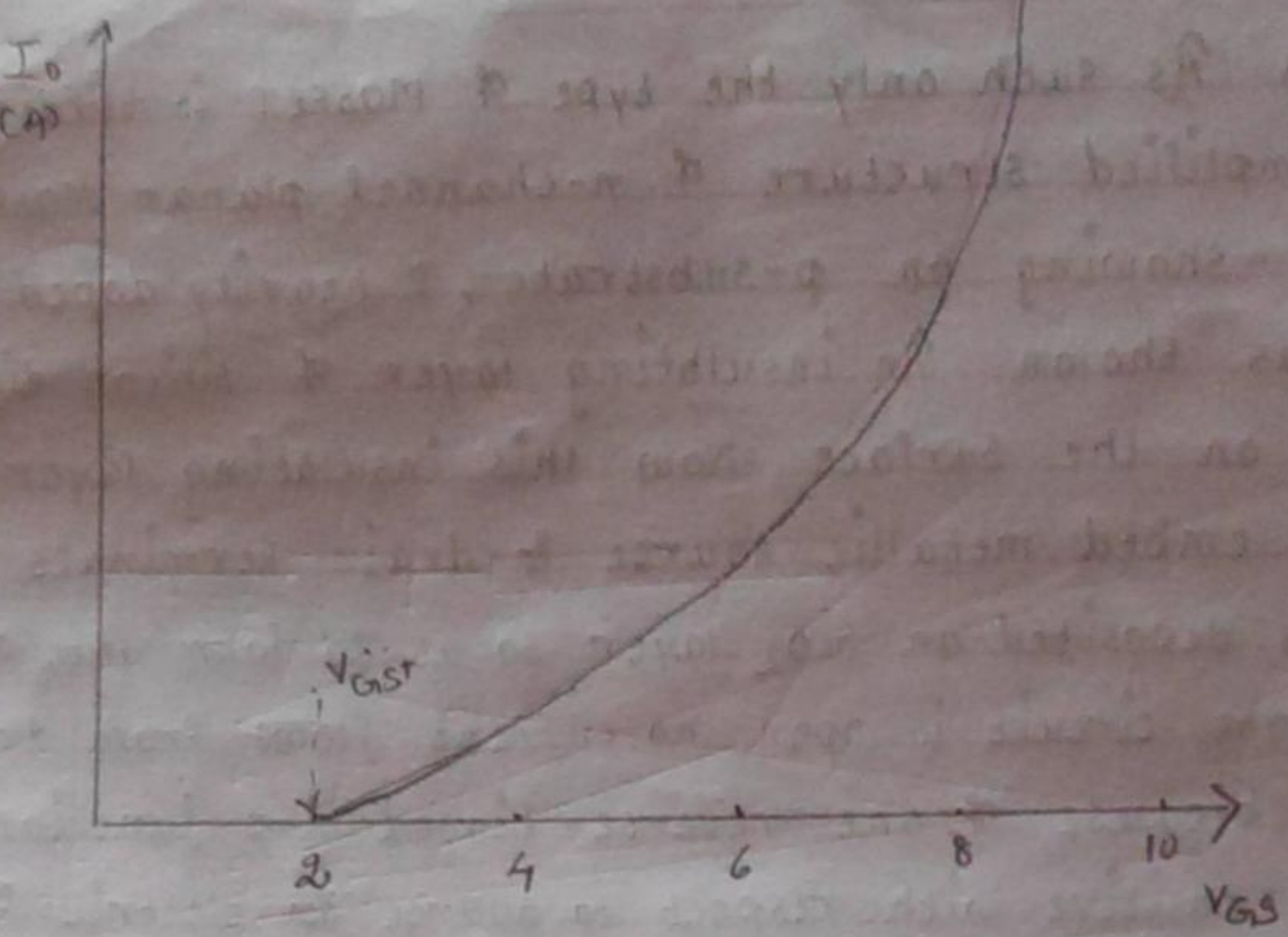


fig c Transfer characteristics

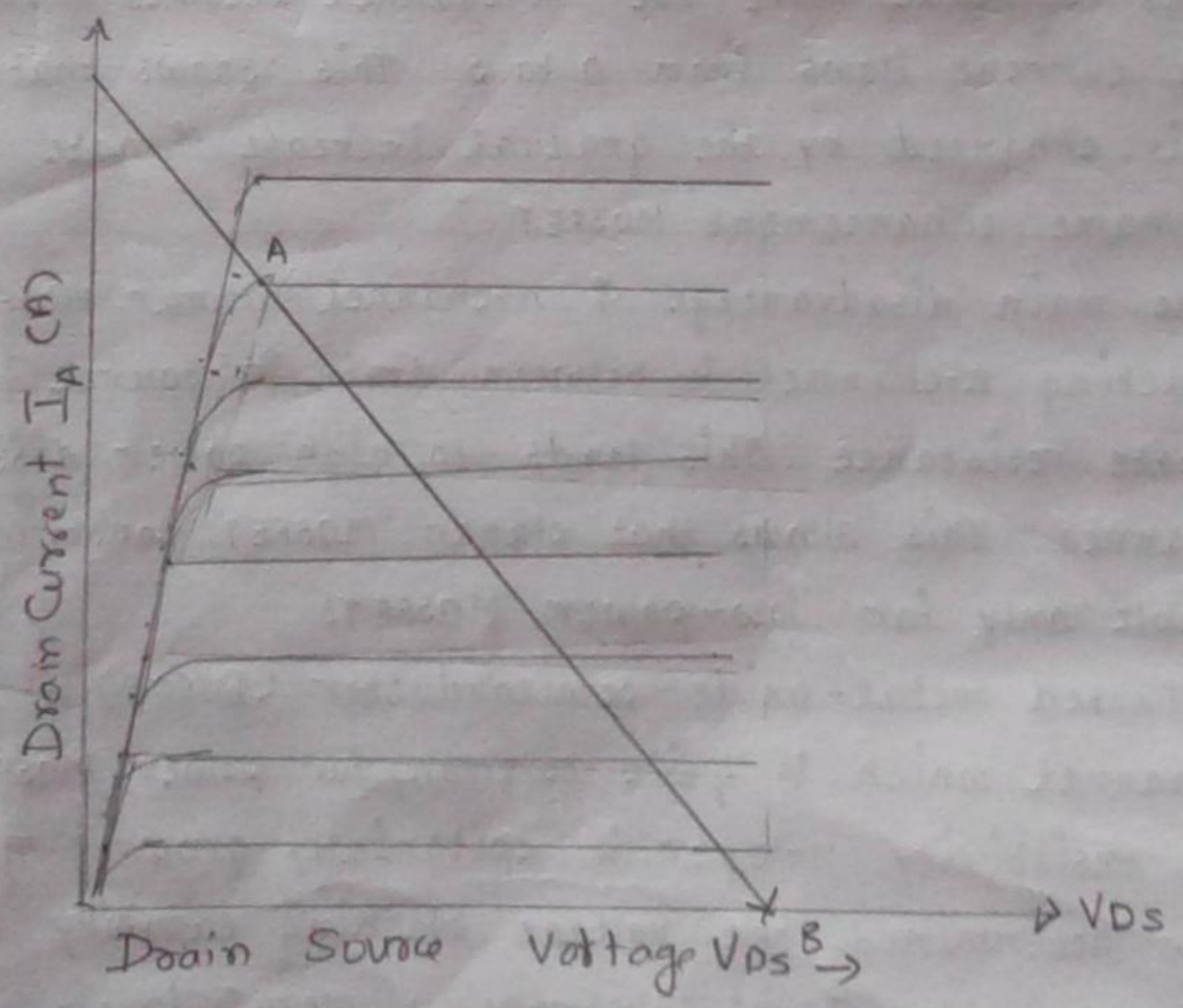


Fig d) Output Characteristics of a power MOSFET

As before SiO_2 layer is added which is then etched so as to fit metallic source & gate terminals. A power MOSFET actually consists of a parallel connections of thousands of basic MOSFET cells on the same chip of silicon.

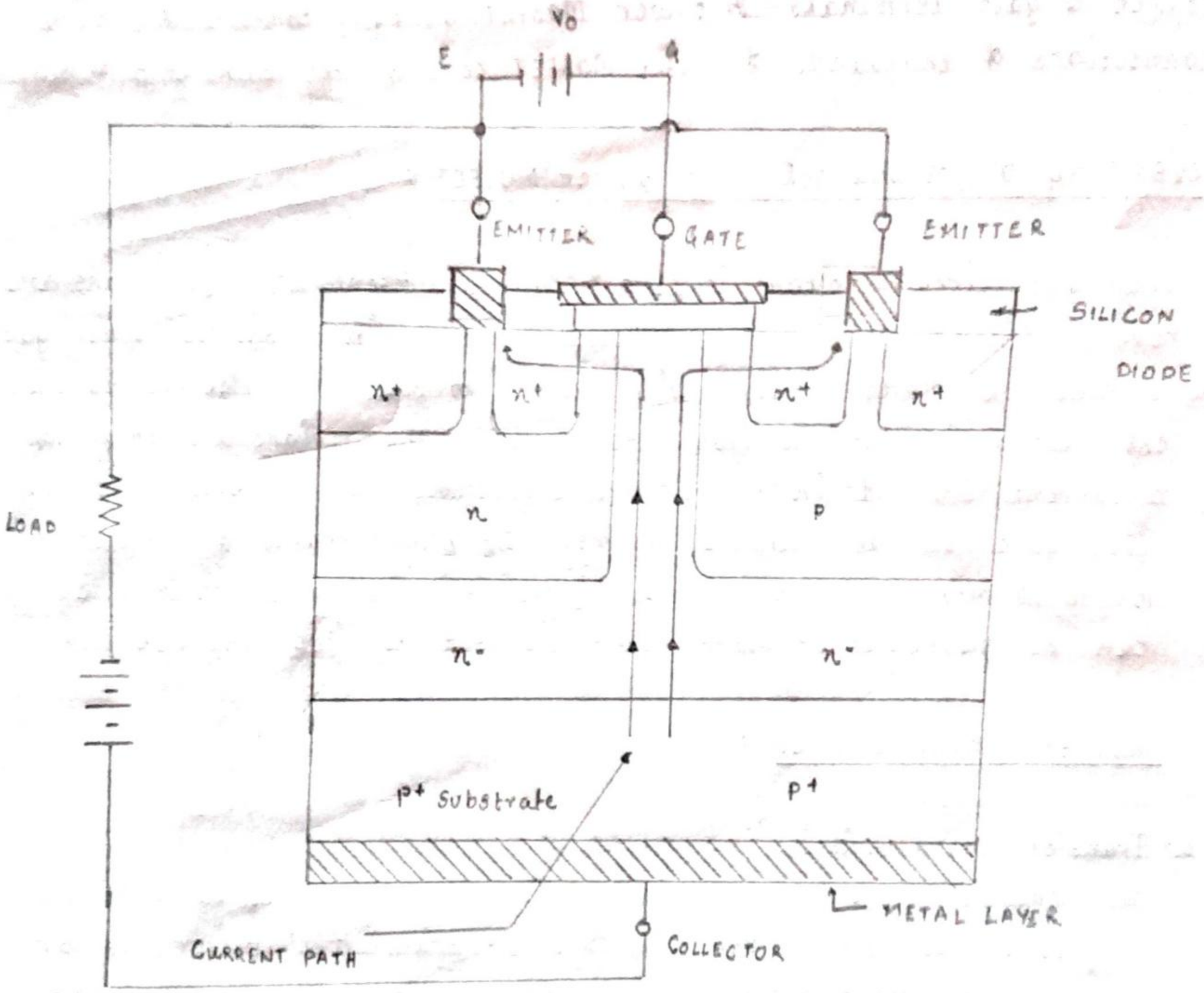
Working of n-channel DMOS power MOSFET :

When gate circuit voltage is zero & V_{DD} is present n^-, p^- junctions are reverse biased & no current flows from drain to source When gate terminal is made positive with respect to source an electric field is established & electrons from n-channel in the regions as shown so a current from drain to source is established as indicated by arrows with gate voltage increased current I_D also increases as expected length of n-channel can be controlled & therefore on-resistance can be made low if short length is used for the channel

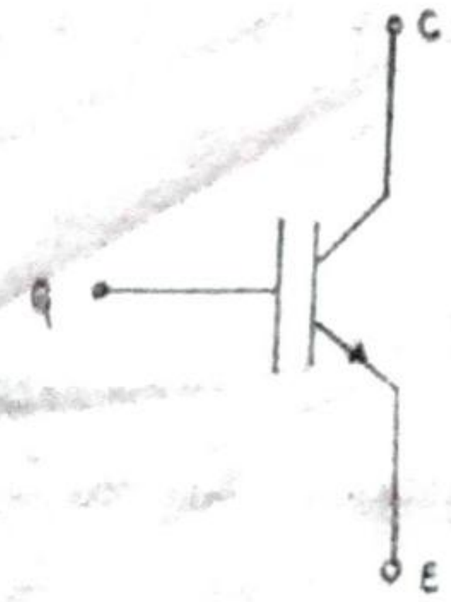
MOSFET Characteristics :

a) Transfer Characteristics:
This characteristic shows variation of drain current I_D as a function of gate-source voltage V_{GS} Fig c) shows transfer characteristics for n-channel power MOSFET It is seen that there is threshold voltage V_{GST} below which the device is off. The magnitude of V_{GST} is of order 2 to 3V.

b) Output Characteristics:
Power MOSFET o/p characteristics indicate variation of drain current I_D as a function of V_{DS} as parameter for low values of V_{DS} graph I_D-V_{DS} is linear constant value of on resistance $R_{DS} = V_{DS}/I_D$ for given V_{GS} if V_{DS} is ↑ o/p characteristic is flat dr. I_D is constant A load line intersects o/p of A & B A - fully on condn & B - fully off state. PMOSFET is switch at A or B like BJT



BASIC STRUCTURE OF IGBT



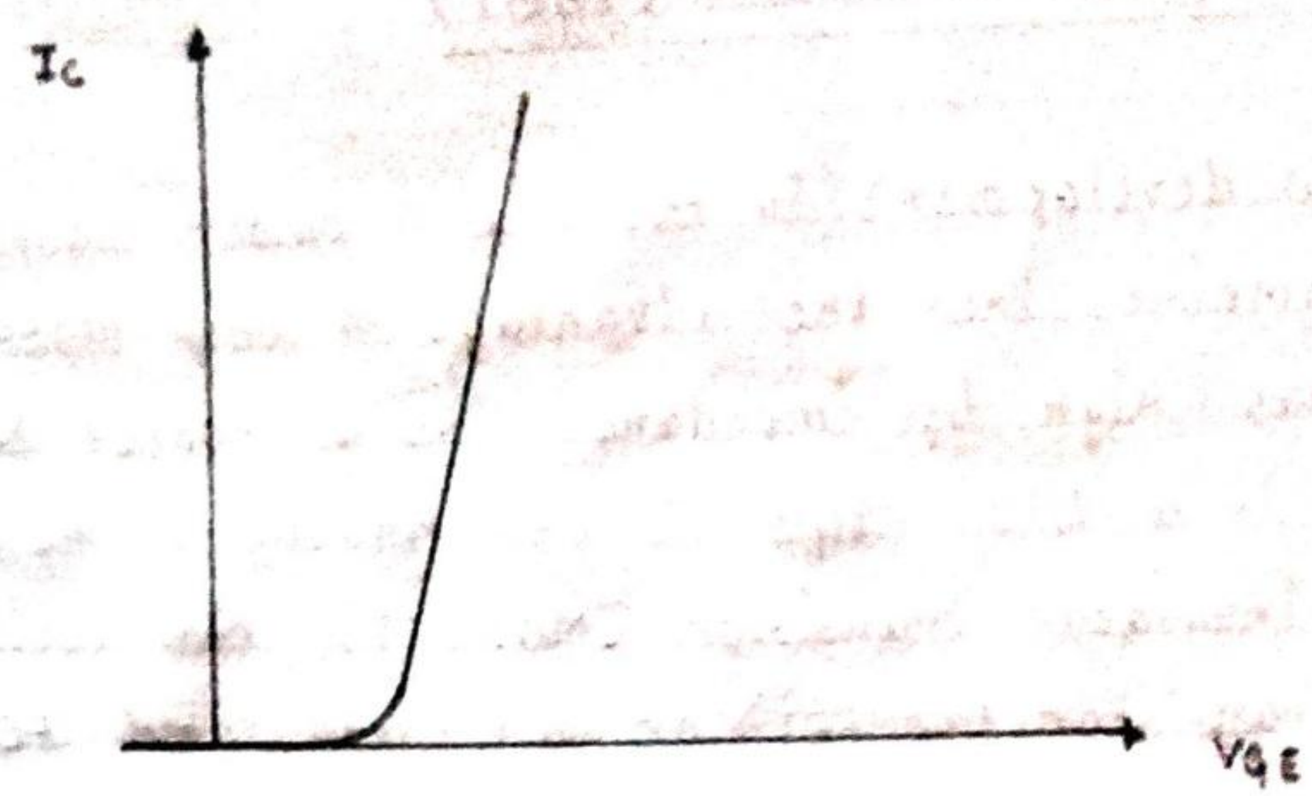
SYMBOL

Insulated Gate Bipolar Transistor (IGBT)

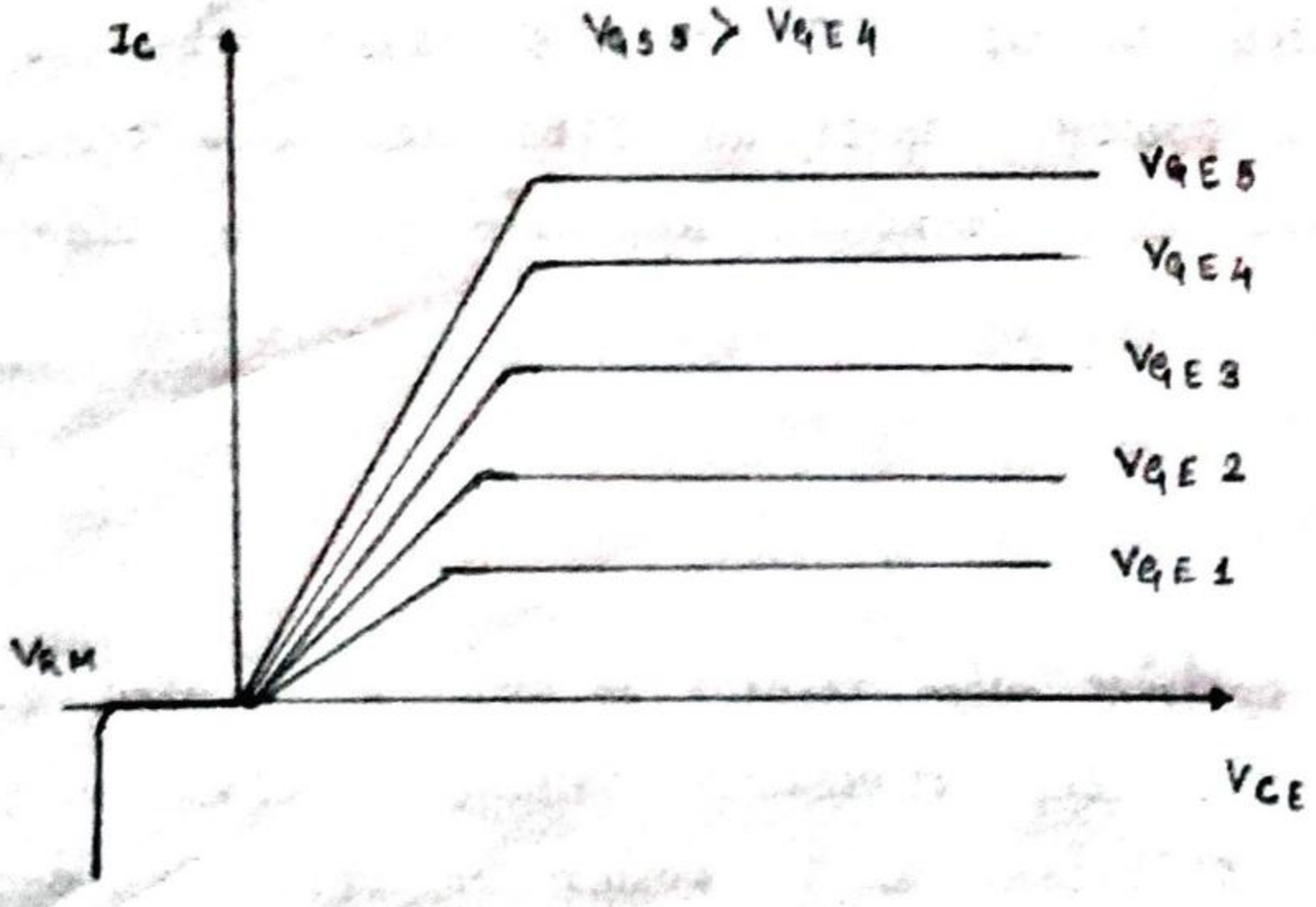
IGBT is a new development in the area of power MOSFET technology This device combines into the advantage of both MOSFET & BJT So an IGBT has high i/p impedance like a MOSFET & low-on-state power loss as in a BJT IGBT is also known as metal-oxide insulated gate insulator transistor (MOSIGT), conductively-modulated field effect transistor (COMFET) or gain-modulated FET (GMFET). IGBT is constructed virtually in the same manner as a power MOSFET. There is however a major difference in the substrate. The n^+ layer substrate at the drain in a power MOSFET is now n^+ layer substrate at the drain in a power MOSFET is now substituted in the IGBT by a p^+ layer substrate called collector like a power MOSFET an IGBT has also thousands of basic structure cells connected approximately on single chip of silicon.

WORKING:

when gate is positive with respect to emitter & with gate-emitter voltage more than the threshold voltage of IGBT an n-channel is formed in the p-regions as in power MOSFET. This n-channel shorts circuits the n^- regions with n^+ emitter regions An electron movement in the n-channel is formed in turn causes substantial hole injection from p^+ substrate layer into the epitaxial n^- layer. Eventually a forward current is established



TRANSFER CHARACTERISTICS



STATIC V-I Characteristics

The 3 layers p^+, n^- & p constitute a pnp transistor with p^+ as emitter n^- as base & p as collector Also n^-, p & n^+ layers constitute npn transistor Here n^- serves as base for pnp transistor & also as collector for npn transistor. P serves as collector for pnp device & also as base for npn transistor The two pnp & npn transistors can therefore be connected to given the equivalent ckt of an IGBT.

IGBT characteristics

a) Transfer characteristics:
It is plot of I_{GC} versus gate-emitter voltage V_{GS}. This characteristic is identical to the power MOSFET. When V_{GS} is less than threshold voltage V_{GEF} IGBT is in off-state. When device is off junction blocks forward voltage. & in case reverse voltage appears across collector & emitter junction J blocks it.

b) STATIC V-I characteristics:
It shows the plot of collector current I_C vs collector-emitter voltage V_{GE} for various values of gate-emitter voltages. In forward direction the shape of the o/p characteristics is similar to that of BJT But here the controlling parameter is gate-emitter voltage V_{GE} because IGBT voltage controlled device

Conclusion: The simulation of transfer & output characteristics of power MOSFET & IGBT have been implemented on Multisim and well comprehended.