

TUTORIAL 2

Q1) Difference between IIR & FIR Filters.

→ Characteristics	IIR Filter	FIR filter.
1) No. of necessary multiplications	Least	Most
2) Sensitivity of filter coefficient	Can be high for direct form	Very Low
3) Probability of overflow errors	Can be high for direct form	Very Low
4) Stability	Depends on system design	Guaranteed
5) Linear Phase	No	Guaranteed
6) Can Simulate prototype analog filters.	Yes	No
7) Required b/w memory	Least	Most
8) H/W filter control complexity	Moderate	Simple
9) Availability of design software	Good	Very good.
10) Ease of designer complexity of design	Complicated	Simple
11) Difficulty of quantization noise analysis	Most Complicated	Least Complicated
12) Supports adaptive filtering	Yes	Yes

Q2) Applications of DSP in Radar Systems.

- i) As a matter of fact, radar is used for detecting stationary & moving objects. Fig. shows the block diagram of a modern radar system. Here, in the transmitter side, the signals are generated & transmitted with the help of an antenna.
- ii) When these signals strike the target object, a portion of the signal is echoed back. This echoed signal is received by the radar system. Depending upon the time duration between the transmitted & received signals,

the distance at which the target is located can be identified.

iii) The main parts of a computer system are the antenna, the tracking computer & the signal processor. Infact, the tracking computer is called the brain of the system.

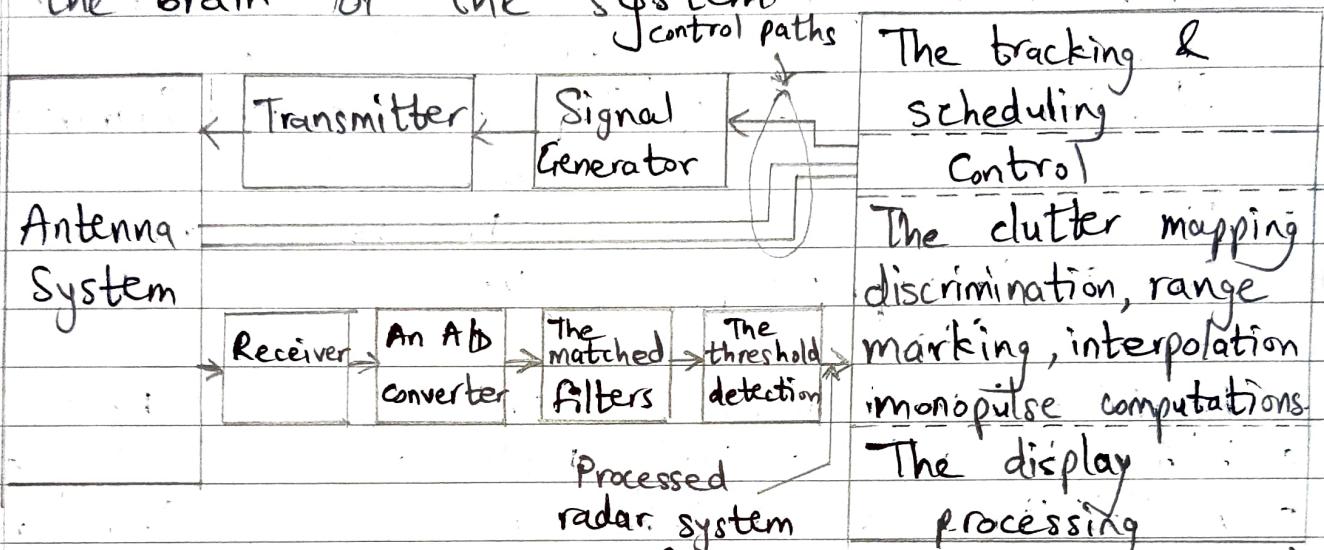


Fig. Illustration of Modern Radar system (Block Diagram)

iv) The tracking computer serves the following main function

- ① It schedules the appropriate antenna positions & transmitted signal as a function of time.
- ② It seeks track of important targets
- ③ It runs the display.

The major functions of signal processors can be listed as under:-

- ① It provides matched filtering.
- ② It provides removal of useless information - threshold detection.

The tracking computer controls the entire operation of the radar system. Some important. Thus,

$$\Delta f = \frac{2V}{C} f_0$$

The tracking computer controls the entire operation of the radar system. Some important radar parameters are discussed in the sections to follow:

1) Antenna Beamwidth:-

The beamwidth of an antenna is given by,

$$\beta \propto \lambda/D$$

here, β = Bandwidth

D = Antenna width

λ = Wavelength

For a pencil beam, the antenna geometry is kept symmetric. Also, β is same in both the horizontal & vertical dimensions.

2) Radar Range

The maximum unambiguous range is given by

$$R_{\max} = cT/2$$

where, c = velocity of light $\approx 3 \times 10^8$ m/s.

T = pulse repetition interval.

3) Radio Range Resolution

In case when two targets are present near each other then the ability of the radar to detect these targets can be measured by the range resolution ΔR . If the signal is having constant frequency, the ΔR is determined by the pulse width. If the pulse width is narrowed, then range resolution can be improved but the maximum range is reduced by decreasing the average power.

4) Doppler Filtering

As a matter of fact, moving targets can be identified by using the Doppler effect. When a continuous sine wave of frequency f_0 is transmitted & the target is moving with a constant velocity, then the received echo signal frequency will be $f_0 + \Delta f$. Thus we have,

$$\Delta f = \frac{2v}{\lambda} f_0 = \frac{2v}{\lambda}$$

here, f_0 = Carrier frequency,

v = Target velocity

λ = Wavelength.

It may be noted that pulsed Doppler signals may be used to get range & velocity resolution.

5) Signal Designing:

Transmitting narrow pulse provides good range but at the same time, it provides poor velocity measurement. In fact, a wide pulse of single frequency provides good velocity but bad range information.

Let us consider the radar model as shown in fig. Let the signal be generated digitally & transmitted through an analog filter.

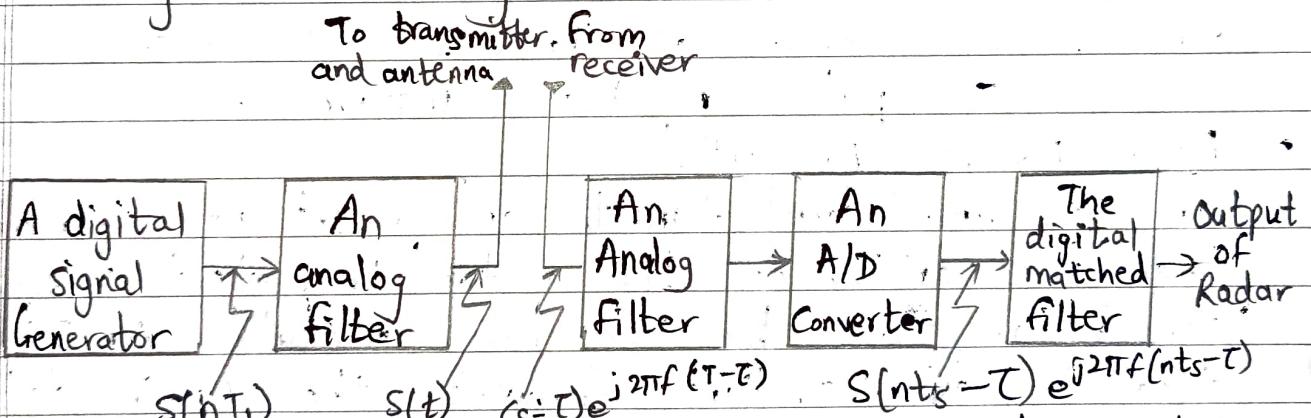


Fig. Illustration of block diagram of a radar model.

- The transmitted signal is $s(t)$. The received signal is $s(t-T)$ which is delayed & frequency shifted.

- The received signal is made to pass through an analog filter, A/D converter and then through a digital matched filter.

- The input signal to the matched filter will be $s(nT_s - T) e^{j2\pi f_c(nT_s - T)}$.

- Q3) Write applications of DSP in Image Processing:
- i) As a matter of fact, any two-dimensional information-bearing function is known as an image. Images are specified by arrays of real or complex numbers represented by finite number of bits.
 - ii) Image signals are two dimensional & speech signals are one-dimensional signals. Smallest element of an image is known as picture Element or Pixel.
 - iii) Image processing is referred as the manipulation of two-dimensional signals with the help of a digital computer.
 - iv) The purpose of image processing is to improve the visual appearance of image for human viewing & perception & to prepare images for measuring of their various features.
 - v) Image processing has found application in the following areas: Medical imagine, remote sensing, processing of images from radars & sonars, storage of business documents, etc.
 - vi) Image processing is concerned with processing of electrical signals extracted from images by digital techniques. It includes the following topics:
 - ① Image formation & Recording
 - ② Image Compression
 - ③ Image Restoration
 - ④ Image Enhancement.
 - vii) Above operations are possible because of high-tech digital computers, artificial intelligence & advanced version of software.

Q4) Compare DSP processor & General Purpose microprocessors.

Parameter	DSP Processor's	Gen. Purpose Microprocessors
1) Instruction cycle	Instructions are executed in single cycle of the clock i.e. true instruction execution of one cycle	Multiple clock cycles are required for instruction execution.
2) Instruction execution	Parallel execution is possible	Execution of instructions is always sequential
3) Operand fetch from memory	Multiple operands are fetched simultaneously	Operands are fetched sequentially.
4) Memories	Separate program and data memories	Normally no such separate memories are present.
5) On-chip/off-chip memories	Program and data memories are present on-chip & extendable off-chip	Normally on-chip cache memory is present. Main memory is off chip.
6) Program flow control	Program sequencer & instruction register & instruction cache	Program counter maintains the flow of execution instruction cache.
7) Queuing/Pipelining	Queuing is implicit through instruction register & instruction cache	Queue is performed explicitly by queue registers for pipelining of instructions.
8) Address generation	Addresses are generated combinably by OAG's & program sequencer.	Program counter is incremented sequentially to generate addresses.
9) Address/data bus multiplexing	Address & data buses are not multiplexed. They are separate on chip as well as off chip.	Address/data buses can be separate on the chip usually multiplexed off chip.

10) Computational units	Three separate computational units: ALU, MAC & shifter.	ALU is the main computational unit.
11) On-chip address & data buses	Separate address & data buses for program memories and data memories & result bus i.e PMA, DMA, PMD, DMD & R-bus	Address & data buses are the two buses on the chip
12) Addressing modes	Direct & Indirect addressing is supported	Direct, indirect, register, register indirect, immediate, etc. addressing modes are supported.
13) Suitable for	Array Processing operations	General purpose processing

(Q5) Write a short note on following with reference to P-DSP (Programmable DSP).

1) Von-neumann Architecture & 2) Harvard Architecture.

→ It may be noted that the MAC operates with the move i.e MAC instruction requires four memory accesses per instruction cycle. An instruction cycle is the time that elapses since an instruction is fetched till the particular instruction completes execution including the time taken for writing the result into a register or memory. Many of the instructions in P-DSP's including the MACD instruction require only one processor clock period 1 instruction cycle. In the conventional microprocessors one instruction cycle corresponds to several clock periods. The four memory accesses/clock period required for the MACD instructions are as follows:

- 1) Fetch the MACD instruction from the program memory
- 2) Fetch one of the operands from the program memory.

3) Fetch the second operand from the data memory.
 4) Write the content of the data memory with address data into the location with address $data + 1$.
 The relatively static impulse response coefficients are stored in the program memory & the samples of the input data are stored in the data memory. If the MACD instruction is to be executed in a machine with Von neumann architecture, it requires the four clock cycle. This is because in the Von-Neumann architecture in fig 1 there is a single address bus & a single data bus for accessing the program as well as data memory area. One of the ways by which the number of clock cycles required for the memory access can be reduced is to use more than one bus for both address & data for example in the Harvard architecture shown fig. 2.

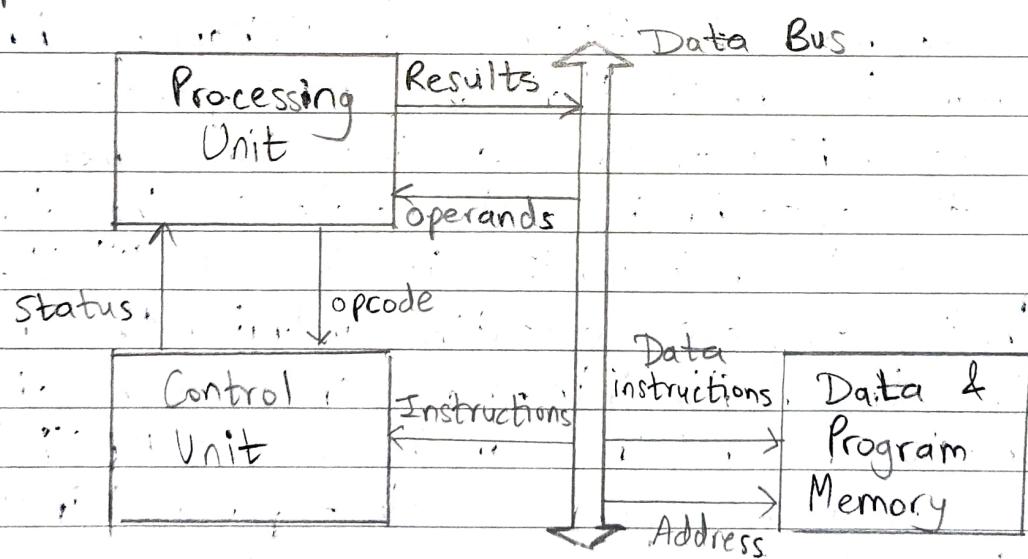


Fig 1 Von-Neumann Architecture

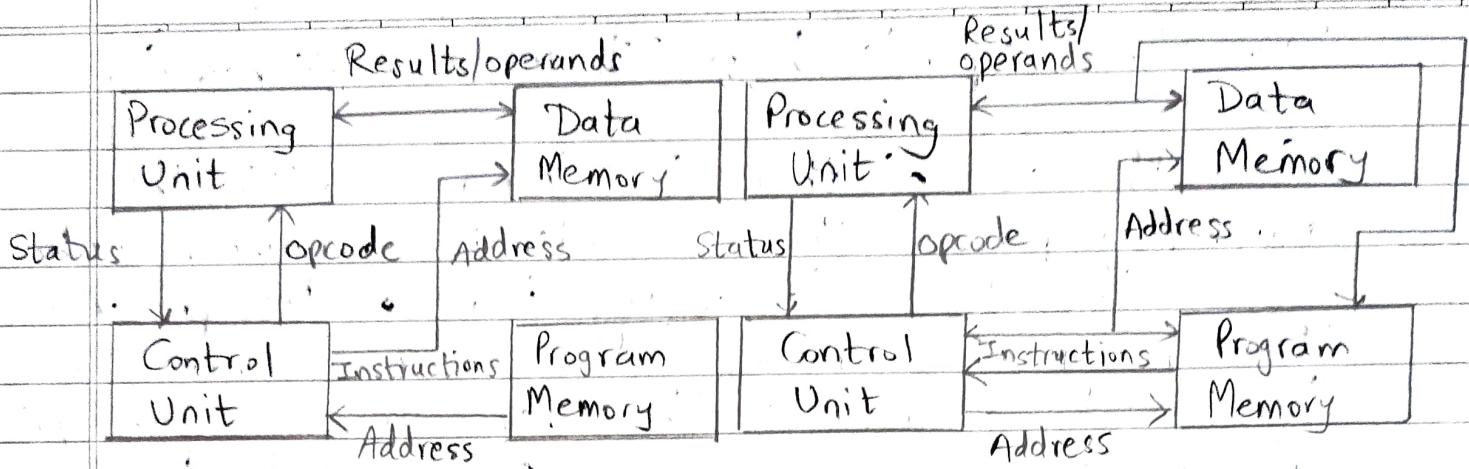


Fig.2 Harvard Architecture

Fig.8 Modified Harvard Architecture

There are two separate buses for the program & data memory. Hence the content of program memory & data memory can be accessed in parallel. The instruction code can be fed from the program memory to the control unit while the operand is fed to the processing unit from the data memory. The processing unit consisting of the registers & processing elements such as MAC units, multiplier, ALU, shifter, etc. are also referred to as data path. The P-DSP's follow the modified harvard architecture shown in fig. 3 one set of bus is used to access a memory that has both program & data & another that has data alone. Data can also be transferred from one memory to another. The modified Harvard architecture is used in several P-DSP's for example P-DSP's from Texas instruments & Analog Devices.

With the Harvard architecture, the number of memory accesses / clock cycle was shown to be two. This can be increased further by using more number of buses. For example, by using three separate address & data buses, the number of memory accesses / clock cycle can be increased to the three. Motorola DSP 5600X, DSP 96002, etc.

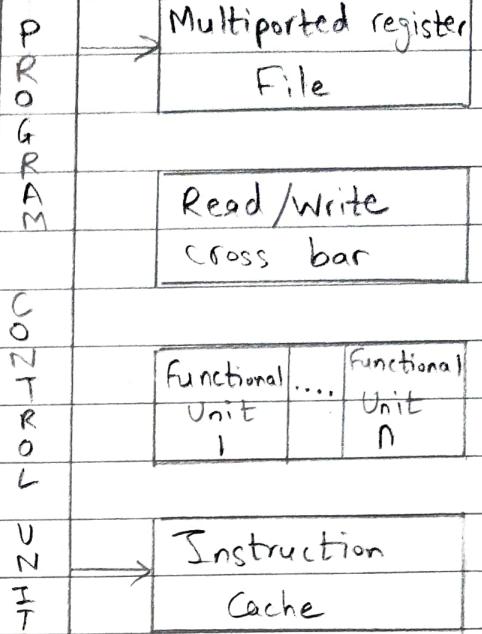
have three separate busses. TMS320C54X has four address buses.

Since the cost of an IC increases with the number of pins in the IC, extending a number of busses outside the chip would unduly increase the price. Hence the P-DSP's use multiple buses only for connecting the on-chip memory to the control unit & data path for accessing off chip memory only a single bus is used for accessing both the program memory & data memory. Because of this, any operation that involves on off-chip memory is slow compared to that using the on-chip memory.

Q7) Explain how a higher throughput is obtained through VLIW architecture. Given an example of a DSP that uses VLIW architecture.

→ Another architecture used for P-DSP's for example in TMS320C6x, is the very long instruction word (VLIW) architecture. These P-DSP's have a number of processing units (data paths). In other words, they have a number of ALU's, M.A.C units, shifters, etc. The VLIW is accessed from memory and its used to specify the operands and operations to be performed by each of the data paths. As shown in fig, the multiple functional units share common multi-parted register file for fetching the operands & storing the results. Parallel random access by the functional units to the register file is facilitated by the read/write cross bar. Execution of the operations in the functional units is carried out concurrently with the load/store operation of data between a RAM & the register file. The performance gains that can be

achieved with VLIW architecture depends on the degree of parallelism in the algorithm selected for a DSP application & the number of functional units. The throughput will be higher only if the algorithm involves execution of independent operations. For example in fig by using eight functional units the time required for convolution can be reduced by a factor of 8 compared to the case where a single functional unit is used. However, it may not always be possible to have independent stream of data for processing. Further the number of functional units is also limited by hardware cost for the multiported register file & cross bar switch.



Block Diagram of VLIW architecture

- Q8) Explain what is meant by instruction pipelining. Explain with one example how pipelining increases throughput efficiency.
- One of the approaches adopted for increasing the efficiency of the advanced microprocessors as well as P-DSP's is instruction pipelining. An instruction cycle starting with the fetching of an instruction & ending with the execution of the instruction including the time storage of the results can be split into a number of ~~micro~~ microinstructions. Execution of each of the microinstructions is also referred to as one phase of an instruction. For example, an instruction cycle requiring four microinstructions can be said to be in four phases as well follows:-
- i) Fetch phase in which the instruction is fetched from the program memory.

- 2) Decode phase in which the instruction is decoded.
- 3) Memory read phase in which the operand required for the execution of the instruction may be read from the data memory.
- 4) Execution phase in which execution as well as the storage of the results in the either one of the registers or memory is carried out.

Each of the above microinstructions may be carried out separately by four functional units. Let us assume that each of the functional units is busy only 25% of the time.

Value of T	Fetch	Decode	Read	Execute	Value of T	Fetch	Decode	Read	Execute
1	I1				1	I1			
2		J1			2	J2	I1		
3			I1		3	I3	I2	I1	
4				I1	4	I4	I3	I2	I1
5	I2				5	I5	I4	I3	I2
6		I2			6	I6	I5	I4	I3
7			J2		7	J7	I6	I5	I4
8				I2	8	I8	I7	I6	I5
9	I3				9	I9	I8	I7	I6
10		I3			10		I9	I8	I7
11			I3		11			I9	I8
12				I3	12				I9

Fig.1 Instruction cycles of processor with no pipelining

Fig.2 Instruction cycle of a processor with pipelining.

This is because only one instruction is processed at a time at the CPU. Fig. 1 shows when a program containing three instructions I1, I2, I3 is executed.

The functional units can be kept busy almost all the time by processing a number of instructions simultaneously. Four instructions I1, I2, I3, I4 can be processed simultaneously as shown in Fig. 2. When I1 enters the decode phase I2 can enter the opode-fetch

phase & I₃ enters the decode phase. When I₁ enters the execute phase I₂ enters the operand read phase I₃ enters the decode phase & I₄ enters the opcode fetch phase. The pipeline is fully loaded now & all the functional units have useful work to do. The instructions that follow I₄ keep the functional units busy till the program is executed. Let I denote the time required for each phase of the instructions. One clock cycle of the processor corresponds to I. In a period of I₂T only three instructions can be executed in a machine without pipelining. In the same period nine instructions can be executed as shown in fig. 2.

It may be noted that the initial latency of a machine with four phases is 4T. Hence for executing a program with N instructions, the time required for execution is (N+4)T with a non-pipelined machine, the time required for executing N instructions is 4NT.

Instruction pipeline shown in fig 2 corresponds to a highly optimistic case. In the case of processors requiring single clock cycle for execution for each of the instructions in the program, the throughput shown in fig. 2 can be achieved. This is normally achieved with restricted instruction set computers (RISC). However in complex Instruction set computers (CISC), there are also instructions with multiple word requiring multiple clock cycles for execution. In this case all the functional units cannot be kept busy all the time. For example, in the case of call & branch instructions of a P-DSP, four phases or T states are required for call/branch instruction to exit execution phase. By that time two more single word instructions or one double instructions enters the instruction pipeline. These instructions should not be executed. Hence two words have to be flushed out of the instruction pipeline, before the instructions are

fetched starting from the new program address.

Q9) What are the on-chip peripherals connected to DSP processors?

→ The DSP processor TMS320CS4X ('54X) devices have different on-chip peripherals as:-

a) General purpose I/O pins:- Each 54X device has 2 general purpose I/O pins - BIO & XF. BIO is an input pin used to monitor the status of external devices. XF is a software controlled output pin that allows to signal external devices.

b) Programmable wait-state Generator - The software programmable unit-state generator extends external bus cycles upto seven multiple cycles to interface with slower external memory & I/O devices. The wait-state generator is incorporated without external hardware.

c) Programmable Bank switching logic:- The programmable bank switching logic can automatically insert one cycle when an access crosses memory bank boundaries inside program memory or data memory. This extracts cycle prevents bus contention by allowing memory devices to release before other devices start acquiring it.

d) Host Port Interface - The host port interface is an 8-bit parallel port that provides an interface to a host processor. The information is exchanged between '54X & the host through the '54X on-chip memory.

e) Hardware Timer :- The '54X features a 16-bit timing circuit with a 4-bit prescalar the timer can be stopped, restarted, reset or disabled by specified status bits.

f) Clock Generator :- Clock Generator consists of an internal oscillator & a PLL circuit. Internal crystal resonator or

external clock source can be used to drive the clock generator. The PLL circuit is used to generate an internal CPU clock.

g) Synchronous Serial ports : The synchronous serial ports are high-speed full-duplex serial ports used for direct-communication with serial devices like codes, ADC, etc. Each synchronous serial port can operate at upto $\frac{1}{4}$ th the machine cycle rate. The transmitter & receiver for this port are double buffered & individually controlled by maskable external interrupt signals.

b) Buffered serial port - The buffered serial port is enhanced with an auto buffering unit & is clocked at full machine cycle rate. It is fully-duplexed & double-buffered to offer flexible data stream length.

i) TDM serial ports:- A TDM serial port is a synchronous port that allows time-division multiplexing of the data. It is often used for multiprocessor applications.

Q10) Explain different Addressing Modes in DSP Processors.

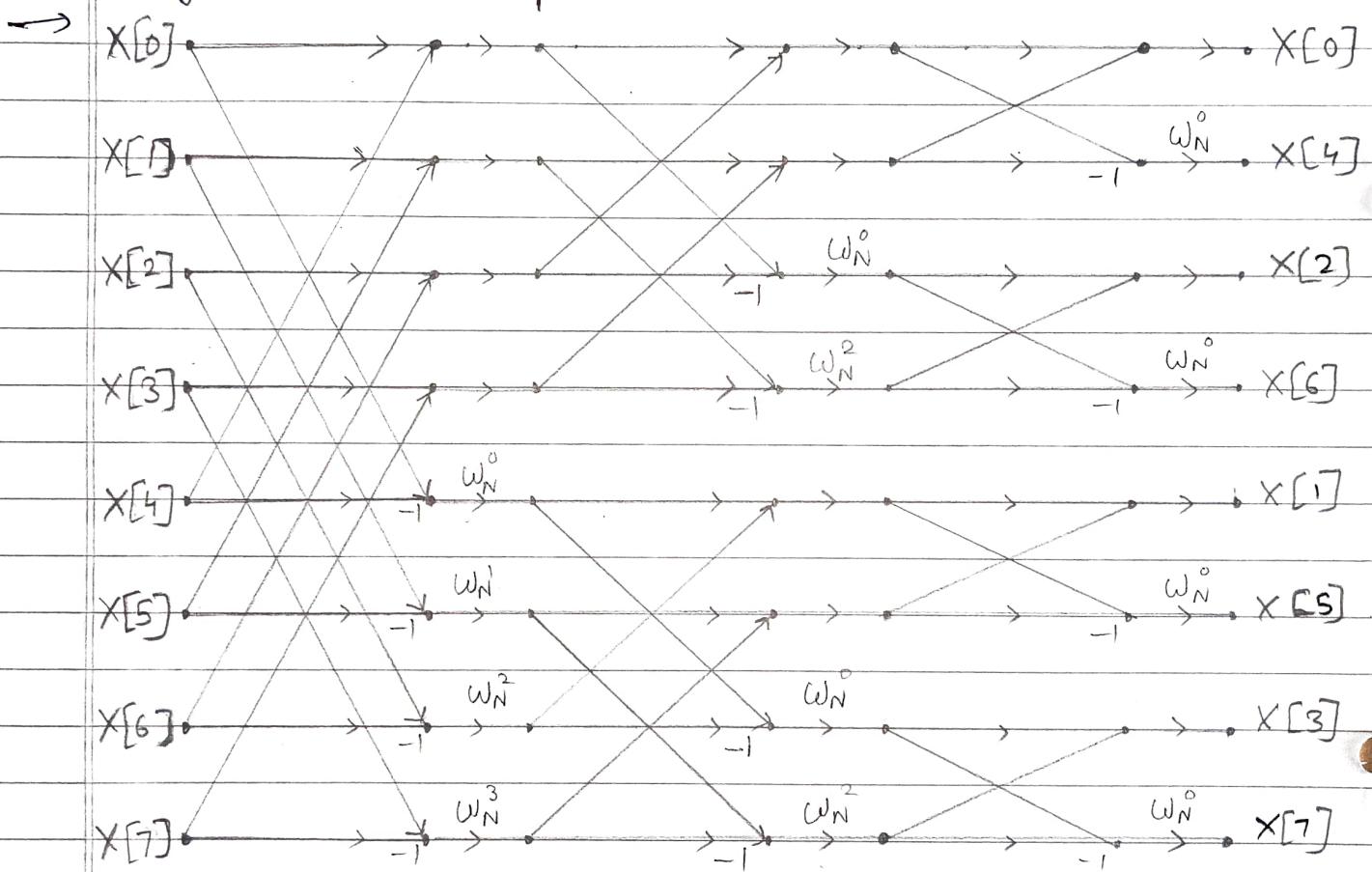
→ The DSP processors belonging to TMS320C3X series supports 6 addressing modes:-

a) Register addressing:- The syntax of register address mode is as follows: 'mnemonic src, dest'. The 'mnemonic' can be any assembly instruction code that supports register addressing. 'src' is source register & 'dst' is the destination register. The TMS320C3X processor register file contains eight extended precision register (R₀-R₇) which can be used.

b) Direct Addressing:- The no. of address bits of TMS3203X processor is 32 bits & addressable data space with 32 bits is 16M words. The data space is organized in 256 pages; each page of 64k words. Data-page pointer (DP), a 32-bit

register holds the data page value. The location of operand is in a specific page is given in the instruction code. The data page pointer is to be loaded first before the data access using direct addressing.

Q11) Draw 8 point DIF FFT flowchart Butterfly diagram from experiment 1.

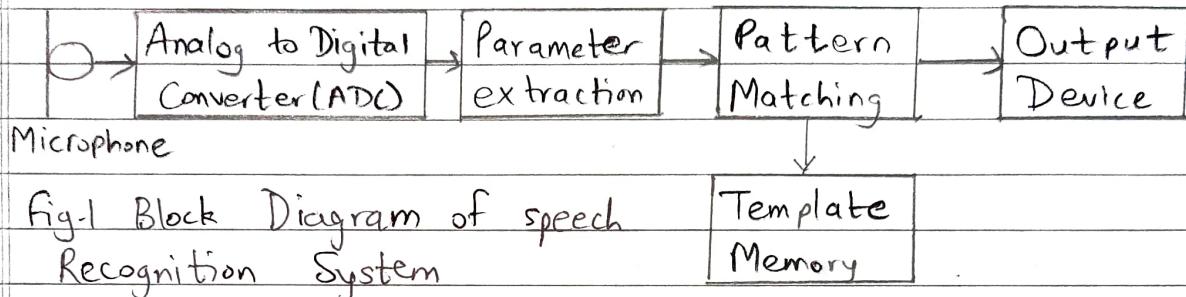


Q12) Compare number of computations in direct DFT with FFT.

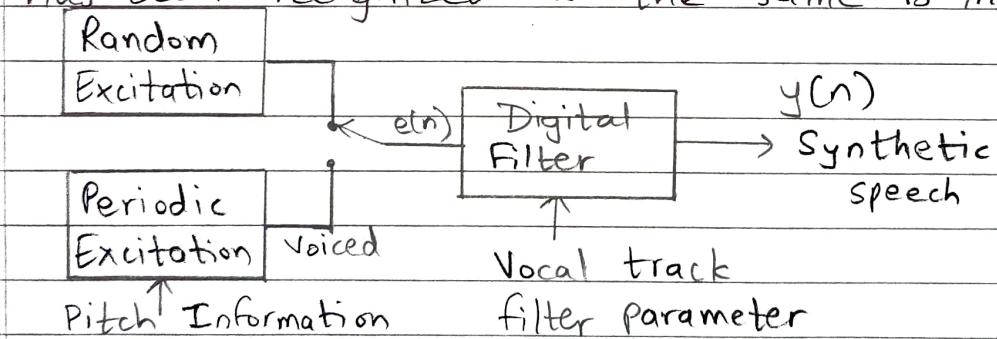
Number of points 'N'	Direct computation		Using FFT	
	Complex Multiplication (N^2)	Complex Addition ($N^2 - N$)	Complex Multiplication ($\frac{N}{2} \log_2 N$)	Complex Addition ($N \log_2 N$)
8	64	56	12	24
16	256	240	32	64
32	1024	9992	80	160
64	4096	4032	192	384

Q13) Describe speech processing system with the help of a block Diagram.

→ Speech Recognition- Speech recognition involves in putting of information into a computer using human voice & then computer quantizes the information & recognizes human speech.



As shown in fig.1 speech voice is input through microphone. The input analog signal is digitized using A/D converter. This digitized output is stored in memory. Recognition process starts after storage. Then here again the spoken word is digitized & its template is compared with template of Memory. As soon as the match occurs, this indicates that the word has been recognized & the same is informed to the user.



DSP processor plays an important role in extracting an important parameter called template from spoken word. The whole operation is done accurately by DSP Processors. Following performance parameters that greatly affect the above system too are overcome by DSP Processor.

1) Noise

2) Microphone characteristics.

③ Pause taken between two words. ④ Correct pronunciation

- Speech Synthesis - In this system, human voice is produced. To achieve this, we use linear predictive coding (LPC) technique. In human speech, voiced sound & unvoiced sound are present, voiced sound is nothing but the vowels. These represent the air flow through vocal cords while unvoiced sound are present. the noise created by forcing air in the vocal tract. Unvoiced sound is generated by random excitation while voiced sound is generated by periodic excitation. Digital filters perfectly simulates the behaviour of the vocal tract. Thus we get human speech.

- Training phase & coding :- Coding algorithms seek to minimize the bit rate in the digital representation of a signal without an objectionable loss of signal quality in the process. Quality of speech refers to how natural it sounds as compared to the words uttered by a human being. High quality is attained at low bit redundancy as well as the knowledge that certain type of coding distortion are imperceptible because they are masked by the signal.

Intelligibility & quality of speech are measured in terms of a performance index called Mean opinion score (mos).

To determine the mos of a speech source, a large number of listeners are requested to rate the given sample of speech & allot marks as shown in fig. 3.

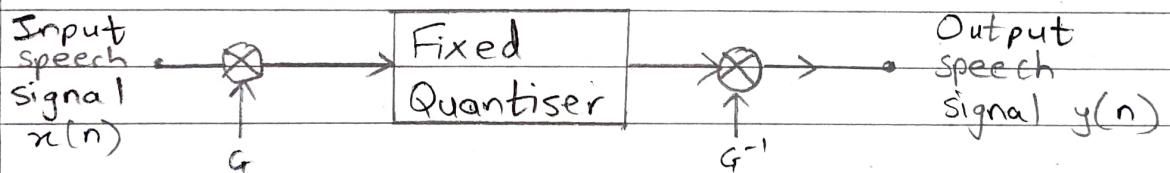
These numerical values, after averaging yield the MOS score for the coder. For a high quality coder, the Mos values range between 4.0 & 4.5.

* Methods of speech coding:

Various Methods of speech coding may be classified as under:-

① Waveform coding.

- a) Pulse coding Modulation (PCM)
- b) Adaptive pulse-code -Modulation (APCM)
- c) Linear Predictive coding -
 - Differential pulse-code Modulation (DPCM)
 - Adaptive Differential Pulse-code Modulation (ADPCM)
 - Delta Modulation (DM)
 - Adaptive Delta Modulation (ADM)
 - Continuously variable-slope Delta Modulation (CVSDM)
- d) Frequency-Domain coding -
 - Transfer coding (TC)
 - Adaptive Transform coding (ATC)
 - Subband coding (SBC)
 - Baseband coding (BBC)
 - Narrowband coding
 - Pitch-Excited coder
 - Optimal scalar Quantisation (OSQ)
 - Segment Quantisation (SQ)



- Q14) Explain in detail :- Methods of speech coding
- Waveform coding aims at reproducing the speech waveform as faithfully as possible. The waveform coders are able to produce high-quality speech at high enough bit rates.
- Waveform coding includes:-
- D) Pulse - code Modulation (PCM) :- PCM is the simplest coding system, a memoryless quantizer & provides essentially transparent coding of telephone speech at 64 kbps. This waveform coding scheme employs uniform quantisation in which

the range of signal value of $x(n)$ is subdivided into small equal bins, each of width Δ ; the step size & all signal values falling within a bin are decoded to one value in that particular bin. Dithering is used to weaken the signal dependent character of quantisation noise. In Dithering, a pseudo random sequence is added to the signal prior to its quantisation & subsequently at the receiver the same sequence is subtracted from the decoder output yielding an almost white quantising error.

2) Adaptive Pulse-code Modulation(APCM).

Here the quantiser adjusts the step size according to the short-term amplitude of the signal fig. gives a schematic illustration of the Adaptive Pulse-code Modulation system.

3) Linear Predictive Coding(LPC).

In this scheme the waveform coding is based on a linear prediction model of speech at any instant as a predicted value plus an error term. For rates of 16 kbps & lower, high speech quality is achieved by using LPC. The most familiar examples of LPC are as under:-

i) Differential-pulse code Modulation(DPCM): In this system, predictor has the simple form as, $a(z) = 1 + a_1 z^{-1}$ where a_1 is fixed negative number calculated by determining the long-term average of the signal spectrum & computing the optimal $a(z)$ for $P=1$. Fixed predictions of higher order, $P > 1$, can also be used but beyond $P=4$, the approach has not much utility.

ii) Adaptive Differentiate pulse-code-Modulation(ADPCM).

In ADPCM the predictor changes or modifies itself according to the requirement of the signal. ADPCM provides high

quality speech at 32 kbps. The speech quality is slightly inferior to that of 64 kbps PCM. ADPCM at 32 kbps is widely used for expanding the number of speech channels by a factor of two, particularly in private networks & international circuits. It is also the basis of low-complexity speech coding in several proposals for personal communication networks.

iii) Delta Modulation (DM)

In DM, the waveform sampling rate is much larger than the Nyquist rate to increase the adjacent sample correlation & the quantisation of the residual or difference signal into a one-bit or two-level strategy enabling the transmission of the difference only. Here bit rate is equal the sampling rate.

iv) Adaptive Delta Modulation (ADM)

In ADM, variable step size is used depending on the quantizer outputs. In a two level quantizer, observation of a single sample of quantiser output does not indicate the slope overload distortion or granularity. Therefore a sequence of quantiser outputs is required for the desired step size adaption.

v) Continuously Variable slop-Delta (CVSD) Modulation.

CVSD Modulation technique includes smooth adaption of the step size with a time control 5-10 ms. CVSD coders are more tolerant to channel errors & decrease the granular noise in output speech at the expense of a high slope overload distortion. CVSD codes give a clean-sounding speech at bit rates less than 24 kbps.

vi) Frequency Domain Coding:

Frequency domain coders uses the non-flat short-term spectral characteristics of the speech signal, constituting the

redundancy & the signals at a level lower than the ear & are called the Irrelevancy. Redundancy & irrelevancy removal in frequency domain coders is accomplished by decomposing the source spectrum into frequency bands containing uncorrelated spectral components of the signal. These components are quantized separately. At the receiver, the components are subjected to an inverse transformation to obtain the reconstructed signal. There are two main forms of speech coding in the frequency domain as follows:

i) Transform Coding (TC):-

TC is a frequency domain technique in which a block of input examples is taken & linearly transformed using DFT or DCT computation via a FFT algorithm. Then the transformation of the signal is efficiently coded by assigning bits to transform coefficient. At receiver, an inverse transformation is used to reconstruct the speech signal.

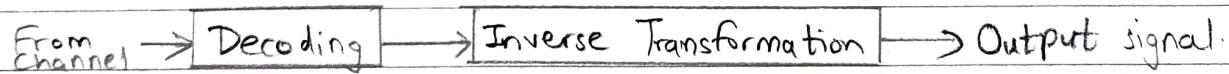
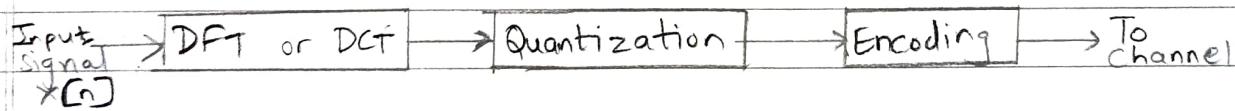


fig.1 Transform coding System.

In TC, total number of bits available to quantize the transform coefficients remains constant whereas in adaptive transform coding, the bit allocation to each coefficient changes from frame to frame. This dynamic bit allocation is controlled by time varying characteristics of speech, which have to be transmitted as side information. The side information is also used to determine the step sizes of the various coefficient quantizer. The number of bits

assigned to each transform coefficient is proportional to its corresponding spectral energy value.

ii) Adaptive Transform Coding (ATC)

In ATC, important thing is the determination of bit assignment or the number of bits used for quantising individual transform coefficient. In the presence of channel errors, the received side information may yield inaccurate bit assignment. This may lead to wrong decoding of the received bit stream into transform coefficients which spoils the quality of speech. Side information should be safe guard against channel noise.

iii) Subband Coding.

The speech signal is applied to an analysis filterbank consisting of a set of bandpass filters. This digital filtration divides the speech signal into a number of non-overlapping frequency bands. By additive recombination of the set of subband signals, we can generate the original sp.

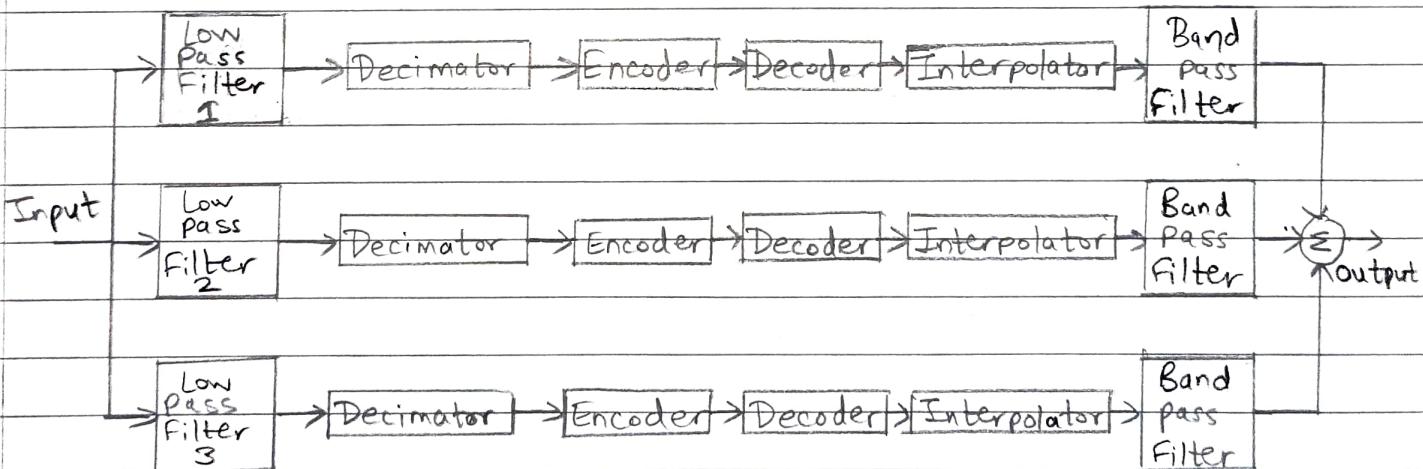


Fig 2 . Subband coder.

Each band of non-overlapping frequency is passed through a low-pass filter (LPF) & decimated. Each band is separately quantized & coded using PCM, DPCM, etc. & transmitted. In the receiver, the sampling rate of each band is raised to that of the source signal by inserting proper number of

Zero samples. Then subband samples appear at the bandpass outputs of the synthesis filter bank. The sum of bandpass output is equal to source signal without quantisation as shown in fig. 2

iii) Baseband coding :

At bit rates $< 12 \text{ kbps}$, the speech quality of waveform encoders falls down. If we wish to achieve higher speech speech quality at lower bit rates, we must consider input / output signal matching characteristics instead of quality resemblance of output speech with input speech. According to fig. in baseband coding, the input signal is inverse filtered to extract the baseband signal. The full signal is not transmitted, only a portion is sent for which a lower transmission rate suffices.

In the receiver, the baseband signal is decoded

iv) Narrowband coding :

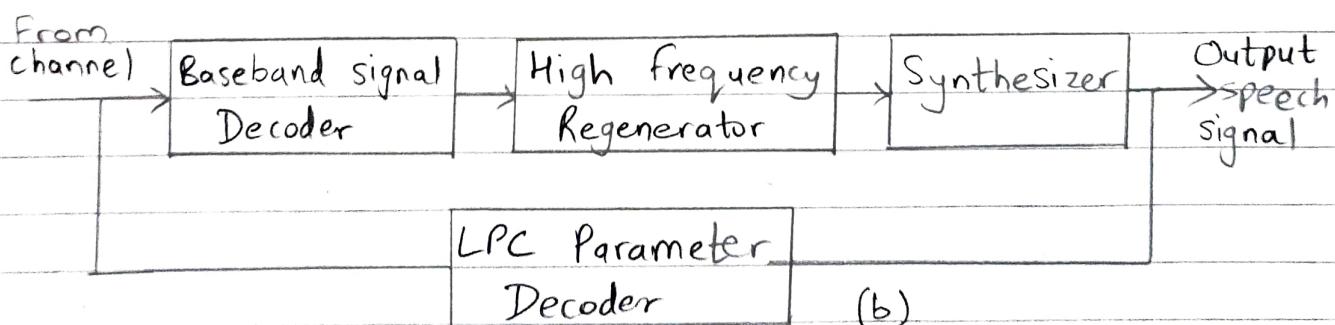
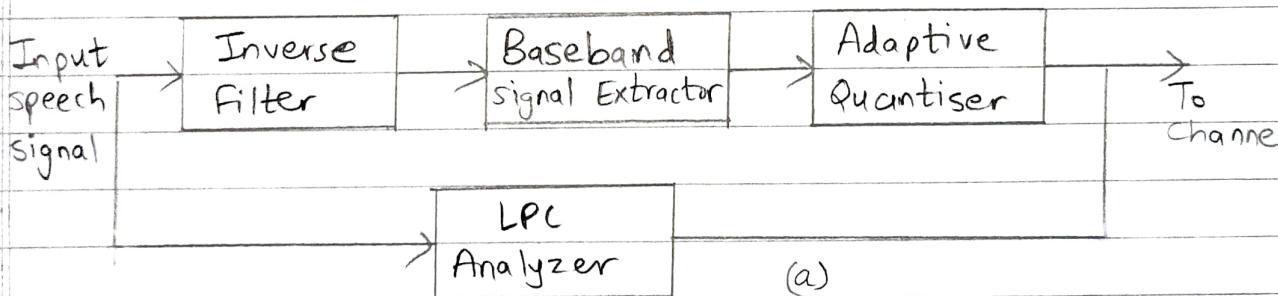


Fig 3. Baseband Coding (BBC) system.

(a) Pitch - Excited coder - This method is based on a mixed source model of speech as shown in fig. 4. Here a pulse

source is used for exciting low frequencies. A white noise source excites the high frequency. The energy level of each frame is decided by a gain parameter. Generally, pitch is quantized to six bits & gain to five bits.

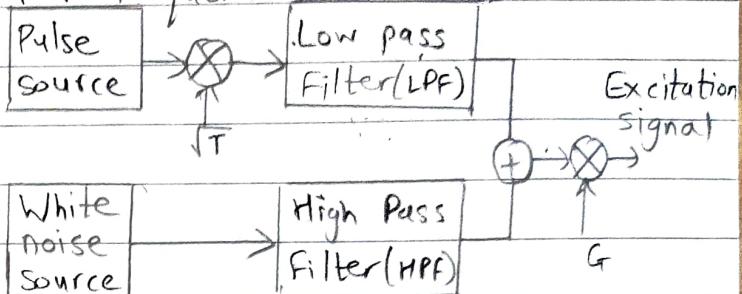


Fig. 4 Pitch-Excited Model

b) Optimal scalar Quantization:

This method exploits the correlation among a set of P parameters represented by a random vector \vec{x} to be quantized to b bits, to decrease the bit rate. It is a three-step process:

- Parameter Decorrelation:- In which a new parameter vector \vec{u} is using a matrix Q whose columns are the eigen vectors of the covariance matrix of random vector \vec{x} as $\vec{y} = Q\vec{x}$
- Bit allocation:- In which the given bits are assigned among the P components of \vec{y} .
- Scalar Quantisation:- In which each component y_i is quantized using b_i bits. At receiving station, the quantized vector \vec{y}' is obtained from \vec{y} by the inverse transformation i.e $\vec{x}' = Q\vec{y}'$.

c) Vector Quantisation:-

This method reduces the bit rate by statistical dependence among parameters beyond correlation. It is based on clustering procedure. Vector quantities consume large amount of memory & computational space. They are used at low bit rates, one bit per parameter in the region where scalar quantisers are insufficient.

d) Segment Quantization:-

Segment quantisation utilizes interdependence between frames

Segments of a suitable size are obtained by dividing the speech into phoneme boundaries. A diphone is the region separating the equilibrium state of the phoneme from that of the next. By wrapping two segments can be made to possess an equivalent number of ~~for~~ frames. While in dynamic time warping, the distance between adjacent segments is minimized. By Dynamic programming, the computational load is decreased.

Q15) Applications of DSP Processors.

→ C1X, C2X, C2XX, C5X, C54X:- Toys, Hard disk drives, modems, cellular phones & active car suspensions.
C3X:- Filters, Analysers, Hi-fi systems, voice mail; Imaging, Bar-code readers, Motor control, 3D graphics or scientific processing.

C4X:- Parallel processing clusters in virtual reality-
Image recognition telecom routing & parallel processing systems.

C6X: Wireless base stations, pooled modems, remote-access servers, digital subscriber loop systems, cable modems & multichannel telephone systems.

C8X:- Video telephony, 3D computer graphics, virtual reality & a number of multimedia applications.

Q16) The first 5 points of the 8 point DFT of a real valued sequence is $0.25, 0.125 - j0.3018, 0, 0.125 - j0.0518, 0$. Determines the remaining ~~the~~ three points

→ Given DFT points are:-

$$X(0) = 0.25$$

$$X(3) = 0.125 - j0.0518$$

$$X(1) = 0.125 - j0.3018$$

$$X(4) = 0$$

$$X(2) = 0$$

Given sequence is a real valued sequence. According to that,

$$x^*(k) = x(N-k) \quad \dots (i)$$

$$\text{or } x(k) = x^*(N-k).$$

This is 8 point DFT. Thus $N=8$

$$\text{Therefore, } x(k) = x^*(8-k)$$

Now, we want remaining three samples namely $x(5), x(6)$ & $x(7)$, we have

$$x(5) = x^*(8-5) = x^*(3)$$

$$\therefore x(3) = 0.125 - j 0.0518$$

$$x^*(3) = 0.125 + j 0.0518$$

$$\therefore x(5) = 0.125 + j 0.0518$$

Substituting $k=6$ in equation (ii), we have

$$x(6) = x^*(8-6) = x^*(2)$$

$$\therefore x(2) = 0 \quad \therefore x^*(2) = 0$$

$$\therefore x(6) = 0$$

Similarly substituting $k=7$ in equation (ii) we obtain

$$x(7) = x^*(8-7) = x^*(1)$$

$$\therefore x(1) = 0.125 - j 0.03018$$

$$\therefore x(7) = 0.125 + j 0.03018$$



D7) Comparison between Impulse Invariance Method & Bilinear Transformation Method.

→ Impulse Invariance Method

i) Poles are transferred by using the expression

$$\frac{1}{s-p_1} \rightarrow \frac{1}{1-e^{p_1 T} z^{-1}}$$

Bilinear Transformation Method

Poles are transferred by using the expression

$$s = \frac{2}{T} \left[\frac{z-1}{z+1} \right]$$

2) Mapping is many to one

Mapping is one to one

3) Aliasing effect is present

Aliasing effect is not present

4) It is not suitable to design high-pass filter & band reject filter

High-pass filter & band reject filter can be designed.

Filter

Teacher's Sign.:

- 5) Only poles of the system can be mapped.
 Poles as well as zero can be mapped.
- 6) No frequency warping effect Frequency warping effect is present.

Q18) The transfer function of analog filter is

$$H_a(s) = \frac{3}{(s+2)(s+3)} \quad \text{with } T = 0.1 \text{ sec.}$$

→ Design the digital IIR filter using BLT.
 → The given transformation (BLT) $H(z)$ is obtained by substituting. $s = \frac{2}{T} \left[\frac{z-1}{z+1} \right]$

Here T = Sampling time = 0.1 sec.

$$s = \frac{2}{0.1} \left[\frac{z-1}{z+1} \right] = 20 \left[\frac{z-1}{z+1} \right]$$

Substituting this value in equation (i), we get

$$H(z) = \frac{3}{\left[\frac{20(z-1)+2}{z+1} \right] \left[\frac{20(z-1)+3}{z+1} \right]} = \frac{3}{\left[\frac{20z-20+2}{z+1} \right] \left[\frac{20z-20+3}{z+1} \right]}$$

$$H(z) = \frac{3(z+1)(z+1)}{(20z-20+2z+2)(20z-20+3z+3)} = \frac{3(z+1)^2}{(22z-18)(23z-17)}$$

$$H(z) = \frac{3(z^2 + 2z + 1)}{506z^2 - 374z - 414z + 306} = \frac{3(z^2 + 2z + 1)}{506z^2 - 788z + 306}$$

$$= \frac{z^2 + 2z + 1}{168.67z^2 - 262.67z + 102}$$

This is required transfer function for digital IIR filter

Q19) Write short note on Aliasing in Bilinear Transformation along with Advantages of BLT.

→ The main difference between impulse invariance and bilinear Transformation is that there is no aliasing.

effect in bilinear transformation. Observe that the complete $j\omega$ axis is mapped on the unit circle only once. But impulse invariance the

segments $\frac{(2k+1)\pi}{T} \leq \omega \leq \frac{(2k+1)\pi}{T}$ of

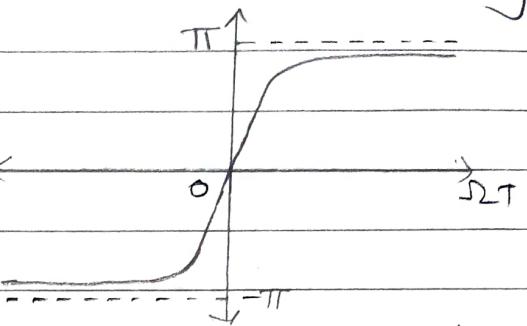
$j\omega$ axis are all mapped on unit circle repeatedly. Thus the transformation

is many to one. Hence problem of aliasing takes place in impulse

invariance method. The problem of with bilinear transformation is that the frequency relationship is non-linear.

Advantages of Bilinear Transformation Method:-

- 1) There is one-to-one transformation from the s -domain to the z -domain
- 2) The mapping is one-to-one
- 3) There is no aliasing effect.
- 4) Stable analog filter is transformed into the stable digital filter.



Mapping between $j\omega$ and $j\Omega$ in bilinear transformation

Q5) Determine the 8-point DFT of the following sequence

$X(n) = \{1, 1, 1, 1, 0, 0, 0, 0\}$. Use in-place radix-2 decimation in time FFT algorithm.

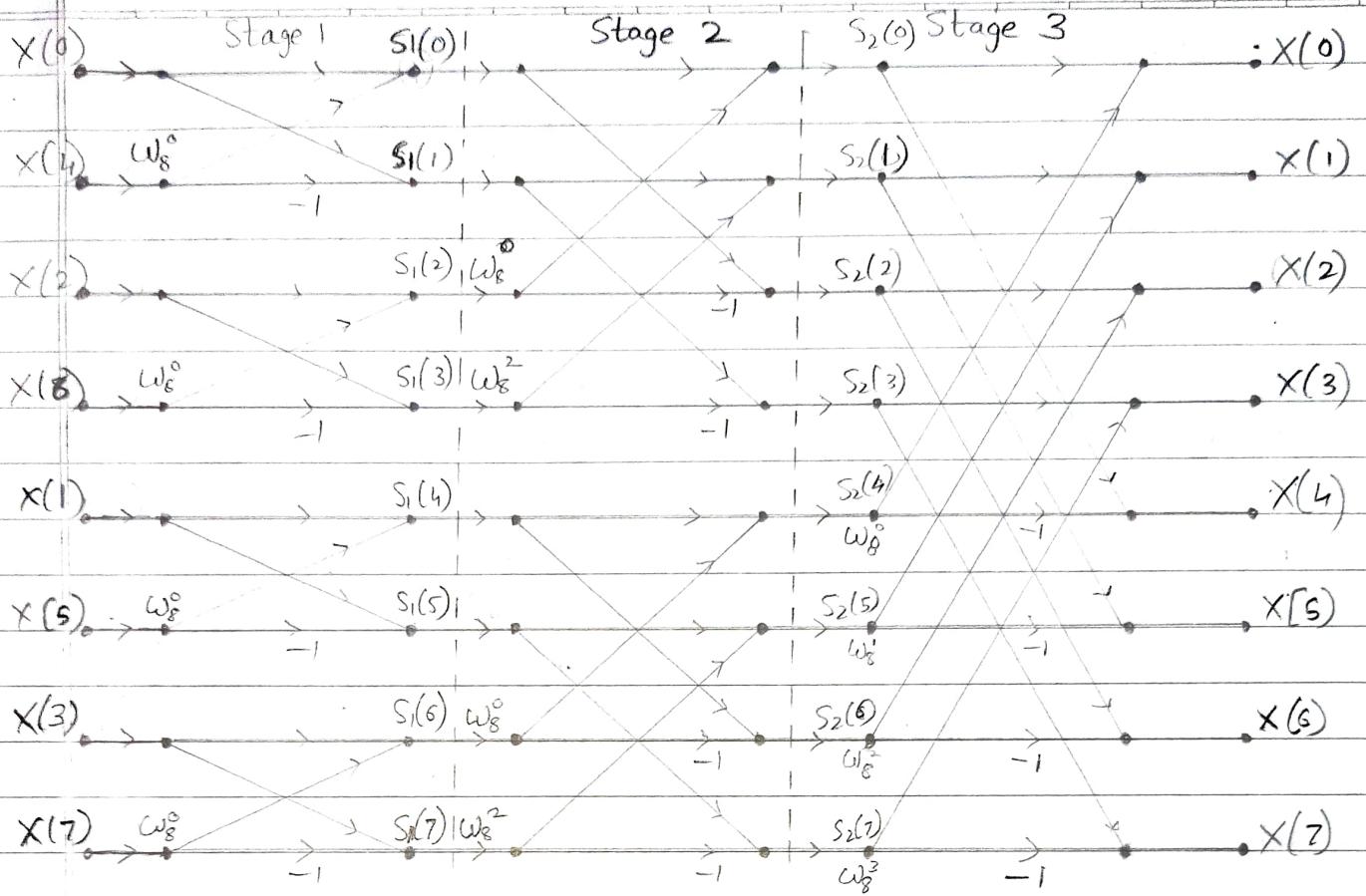
→ The flow chart has been shown in figure. Hence $S_1(n)$ represents output of stage 1 & $S_2(n)$ represents output of stage 2. The different value twiddle factor are

$$\omega_8^0 = e^0 = 1$$

$$\omega_8^1 = e^{-j\pi/4} = 0.707 - j0.707$$

$$\omega_8^2 = e^{-j\pi/2} = -j$$

$$\omega_8^3 = -0.707 - j0.707$$



Output of Stage 1

$$S_1(0) = X(0) + w_8^0 X(4) = 1$$

$$S_1(1) = X(0) - w_8^0 X(4) = 1$$

$$S_1(2) = X(2) + w_8^0 X(6) = 1$$

$$S_1(3) = X(2) - w_8^0 X(6) = 1$$

$$S_1(4) = X(1) + w_8^0 X(5) = 1$$

$$S_1(5) = X(1) - w_8^0 X(5) = 1$$

$$S_1(6) = X(3) + w_8^0 X(7) = 1$$

$$S_1(7) = X(3) - w_8^0 X(7) = 1$$

Output of Stage 2

$$S_2(0) = S_1(0) + w_8^0 S_1(2) = 1 + 1 \times 1 = 2$$

$$S_2(1) = S_1(1) + w_8^0 S_1(3) = 1 - j$$

$$S_2(2) = S_1(0) - w_8^0 S_1(2) = 1 - 1 = 0$$

$$S_2(3) = S_1(1) - w_8^0 S_1(3) = 1 + j$$

$$\begin{aligned}
 S_2(4) &= S_1(4) + \omega_8^0 S_1(6) = 1 + 1 = 2 \\
 S_2(5) &= S_1(5) + \omega_8^0 S_1(7) = 1 - j \\
 S_2(6) &= S_1(4) - \omega_8^0 S_1(6) = 1 - 1 = 0 \\
 S_2(7) &= S_1(5) - \omega_8^0 S_1(7) = 1 + j
 \end{aligned}$$

Output of stages

$$\begin{aligned}
 X(0) &= S_2(0) + \omega_8^0 S_2(4) = 2 + 2 = 4 \\
 X(1) &= S_2(1) + \omega_8^1 S_2(5) = (1 - j) + (0.707 - j0.707)(1 - j) = 1 - 2.414j \\
 X(2) &= S_2(2) + \omega_8^2 S_2(6) = 0 \\
 X(3) &= S_2(3) + \omega_8^3 S_2(7) = (1 + j) + (-0.707 - j0.707)(1 + j) = 1 - 0.414j \\
 X(4) &= S_2(0) - \omega_8^0 S_2(4) = 2 - 2 = 0 \\
 X(5) &= S_2(1) - \omega_8^1 S_2(5) = (1 - j) - (0.707 - j0.707)(1 - j) = 1 + 0.414j \\
 X(6) &= S_2(2) - \omega_8^2 S_2(6) = 0 \\
 X(7) &= S_2(3) - \omega_8^3 S_2(7) = (1 + j) - (-0.707 - j0.707)(1 + j) = 1 + 2.414j \\
 X(k) &= \{4, 1 - 2.414j, 0, 1 - 0.414j, 0, 1 + 0.414j, 0, 1 + 2.414j\}
 \end{aligned}$$