```
`timescale 1ns / 1ps
// Company:
// Engineer:
// Create Date: 03/02/2020 09:13:50 PM
// Design Name:
// Module Name: state machine
// Project Name:
// Target Devices:
// Tool Versions:
// Description:
//
// Dependencies:
// Revision:
// Revision 0.01 - File Created
// Additional Comments:
module state machine(
  );
endmodule
`timescale 1ns / 1ps
// Company:
// Engineer:
// Create Date: 02/10/2020 02:16:43 AM
// Design Name:
// Module Name: StateMachine
// Project Name:
// Target Devices:
// Tool Versions:
// Description:
//
// Dependencies:
//
// Revision:
// Revision 0.01 - File Created
// Additional Comments:
//
```

```
module state machine(
   input start, clk, crash, twoSecs,
   output started, blinkCar, resetScore, starting, resetTimer, loadRoad,
countScore, blinkScore, resetLED
   );
   wire SPAWN, STARTING, STARTED, STOPPED;
   wire Next SPAWN, Next STARTING, Next STARTED, Next STOPPED;
   wire [6:0]PS;
   wire [6:0]NS;
   assign SPAWN = PS[0];
   assign STARTING = PS[1];
   assign STARTED = PS[2];
   assign STOPPED = PS[3];
   assign NS[0] = Next SPAWN;
   assign NS[1] = Next STARTING;
   assign NS[2] = Next STARTED;
   assign NS[3] = Next STOPPED;
    assign Next SPAWN = SPAWN & ~start;
    assign Next STARTING = (((SPAWN | STOPPED) & start) | (STARTING & ~twoSecs));
    assign Next STARTED = (STARTING & twoSecs) | (STARTED & ~crash);
    assign Next STOPPED = (STARTED & crash) | (STOPPED & ~start);
    assign blinkCar = STOPPED | STARTING;
    assign blinkScore = STOPPED;
    assign loadRoad = (SPAWN & ~start) | (STOPPED & start);
    assign resetTimer = ((SPAWN|STOPPED) & start) | (STARTING & twoSecs);
    assign started = STARTED;
    assign starting = STARTING;
    assign resetScore = SPAWN | STARTING;
    assign countScore = STARTED;
    assign resetLED = STARTING & twoSecs;
//
     assign Next WAITING = ( (WAITING | LtR | LtR R | RtL | RtL L) & (L & R) );
//
     assign Next LtR = ( (LtR | WAITING | LtR C) & (\simL & R) );
//
     assign Next LtR C = ((LtR C | LtR | LtR R) & (~L & ~R));
//
     assign Next LtR R = ((LtR R | LtR C) & (L & ~R));
     assign Next RtL = ( (RtL | WAITING | RtL C) & (L & ~R) );
//
     assign Next RtL C = ((RtL C | RtL | RtL L) & (~L & ~R));
//
//
     assign Next RtL L = ((RtL L | RtL C) & (\sim L \& R));
```

```
// assign LeftFromLeft = (RtL_L & L & R);
// assign DisplayTimer = ~WAITING;
// assign ResetTimer = WAITING;

FDRE #(.INIT(1'b1)) Q0_FF (.C(clk),.CE(1'b1),.D(NS[0]),.Q(PS[0]));
   FDRE #(.INIT(1'b0)) Q6_FF[3:1]
(.C({3{clk}}),.CE({3{1'b1}}),.D(NS[3:1]),.Q(PS[3:1]));
endmodule
```

assign LeftFromRight = (LtR\_R & L & R);

//