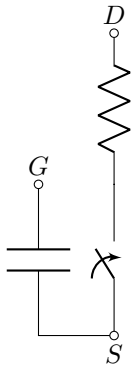
Lecture 2 - Notes

Rahul Arya

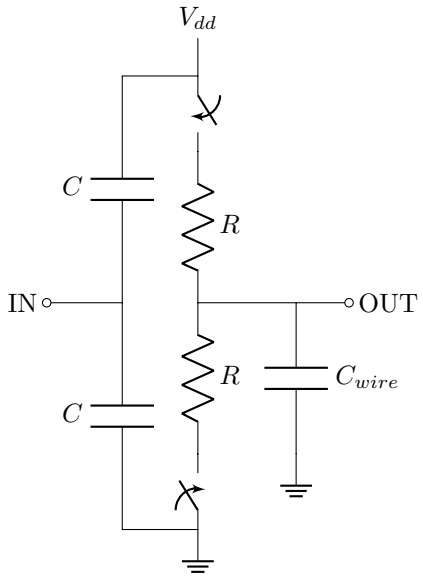
January 2019

1 CMOS Capacitance and Homogeneous Linear Differential Equations

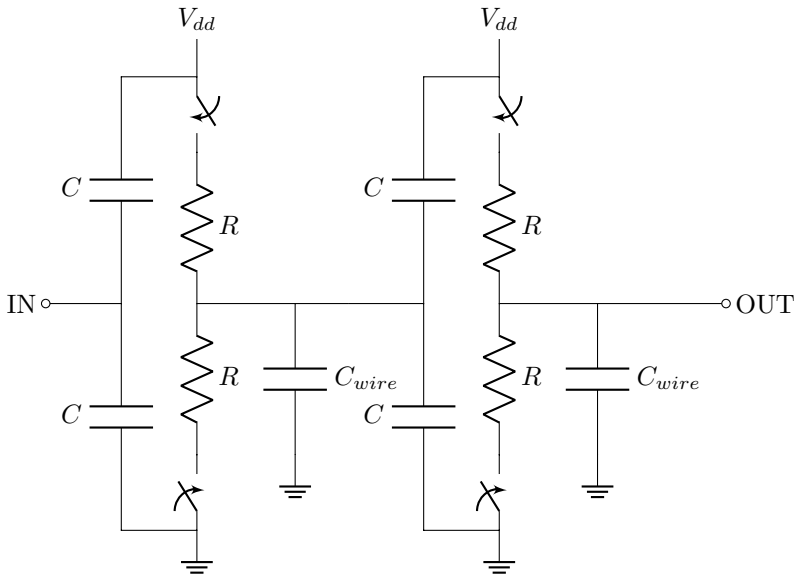
So far, we have viewed CMOS transistors as components with either 0 or infinite resistance, depending on the voltage between their gate and the source. However, in reality, they possess some internal resistance between the source and the drain, even when current is flowing. Moreover, there exists some capacitance between the gate and source, regardless of the state of the transistor. Thus, we can view a CMOS transistor as follows:



Putting two of these transistors together to form a CMOS inverter, we obtain



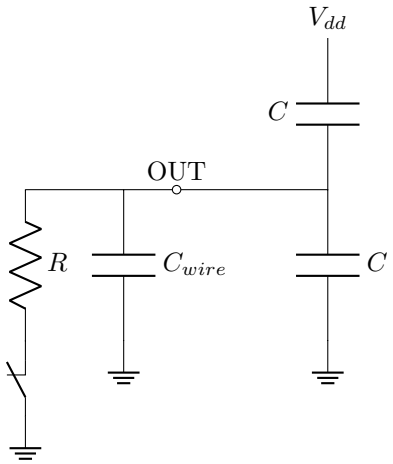
We will show that these resistances and capacitances effectively add a *delay* to CMOS circuits, so changes to the input will take some time to "propagate" to the output. Note that the wire leading to the OUT terminal also has some capacitance to ground. In fact, in modern transistors, that capacitance is larger than the capacitance between the gate and the source. Thus, to obtain a more complete picture, we will consider two inverters connected together, as follows:



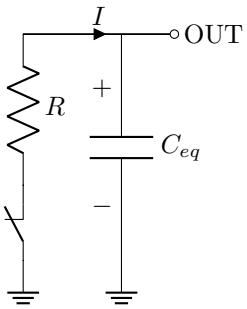
However, we will only analyze the first inverter. We will first consider the case

when the first inverter starts with the input connected to ground, with the system as a whole in steady state. From the previous lecture, we know that the first output terminal will be outputting a logical 1, and so is at voltage V_{dd}. Right now, the lower left switch (of the NMOS transistor) is open, and the upper left switch (of the PMOS transistor) is closed.

At time $t = 0$, we connect the input to V_{dd}. The lower switch immediately closes, and the upper switch immediately opens. Thus, deleting disconnected components and other components that do not directly affect the first inverter, we obtain the following circuit:



It can be shown that we can rearrange the remaining capacitors into a single equivalent capacitance C_{eq}, to obtain the circuit:



Let $Q(t)$ be the charge on the capacitor (following passive sign convention). Thus, by KVL and the capacitor equation $Q = VC$, moving counterclockwise around the circuit, we obtain

$$0 = I(t)R + \frac{Q(t)}{C_{eq}}.$$

Let $V_C(t)$ be the voltage across the capacitor (and also the voltage at the output

terminal). From Ohm's Law,

$$\begin{aligned} I(t)R &= 0 - V(t) \\ &= -V(t) \\ \implies \quad I(t) &= -\frac{V(t)}{R}. \end{aligned}$$

From the capacitor equation,

$$\begin{aligned} Q(t) &= C_{eq}V(t) \\ \implies \quad I(t) &= C_{eq}\frac{\mathrm{d}V}{\mathrm{d}t}. \end{aligned}$$

Combining these two results for $I(t)$, we obtain

$$\begin{aligned} C_{eq}\frac{\mathrm{d}V}{\mathrm{d}t} &= -\frac{V(t)}{R} \\ \implies \quad \frac{\mathrm{d}V}{\mathrm{d}t} &= -\frac{1}{RC_{eq}}V(t). \end{aligned}$$

Thus, we have obtained a first order homogeneous linear differential equation for the voltage at the output terminal. Recall that the initial output voltage was $V(0) = V_{dd}$, since the first inverter previously had its input connected to ground.

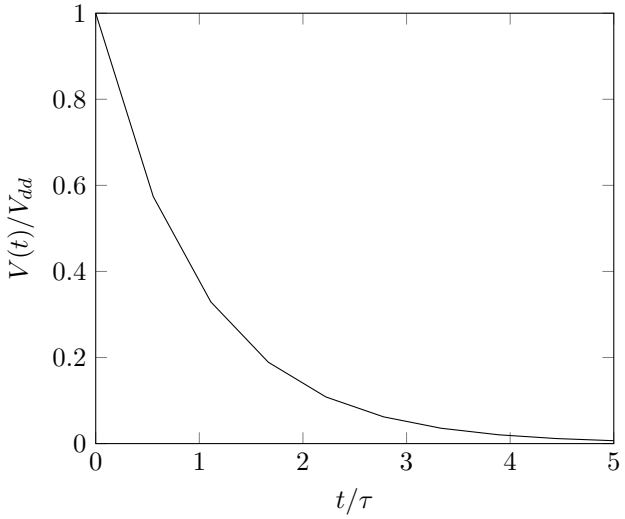
Solving using known techniques, we obtain

$$\begin{aligned} \frac{1}{V(t)}\mathrm{d}V &= -\frac{1}{RC_{eq}} \\ \implies \quad \ln V(t) - \ln V(0) &= -\frac{t}{RC_{eq}} \\ \implies \quad V(t) &= V(0)e^{-t/(RC_{eq}} \\ \implies \quad V(t) &= V_{dd}e^{-t/(RC_{eq})}. \end{aligned}$$

We call the quantity RC_{eq}, which has units of time, the *time constant* τ of this circuit. Thus, we can write the output voltage as

$$V(t) = V_{dd}e^{-t/\tau},$$

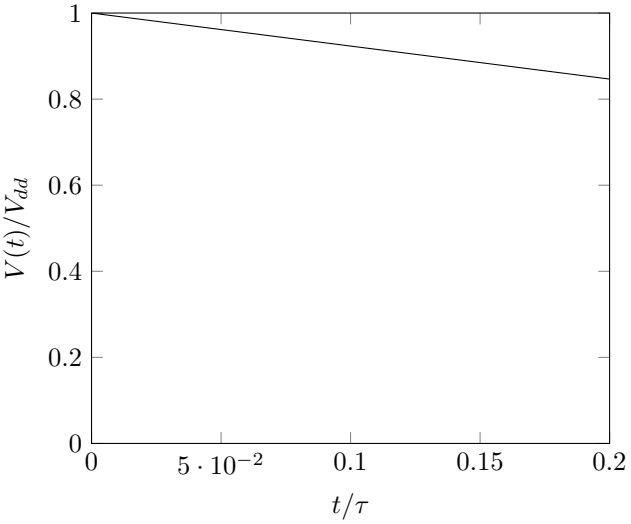
which is the form in which it is most commonly seen. Plotting this function,



we see that it tends rapidly to 0 (which is the steady state solution of an inverted with the input voltage set to a logical 1), but never actually reaches it.

From the formula, we also see that every τ units of time, the voltage gets closer to the target voltage 0 by a constant. After τ seconds, $V(t)$ drops to $0.37V_{dd}$. After 3τ seconds, $V(t)$ drops to $0.05V_{dd}$. And after 7τ seconds, $V(t)$ drops to $0.001V_{dd}$, which we can treat as 0 for all practical purposes.

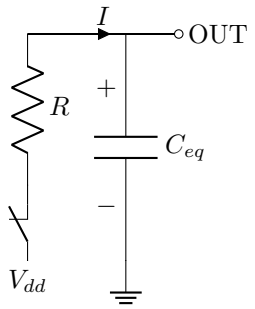
It may be conjectured at this stage that this resistance and capacitance business doesn't really matter, since $V(t)$ approaches the target voltage very quickly. However, this behavior is only true for values of t of the order of τ. Looking at just the early portion of this graph ($0 \leq t \leq \tau/5$),



we see that $V(t)$ barely drops from its initial value of V_{dd}, so the importance of these capacitive effects really depends on the time scales that we are working in.

2 Inhomogeneous Differential Equations

We can obtain similar results in the case of an inverter switching from an input of logical 1 to logical 0. Skipping over some steps, we obtain the equivalent circuit



More precisely, using the same variable definitions as before and following a similar approach, we obtain the differential equation

$$\frac{\mathrm{d}V}{\mathrm{d}t} = \frac{1}{RC_{eq}}(V_{dd} - V(t)).$$

This equation is an *inhomogeneous* linear first order differential equation. We say it is inhomogeneous because there is a constant term, in addition to the $V(t)$ and $\frac{\mathrm{d}V}{\mathrm{d}t}$ terms. To solve this equation, one way is to come up with a substitution for $V(t)$ that makes the equation homogeneous. Here, we will guess the substitution

$$\begin{aligned} & V_\Delta(t) = V(t) - V_{dd} \\ \implies \quad & \frac{\mathrm{d}V_\Delta}{\mathrm{d}t} = \frac{\mathrm{d}V}{\mathrm{d}t}. \end{aligned}$$

Making the substitution, we obtain a homogeneous differential equation, which we can solve using standard techniques to obtain

$$\begin{aligned} \frac{\mathrm{d}V_\Delta}{\mathrm{d}t} &= -\frac{1}{RC_{eq}} V_\Delta(t) \\ \frac{1}{V_\Delta(t)}\mathrm{d}V &= -\frac{1}{RC_{eq}}\,\mathrm{d}t \\ \implies \quad \ln V_\Delta(t) - \ln V_\Delta(0) &= -\frac{t}{RC_{eq}} \\ \implies \quad V_\Delta(t) &= V_\Delta(0)e^{-t/(RC_{eq}} \\ &= V_\Delta(0)e^{-t/\tau} \end{aligned}$$

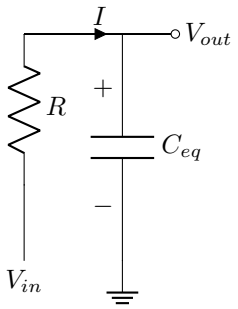
Since the input to the inverter was initially at logical 1 for $t < 0$, the output started at logical 0, so we have that $V(0) = 0$. Thus, $V_\Delta(0) = -V_{dd}$. Substituting into our solution for the differential equation, we obtain

$$\begin{aligned} & V_\Delta(t) = V_\Delta(0)e^{-t/\tau} \\ \implies \quad & V(t) - V_{dd} = -V_{dd}e^{-t/\tau} \\ \implies \quad & V(t) = V_{dd}(1 - e^{-t/\tau}). \end{aligned}$$

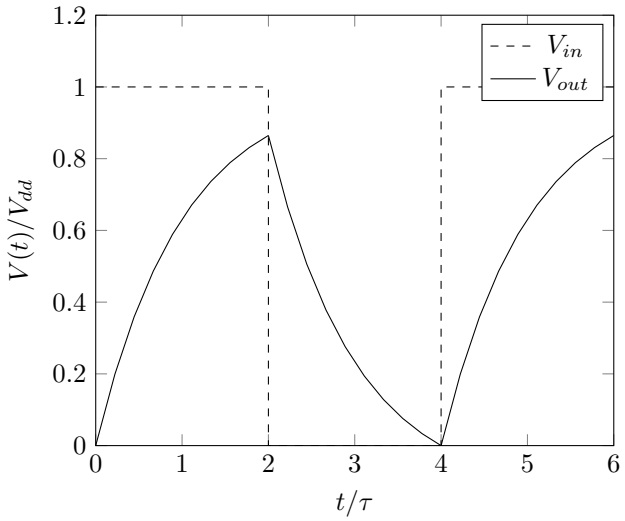
Thus, we observe similar behavior to before, with $V(t)$ starting at 0 and approaching V_{dd} in the limit, but never quite reaching it.

3 Propagation Delay

Let's now look at a simpler circuit, with a resistor and capacitor in parallel, like so:



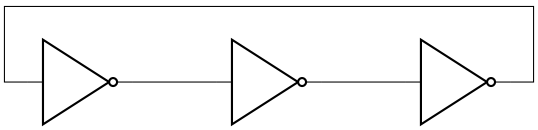
This circuit is fairly similar to the ones that we have previously looked at, except that there is no switch between the input voltage and the resistor. Now, we will set V_{in} to a square wave, and observe the voltage V_{out}. Using techniques very similar to what we have previously used, we obtain a graph that looks like this:



Intuitively, we can see that the capacitor causes V_{out} to "lag" behind V_{in}.

This lag is one factor that limits the performance of more complex circuits. We wish to minimize the time constant τ, in order to run our circuits at as high a frequency as possible. Recall that $\tau = RC$. We know that the capacitance of a capacitor is proportional to its area and inversely proportional to the distance between its plates. Thus, halving all dimensions of a capacitor will halve its capacitance, so by making transistors smaller, we can reduce their capacitance quite substantially. Although reducing the size of a resistor does not reduce its resistance, improvements in materials can again reduce the resistance of transistors quite substantially.

However, this lag can also be beneficial, in creating timing circuits. Consider a circuit consisting of three inverters placed in series in a loop, as shown:



Imagine a logical 0 input to the first inverter. This will feed a logical 1 into the second inverter, a logical 0 to the third, and finally a logical 1 back to the first inverter. Thus, the voltage at the input to the first inverter (and at all other nodes in this circuit) will flip back and forth at a period based on the time constants of each of the inverters.

4 Power Consumption

The natural question to ask is: how fast can we make digital circuits, with today's technology? As it turns out, the limiting factor to circuit performance

is not the time constant, but rather issues of heat dissipation. One circuit we can look at is a similar oscillating circuit consisting of 11 such transistors with capacitances of 10 fF, running at a frequency of 10 GHz at a voltage of 1 V. Clearly, each capacitor in each transistor will repeatedly be charged and discharged. When charged, each capacitor will store the energy

$$\frac{1}{2}QV = \frac{C}{2}V^2 \approx 5\,\text{fJ}.$$

It can also be easily calculated, using the techniques described above, that the energy lost to the resistor when charging the capacitor also equals $\frac{C}{2}V^2 \approx 5\,\text{pJ}$. Thus, the net energy dissipated per cycle per transistor is

$$\Delta E = CV^2 \approx 10\,\text{fJ}.$$

Multiplying by the number of transistors (22) and the number of cycles per second (10 billion), we obtain a net power output of

$$22 \cdot 10\,\text{GHz} \cdot 10\,\text{fJ} = 2.2\,\text{mW},$$

with each transistor generating power of 100 µW.

This is not very much. However, we must remember that the important measure to take into consideration is not the heat generated, but the heat generated per unit area. In order to achieve these frequencies, each transistor has an area of just $2\,\mu\text{m}^2$, so the power density is

$$\frac{P}{A} = \frac{100\,\mu\text{W}}{2\,\mu\text{m}^2} = 50\,\text{Wmm}^{-2}.$$

This seems to be a much more impressive quantity. For comparison, the surface of the sun only has a heat flux of about $25\,\text{Wmm}^{-2}$!

This effect is a key factor in the cessation of Moore's law - while we continue to make increasingly smaller transistors, we become unable to cool their processors. So while we can make a 10 GHz processor quite easily, we can't cool it!