# CPE 221 Classwork 13: Machine Code in ARM

Student Name (as in Canvas): _____

A Number: _____

Points: 20

## 1 Encode STRB (10 Points)

```
STRB R10, [R6, #40]!
```

**Solution**

0x E5E6A028

**Explanation**

Pre-indexed Word Load:

- Load word into R10, L = 0, B = 1 (Byte)
- Base register R6
- Immediate offset of 40, which is positive, U = 1
- Pre-indexed (update base register) P = 1 W = 1, P

| 31:28 | 27:26 | 25 | 24 | 23 | 22 | 21 | 20 | 19:16 | 15:12 | 11:0 |
|---|---|---|---|---|---|---|---|---|---|---|
| cond | op | $\bar{I}$ | P | U | B | W | L | Rn | Rd | Src2 |
| 1110 | 01 | 0 | 1 | 1 | 1 | 1 | 0 | 0110 | 1010 | 0000 0010 1000 |

## 2 Encode POP Instruction (5 Points)

Encode the assembly instruction `POP {R3, R8, R0}` into machine code.

**Solution**

0x E8BD0109

**Explanation**

Equivalent to
`LDMFD SP! {R3, R8, R0}`

| 31:28 | 27:26 | 25 | 24 | 23 | 22 | 21 | 20 | 19:16 | 15:0 |
|---|---|---|---|---|---|---|---|---|---|
| cond | op | I | P | U | S | W | L | Rn | register list |
| 1110 | 10 | 0 | 0 | 1 | 0 | 1 | 1 | 1101 | 000000010000 1001 |

P = 0 Post-indexing mode, U = 1 for increment, W = 1 write back, updates SP after loading,
L = 1 for LDM (Load operation)
S = 0 by default.
Rn is the base register which is SP. Register list uses bit masking.

## 3 Encode LDR Instruction (5 Points)

Encode the assembly instruction `LDR R9, [R5, #-32]` into machine code.

**Solution**

`0x E5159020`

**Explanation**

- Load word into R9, L = 1, B = 0 (no Byte)
- Base register R5
- Immediate offset of -32, which is negative, U = 0
- No writeback, W = 0 (no pre-indexing)
- P = 1 (Offset)
- Immediate is there $\bar{I} = 0$

| 31:28 | 27:26 | 25 | 24 | 23 | 22 | 21 | 20 | 19:16 | 15:12 | 11:0 |
|---|---|---|---|---|---|---|---|---|---|---|
| cond | op | $\bar{I}$ | P | U | B | W | L | Rn | Rd | Src2 |
| 1110 | 01 | 0 | 1 | 0 | 0 | 0 | 1 | 0101 | 1001 | 0000 0010 0000 |