Contact

- **E-mail ID:** katiyar_ravins@iitgn.ac.in
- **Website:** Ravins Katiyar
- **LinkedIn:** ravins-katiyar-633585192
- **Phone No.:** +91 7054898917

Top Skills

- Analog Circuits
- Semiconductor Device Physics
- Microfabrication
- Digital VLSI Design

Workshops

- One day **Xilinx Vivado** Workshop at IIT Gandhinagar in February 2020

Languages

- English
- Hindi

Hobbies

- Reading books
- Cricket
- Badminton

Ravins Katiyar

IIT Gandhinagar

Education

2019 - Present, IIT Gandhinagar, Gujarat
M.Tech Electrical Engineering (VLSI and Microelectronics) : **8.6 CGPA**

2014 - 2018, U.I.E.T, C.S.J.M. University Kanpur, Uttar Pradesh
B.Tech Electronics and Communication Engineering : **7.23 CGPA**

2012 - 2013, A.P.V.N.I. College, Ranipur, Kanpur Dehat, Uttar Pradesh
12th (U.P. Board) : **88.4 %**

2010 - 2011, A.P.V.N.H. School, Ranipur, Kanpur Dehat, Uttar Pradesh
10th (U.P. Board) : **71.3 %**

Skills

Tools

- Cadence Virtuoso
- Mentor Graphics Calibre
- Xilinx Vivado
- Sentaurus TCAD

Hardware Description and Verification Languages

- Verilog

Programming/Scripting Languages

- Pcell
- Ocean
- Python
- MATLAB

M.Tech Thesis

Process integration of double poly BJT for RF applications (Prof. Nihar R. Mohapatra)

- Developing a novel silicon based BICMOS process for Bipolar Junction Transistor having very few additional simple process steps along with CMOS fabrication
- Working on modification in doping profile and geometry of transistor to get better F_t, F_{max}, V_A and $V_{breakdown}$ compared to the state-of-the-art of Si-based BJT, which are important figure merits of transistor for RF applications

Calibration of electrical parameter of single poly BJT

- Done calibration of electrical parameter for silicon and poly-silicon of single poly BJT from the measured data of fabricated devices, using those parameters in electrical characterization of double poly BJT

Device layouts of single poly BJT

- Done layouts of Single poly BJT including DC and RF pads and some test structures of C-B, E-B diode to measure the junction capacitance

Course Projects

Current Mirror based Band-gap Reference Circuit Design (Prof. Nihar R. Mohapatra)

- A first order Current Mirror based BGR was designed using 0.18um CMOS technology with a supply voltage of 1.8V to achieve a precise output voltage reference of 1.12V at 27°C room temperature and achieve 0.2ppm/°C of low temperature coefficient with temperature range of -40°C to 125°C.

High Impedance Current Mirror Design (Prof. Nihar R. Mohapatra)

- Designed a circuit that offered a very high impedance due to the presence of the PMOS at both legs since no auxiliary biasing circuit was used. It can be used for applications which operate with very low current.

Single stage Folded-cascode Opamp design with the single ended output (Prof. Nihar R. Mohapatra)

- Designed a single ended folded cascode opamp with V_{DD} = 1.8V, Gain = 92dB, CMRR = 100dB, ICMR = 0.2-0.4V, Voltage Swing = 0.5V, PSRR+ = 80dB, PSRR- = 80dB, Power = 20uW, and GBW = 1MHz. Design was carried out in **SCL 180nm** Technology Node.

Gm-Cc Low Pass Filter Design (Prof. Nihar R. Mohapatra)

- Designed a Gm-Cc Low Pass Filter using folded-cascode opamp with Gain = 0.8-1V/V, F_{3dB} = 1KHz, Power Budget = 100uW, V_{DD} = 1.8V, ICMR = 0.2V- 0.4V. Design was carried out in **SCL 180nm** Technology Node.

Level Shifter Design (Prof. Nihar R. Mohapatra)

- Designed a Level shifter for a multi-supply application. The design converted minimum of 0.1V input signal into 1V output signal. The level shifter had a propagation delay of 10.99ns and power dissipation of 1.52nW. The operating condition was V_{DDL} = 0.2V, V_{DDH} = 1V.

Positions of Responsibility

- Teaching assistant in **Analog Circuit Lab** for undergraduate students at IIT Gandhinagar

Academic Experiences

- Have 2 month academic experience in **wafer characterisation**, done electrical measurement of several STI and Non STI based LDMOS devices
- Have some experience in **device layouts**, developed test structures for single poly BJT devices