Contact

- **LinkedIn:** rk-pothal
- **Phone No.:** +91 9853006156

Top Skills

- Analog Circuit Design
- Analog Layout Design
- Design Verification

Workshops

- Attended **Processor Design** Workshop at IIT-GN
- Participated in a seminar about **Highly-efficient, affordable PMICs in HV 0.35um CMOS technology** at IIT-GN

Languages

- English
- Hindi
- Odia (Native)

Hobbies

- Tinkering
- Cricket
- Badminton
- Cooking

Rakesh Kumar Pothal

IIT Gandhinagar
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Education

2018 - Present, IIT Gandhinagar, Gujarat
M.Tech Electrical Engineering (VLSI and Microelectronics) : 7.19 CGPA

2011 - 2014, IGIT, Sarang, Odisha
B.Tech (BPUT, Odisha) Electronics and Telecommunication Engineering : 7.99 CGPA

2008 - 2011, BOSE, Cuttack, Odisha
Diploma (SCTEVT) : 80.1 percentage

2008 Bhuban High School, Bhuban, Dhenkanal, Odisha
10th (BSE, Odisha) : 81.2 percentage

Experience

June 2015- January 2017, Part Time Guest Faculty in Orissa Institute of Engineering and Technology, Dhenkanal

- **Company Profile**: Academic Institution
- **Role**: Guest Faculty and Lab Instructor
- **Work profile**: Lecturer in Analog Electronics, Network Theory, Signals and Systems, and Instructor in Analog Lab

Skills

Tools

- Cadence Virtuoso
- Cadence Liberate
- Calibre
- QuestaSim
- Design Compiler
- Innovus
- Xilinx Vivado
- Sentaurus TCAD
- MATLAB Simulink

Programming/Scripting Languages

- Verilog
- VHDL
- SystemVerilog
- SKILL
- C++

M.Tech Thesis

On-chip Power Management IC (from schematic to layout) (Prof. Nihar R Mohapatra)

- Designing a full on-chip **Low-Drop Out (LDO) Regulator** for bio-medical applications
- Designing **Switching DC-DC Converter and Control Techniques** (Buck-Boost Converter) for ASICs
- Extending work to **Advanced Topics in PMIC** (Digitally controlled LDO, Single-Inductor Multiple-Output (SIMO) Converter)

Major Projects

Single and Double stage Op-Amps (schematic to layout)
(Prof. Nihar R Mohapatra)

- Designed and implemented low-power and high speed Op-Amps in 180nm technology using Cadence Virtuoso adhering to the specified design constraint parameters like **gain, bandwidth, voltage swing** etc.

Bandgap Reference Circuit (schematic to layout)
(Prof. Nihar R Mohapatra)

- Implemented Op-Amp based β **- multiplier BGR** Circuit in 180nm technology node using Cadence Virtuoso

Study and implementation of Robust Clock Networks
(Prof. Joycee Mekie)

- Simulated both **un-buffered and buffered robust clock networks** in sub-threshold and threshold regimes in Cadence Virtuoso UMC 65nm technology node

Industrial Automation
(Prof. Uttama Lahiri)

- Implemented multi-sensor based hardware of Industrial Automation using **Arduino Uno** and various sensors like **Ultrasonic, IR, Moisture, Temperature Sensor** and **LDR**

Verilog and VHDL Projects

FIFO
(Prof. Joycee Mekie)

- Implemented the 32 bit synthesizable **synchronous FIFO** with a depth of 16 with read and write control

Noise Cancelling FIR Filter
(Prof. Nithin V George)

- Designed a noise cancelling direct and transpose form FIR Filter using **LMS Algorithm** in VHDL in Xilinx Vivado

Positions of Responsibility

- Engaged in teaching tools such as **Cadence Virtuoso and Xilinx Vivado** to juniors at IIT Gandhinagar
- Teaching Assistant for **Analog and Digital course**, IIT Gandhinagar

Achievements

- Awarded runner-up position in under-16 cricket Vinoo Mankad Trophy against 16 teams
- Topped the school in class 10 among 82 batchmates