

# Experiments with Performance Portability\*

1<sup>st</sup> Rahul Kumar Gayatri

NERSC

Lawrence Berkeley National Lab

Berkeley, USA

rgayatri@lbl.gov

2<sup>nd</sup> Jack Deslippe

NERSC

Lawrence Berkeley National Lab

Berkeley, USA

jdeslippe@lbl.gov

**Abstract**—With the race to reach the exascale flop count at its peak, most of the big machines are now comprised of thousands of nodes, where each node is some combination of a multi-core CPU and one or more accelerators. While this presents a great opportunity from the hardware perspective, it leads to a situation where the software, i.e., the applications that try to maximize their performance on such architectures become more complicated than necessary. The reason for this is that the application programmer now has to write implementations for CPU and accelerator parts of the code. To address this issue, multiple programming models have evolved in the last few years which abstract the implementation details specific to the hardware while presenting a uniform view of the code. The goal of such programming models is to provide a simple interface, either directive-based or library-based, which can be used to distribute parts of the code among the available threads or offload kernels onto accelerators. In this paper we discuss few of the widely used on-node programming models that aim to alleviate the programmers burden by providing a clean and user friendly interface to parallelize their code. We look at the effort required in learning and using these programming models and their performance relative to the optimal native architecture dependent implementations. We also discuss how portable the programming models are with respect to executing a particular code on an architecture different than the one it was developed on. This paper, however, does not participate in the debate on the definition of “Performance Portability”, but rather focuses on the effort needed to write applications using different programming models. We present results from a couple of material science kernels and their various implementations. We focus on the following programming models: OpenMP{3.5, 4.5}, OpenACC, Kokkos, Raja, Cuda. We ran our benchmarks on Intel’s Xeon and XeonPhi, IBM’s Power8 and Power9 and Nvidia’s Pascal and Volta GPUs.

**Index Terms**—Performance Portability, Parallel Programming Models, multi-core CPUs, accelerators, exascale.

## I. INTRODUCTION

This document is a model and instructions for L<sup>A</sup>T<sub>E</sub>X. Please observe the conference page limits.

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TABLE I  
TABLE TYPE STYLES

Table Head	Table Column Head		
	<i>Table column subhead</i>	<i>Subhead</i>	<i>Subhead</i>
copy	More table copy <sup>a</sup>		

<sup>a</sup>Sample of a Table footnote.

Fig. 1. Example of a figure caption.

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#### ACKNOWLEDGMENT

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