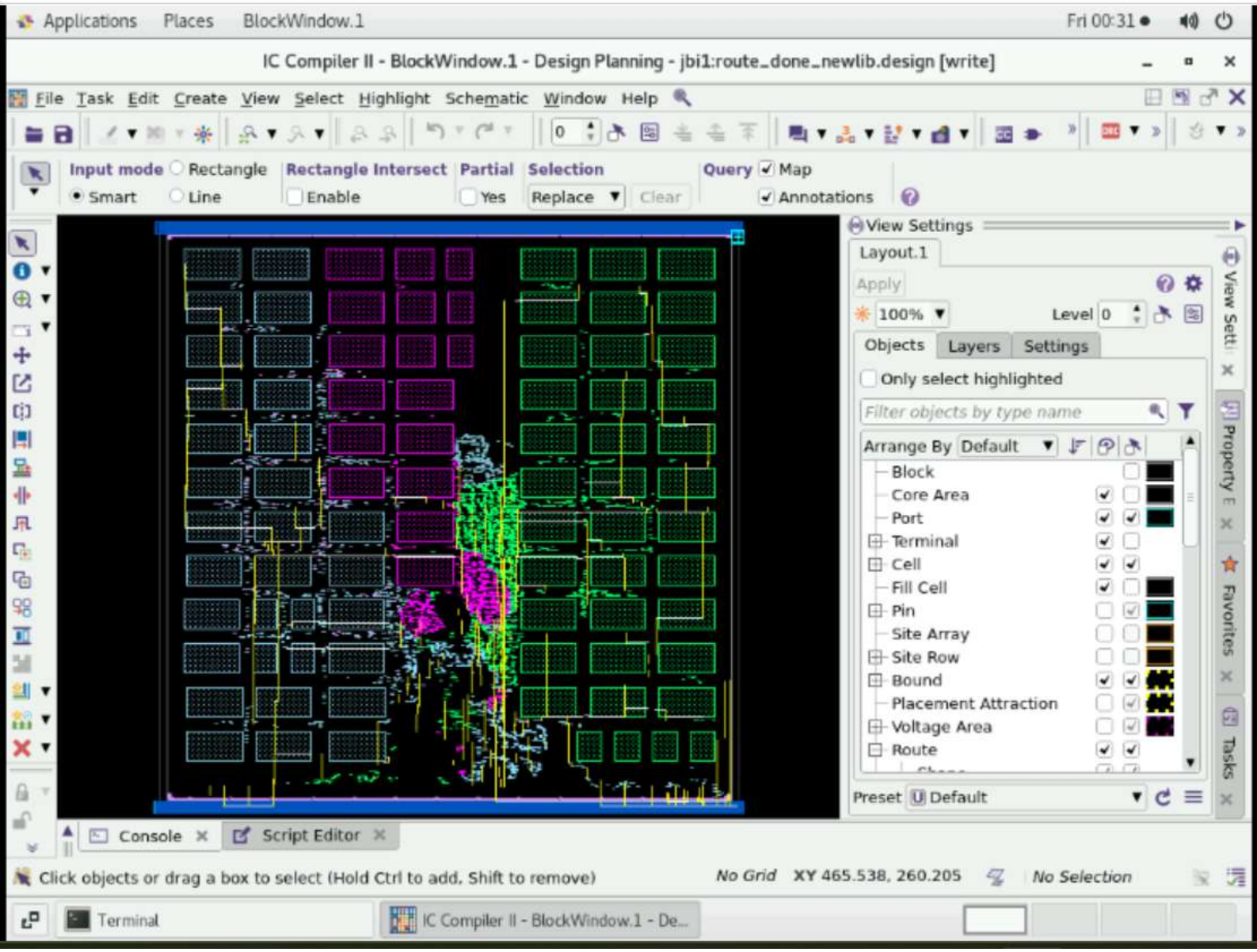
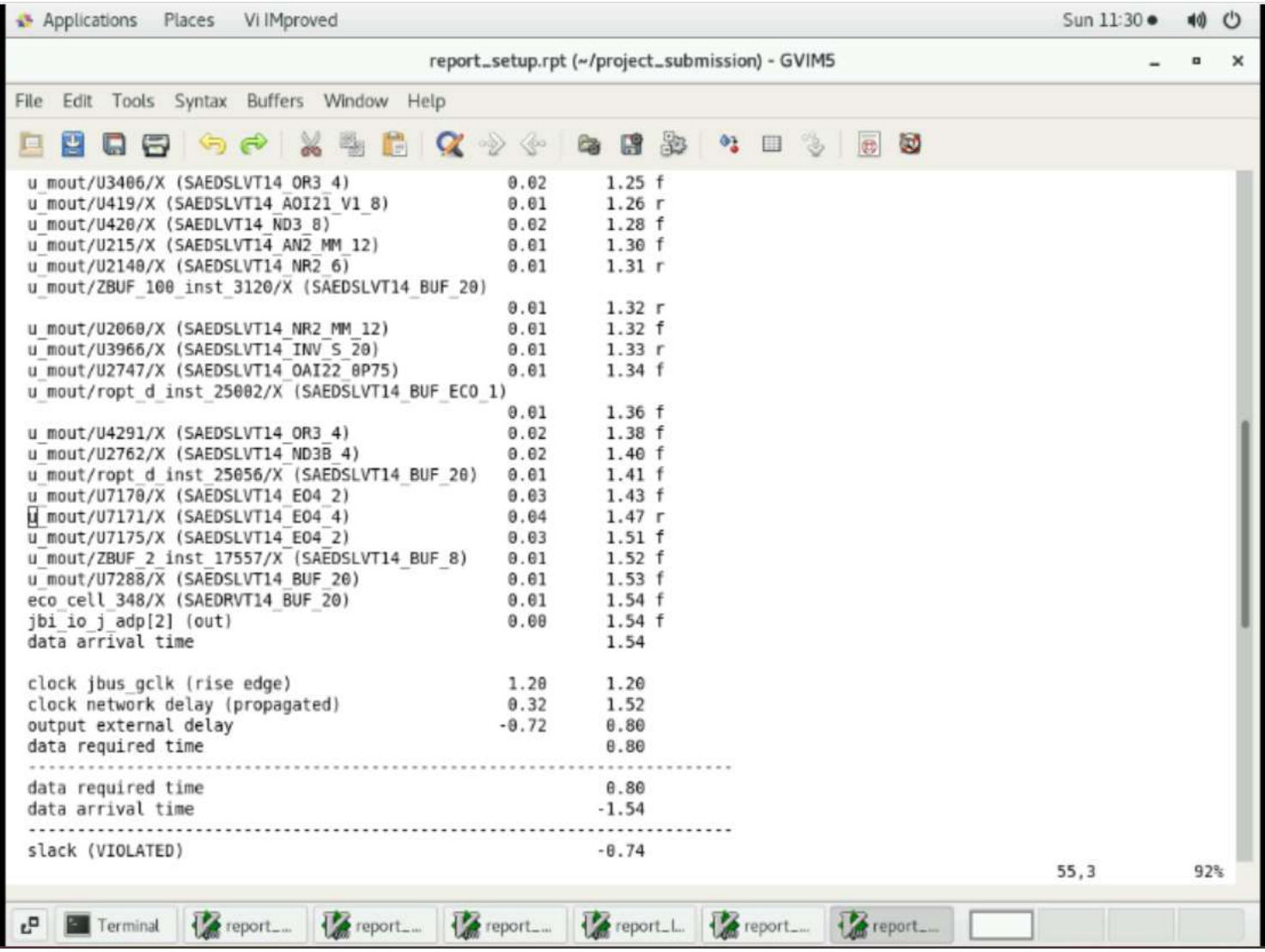
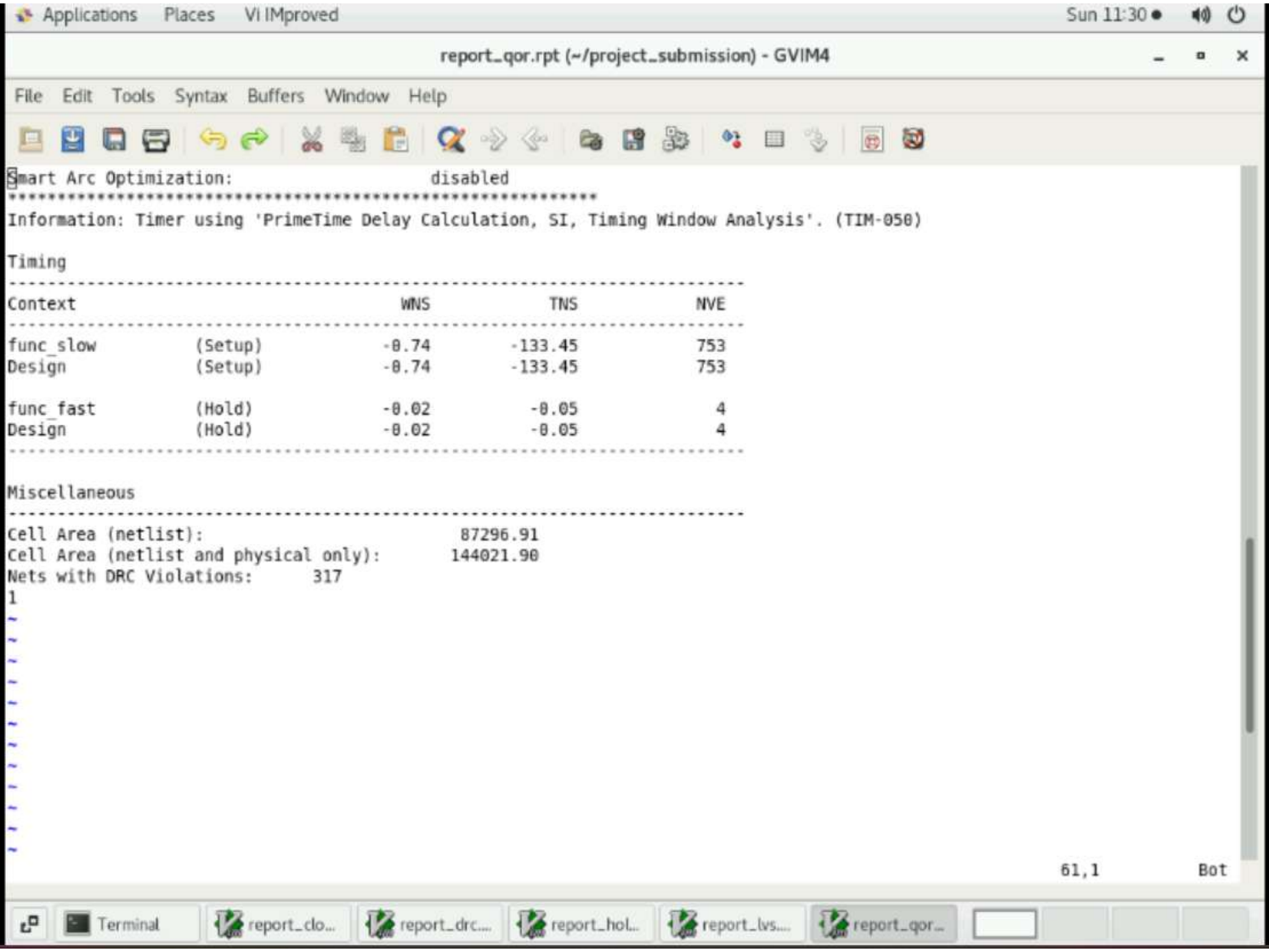
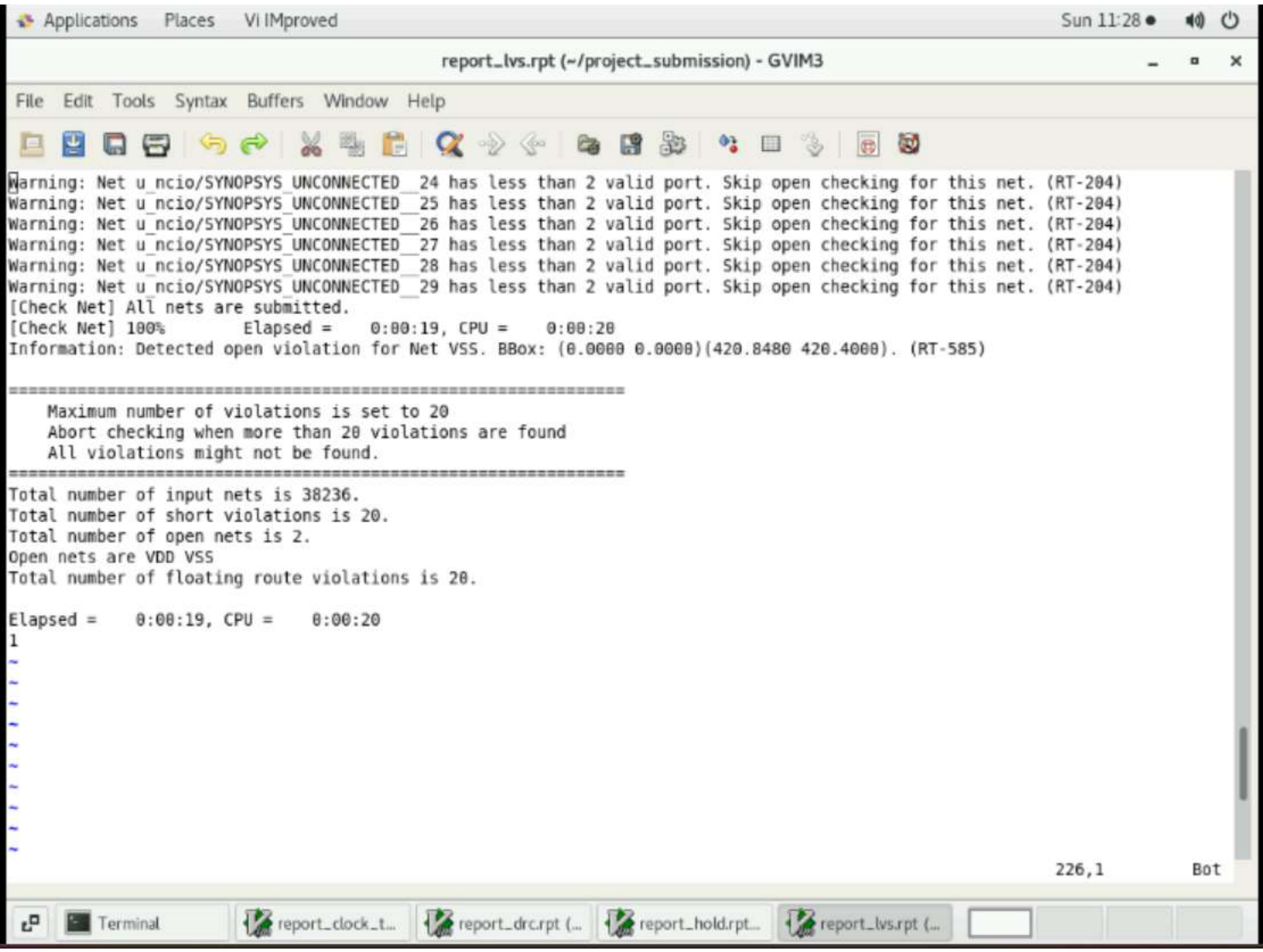
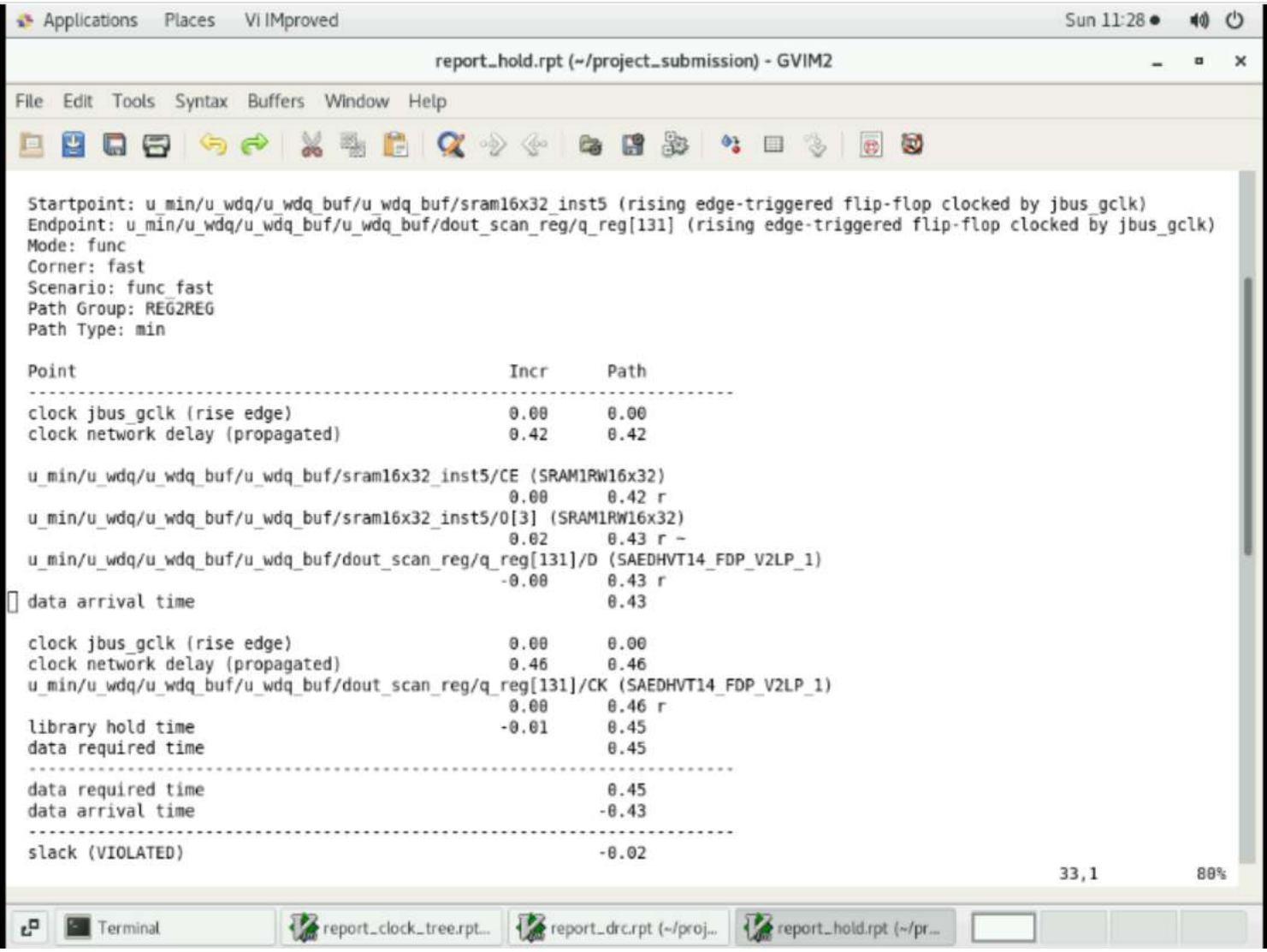
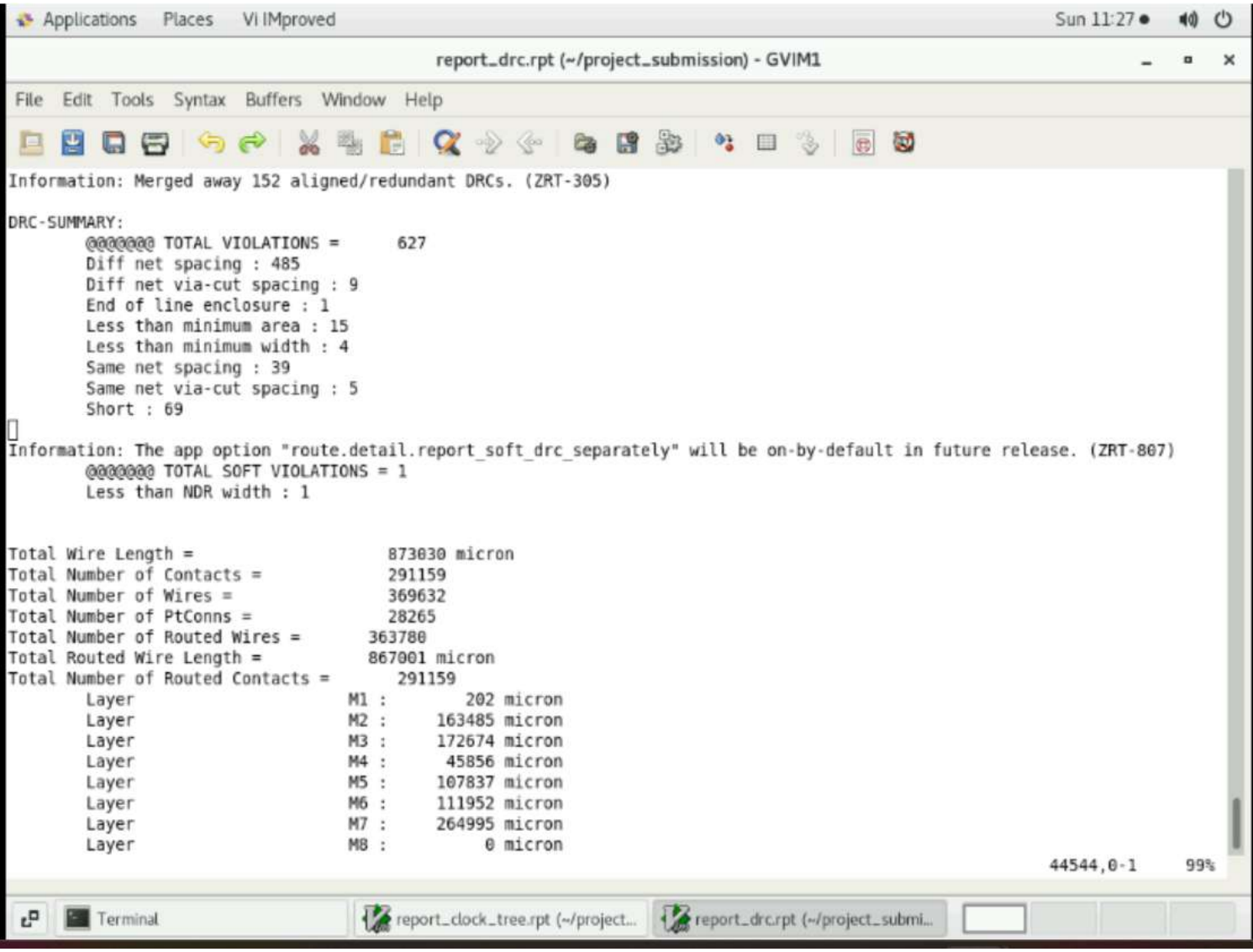

Applications
Places
BlockWindow.1
Fri 00:31
IC Compiler II - BlockWindow.1 - Design Planning - jbi1:route_done_newlib.design [write]
File Task Edit Create View Select Highlight Schematic Window Help
Input mode
Smart
Rectangle
Line
Rectangle Intersect
Enable
Partial
Yes
Selection
Replace
Clear
Query
Map
Annotations
View Settings
Layout.1
Apply
100%
Level
Objects
Layers
Settings
Only select highlighted
Filter objects by type name
Arrange By
Default
Block
Core Area
Port
Terminal
Cell
Fill Cell
Pin
Site Array
Site Row
Bound
Placement Attraction
Voltage Area
Route
Preset
Default
Console
Script Editor
Click objects or drag a box to select (Hold Ctrl to add, Shift to remove)
No Grid
XY 465.538, 260.205
No Selection
Terminal
IC Compiler II - BlockWindow.1 - De...

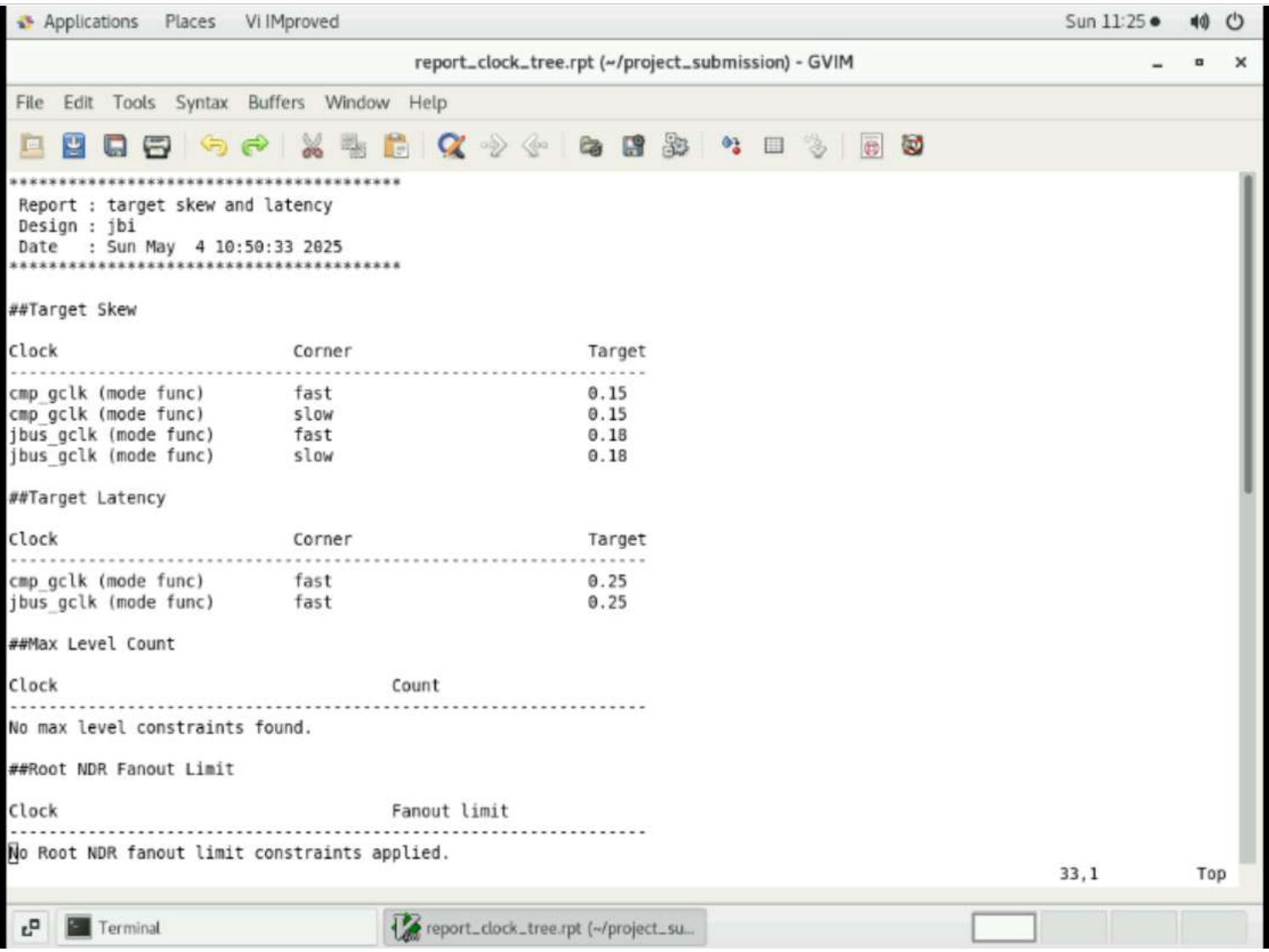

Applications Places Vi IMproved
Sun 11:30
report_setup.rpt (~/project_submission) - GVIM5
File Edit Tools Syntax Buffers Window Help
u_mout/U3406/X (SAEDSLVT14_OR3_4) 0.02 1.25 f
u_mout/U419/X (SAEDSLVT14_AOI21_V1_8) 0.01 1.26 r
u_mout/U420/X (SAEDLVT14_ND3_8) 0.02 1.28 f
u_mout/U215/X (SAEDSLVT14_AN2_MM_12) 0.01 1.30 f
u_mout/U2140/X (SAEDSLVT14_NR2_6) 0.01 1.31 r
u_mout/ZBUF_100_inst_3120/X (SAEDSLVT14_BUF_20)
0.01 1.32 r
u_mout/U2060/X (SAEDSLVT14_NR2_MM_12) 0.01 1.32 f
u_mout/U3966/X (SAEDSLVT14_INV_S_20) 0.01 1.33 r
u_mout/U2747/X (SAEDSLVT14_OAI22_0P75) 0.01 1.34 f
u_mout/ropt_d_inst_25002/X (SAEDSLVT14_BUF_ECO_1)
0.01 1.36 f
u_mout/U4291/X (SAEDSLVT14_OR3_4) 0.02 1.38 f
u_mout/U2762/X (SAEDSLVT14_ND3B_4) 0.02 1.40 f
u_mout/ropt_d_inst_25056/X (SAEDSLVT14_BUF_20) 0.01 1.41 f
u_mout/U7170/X (SAEDSLVT14_EO4_2) 0.03 1.43 f
u_mout/U7171/X (SAEDSLVT14_EO4_4) 0.04 1.47 r
u_mout/U7175/X (SAEDSLVT14_EO4_2) 0.03 1.51 f
u_mout/ZBUF_2_inst_17557/X (SAEDSLVT14_BUF_8) 0.01 1.52 f
u_mout/U7288/X (SAEDSLVT14_BUF_20) 0.01 1.53 f
eco_cell_348/X (SAEDRVT14_BUF_20) 0.01 1.54 f
jbi_io_j_adp[2] (out) 0.00 1.54 f
data arrival time 1.54
clock jbus_gclk (rise edge) 1.20 1.20
clock network delay (propagated) 0.32 1.52
output external delay -0.72 0.80
data required time 0.80
data required time 0.80
data arrival time -1.54
slack (VIOLATED) -0.74
55,3 92%
Terminal
report_...
report_...
report_...
report_l...
report_...
report_...


Applications Places Vi IMproved
Sun 11:30
report_qor.rpt (~/project_submission) - GVIM4
File Edit Tools Syntax Buffers Window Help
Smart Arc Optimization: disabled
Information: Timer using 'PrimeTime Delay Calculation, SI, Timing Window Analysis'. (TIM-050)
Timing
Context WNS TNS NVE
func_slow (Setup) -0.74 -133.45 753
Design (Setup) -0.74 -133.45 753
func_fast (Hold) -0.02 -0.05 4
Design (Hold) -0.02 -0.05 4
Miscellaneous
Cell Area (netlist): 87296.91
Cell Area (netlist and physical only): 144021.90
Nets with DRC Violations: 317
1
61,1 Bot
Terminal
report_clo...
report_drc...
report_hol...
report_lvs...
report_qor...


Applications Places Vi IMproved
Sun 11:28
report_lvs.rpt (~/project_submission) - GVIM3
File Edit Tools Syntax Buffers Window Help
Warning: Net u_ncio/SYNOPSYS_UNCONNECTED__24 has less than 2 valid port. Skip open checking for this net. (RT-204)
Warning: Net u_ncio/SYNOPSYS_UNCONNECTED__25 has less than 2 valid port. Skip open checking for this net. (RT-204)
Warning: Net u_ncio/SYNOPSYS_UNCONNECTED__26 has less than 2 valid port. Skip open checking for this net. (RT-204)
Warning: Net u_ncio/SYNOPSYS_UNCONNECTED__27 has less than 2 valid port. Skip open checking for this net. (RT-204)
Warning: Net u_ncio/SYNOPSYS_UNCONNECTED__28 has less than 2 valid port. Skip open checking for this net. (RT-204)
Warning: Net u_ncio/SYNOPSYS_UNCONNECTED__29 has less than 2 valid port. Skip open checking for this net. (RT-204)
[Check Net] All nets are submitted.
[Check Net] 100% Elapsed = 0:00:19, CPU = 0:00:20
Information: Detected open violation for Net VSS. BBox: (0.0000 0.0000)(420.8480 420.4000). (RT-585)
Maximum number of violations is set to 20
Abort checking when more than 20 violations are found
All violations might not be found.
Total number of input nets is 38236.
Total number of short violations is 20.
Total number of open nets is 2.
Open nets are VDD VSS
Total number of floating route violations is 20.
Elapsed = 0:00:19, CPU = 0:00:20
1
226,1 Bot
Terminal
report_clock_t...
report_drc.rpt (...
report_hold.rpt...
report_lvs.rpt (...


Applications Places Vi IMproved
Sun 11:28
report_hold.rpt (~/project_submission) - GVIM2
File Edit Tools Syntax Buffers Window Help
Startpoint: u_min/u_wdq/u_wdq_buf/u_wdq_buf/sram16x32_inst5 (rising edge-triggered flip-flop clocked by jbus_gclk)
Endpoint: u_min/u_wdq/u_wdq_buf/u_wdq_buf/dout_scan_reg/q_reg[131] (rising edge-triggered flip-flop clocked by jbus_gclk)
Mode: func
Corner: fast
Scenario: func_fast
Path Group: REG2REG
Path Type: min
Point Incr Path
clock jbus_gclk (rise edge) 0.00 0.00
clock network delay (propagated) 0.42 0.42
u_min/u_wdq/u_wdq_buf/u_wdq_buf/sram16x32_inst5/CE (SRAM1RW16x32)
0.00 0.42 r
u_min/u_wdq/u_wdq_buf/u_wdq_buf/sram16x32_inst5/O[3] (SRAM1RW16x32)
0.02 0.43 r
u_min/u_wdq/u_wdq_buf/u_wdq_buf/dout_scan_reg/q_reg[131]/D (SAEDHVT14_FDP_V2LP_1)
-0.00 0.43 r
data arrival time 0.43
clock jbus_gclk (rise edge) 0.00 0.00
clock network delay (propagated) 0.46 0.46
u_min/u_wdq/u_wdq_buf/u_wdq_buf/dout_scan_reg/q_reg[131]/CK (SAEDHVT14_FDP_V2LP_1)
0.00 0.46 r
library hold time -0.01 0.45
data required time 0.45
data required time 0.45
data arrival time -0.43
slack (VIOLATED) -0.02
33,1 80%
Terminal
report_clock_tree.rpt...
report_drc.rpt (~/proj...
report_hold.rpt (~/pr...


Applications Places Vi IMproved
Sun 11:27
report_drc.rpt (~/project_submission) - GVIM1
File Edit Tools Syntax Buffers Window Help
Information: Merged away 152 aligned/redundant DRCs. (ZRT-305)
DRC-SUMMARY:
@@@@@@@ TOTAL VIOLATIONS = 627
Diff net spacing : 485
Diff net via-cut spacing : 9
End of line enclosure : 1
Less than minimum area : 15
Less than minimum width : 4
Same net spacing : 39
Same net via-cut spacing : 5
Short : 69
Information: The app option "route.detail.report_soft_drc_separately" will be on-by-default in future release. (ZRT-807)
@@@@@@@ TOTAL SOFT VIOLATIONS = 1
Less than NDR width : 1
Total Wire Length = 873030 micron
Total Number of Contacts = 291159
Total Number of Wires = 369632
Total Number of PtConns = 28265
Total Number of Routed Wires = 363780
Total Routed Wire Length = 867001 micron
Total Number of Routed Contacts = 291159
Layer M1 : 202 micron
Layer M2 : 163485 micron
Layer M3 : 172674 micron
Layer M4 : 45856 micron
Layer M5 : 107837 micron
Layer M6 : 111952 micron
Layer M7 : 264995 micron
Layer M8 : 0 micron
44544,0-1 99%
Terminal
report_clock_tree.rpt (~/project...
report_drc.rpt (~/project_submi...


Applications Places Vi IMproved
Sun 11:25
report_clock_tree.rpt (~/project_submission) - GVIM
File Edit Tools Syntax Buffers Window Help
****
Report : target skew and latency
Design : jbi
Date : Sun May 4 10:50:33 2025
****
##Target Skew
Clock Corner Target
cmp_gclk (mode func) fast 0.15
cmp_gclk (mode func) slow 0.15
jbus_gclk (mode func) fast 0.18
jbus_gclk (mode func) slow 0.18
##Target Latency
Clock Corner Target
cmp_gclk (mode func) fast 0.25
jbus_gclk (mode func) fast 0.25
##Max Level Count
Clock Count
No max level constraints found.
##Root NDR Fanout Limit
Clock Fanout limit
No Root NDR fanout limit constraints applied.
33,1 Top
Terminal
report_clock_tree.rpt (~/project_su...