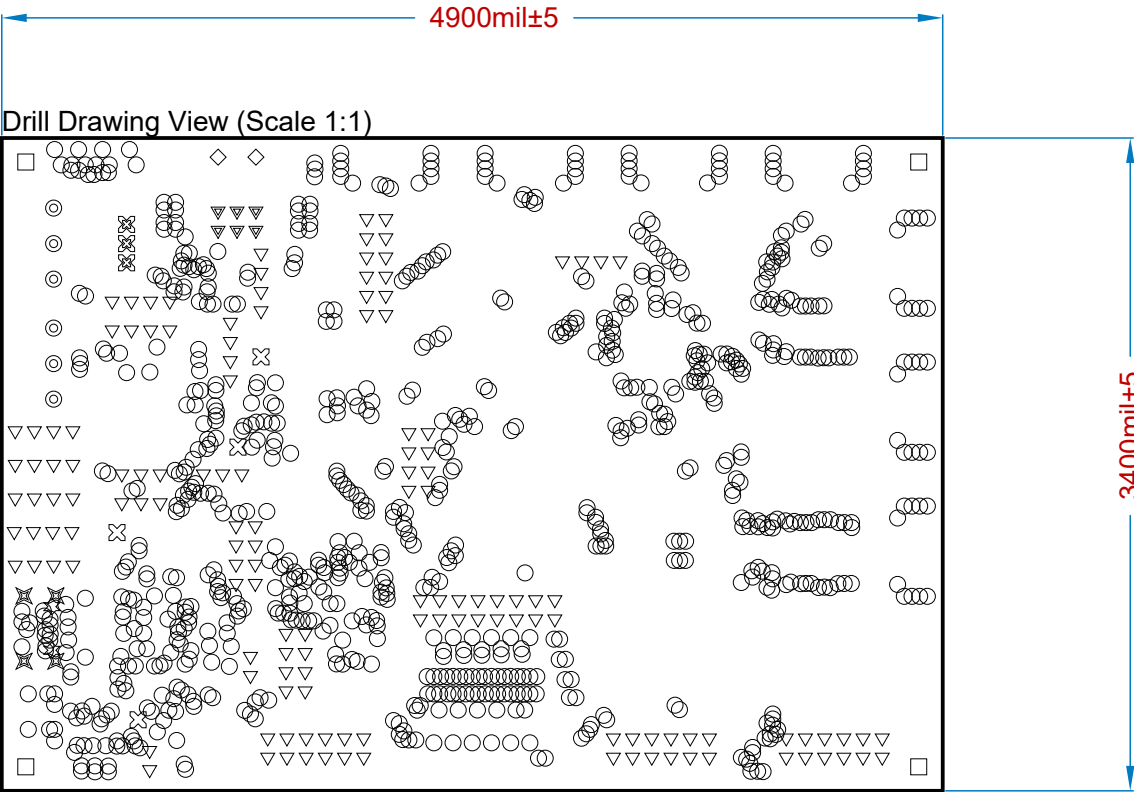


THIS DOCUMENT AND THE DATA DISCLOSED HEREIN OR HEREWITH IS THE PROPERTY OF ALTUM LIMITED AND MAY BE FREELY DISTRIBUTED IN WHOLE. NO RIGHTS ARE RESERVED OR EXPRESS OR IMPLIED WARANTEE GIVEN.

REV STATUS OF SHEETS	REV											REVISIONS				
	SHEET										ZONE	REV	DESCRIPTION	DATE	APPROVED	



- Notes:
- 6 layers.
 - FR370-HR for all layers.
 - ENIG plating.
 - Silkscreen (both sides): white.
 - Soldermask (both sides): green.
 - Electrical testing: connectivity (.ipc file attached).
 - Remove unused pads from internal layers.
 - Fabricate PCB to meet the requirements of IPC-6012 class 2. No Coupon.
 - Customer contacts: Rahul Kumar (rahulkumar@berkeley.edu, 408-702-5845), Felicia Guo (felicia_guo@berkeley.edu, 917-520-6865) & Anita Flynn (aflynn@berkeley.edu, 510-681-3931).
 - Controlled impedance traces are only on the L1_Top layer. All are single-ended 50 ohm +-10%, and are drawn with width 8.501mils. Please adjust as needed.

Drill Table

Symbol	Count	Hole Size	Plated	Hole Tolerance
○	846	8.00mil	Plated	+/-3.00mil
✕	4	21.65mil	Plated	+/-3.00mil
☆	2	25.98mil	Non-Plated	+/-2.00mil
⊗	3	28.00mil	Plated	+/-3.00mil
▽	141	40.00mil	Plated	+/-3.00mil
▼	6	53.00mil	Plated	+/-3.00mil
◎	6	59.00mil	Plated	+/-3.00mil
⊠	4	63.00mil	Plated	+/-3.00mil
◇	2	70.00mil	Non-Plated	+/-2.00mil
□	4	128.74mil	Non-Plated	+/-2.00mil
1018 Total				

THIRD ANGLE PROJECTION

NEXT ASSY

USED ON

APPLICATION

PART NO: STAC-v1

APPROVALS

DATE

ENGINEER: Rahul Kumar

12/20/2023

DESIGNER: Rahul Kumar

12/20/2023

CHECKER: Anita Flynn

12/20/2023

Reference Documents

BOM DOC:

ASSY DOC:

SCH DOC:

PCB DOC:

DESIGN ITEM:

DESIGN ITEM REVISION:

TITLE:

STAC V1 X1 Board

SIZE: B

CAGE CODE:

DWG NO:

REV:

SCALE:

FILE NAME: STAC-v1-pcb.PCBDwf

SHEET: 1 OF 4

Berkeley Wireless Research Center (BWRC)

Doc No: STAC-V1-PCB-001
Rev: 1.0

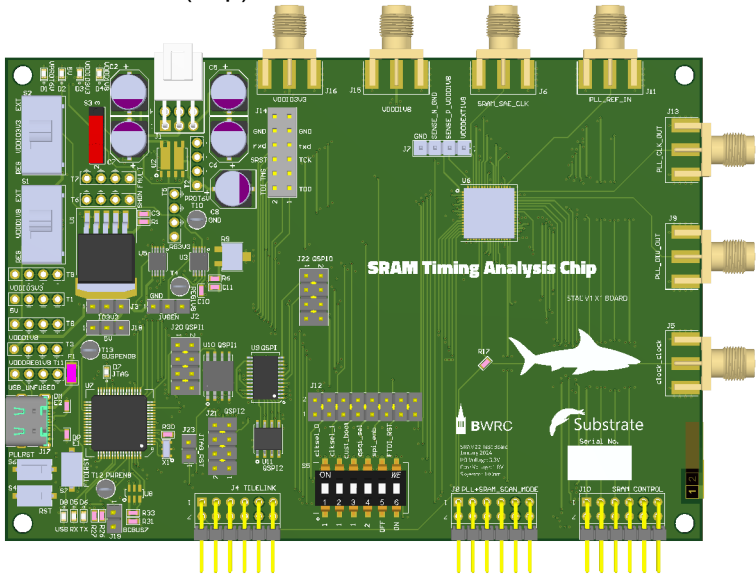
THIS DOCUMENT AND THE DATA DISCLOSED HEREIN OR HEREWITH IS THE PROPERTY OF ALTUM LIMITED AND MAY BE FREELY DISTRIBUTED IN WHOLE. NO RIGHTS ARE RESERVED OR EXPRESS OR IMPLIED WARANTEE GIVEN.

REV STATUS OF SHEETS	REV											REVISIONS				
	SHEET											ZONE	REV	DESCRIPTION	DATE	APPROVED

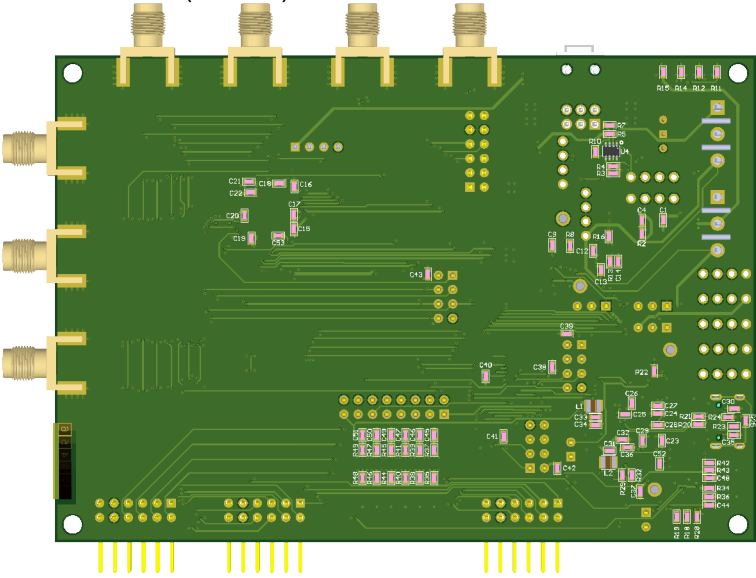
Layer Stack Legend

Material	Layer	Thickness	Dielectric Material	Type	Gerber
	Top Overlay			Legend	GTO
Surface Material	Top Solder	0.50mil	Solder Resist	Solder Mask	GTS
CF-003	L1_TOP	1.38mil		Signal	GTL
Core		5.00mil	FR4-370HR	Dielectric	
CF-003	L2_GND	0.71mil		Signal	G1
Prepreg		10.30mil	FR4-370HR	Dielectric	
CF-003	L3_VDD_SIG	0.71mil		Signal	G2
Core		18.00mil	FR4-370HR	Dielectric	
CF-003	L4_GND	0.71mil		Signal	G3
Prepreg		10.30mil	FR4-370HR	Dielectric	
CF-003	L5_GND	0.71mil		Signal	G4
Core		5.00mil	FR4-370HR	Dielectric	
CF-003	L6_BOT	1.38mil		Signal	GBL
Surface Material	Bottom Solder	0.50mil	Solder Resist	Solder Mask	GBS
	Bottom Overlay			Legend	GBO
Total thickness: 55.18mil					

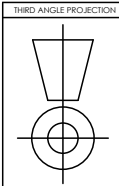
Realistic View (Top)



Realistic View (Bottom)



PART NO: STAC-v1			
APPROVALS		DATE	
ENGINEER: Rahul Kumar		12/20/2023	
DESIGNER: Rahul Kumar		12/20/2023	
CHECKER: Anita Flynn		12/20/2023	
BOM DOC:		Reference Documents	
ASSY DOC:			
SCH DOC:			
PCB DOC:			
DESIGN ITEM:		DESIGN ITEM REVISION:	
TITLE:		STAC V1 X1 Board	
SIZE: B	CAGE CODE:	DWG NO:	REV:
SCALE:	FILE NAME:	STAC-v1-pcb.PCBDwf	
		SHEET:	2 OF 4

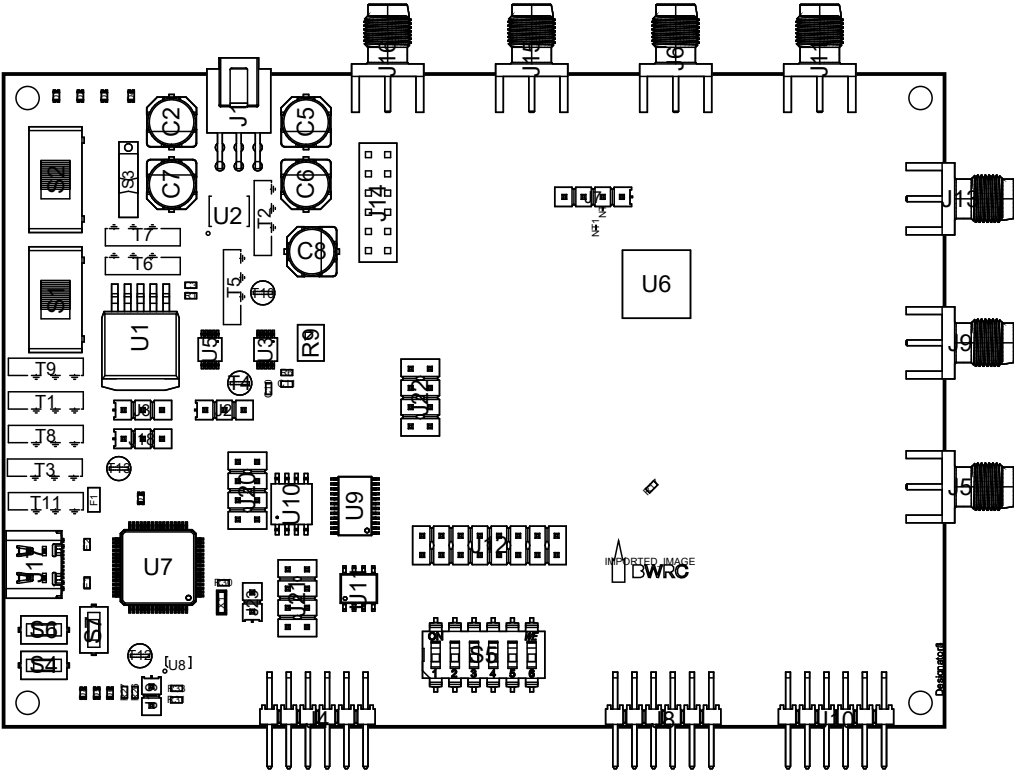


4

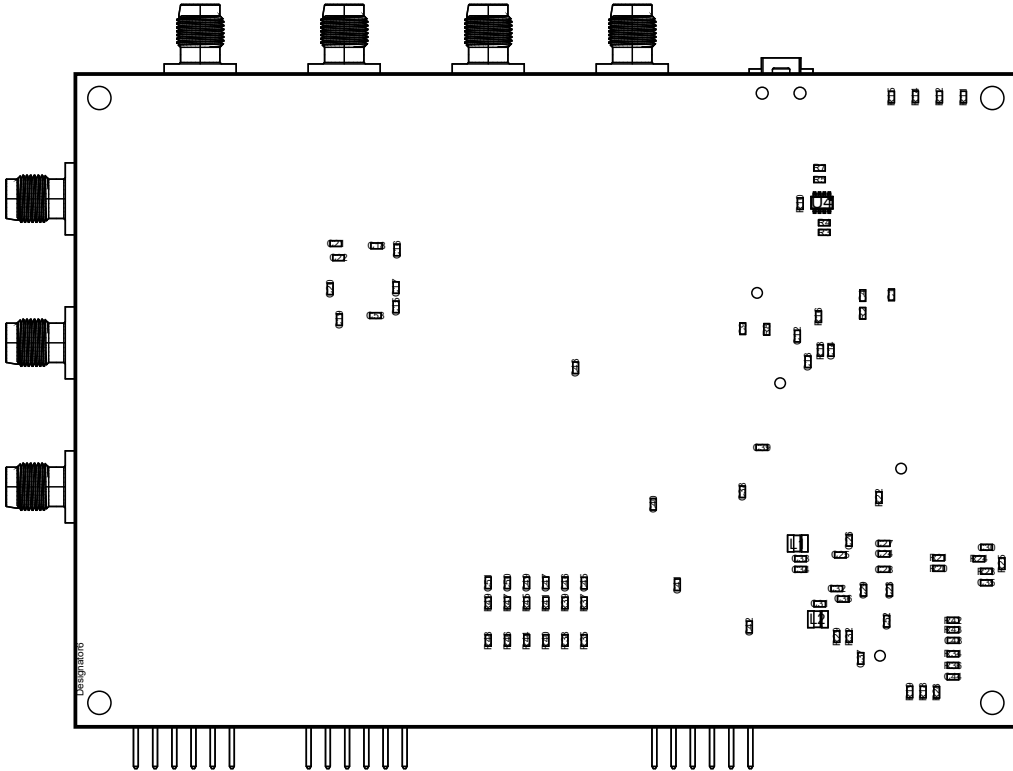
THIS DOCUMENT AND THE DATA DISCLOSED HEREIN OR HEREWITH IS THE PROPERTY OF ALTIUM LIMITED AND MAY BE FREELY DISTRIBUTED IN WHOLE. NO RIGHTS ARE RESERVED OR EXPRESS OR IMPLIED WARANTEE GIVEN.


REV STATUS OF SHEETS	REV										REVISIONS				
	SHEET										ZONE	REV	DESCRIPTION	DATE	APPROVED

View from Top side (Scale 1:1)



View from Bottom side (Scale 1:1)



<div>THIRD ANGLE PROJECTION</div> 		PART NO: STAC-v1		Berkeley Wireless Research Center (BWRC)					
		APPROVALS						DATE	
		ENGINEER:	Rahul Kumar					12/20/2023	
		DESIGNER:	Rahul Kumar					12/20/2023	
		CHECKER:	Anita Flynn					12/20/2023	
		THIRD ANGLE PROJECTION				DESIGN ITEM:		DESIGN ITEM REVISION:	
				Reference Documents		TITLE:			
				BOM DOC:		STAC			
						V1 X1 Board			
				ASSY DOC:		SIZE:	CAGE CODE:		
						B	DWG NO:		
				SCH DOC:			REV:		
				PCB DOC:		SCALE:	FILE NAME:		
NEXT ASSY		USED ON				STAC-v1-pcb.PCBDwf			
APPLICATION						SHEET:	4 OF 4		