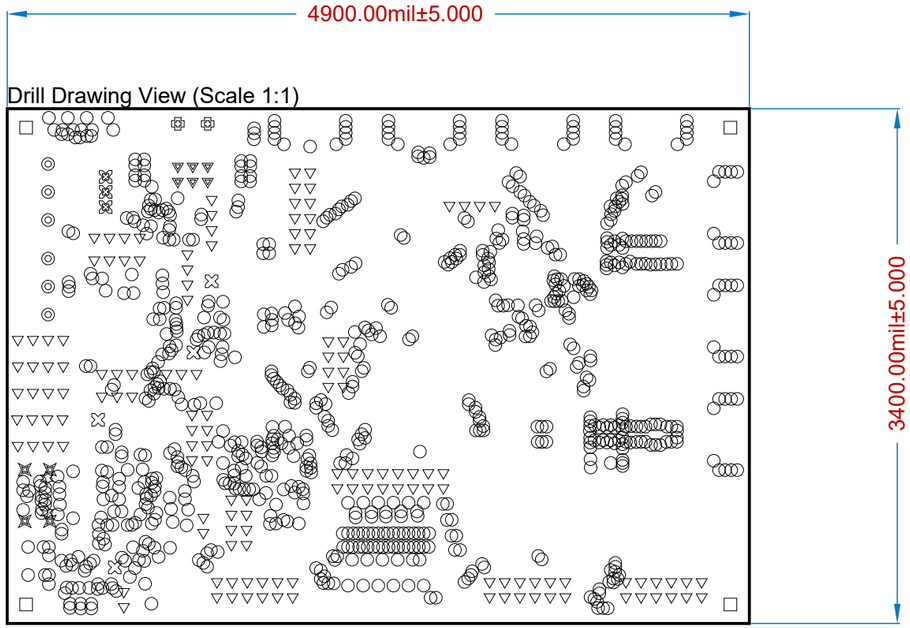
REV STATUS OF SHEETS												
	REV											
	SHEET											

REVISIONS

ZONE	REV	DESCRIPTION	DATE	APPROVED



Drill Drawing View (Scale 1:1)

Drill Table

Symbol	Count	Hole Size	Plated	Hole Tolerance
○	853	0.20mm	Plated	+/-0.08mm
⊠	4	0.55mm	Plated	+/-0.08mm
⛭	2	0.66mm	Non-Plated	
⊠	3	0.71mm	Plated	+/-0.08mm
▽	141	1.02mm	Plated	+/-0.08mm
▽	6	1.35mm	Plated	+/-0.08mm
◎	6	1.50mm	Plated	+/-0.08mm
⊠	4	1.60mm	Plated	+/-0.08mm
⛭	2	1.78mm	Plated	+/-0.05mm
□	4	3.27mm	Non-Plated	+/-0.05mm
	1025 Total			

Notes:

1. 6 layers.
2. FR370-HR for all layers.
3. ENIG plating.
4. Silkscreen (both sides): white
5. Soldermask (both sides): blue
6. Electrical testing: connectivity (.ipc file attached)
7. Remove unused pads from internal layers.
8. Fabricate PCB to meet the requirements of IPC-6012 class 2. No Coupon
9. Customer contacts: Rahul Kumar, rahulkumar@berkeley.edu, (M) (408) 702-5845 & Anita Flynn, aflynn@berkeley.edu, (M) (510) 681-3931
10. Controlled impedance traces are only on the L1_Top layer. All are single-ended 50 ohm +-10%, and are drawn with width 8.501mils. Please adjust as needed.
11. Two mounted cross sections requested.

.lt

DWG NO: =DOC_NO_ASSY_ REV: .lte

PART NO: =PCB_PART_NUMBER

APPROVALS	DATE
ENGINEER: =PCB_ENGINEER	=PCB_ENGINEE
DESIGNER: =PCB_DESIGNER	=PCB_DESIGNE
CHECKER: =PCB_CHECKER	=PCB_CHECKE

Reference Documents

BOM DOC:	=DOC_NO_BOM
ASSY DOC:	=DOC_NO_FAB_DWG
SCH DOC:	=DOC_NO_SCH_DWG
PCB DOC:	=PCB_DWG_NO

THIRD ANGLE PROJECTION

NEXT ASSY	USED ON
APPLICATION	

Altium™

=Address1
=Address2
=Address3
=Address4

DESIGN ITEM: .Item

DESIGN ITEM REVISION: .ItemRevision

TITLE:
STAC
V1 X1 Board

SIZE:	CAGE CODE:	DWG NO:	REV:
B	=CAGE_CO		

SCALE: | FILE NAME: STAC-v1-pcb.PCBDwf | SHEET: 1 OF 3

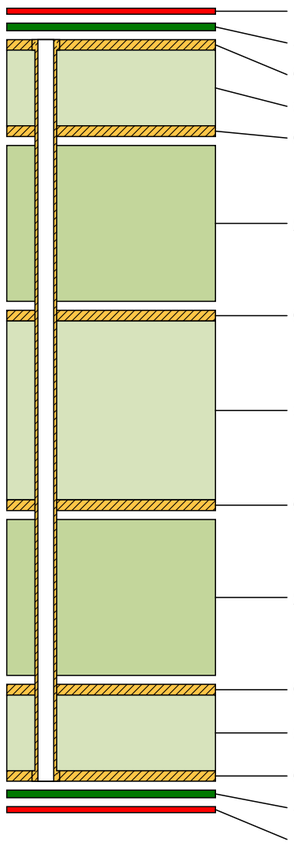
REV STATUS OF SHEETS												
REV												
SHEET												

DWG NO: =DOC_NO_ASSY_DWG REV: .lfe

REVISIONS

ZONE	REV	DESCRIPTION	DATE	APPROVED

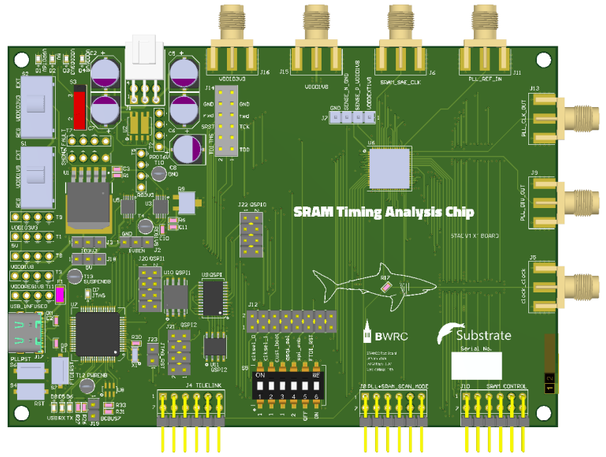
Layer Stack Legend



Material	Layer	Thickness	Dielectric Material	Type	Gerber
	Top Overlay			Legend	GTO
Surface Material	Top Solder	0.01mm	Solder Resist	Solder Mask	GTS
CF-003	**L1_TOP**	**0.02mm**		**Signal**	**GTL**
Core		*0.13mm*	*FR4-370HR*	*Dielectric*	
CF-003	**L2_GND**	**0.02mm**		**Signal**	**G1**
Prepreg		*0.26mm*	*FR4-370HR*	*Dielectric*	
CF-003	**L3_VDD_SIG**	**0.02mm**		**Signal**	**G2**
Core		*0.46mm*	*FR4-370HR*	*Dielectric*	
CF-003	**L4_GND**	**0.02mm**		**Signal**	**G3**
Prepreg		*0.26mm*	*FR4-370HR*	*Dielectric*	
CF-003	**L5_GND**	**0.02mm**		**Signal**	**G4**
Core		*0.13mm*	*FR4-370HR*	*Dielectric*	
CF-003	**L6_BOT**	**0.02mm**		**Signal**	**GBL**
Surface Material	Bottom Solder	0.01mm	Solder Resist	Solder Mask	GBS
	Bottom Overlay			Legend	GBO

Total thickness: 1.37mm

Realistic View



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DWG NO: =DOC_NO_ASSY_ REV: .lfe

THIRD ANGLE PROJECTION

NEXT ASSY	USED ON
APPLICATION	

PART NO: =PCB_PART_NUMBER

APPROVALS	DATE
ENGINEER: =PCB_ENGINEER	=PCB_ENGINEE
DESIGNER: =PCB_DESIGNER	=PCB_DESIGNE
CHECKER: =PCB_CHECKER	=PCB_CHECKE

Reference Documents

BOM DOC:	=DOC_NO_BOM
ASSY DOC:	=DOC_NO_FAB_DWG
SCH DOC:	=DOC_NO_SCH_DWG
PCB DOC:	=PCB_DWG_NO

Altium™

=Address1
=Address2
=Address3
=Address4

DESIGN ITEM: .Item | DESIGN ITEM REVISION: .ItemRevision

TITLE: STAC V1 X1 Board

SIZE:	CAGE CODE:	DWG NO:	REV:
B	=CAGE_CO		

SCALE: | FILE NAME: STAC-v1-pcb.PCBDwf | SHEET: 2 OF 3

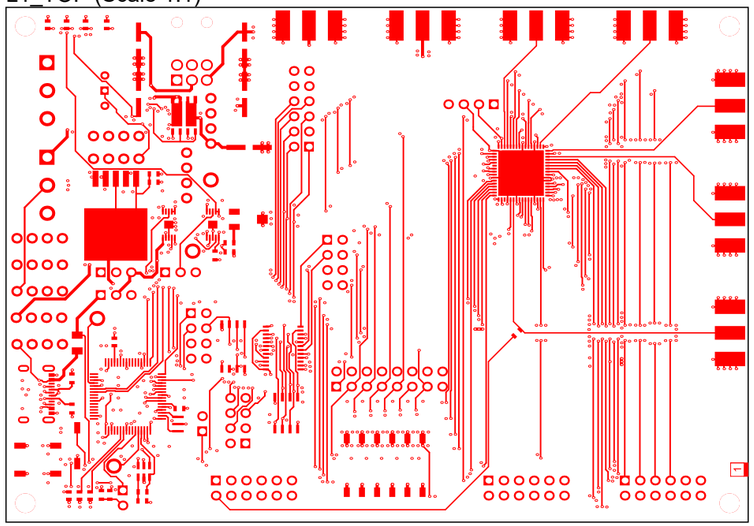
DWG NO: =DOC_NO_ASSY_DWG REV: .Ite

REV STATUS OF SHEETS												
	REV											
	SHEET											

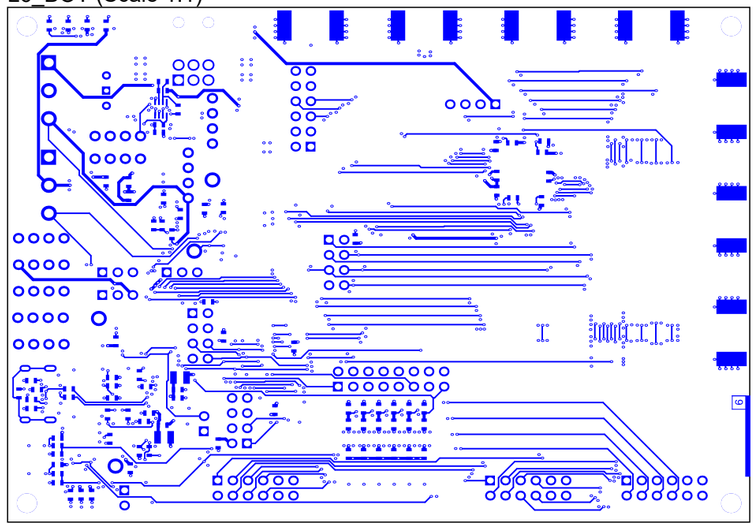
REVISIONS

ZONE	REV	DESCRIPTION	DATE	APPROVED

L1_TOP (Scale 1:1)



L6_BOT (Scale 1:1)



PART NO: =PCB_PART_NUMBER

APPROVALS		DATE
ENGINEER:	=PCB_ENGINEER	=PCB_ENGINEE
DESIGNER:	=PCB_DESIGNER	=PCB_DESIGNE
CHECKER:	=PCB_CHECKER	=PCB_CHECKE

Reference Documents

BOM DOC:	=DOC_NO_BOM
ASSY DOC:	=DOC_NO_FAB_DWG
SCH DOC:	=DOC_NO_SCH_DWG
PCB DOC:	=PCB_DWG_NO

THIRD ANGLE PROJECTION

NEXT ASSY	USED ON
APPLICATION	

Altium™

=Address1
=Address2
=Address3
=Address4

DESIGN ITEM: .Item

DESIGN ITEM REVISION: .ItemRevision

TITLE:
STAC
V1 X1 Board

SIZE:	CAGE CODE:	DWG NO:	REV:
B	=CAGE_CO		

SCALE: | FILE NAME: STAC-v1-pcb.PCBDwf | SHEET: 3 OF 3

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DWG NO: =DOC_NO_ASSY_ REV: .Ite