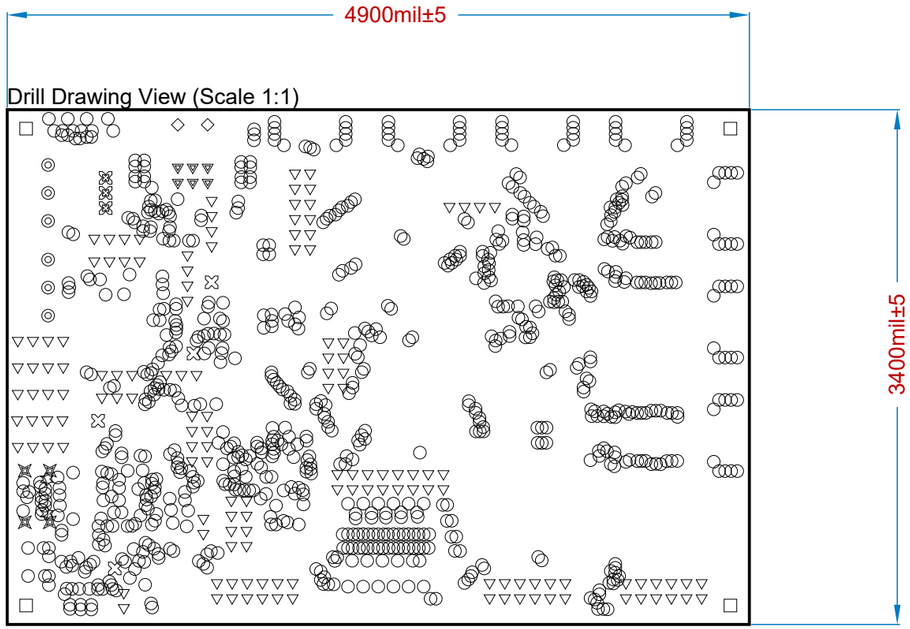
REV STATUS OF SHEETS											
	REV										
	SHEET										

REVISIONS

ZONE	REV	DESCRIPTION	DATE	APPROVED



Drill Drawing View (Scale 1:1)

Drill Table

Symbol	Count	Hole Size	Plated	Hole Tolerance
○	846	8.00mil	Plated	+/-3.00mil
⊠	4	21.65mil	Plated	+/-3.00mil
✡	2	25.98mil	Non-Plated	+/-2.00mil
⊗	3	28.00mil	Plated	+/-3.00mil
▽	141	40.00mil	Plated	+/-3.00mil
▼	6	53.00mil	Plated	+/-3.00mil
◎	6	59.00mil	Plated	+/-3.00mil
⊠	4	63.00mil	Plated	+/-3.00mil
◇	2	70.00mil	Non-Plated	+/-2.00mil
□	4	128.74mil	Non-Plated	+/-2.00mil
	1018 Total			

Notes:

1. 6 layers.
2. FR370-HR for all layers.
3. ENIG plating.
4. Silkscreen (both sides): white.
5. Soldermask (both sides): green.
6. Electrical testing: connectivity (.ipc file attached).
7. Remove unused pads from internal layers.
8. Fabricate PCB to meet the requirements of IPC-6012 class 2. No Coupon.
9. Customer contacts: Rahul Kumar (rahulkumar@berkeley.edu, 408-702-5845), Felicia Guo (felicia_guo@berkeley.edu, 917-520-6865) & Anita Flynn (aflynn@berkeley.edu, 510-681-3931).
10. Controlled impedance traces are only on the L1_Top layer. All are single-ended 50 ohm +-10%, and are drawn with width 8.501mils. Please adjust as needed.

.lte

=DOC_NO_ASSY_ .lte

PART NO: STAC-v1

APPROVALS		DATE
ENGINEER:	Rahul Kumar	12/20/2023
DESIGNER:	Rahul Kumar	12/20/2023
CHECKER:	Anita Flynn	12/20/2023

Reference Documents

BOM DOC:

ASSY DOC:

SCH DOC:

PCB DOC:

NEXT ASSY | USED ON

APPLICATION

THIRD ANGLE PROJECTION

Berkeley Wireless Research Center (BWRC)

DESIGN ITEM: | DESIGN ITEM REVISION:

TITLE:
STAC
V1 X1 Board

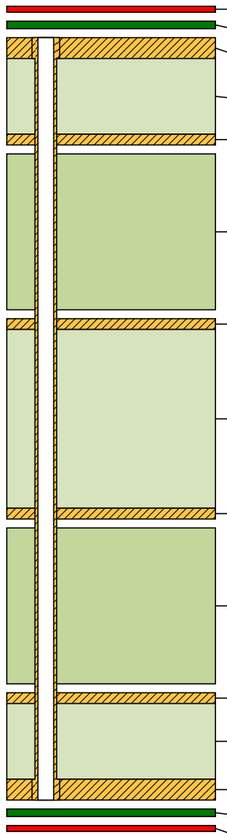
SIZE: B | CAGE CODE: | DWG NO: | REV:

SCALE: | FILE NAME: STAC-v1-pcb.PCBDwf | SHEET: 1 OF 4

REV STATUS OF SHEETS												
	REV											
	SHEET											

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPROVED

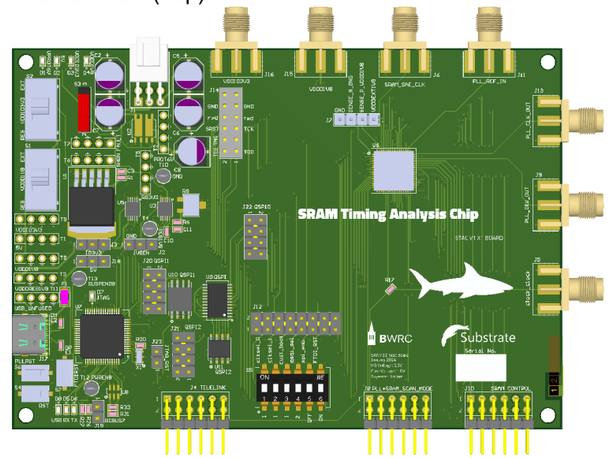
Layer Stack Legend



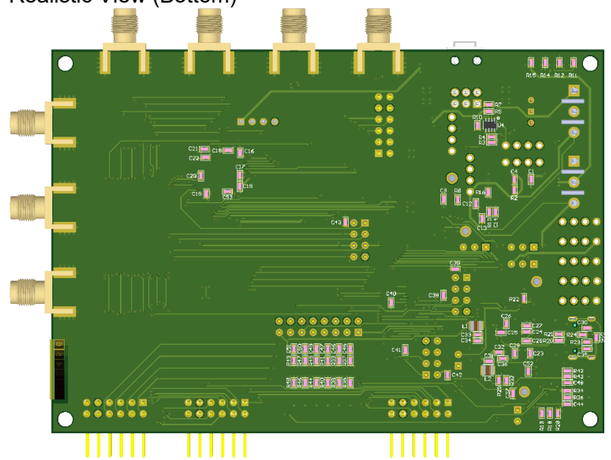
Material	Layer	Thickness	Dielectric Material	Type	Gerber
	Top Overlay			Legend	GTO
Surface Material	Top Solder	0.50mil	Solder Resist	Solder Mask	GTS
CF-003	**L1_TOP**	**1.38mil**		**Signal**	**GTL**
Core		*5.00mil*	*FR4-370HR*	*Dielectric*	
CF-003	**L2_GND**	**0.71mil**		**Signal**	**G1**
Prepreg		*10.30mil*	*FR4-370HR*	*Dielectric*	
CF-003	**L3_VDD_SIG**	**0.71mil**		**Signal**	**G2**
Core		*18.00mil*	*FR4-370HR*	*Dielectric*	
CF-003	**L4_GND**	**0.71mil**		**Signal**	**G3**
Prepreg		*10.30mil*	*FR4-370HR*	*Dielectric*	
CF-003	**L5_GND**	**0.71mil**		**Signal**	**G4**
Core		*5.00mil*	*FR4-370HR*	*Dielectric*	
CF-003	**L6_BOT**	**1.38mil**		**Signal**	**GBL**
Surface Material	Bottom Solder	0.50mil	Solder Resist	Solder Mask	GBS
	Bottom Overlay			Legend	GBO

Total thickness: 55.18mil

Realistic View (Top)



Realistic View (Bottom)



.lte

PART NO: STAC-v1			
APPROVALS	DATE	Berkeley Wireless Research Center (BWRC)	
ENGINEER: Rahul Kumar	12/20/2023		
DESIGNER: Rahul Kumar	12/20/2023		
CHECKER: Anita Flynn	12/20/2023	DESIGN ITEM:	DESIGN ITEM REVISION:
Reference Documents		TITLE: STAC V1 X1 Board	
BOM DOC:		SIZE: B	CAGE CODE:
ASSY DOC:		DWG NO:	REV:
SCH DOC:		SCALE:	FILE NAME: STAC-v1-pcb.PCBDwf
PCB DOC:		SHEET: 2 OF 4	
NEXT ASSY / USED ON			
APPLICATION			

THIRD ANGLE PROJECTION

=DOC_NO_ASSY
.lte

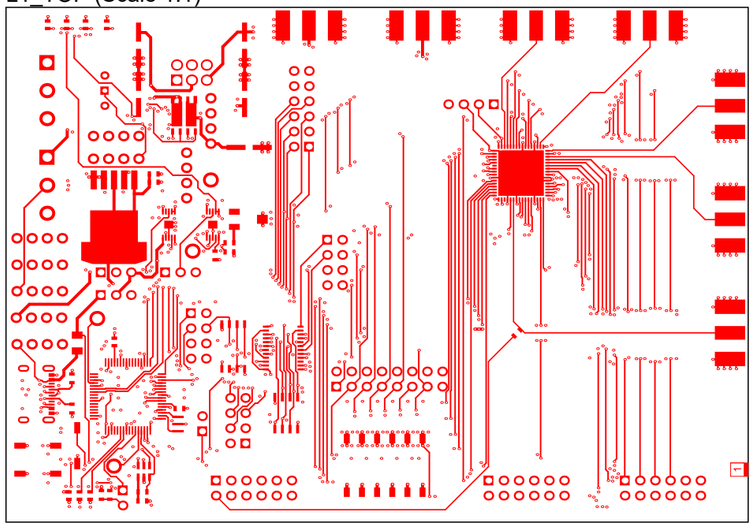
REV STATUS OF SHEETS												
	REV											
	SHEET											

DWG NO: | REV: .lte

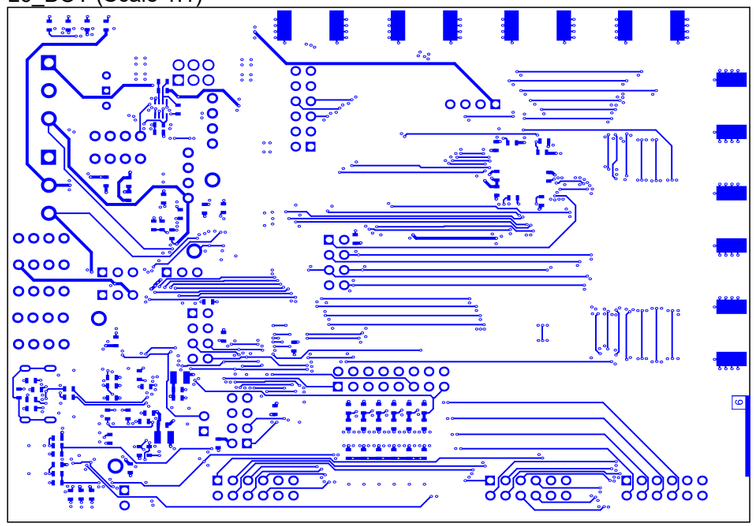
REVISIONS

ZONE	REV	DESCRIPTION	DATE	APPROVED

L1_TOP (Scale 1:1)



L6_BOT (Scale 1:1)



.lt

DWG NO: =DOC_NO_ASSY_ REV: .lte

PART NO: STAC-v1

APPROVALS		DATE
ENGINEER:	Rahul Kumar	12/20/2023
DESIGNER:	Rahul Kumar	12/20/2023
CHECKER:	Anita Flynn	12/20/2023

Reference Documents

BOM DOC:

ASSY DOC:

SCH DOC:

PCB DOC:

THIRD ANGLE PROJECTION

NEXT ASSY | USED ON

APPLICATION

Berkeley Wireless Research Center (BWRC)

DESIGN ITEM: | DESIGN ITEM REVISION:

TITLE: STAC V1 X1 Board

SIZE: B | CAGE CODE: | DWG NO: | REV:

SCALE: | FILE NAME: STAC-v1-pcb.PCBDwf | SHEET: 3 OF 4

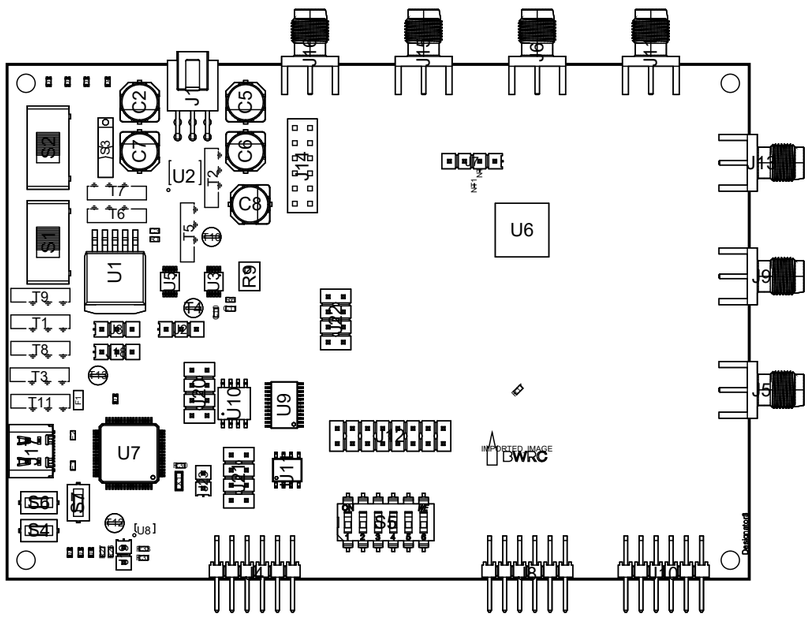
REV STATUS OF SHEETS												
	REV											
	SHEET											

DWG NO: REV: .lfe

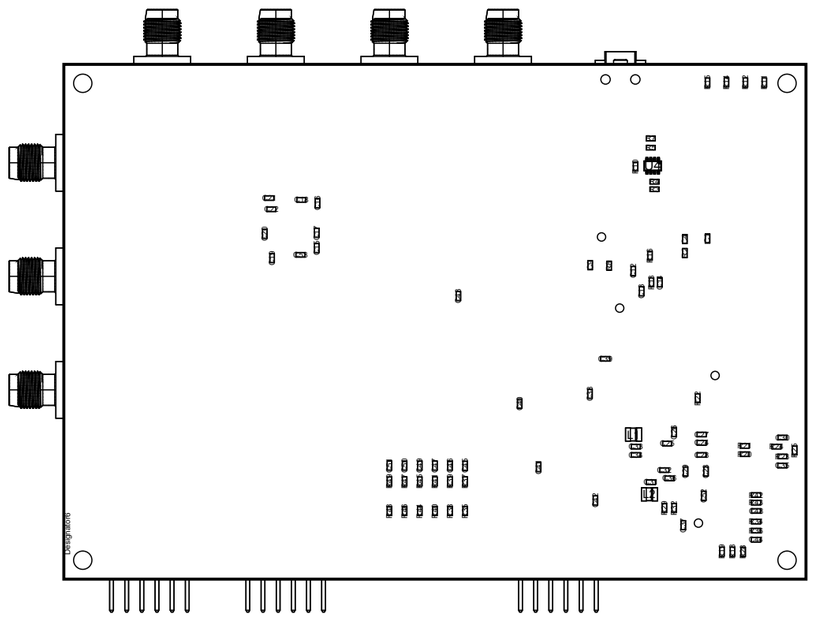
REVISIONS

ZONE	REV	DESCRIPTION	DATE	APPROVED

View from Top side (Scale 1:1)



View from Bottom side (Scale 1:1)



.lfe

DWG NO =DOC_NO_ASSY_ REV .lfe

PART NO: STAC-v1

APPROVALS		DATE
ENGINEER:	Rahul Kumar	12/20/2023
DESIGNER:	Rahul Kumar	12/20/2023
CHECKER:	Anita Flynn	12/20/2023

Reference Documents

BOM DOC:

ASSY DOC:

SCH DOC:

PCB DOC:

NEXT ASSY | USED ON

APPLICATION

THIRD ANGLE PROJECTION

Berkeley Wireless Research Center (BWRC)

DESIGN ITEM: | DESIGN ITEM REVISION:

TITLE:
STAC
V1 X1 Board

SIZE: B | CAGE CODE: | DWG NO: | REV:

SCALE: | FILE NAME: STAC-v1-pcb.PCBDwf | SHEET: 4 OF 4