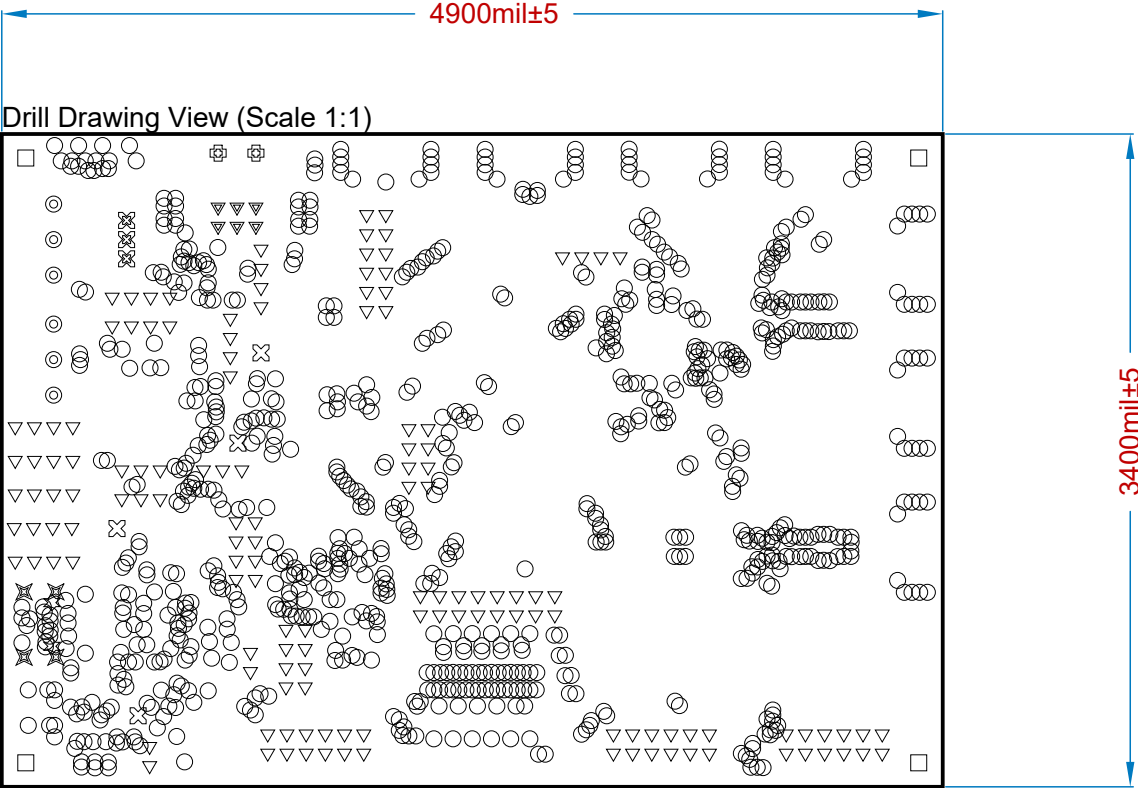


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REV STATUS OF SHEETS	REV											REVISIONS				
	SHEET											ZONE	REV	DESCRIPTION	DATE	APPROVED



- Notes:
- 6 layers.
 - FR370-HR for all layers.
 - ENIG plating.
 - Silkscreen (both sides): white.
 - Soldermask (both sides): blue.
 - Electrical testing: connectivity (.ipc file attached).
 - Remove unused pads from internal layers.
 - Fabricate PCB to meet the requirements of IPC-6012 class 2. No Coupon.
 - Customer contacts: Rahul Kumar (rahulkumar@berkeley.edu, (408) 702-5845), Felicia Guo (felicia_guo@berkeley.edu, 917-520-6865) & Anita Flynn (aflynn@berkeley.edu, 510-681-3931).
 - Controlled impedance traces are only on the L1_Top layer. All are single-ended 50 ohm +/-10%, and are drawn with width 8.501mils. Please adjust as needed.

Drill Table

Symbol	Count	Hole Size	Plated	Hole Tolerance
○	851	0.20mm	Plated	+/-0.08mm
✕	4	0.55mm	Plated	+/-0.08mm
☆	2	0.66mm	Non-Plated	+/-0.05mm
⊗	3	0.71mm	Plated	+/-0.08mm
▽	141	1.02mm	Plated	+/-0.08mm
▼	6	1.35mm	Plated	+/-0.08mm
⊙	6	1.50mm	Plated	+/-0.08mm
⊗	4	1.60mm	Plated	+/-0.08mm
⊕	2	1.78mm	Plated	+/-0.05mm
□	4	3.27mm	Non-Plated	+/-0.05mm
1023 Total				

THIRD ANGLE PROJECTION

NEXT ASSY

USED ON

APPLICATION

PART NO: =PCB_PART_NUMBER

APPROVALS

DATE

ENGINEER: =PCB_ENGINEER

DESIGNER: =PCB_DESIGNER

CHECKER: =PCB_CHECKER

BOM DOC: =DOC_NO_BOM

ASSY DOC: =DOC_NO_FAB_DWG

SCH DOC: =DOC_NO_SCH_DWG

PCB DOC: =PCB_DWG_NO

Reference Documents

DESIGN ITEM: .Item

DESIGN ITEM REVISION: .ItemRevision

TITLE: STAC V1 X1 Board

SIZE: B

CAGE CODE: =CAGE_CO

SCALE:

FILE NAME: STAC-v1-pcb.PCBDwf

SHEET: 1 OF 3

Altium

=Address1
=Address2
=Address3
=Address4

REV: =DOC_NO_ASSY_.It

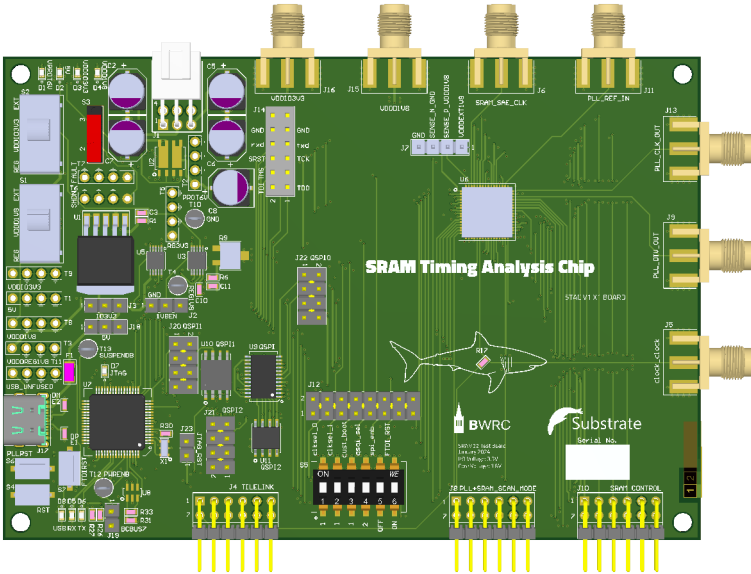
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REV STATUS OF SHEETS	REV										REVISIONS				
	SHEET										ZONE	REV	DESCRIPTION	DATE	APPROVED

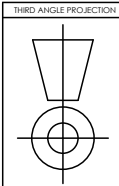
Layer Stack Legend

Material	Layer	Thickness	Dielectric Material	Type	Gerber
	Top Overlay			Legend	GTO
	Surface Material	0.01mm	Solder Resist	Solder Mask	GTS
CF-003	L1_TOP	0.02mm		Signal	GTL
Core		0.13mm	FR4-370HR	Dielectric	
CF-003	L2_GND	0.02mm		Signal	G1
Prepreg		0.26mm	FR4-370HR	Dielectric	
CF-003	L3_VDD_SIG	0.02mm		Signal	G2
Core		0.46mm	FR4-370HR	Dielectric	
CF-003	L4_GND	0.02mm		Signal	G3
Prepreg		0.26mm	FR4-370HR	Dielectric	
CF-003	L5_GND	0.02mm		Signal	G4
Core		0.13mm	FR4-370HR	Dielectric	
CF-003	L6_BOT	0.02mm		Signal	GBL
Surface Material	Bottom Solder	0.01mm	Solder Resist	Solder Mask	GBS
	Bottom Overlay			Legend	GBO
Total thickness: 1.37mm					

Realistic View



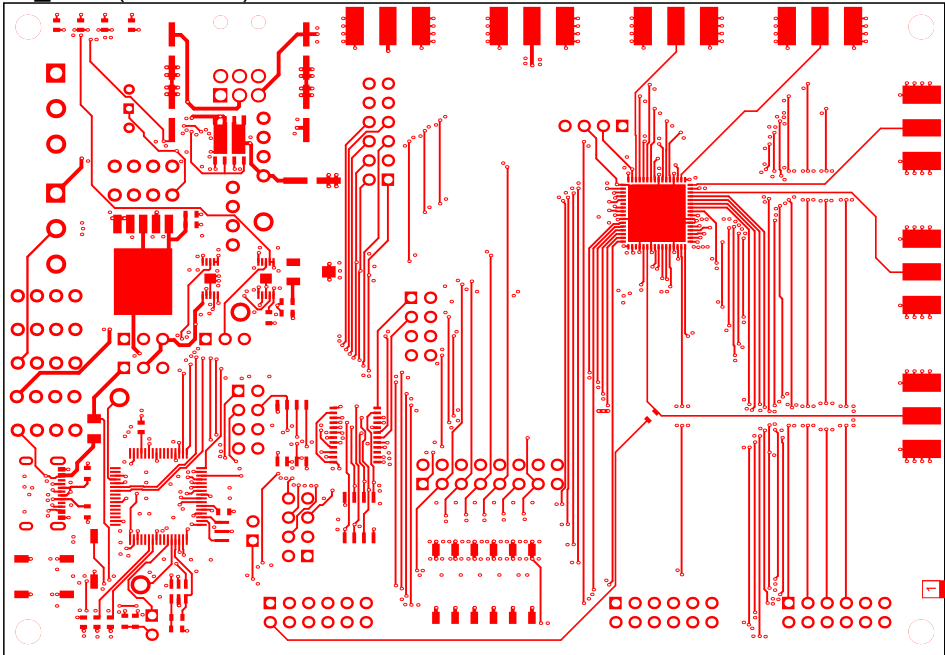
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APPROVALS		DATE			
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DESIGNER: =PCB_DESIGNER		=PCB_DESIGNER			
CHECKER: =PCB_CHECKER		=PCB_CHECKER			
Reference Documents		DESIGN ITEM: .Item		DESIGN ITEM REVISION: .ItemRevision	
BOM DOC: =DOC_NO_BOM		TITLE: STAC			
ASSY DOC: =DOC_NO_FAB_DWG		V1 X1 Board			
SCH DOC: =DOC_NO_SCH_DWG		SIZE: B		CAGE CODE: =CAGE_CO	
PCB DOC: =PCB_DWG_NO		DWG NO:		REV:	
		SCALE:		FILE NAME: STAC-v1-pcb.PCBDwf	
				SHEET: 2 OF 3	



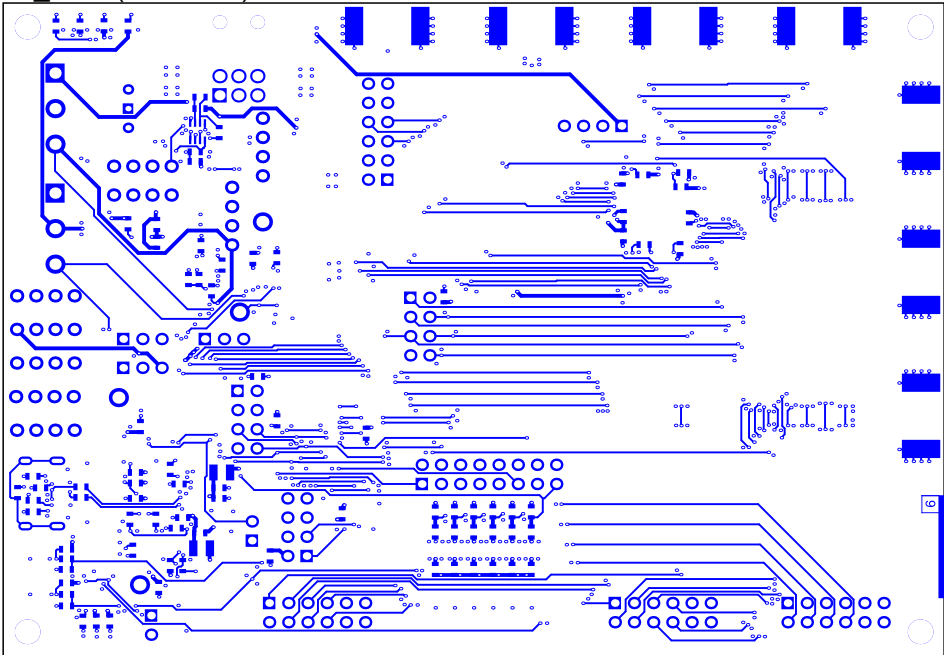
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REV STATUS OF SHEETS	REV											REVISIONS				
	SHEET										ZONE	REV	DESCRIPTION	DATE	APPROVED	

L1 TOP (Scale 1:1)



L6 BOT (Scale 1:1)



PART NO: =PCB_PART_NUMBER		APPROVALS		DATE	=Address1	
ENGINEER:	=PCB_ENGINEER	=PCB_ENGINEER		=PCB_ENGINEER	=Address2	
DESIGNER:	=PCB_DESIGNER	=PCB_DESIGNER		=PCB_DESIGNER	=Address3	
CHECKER:	=PCB_CHECKER	=PCB_CHECKER		=PCB_CHECKER	=Address4	
Reference Documents		BOM DOC:		=DOC_NO_BOM	DESIGN ITEM: .Item	
ASSY DOC:		=DOC_NO_FAB_DWG		DESIGN ITEM REVISION: .ItemRevision		
SCH DOC:		=DOC_NO_SCH_DWG		TITLE: STAC		
PCB DOC:		=PCB_DWG_NO		V1 X1 Board		
THIRD ANGLE PROJECTION		NEXT ASSY		USED ON	SIZE: B	CAGE CODE: =CAGE_CO
APPLICATION		SCALE:		FILE NAME: STAC-v1-pcb.PCBDwf	DWG NO:	REV:
				SHEET: 3 OF 3		