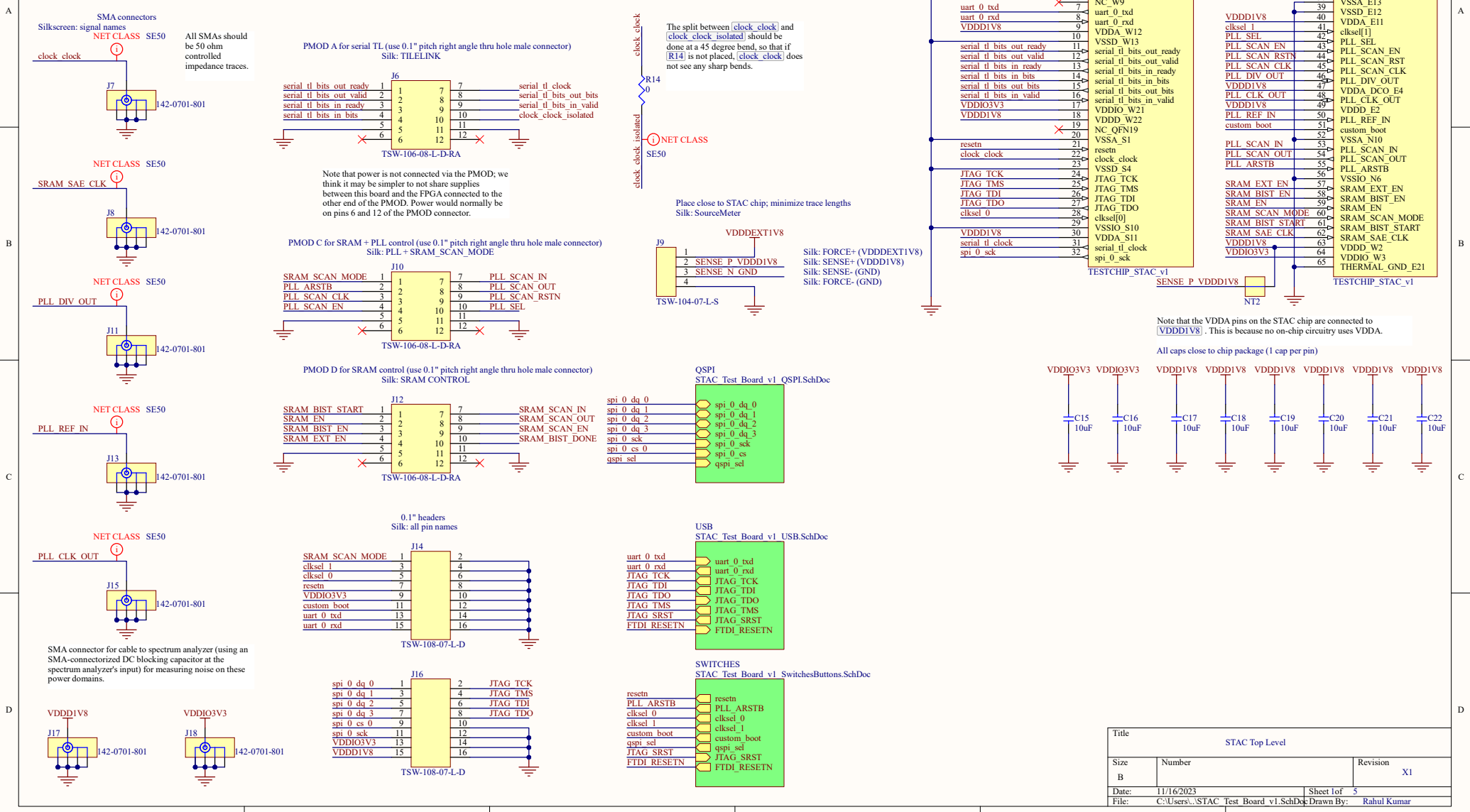
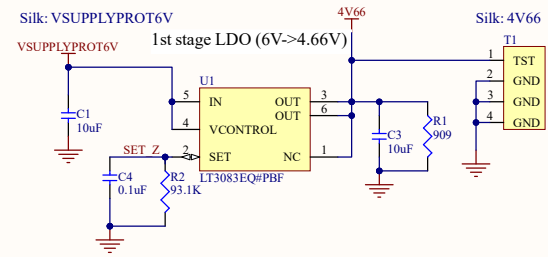
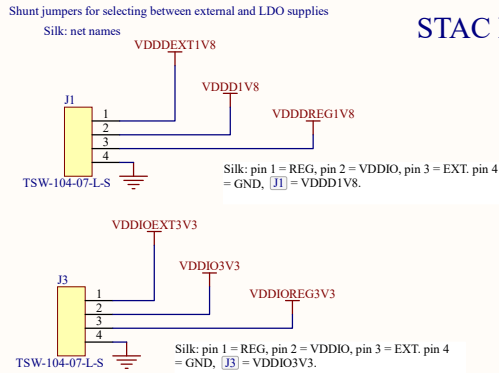
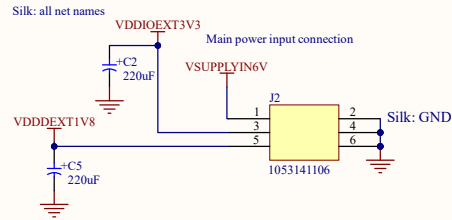


SRAM Timing Analysis Chip (STAC) Test Board

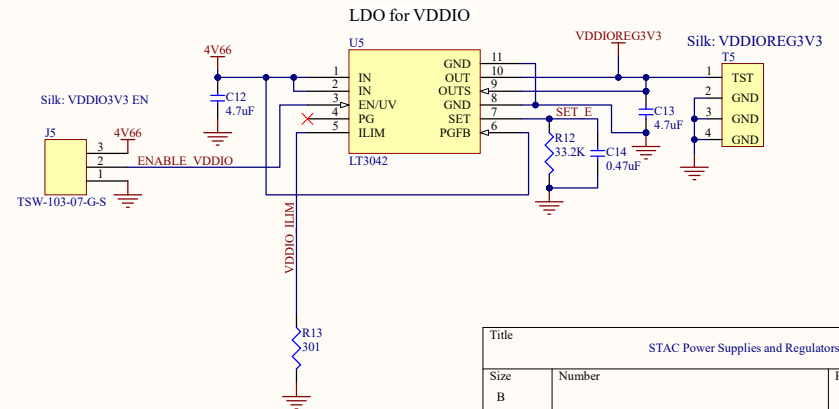
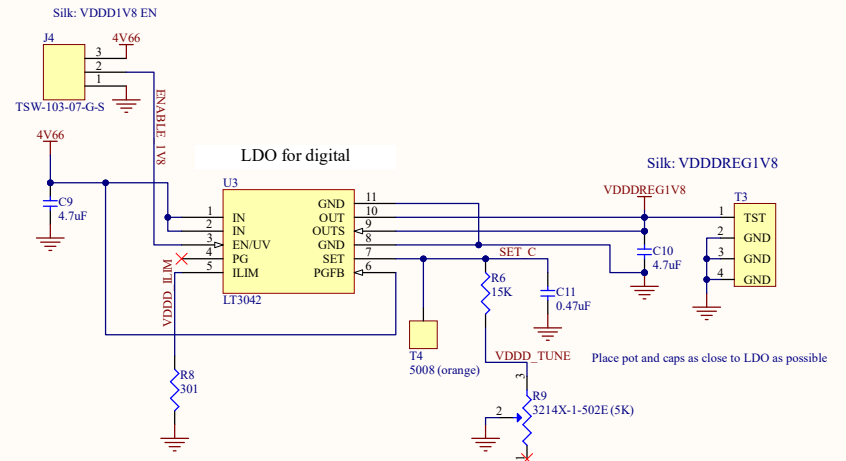
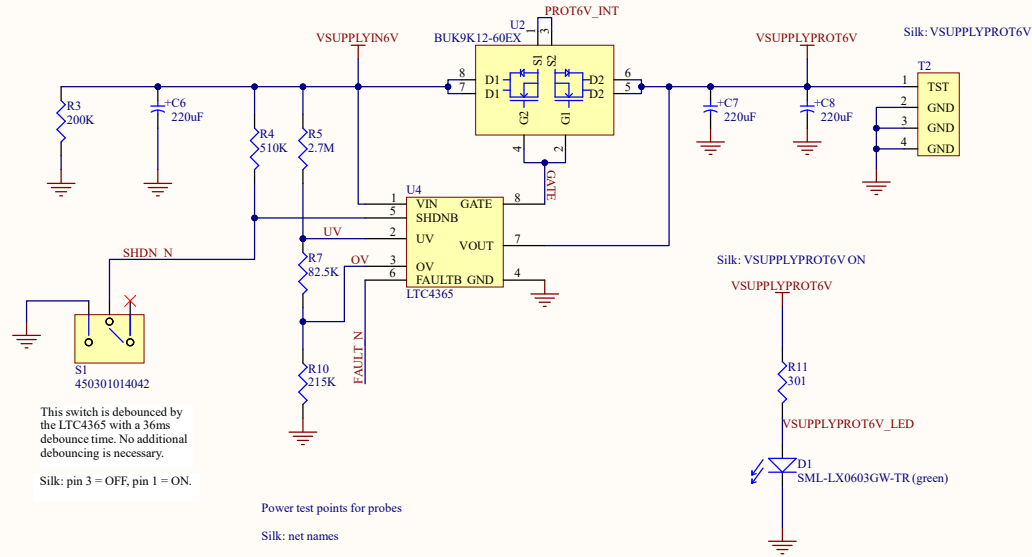
STAC Top Level



STAC Power Supplies and Regulators

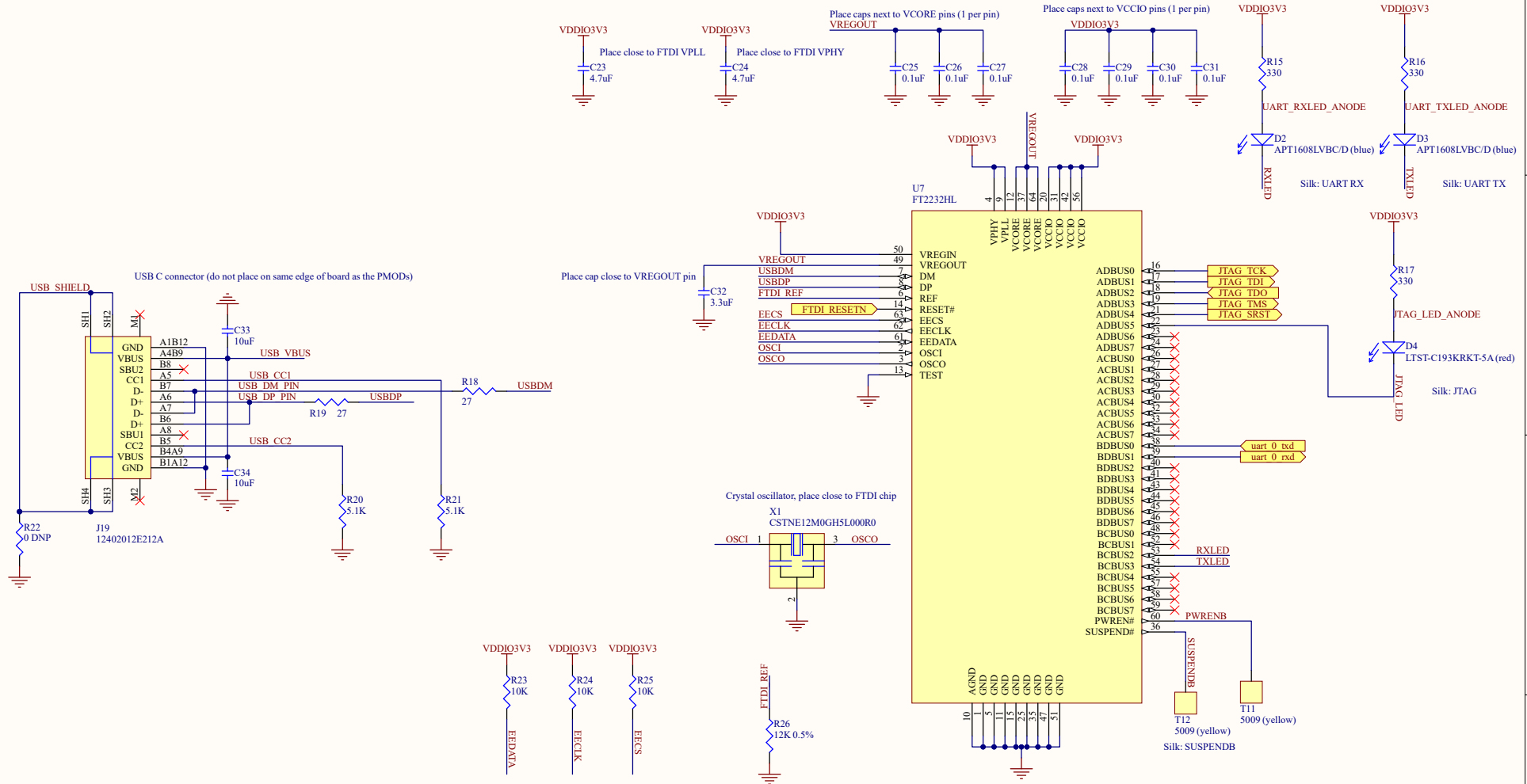


Power Protection for board supply (6V)



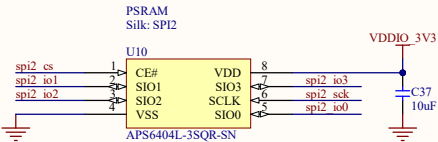
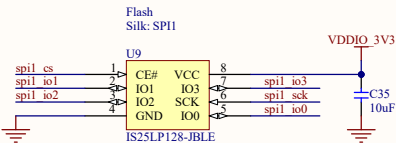
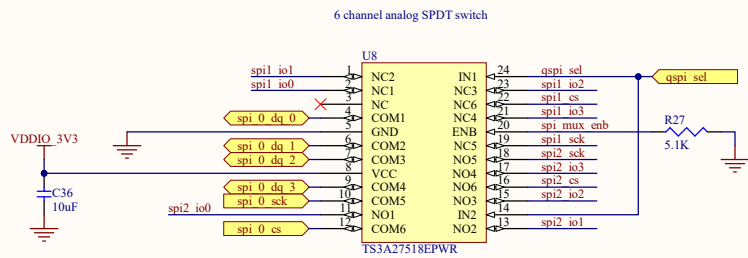
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Size		Number			Revision		
B					X1		
Date:		11/16/2023			Sheet 2 of		5
File:		C:\Users\...STAC Test Board v1 Power			Submitted By:		Rahul Kumar

STAC USB to UART/JTAG



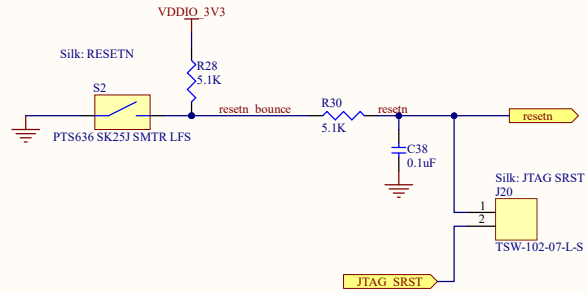
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STAC Quad-SPI Peripherals

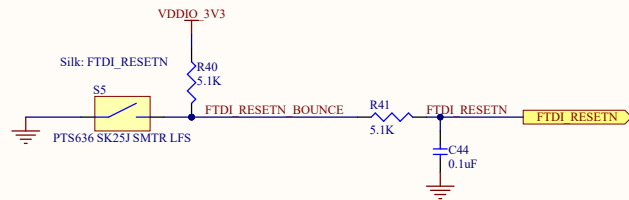
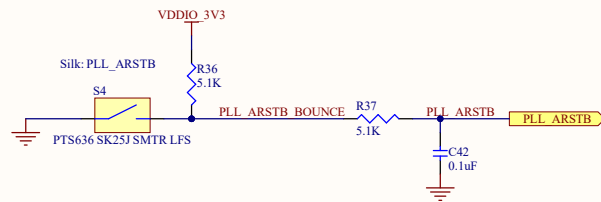
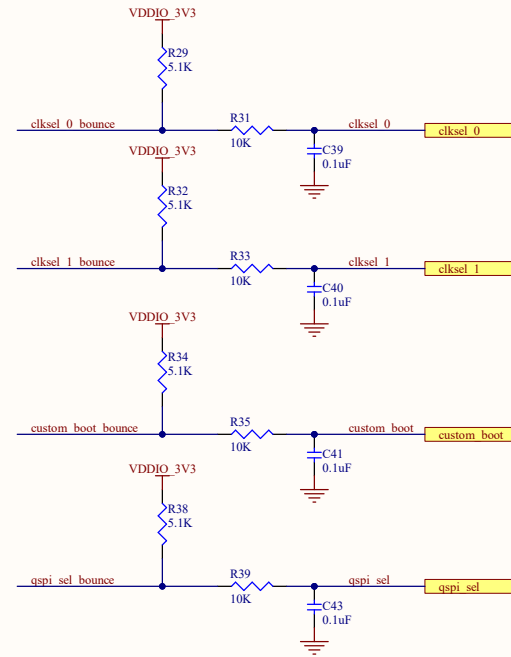
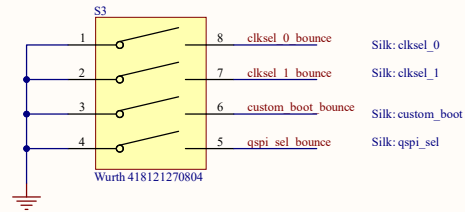


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STAC Quad-SPI Peripherals		
Size	Number	Revision
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Date:	11/16/2023	Sheet 4 of 5
File:	C:\Users\STAC Test Board v1 QSPI	Drawn By: Rahul Kumar

STAC User Switches and Buttons



Add silkscreen annotation showing that when the switch is closed, the corresponding signal is OFF (0) and when the switch is open, the signal is ON (1). For `[qspi_sel]`, switch closed enables SPI1; switch open enables SPI2.



Title		
STAC User Switches and Buttons		
Size	Number	Revision
B		X1
Date:	11/16/2023	Sheet 5 of 5
File:	C:\Users\...STAC Test Board v1 Switches and Buttons	Rahul Kumar