

SRAM Timing Analysis Chip (STAC) Test Board

STAC Top Level

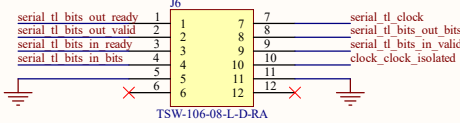
STAC Power
STAC Test Board v1_Power

SMA connectors
Silkscreen: signal names
NET CLASS SE50

clock clock

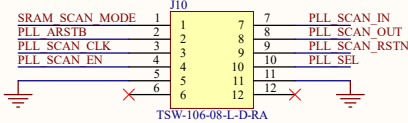
All SMAs should
be 50 ohm
controlled
impedance traces.

PMOD A for serial TL (use 0.1" pitch right angle thru hole male connector)
Silk: TILELINK

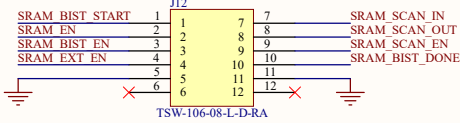


Note that power is not connected via the PMOD; we think it may be simpler to not share supplies between this board and the FPGA connected to the other end of the PMOD. Power would normally be on pins 6 and 12 of the PMOD connector.

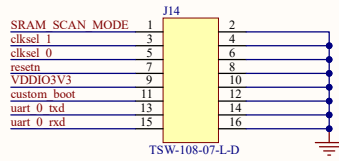
PMOD C for SRAM + PLL control (use 0.1" pitch right angle thru hole male connector)
Silk: PLL + SRAM_SCAN_MODE



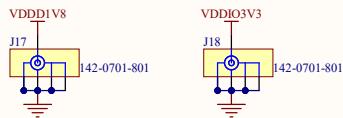
PMOD D for SRAM control (use 0.1" pitch right angle thru hole male connector)
Silk: SRAM_SCAN_MODE



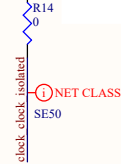
0.1" headers
Silk: all pin names



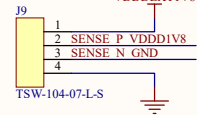
SMA connector for cable to spectrum analyzer (using an SMA-connectorized DC blocking capacitor at the spectrum analyzer's input) for measuring noise on these power domains.



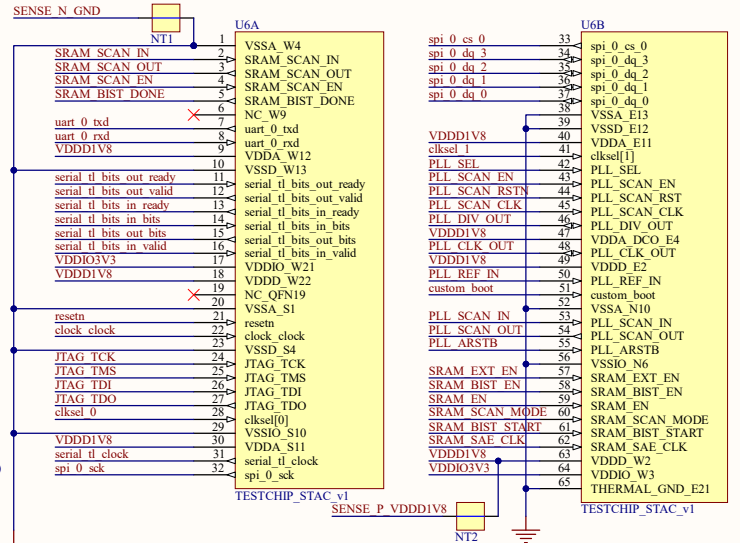
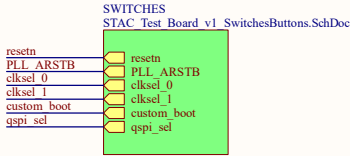
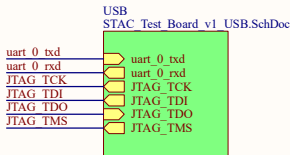
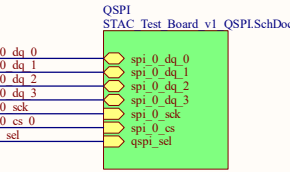
The split between [clock_clock] and [clock_clock_isolated] should be done at a 45 degree bend, so that if [R14] is not placed, [clock_clock] does not see any sharp bends.



Place close to STAC chip; minimize trace lengths
Silk: SourceMeter

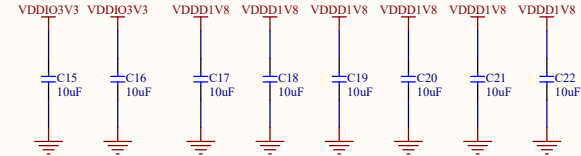


Silk: FORCE+ (VDDDD1V8)
Silk: SENSE+ (VDDDD1V8)
Silk: SENSE- (GND)
Silk: FORCE- (GND)



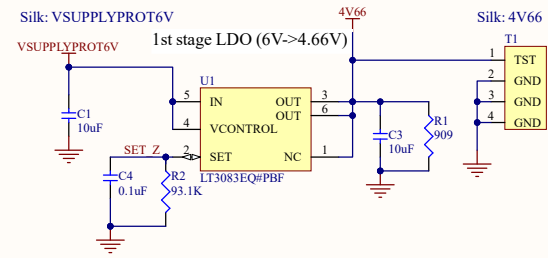
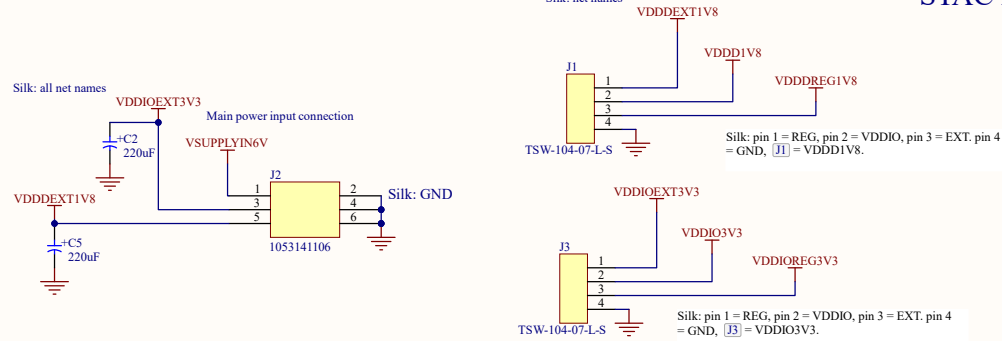
Note that the VDDA pins on the STAC chip are connected to [VDDDD1V8]. This is because no on-chip circuitry uses VDDA.

All caps close to chip package (1 cap per pin)

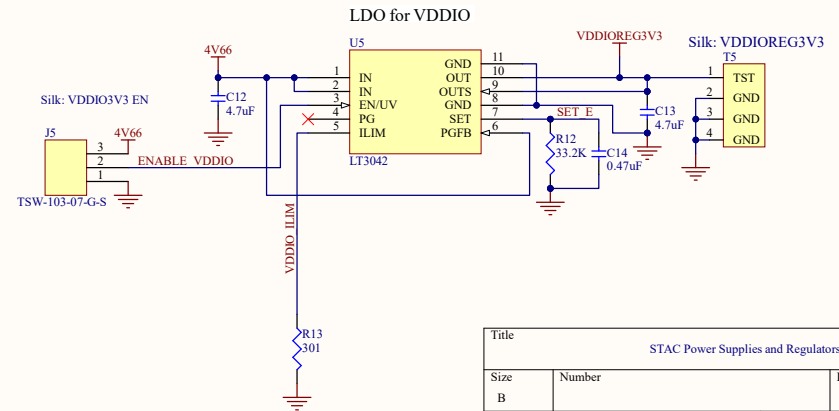
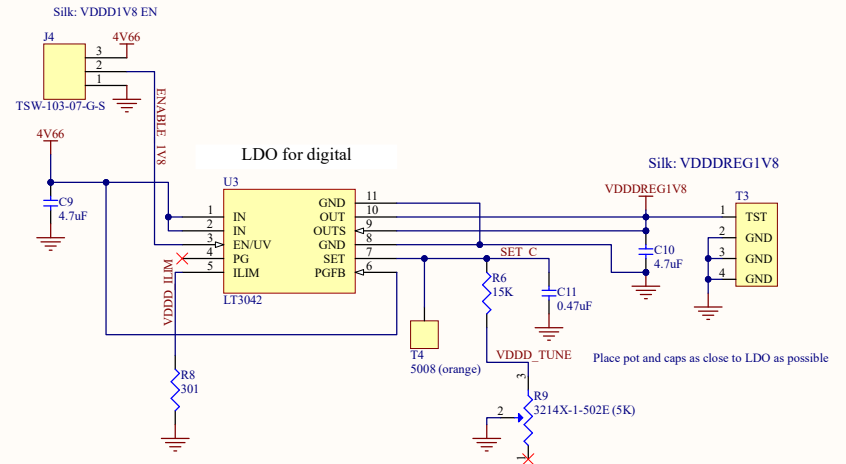
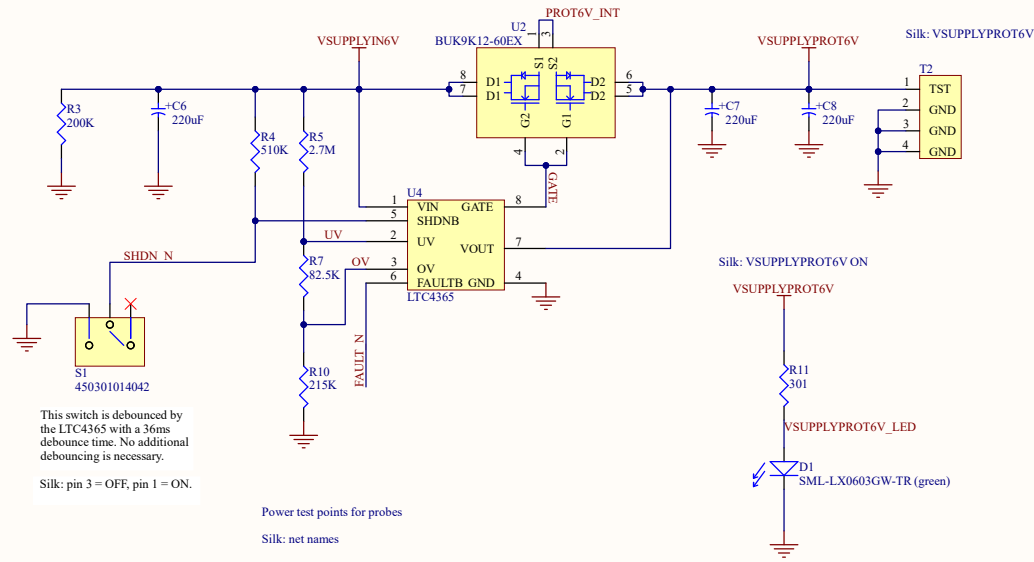


Title		
STAC Top Level		
Size	Number	Revision
B		X1
Date:	11/13/2023	Sheet 1 of 5
File:	C:\Users\STAC Test Board v1.SchDoc	Drawn By: Rahul Kumar

STAC Power Supplies and Regulators

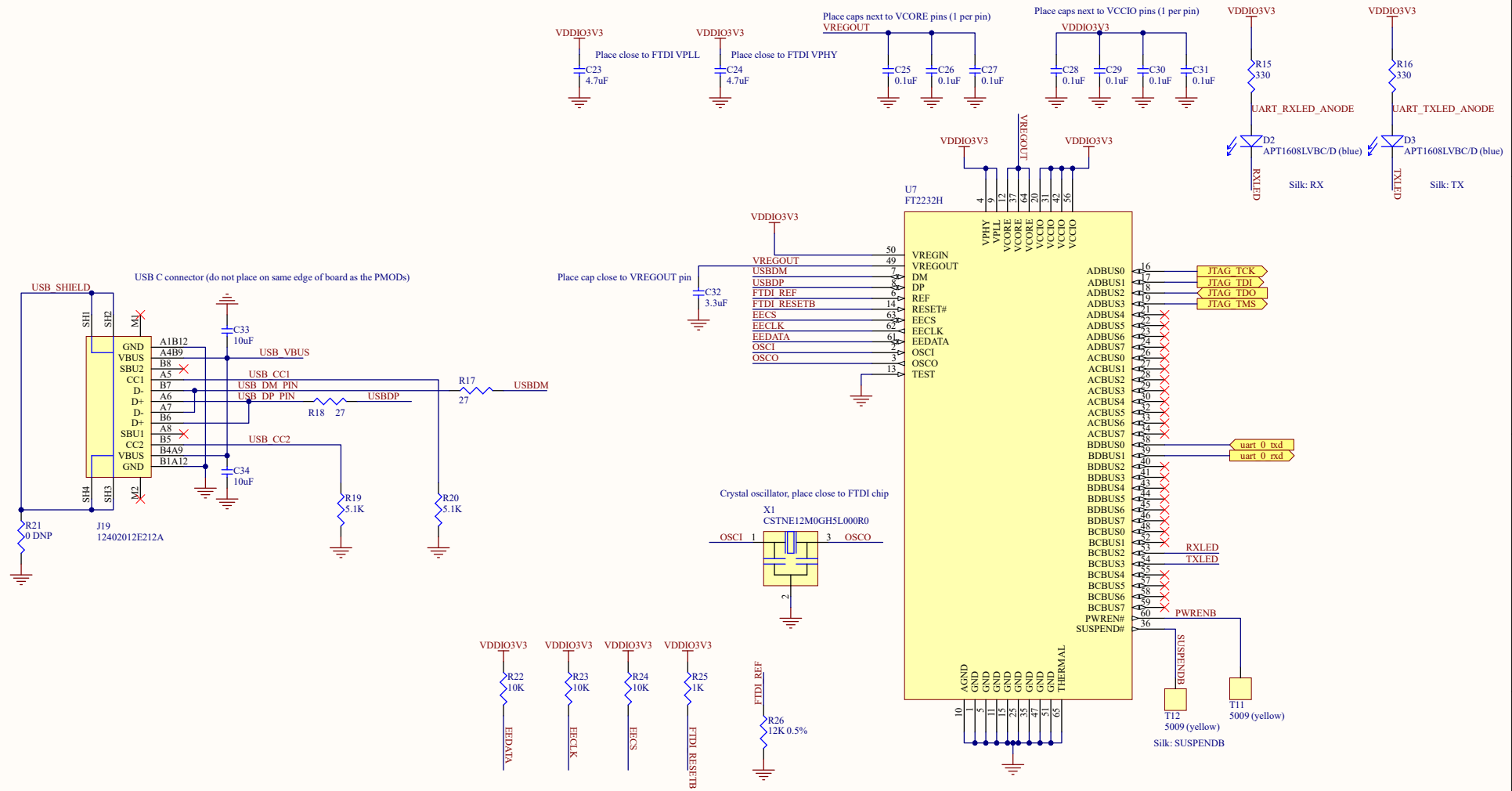


Power Protection for board supply (6V)



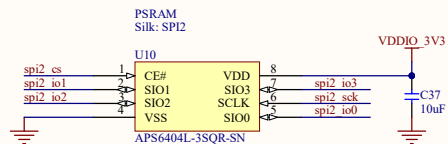
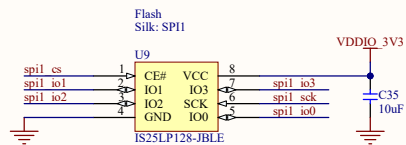
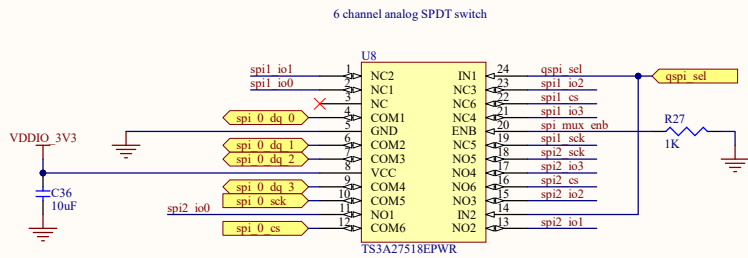
Title				STAC Power Supplies and Regulators			
Size		Number			Revision		
Date		11/13/2023			X1		
File:		C:\Users\...STAC Test Board v1 Power			Sheet 2 of 5		
Drawn By:		Rahul Kumar			5		

STAC USB to UART/JTAG



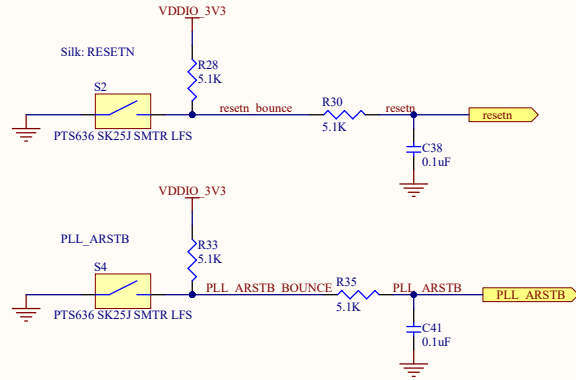
Title				STAC USB to UART/JTAG			
Size		Number			Revision		
Date		11/13/2023			X1		
B:		11/13/2023			5		
File:		C:\Users\...STAC Test Board v1 USB...			Rahul Kumar		

STAC Quad-SPI Peripherals

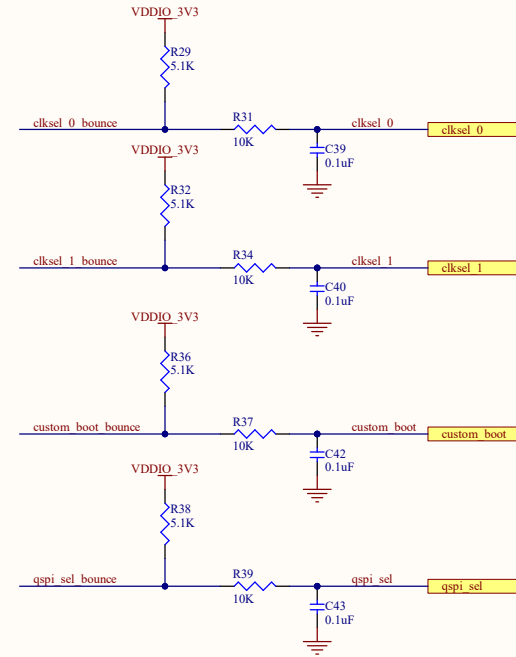
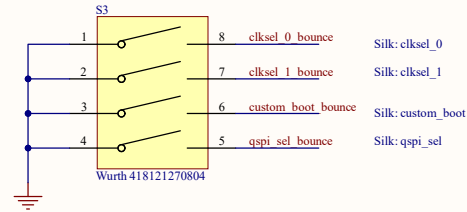


Title		
STAC Quad-SPI Peripherals		
Size	Number	Revision
B		X1
Date:	11/13/2023	Sheet 4 of 5
File:	C:\Users\STAC Test Board v1	QSPI Silkscreen By: Rahul Kumar

STAC User Switches and Buttons



Add silkscreen annotation showing that when the switch is closed, the corresponding signal is OFF (0) and when the switch is open, the signal is ON (1). For [qspi_sel], switch closed enables SPI1; switch open enables SPI2.



Title		
STAC User Switches and Buttons		
Size B	Number	Revision X1
Date: 11/13/2023	Sheet 5 of 5	
File: C:\Users\..STAC Test Board v1 Switches and Buttons	Rahul Kumar	