SRAM Timing Analysis Chip (STAC) Test Board

STAC Top Level

STAC_Power
STAC_Test_Board_v1_Power

SMA connectors
Silkscreen: signal names

NET CLASS SE50
clock_clock
J7
142-0701-801

All SMAs should be 50 ohm controlled impedance traces.

NET CLASS SE50
SRAM_SAE_CLK
J8
142-0701-801

NET CLASS SE50
PLL_DIV_OUT
J11
142-0701-801

NET CLASS SE50
PLL_REF_IN
J13
142-0701-801

NET CLASS SE50
PLL_CLK_OUT
J15
142-0701-801

SMA connector for cable to spectrum analyzer (using an SMA-connectorized DC blocking capacitor at the spectrum analyzer's input) for measuring noise on these power domains.

VDDD1V8
J17
142-0701-801

VDDIO3V3
J18
142-0701-801

PMOD A for serial TL (use 0.1" pitch right angle thru hole male connector)
Silk: TILELINK

J6
TSW-106-08-L-D-RA

serial_tl_bits_out_ready	1	7	serial_tl_clock
serial_tl_bits_out_valid	2	8	serial_tl_bits_out_bits
serial_tl_bits_in_ready	3	9	serial_tl_bits_in_valid
serial_tl_bits_in_bits	4	10	clock_clock_isolated
	5	11	
	6	12	

Note that power is not connected via the PMOD; we think it may be simpler to not share supplies between this board and the FPGA connected to the other end of the PMOD. Power would normally be on pins 6 and 12 of the PMOD connector.

PMOD C for SRAM + PLL control (use 0.1" pitch right angle thru hole male connector)
Silk: PLL + SRAM_SCAN_MODE

J10
TSW-106-08-L-D-RA

SRAM_SCAN_MODE	1	7	PLL_SCAN_IN
PLL_ARSTB	2	8	PLL_SCAN_OUT
PLL_SCAN_CLK	3	9	PLL_SCAN_RSTN
PLL_SCAN_EN	4	10	PLL_SEL
	5	11	
	6	12	

PMOD D for SRAM control (use 0.1" pitch right angle thru hole male connector)
Silk: SRAM CONTROL

J12
TSW-106-08-L-D-RA

SRAM_BIST_START	1	7	SRAM_SCAN_IN
SRAM_EN	2	8	SRAM_SCAN_OUT
SRAM_BIST_EN	3	9	SRAM_SCAN_EN
SRAM_EXT_EN	4	10	SRAM_BIST_DONE
	5	11	
	6	12	

0.1" headers
Silk: all pin names

J14
TSW-108-07-L-D

SRAM_SCAN_MODE	1	2	
clksel_1	3	4	
clksel_0	5	6	
resetn	7	8	
VDDIO3V3	9	10	
custom_boot	11	12	
uart_0_txd	13	14	
uart_0_rxd	15	16	

J16
TSW-108-07-L-D

spi_0_dq_0	1	2	JTAG_TCK
spi_0_dq_1	3	4	JTAG_TMS
spi_0_dq_2	5	6	JTAG_TDI
spi_0_dq_3	7	8	JTAG_TDO
spi_0_cs_0	9	10	
spi_0_sck	11	12	
VDDIO3V3	13	14	
VDDD1V8	15	16	

clock_clock
R14
0
clock_clock_isolated
NET CLASS
SE50

The split between clock_clock and clock_clock_isolated should be done at a 45 degree bend, so that if R14 is not placed, clock_clock does not see any sharp bends.

Place close to STAC chip; minimize trace lengths
Silk: SourceMeter

J9
TSW-104-07-L-S

	1	VDDDEXT1V8
SENSE_P_VDDD1V8	2	
SENSE_N_GND	3	
	4	

Silk: FORCE+ (VDDDEXT1V8)
Silk: SENSE+ (VDDD1V8)
Silk: SENSE- (GND)
Silk: FORCE- (GND)

QSPI
STAC_Test_Board_v1_QSPI.SchDoc

spi_0_dq_0	spi_0_dq_0
spi_0_dq_1	spi_0_dq_1
spi_0_dq_2	spi_0_dq_2
spi_0_dq_3	spi_0_dq_3
spi_0_sck	spi_0_sck
spi_0_cs_0	spi_0_cs
qspi_sel	qspi_sel

USB
STAC_Test_Board_v1_USB.SchDoc

uart_0_txd	uart_0_txd
uart_0_rxd	uart_0_rxd
JTAG_TCK	JTAG_TCK
JTAG_TDI	JTAG_TDI
JTAG_TDO	JTAG_TDO
JTAG_TMS	JTAG_TMS
JTAG_SRST	JTAG_SRST
FTDI_RESETN	FTDI_RESETN

SWITCHES
STAC_Test_Board_v1_SwitchesButtons.SchDoc

resetn	resetn
PLL_ARSTB	PLL_ARSTB
clksel_0	clksel_0
clksel_1	clksel_1
custom_boot	custom_boot
qspi_sel	qspi_sel
JTAG_SRST	JTAG_SRST
FTDI_RESETN	FTDI_RESETN

SENSE_N_GND
NT1

U6A
TESTCHIP_STAC_v1

		1	VSSA_W4
SRAM_SCAN_IN		2	SRAM_SCAN_IN
SRAM_SCAN_OUT		3	SRAM_SCAN_OUT
SRAM_SCAN_EN		4	SRAM_SCAN_EN
SRAM_BIST_DONE		5	SRAM_BIST_DONE
		6	NC_W9
uart_0_txd		7	uart_0_txd
uart_0_rxd		8	uart_0_rxd
VDDD1V8		9	VDDA_W12
		10	VSSD_W13
serial_tl_bits_out_ready		11	serial_tl_bits_out_ready
serial_tl_bits_out_valid		12	serial_tl_bits_out_valid
serial_tl_bits_in_ready		13	serial_tl_bits_in_ready
serial_tl_bits_in_bits		14	serial_tl_bits_in_bits
serial_tl_bits_out_bits		15	serial_tl_bits_out_bits
serial_tl_bits_in_valid		16	serial_tl_bits_in_valid
VDDIO3V3		17	VDDIO_W21
VDDD1V8		18	VDDD_W22
		19	NC_QFN19
		20	VSSA_S1
resetn		21	resetn
clock_clock		22	clock_clock
		23	VSSD_S4
JTAG_TCK		24	JTAG_TCK
JTAG_TMS		25	JTAG_TMS
JTAG_TDI		26	JTAG_TDI
JTAG_TDO		27	JTAG_TDO
clksel_0		28	clksel[0]
		29	VSSIO_S10
VDDD1V8		30	VDDA_S11
serial_tl_clock		31	serial_tl_clock
spi_0_sck		32	spi_0_sck

U6B
TESTCHIP_STAC_v1

spi_0_cs_0		33	spi_0_cs_0
spi_0_dq_3		34	spi_0_dq_3
spi_0_dq_2		35	spi_0_dq_2
spi_0_dq_1		36	spi_0_dq_1
spi_0_dq_0		37	spi_0_dq_0
		38	VSSA_E13
		39	VSSD_E12
VDDD1V8		40	VDDA_E11
clksel_1		41	clksel[1]
PLL_SEL		42	PLL_SEL
PLL_SCAN_EN		43	PLL_SCAN_EN
PLL_SCAN_RSTN		44	PLL_SCAN_RST
PLL_SCAN_CLK		45	PLL_SCAN_CLK
PLL_DIV_OUT		46	PLL_DIV_OUT
VDDD1V8		47	VDDA_DCO_E4
PLL_CLK_OUT		48	PLL_CLK_OUT
VDDD1V8		49	VDDD_E2
PLL_REF_IN		50	PLL_REF_IN
custom_boot		51	custom_boot
		52	VSSA_N10
PLL_SCAN_IN		53	PLL_SCAN_IN
PLL_SCAN_OUT		54	PLL_SCAN_OUT
PLL_ARSTB		55	PLL_ARSTB
		56	VSSIO_N6
SRAM_EXT_EN		57	SRAM_EXT_EN
SRAM_BIST_EN		58	SRAM_BIST_EN
SRAM_EN		59	SRAM_EN
SRAM_SCAN_MODE		60	SRAM_SCAN_MODE
SRAM_BIST_START		61	SRAM_BIST_START
SRAM_SAE_CLK		62	SRAM_SAE_CLK
VDDD1V8		63	VDDD_W2
VDDIO3V3		64	VDDIO_W3
		65	THERMAL_GND_E21

SENSE_P_VDDD1V8
NT2

Note that the VDDA pins on the STAC chip are connected to VDDD1V8. This is because no on-chip circuitry uses VDDA.

All caps close to chip package (1 cap per pin)

VDDIO3V3	VDDIO3V3	VDDD1V8	VDDD1V8	VDDD1V8	VDDD1V8	VDDD1V8	VDDD1V8
C15 10uF	C16 10uF	C17 10uF	C18 10uF	C19 10uF	C20 10uF	C21 10uF	C22 10uF

Title	STAC Top Level		
Size	Number		Revision
B			X1
Date:	11/14/2023	Sheet 1 of	5
File:	C:\Users\..\STAC_Test_Board_v1.SchDoc	Drawn By:	Rahul Kumar

STAC Power Supplies and Regulators

Shunt jumpers for selecting between external and LDO supplies

Silk: net names

VDDDEXT1V8
VDDD1V8
VDDDREG1V8
J1
TSW-104-07-L-S

Silk: pin 1 = REG, pin 2 = VDDIO, pin 3 = EXT. pin 4 = GND, J1 = VDDD1V8.

Silk: all net names

VDDIOEXT3V3
Main power input connection
+C2 220uF
VSUPPLYIN6V
J2
VDDDEXT1V8
Silk: GND
+C5 220uF
1053141106

VDDIOEXT3V3
VDDIO3V3
VDDIOREG3V3
J3
TSW-104-07-L-S

Silk: pin 1 = REG, pin 2 = VDDIO, pin 3 = EXT. pin 4 = GND, J3 = VDDIO3V3.

Silk: VSUPPLYPROT6V
VSUPPLYPROT6V
1st stage LDO (6V->4.66V)
4V66
Silk: 4V66
U1
IN OUT OUT VCONTROL SET NC
LT3083EQ#PBF
C1 10uF
C3 10uF
R1 909
SET_Z
C4 0.1uF
R2 93.1K
T1 TST GND GND GND

Power Protection for board supply (6V)

PROT6V_INT
U2
BUK9K12-60EX
VSUPPLYIN6V
VSUPPLYPROT6V
Silk: VSUPPLYPROT6V
R3 200K
+C6 220uF
R4 510K
R5 2.7M
+C7 220uF
+C8 220uF
T2 TST GND GND GND
U4
VIN GATE SHDNB UV VOUT OV FAULTB GND
LTC4365
UV
OV
R7 82.5K
R10 215K
FAULT_N
GATE
SHDN_N
S1
450301014042

This switch is debounced by the LTC4365 with a 36ms debounce time. No additional debouncing is necessary.

Silk: pin 3 = OFF, pin 1 = ON.

Power test points for probes

Silk: net names

SHDN_N T6 TST GND GND GND
FAULT_N T7 TST GND GND GND
VDDD1V8 T8 TST GND GND GND
VDDIO3V3 T9 TST GND GND GND

T10 5006 (black)

Silk: GND

Silk: VSUPPLYPROT6V ON
VSUPPLYPROT6V
R11 301
VSUPPLYPROT6V_LED
D1 SML-LX0603GW-TR (green)

Silk: VDDD1V8 EN
J4
TSW-103-07-G-S
4V66
ENABLE_1V8

LDO for digital

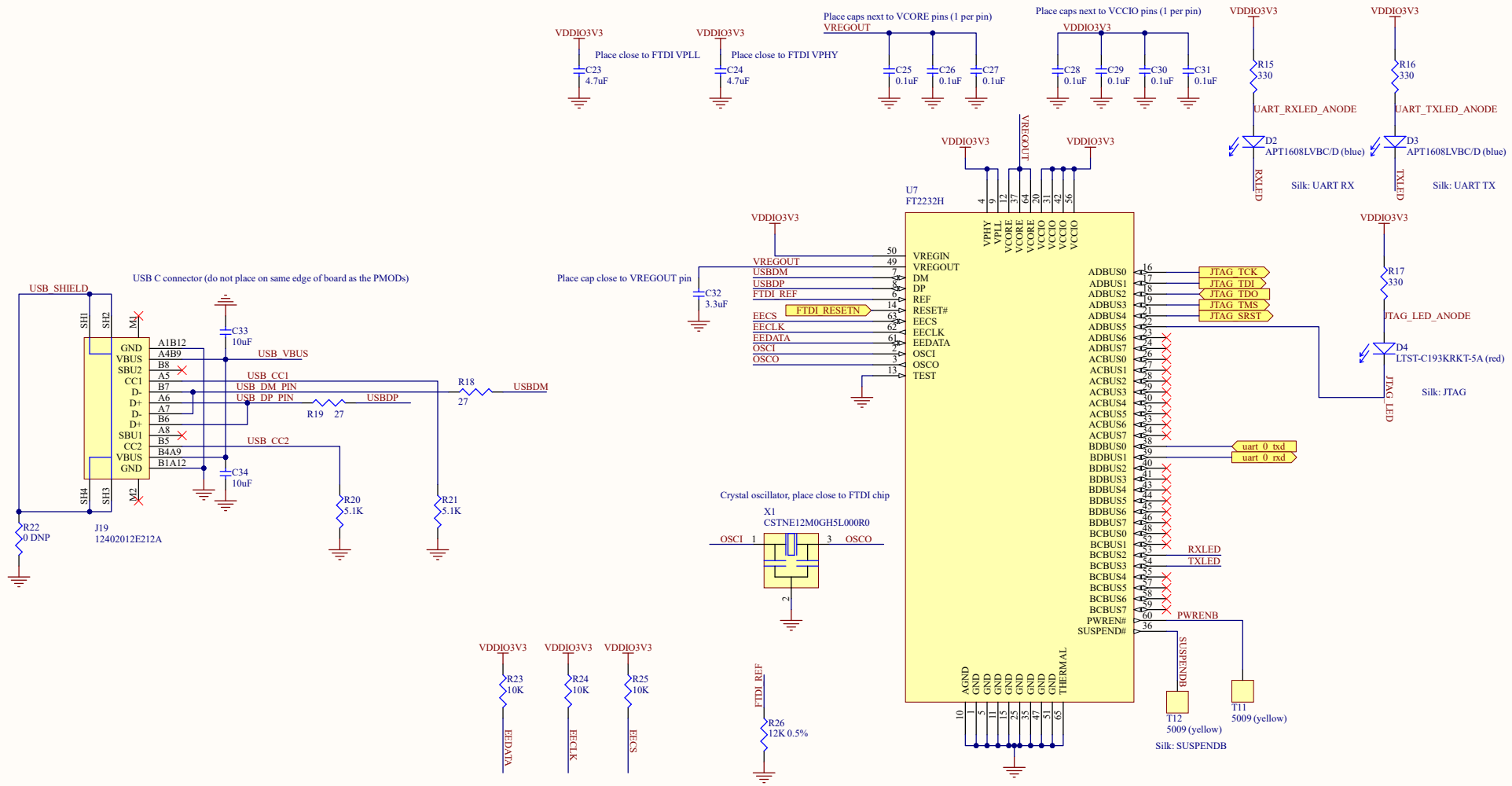
U3
IN IN EN/UV PG ILIM GND OUT OUTS GND SET PGFB
LT3042
C9 4.7uF
VDDD_ILIM
R8 301
SET_C
R6 15K
C11 0.47uF
T4 5008 (orange)
VDDD_TUNE
R9 3214X-1-502E (5K)
Place pot and caps as close to LDO as possible
Silk: VDDDREG1V8
VDDDREG1V8
C10 4.7uF
T3 TST GND GND GND

LDO for VDDIO

Silk: VDDIO3V3 EN
J5
TSW-103-07-G-S
4V66
ENABLE_VDDIO
U5
IN IN EN/UV PG ILIM GND OUT OUTS GND SET PGFB
LT3042
C12 4.7uF
VDDIO_ILIM
R13 301
SET_E
R12 33.2K
C14 0.47uF
VDDIOREG3V3
C13 4.7uF
Silk: VDDIOREG3V3
T5 TST GND GND GND

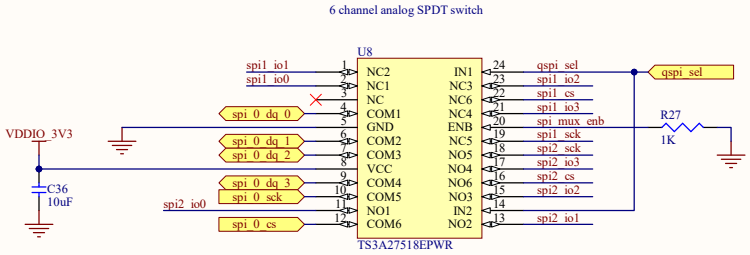
Title	STAC Power Supplies and Regulators	
Size: B	Number	Revision: X1
Date: 11/14/2023	Sheet 2 of 5	
File: C:\Users\..\STAC_Test_Board_v1_Power.SchDoc	Drawn By: Rahul Kumar	

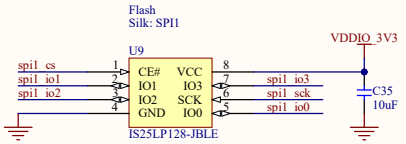
STAC USB to UART/JTAG

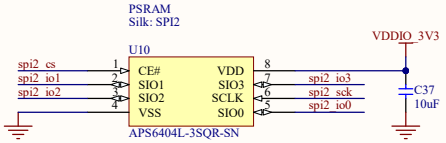


Title	STAC USB to UART/JTAG	
Size: B	Number:	Revision: X1
Date: 11/14/2023	Sheet 3 of 5	
File: C:\Users\..\STAC_Test_Board_v1_USB.SchDoc	Drawn By: Rahul Kumar	

STAC Quad-SPI Peripherals

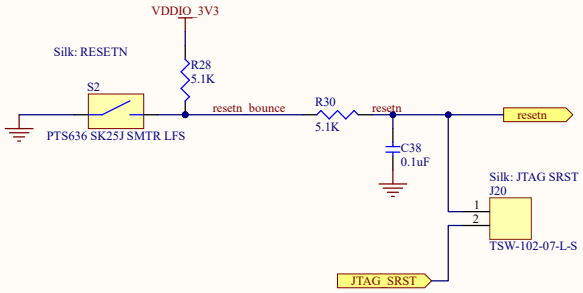


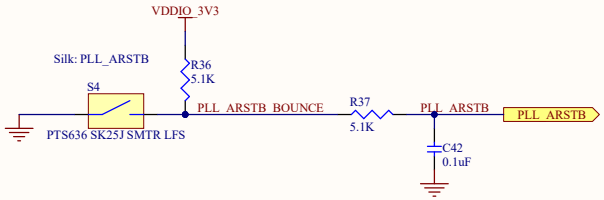


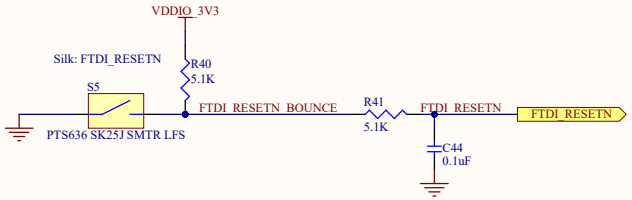


Title: STAC Quad-SPI Peripherals		
Size: B	Number:	Revision: X1
Date: 11/14/2023	Sheet 4 of 5	
File: C:\Users\..\STAC_Test_Board_v1_QSPI.SchDoc	Drawn By: Rahul Kumar	

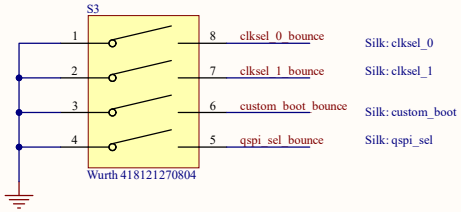
STAC User Switches and Buttons

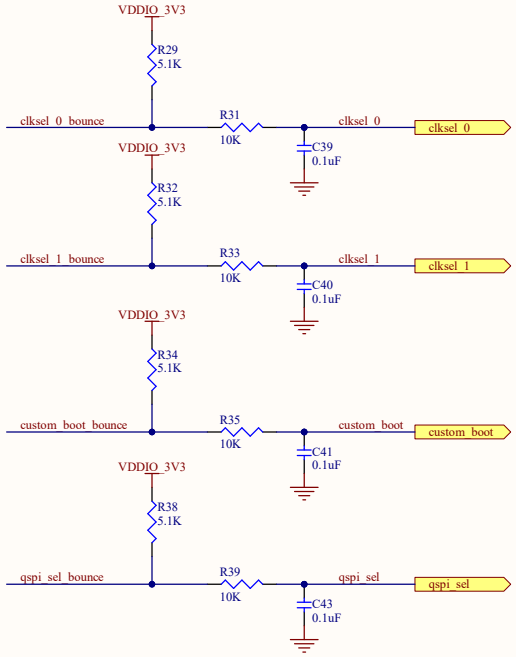






Add silkscreen annotation showing that when the switch is closed, the corresponding signal is OFF (0) and when the switch is open, the signal is ON (1). For qspi_sel, switch closed enables SPI1; switch open enables SPI2.





Title	STAC User Switches and Buttons		
Size: B	Number:		Revision: X1
Date: 11/14/2023		Sheet 5 of 5	
File: C:\Users\..\STAC_Test_Board_v1_Switches_Buttons.SchDoc		Drawn By: Rahul Kumar	