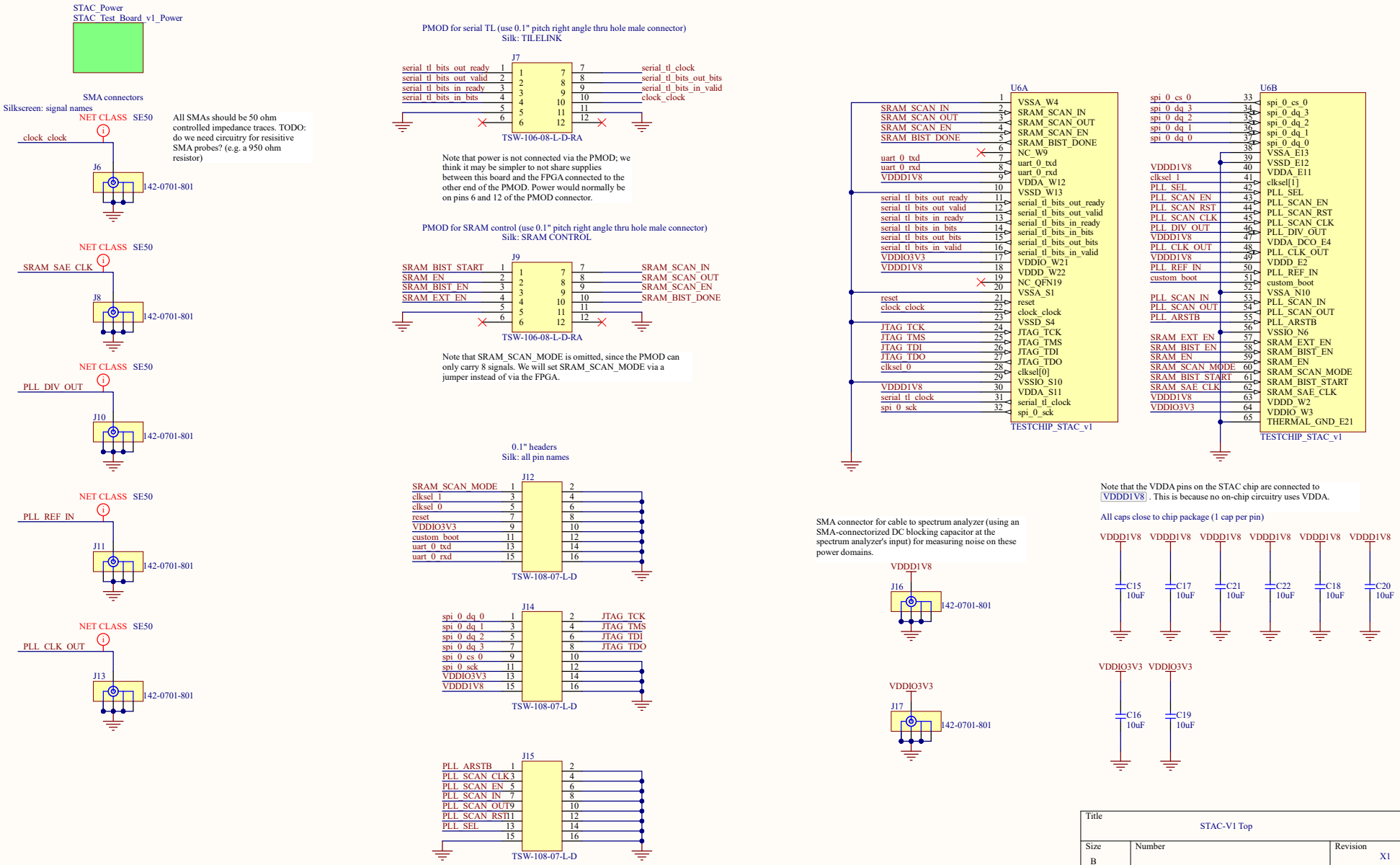
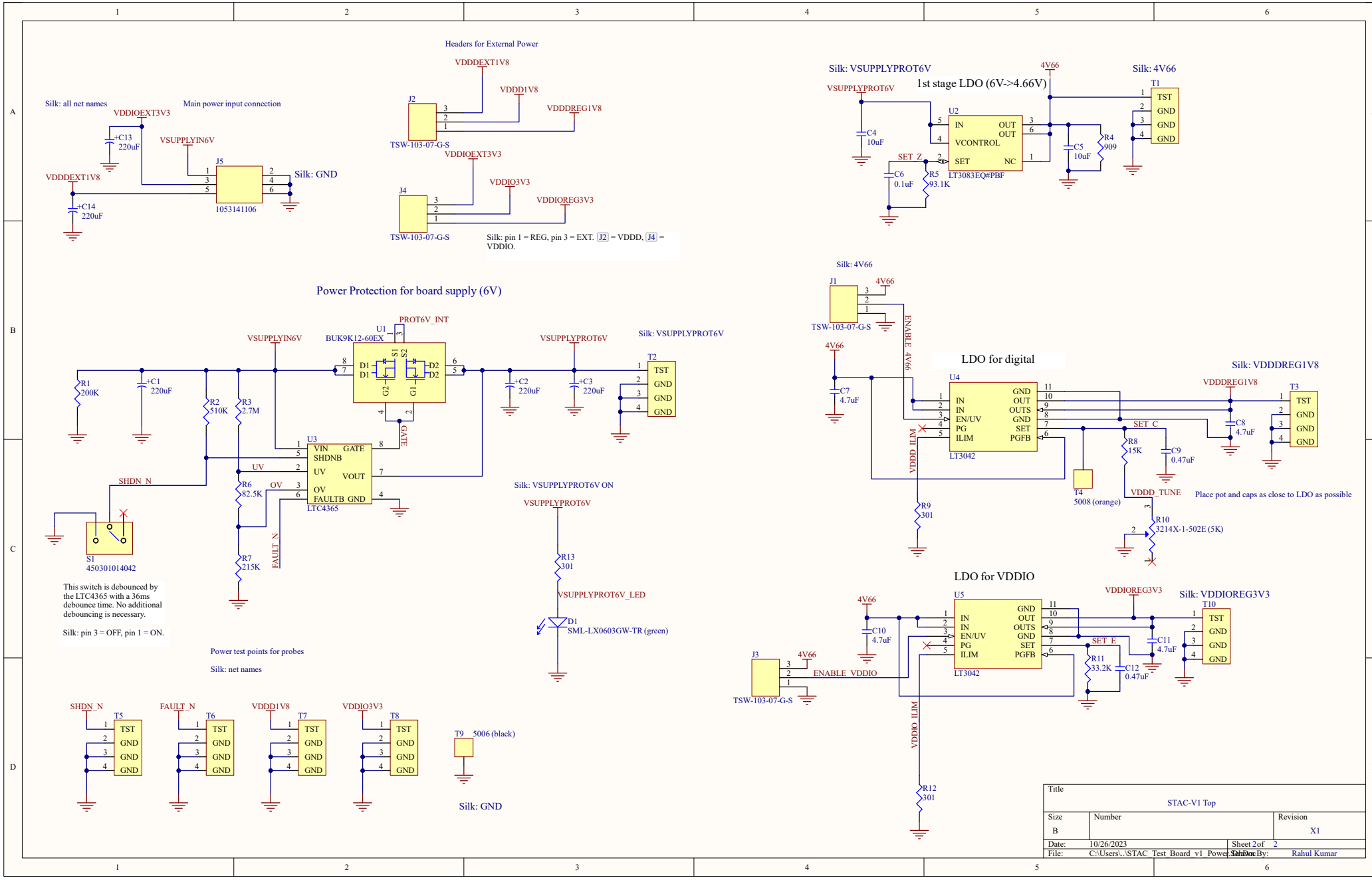

STAC_Power
STAC_Test_Board_v1_Power
SMA connectors
Silkscreen: signal names
NET CLASS SE50
clock_clock
J6
142-0701-801
All SMAs should be 50 ohm controlled impedance traces. TODO: do we need circuitry for resisitive SMA probes? (e.g. a 950 ohm resistor)
NET CLASS SE50
SRAM_SAE_CLK
J8
142-0701-801
NET CLASS SE50
PLL_DIV_OUT
J10
142-0701-801
NET CLASS SE50
PLL_REF_IN
J11
142-0701-801
NET CLASS SE50
PLL_CLK_OUT
J13
142-0701-801
PMOD for serial TL (use 0.1" pitch right angle thru hole male connector)
Silk: TILELINK
J7
serial_tl_bits_out_ready
serial_tl_bits_out_valid
serial_tl_bits_in_ready
serial_tl_bits_in_bits
serial_tl_clock
serial_tl_bits_out_bits
serial_tl_bits_in_valid
clock_clock
TSW-106-08-L-D-RA
Note that power is not connected via the PMOD; we think it may be simpler to not share supplies between this board and the FPGA connected to the other end of the PMOD. Power would normally be on pins 6 and 12 of the PMOD connector.
PMOD for SRAM control (use 0.1" pitch right angle thru hole male connector)
Silk: SRAM CONTROL
J9
SRAM_BIST_START
SRAM_EN
SRAM_BIST_EN
SRAM_EXT_EN
SRAM_SCAN_IN
SRAM_SCAN_OUT
SRAM_SCAN_EN
SRAM_BIST_DONE
TSW-106-08-L-D-RA
Note that SRAM_SCAN_MODE is omitted, since the PMOD can only carry 8 signals. We will set SRAM_SCAN_MODE via a jumper instead of via the FPGA.
0.1" headers
Silk: all pin names
J12
SRAM_SCAN_MODE
clksel_1
clksel_0
reset
VDDIO3V3
custom_boot
uart_0_txd
uart_0_rxd
TSW-108-07-L-D
J14
spi_0_dq_0
spi_0_dq_1
spi_0_dq_2
spi_0_dq_3
spi_0_cs_0
spi_0_sck
VDDIO3V3
VDDD1V8
JTAG_TCK
JTAG_TMS
JTAG_TDI
JTAG_TDO
TSW-108-07-L-D
J15
PLL_ARSTB
PLL_SCAN_CLK
PLL_SCAN_EN
PLL_SCAN_IN
PLL_SCAN_OUT
PLL_SCAN_RST
PLL_SEL
TSW-108-07-L-D
U6A
VSSA_W4
SRAM_SCAN_IN
SRAM_SCAN_OUT
SRAM_SCAN_EN
SRAM_BIST_DONE
NC_W9
uart_0_txd
uart_0_rxd
VDDA_W12
VSSD_W13
serial_tl_bits_out_ready
serial_tl_bits_out_valid
serial_tl_bits_in_ready
serial_tl_bits_in_bits
serial_tl_bits_out_bits
serial_tl_bits_in_valid
VDDIO_W21
VDDD_W22
NC_QFN19
VSSA_S1
reset
clock_clock
VSSD_S4
JTAG_TCK
JTAG_TMS
JTAG_TDI
JTAG_TDO
clksel[0]
VSSIO_S10
VDDA_S11
serial_tl_clock
spi_0_sck
TESTCHIP_STAC_v1
U6B
spi_0_cs_0
spi_0_dq_3
spi_0_dq_2
spi_0_dq_1
spi_0_dq_0
VSSA_E13
VSSD_E12
VDDA_E11
clksel[1]
PLL_SEL
PLL_SCAN_EN
PLL_SCAN_RST
PLL_SCAN_CLK
PLL_DIV_OUT
VDDA_DCO_E4
PLL_CLK_OUT
VDDD_E2
PLL_REF_IN
custom_boot
VSSA_N10
PLL_SCAN_IN
PLL_SCAN_OUT
PLL_ARSTB
VSSIO_N6
SRAM_EXT_EN
SRAM_BIST_EN
SRAM_EN
SRAM_SCAN_MODE
SRAM_BIST_START
SRAM_SAE_CLK
VDDD_W2
VDDIO_W3
THERMAL_GND_E21
TESTCHIP_STAC_v1
Note that the VDDA pins on the STAC chip are connected to VDDD1V8 . This is because no on-chip circuitry uses VDDA.
All caps close to chip package (1 cap per pin)
VDDD1V8
C15 10uF
C17 10uF
C21 10uF
C22 10uF
C18 10uF
C20 10uF
VDDIO3V3
C16 10uF
C19 10uF
SMA connector for cable to spectrum analyzer (using an SMA-connectorized DC blocking capacitor at the spectrum analyzer's input) for measuring noise on these power domains.
J16
J17
142-0701-801
Title
STAC-V1 Top
Size
B
Number
Revision
X1
Date: 10/26/2023
Sheet 1 of 2
File: C:\Users\..\STAC_Test_Board_v1.SchDoc
Drawn By: Rahul Kumar


Silk: all net names
Main power input connection
VDDIOEXT3V3
+C13 220uF
VSUPPLYIN6V
J5
VDDEXT1V8
+C14 220uF
1053141106
Silk: GND
Headers for External Power
VDDEXT1V8
VDDD1V8
VDDREG1V8
J2
TSW-103-07-G-S
VDDIOEXT3V3
VDDIO3V3
VDDIOREG3V3
J4
TSW-103-07-G-S
Silk: pin 1 = REG, pin 3 = EXT. J2 = VDDD, J4 = VDDIO.
Silk: VSUPPLYPROT6V
1st stage LDO (6V->4.66V)
4V66
Silk: 4V66
VSUPPLYPROT6V
C4 10uF
U2
IN
OUT
OUT
VCONTROL
SET
NC
LT3083EQ#PBF
SET_Z
C6 0.1uF
R5 93.1K
C5 10uF
R4 909
T1
TST
GND
GND
GND
Power Protection for board supply (6V)
PROT6V_INT
U1
BUK9K12-60EX
VSUPPLYIN6V
VSUPPLYPROT6V
Silk: VSUPPLYPROT6V
R1 200K
+C1 220uF
R2 510K
R3 2.7M
D1
D1
D2
D2
S1
S2
G2
G1
GATE
+C2 220uF
+C3 220uF
T2
TST
GND
GND
GND
U3
VIN
GATE
SHDNB
UV
VOUT
OV
FAULTB
GND
LTC4365
SHDN_N
UV
OV
R6 82.5K
R7 215K
FAULT_N
S1 45030101404 2
This switch is debounced by the LTC4365 with a 36ms debounce time. No additional debouncing is necessary.
Silk: pin 3 = OFF, pin 1 = ON.
Silk: VSUPPLYPROT6V ON
VSUPPLYPROT6V
R13 301
VSUPPLYPROT6V_LED
D1 SML-LX0603GW-TR (green)
Power test points for probes
Silk: net names
SHDN_N
FAULT_N
VDDD1V8
VDDIO3V3
T5
T6
T7
T8
TST
GND
GND
GND
T9 5006 (black)
Silk: GND
Silk: 4V66
J1
4V66
TSW-103-07-G-S
ENABLE_4V66
4V66
C7 4.7uF
LDO for digital
U4
IN
IN
EN/UV
PG
ILIM
GND
OUT
OUTS
GND
SET
PGFB
LT3042
VDDD_ILIM
R9 301
T4 5008 (orange)
SET_C
R8 15K
C9 0.47uF
VDDD_TUNE
R10 3214X-1-502E (5K)
Silk: VDDDREG1V8
VDDDREG1V8
C8 4.7uF
T3
TST
GND
GND
GND
Place pot and caps as close to LDO as possible
LDO for VDDIO
U5
4V66
C10 4.7uF
J3
4V66
TSW-103-07-G-S
ENABLE_VDDIO
VDDIO_ILIM
R12 301
VDDIOREG3V3
Silk: VDDIOREG3V3
T10
TST
GND
GND
GND
C11 4.7uF
SET_E
R11 33.2K
C12 0.47uF
Title
STAC-V1 Top
Size
B
Number
Revision
X1
Date: 10/26/2023
Sheet 2 of 2
File: C:\Users\..\STAC_Test_Board_v1_Power.SchDoc
Drawn By: Rahul Kumar