RAHUL KANDE

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EDUCATION

Texas A&M University, College Station, Texas — May 2018 - Present
Ph.D. in Computer Engineering — GPA: **3.89** on scale of **4**

Indian Institute of Technology, Guwahati, India — May 2013 – May 2017
Bachelor of Technology in Electronics and Communication Engineering — GPA: **8.91** on scale of **10**
(Minor in Computer Science and Engineering)

Related Coursework :

Advanced Computer Architecture	Advanced Design Verification	Intro. to Formal Verification
Microarchitecture Prediction	Microprocessor System Design	Software Security
Secure Computer Systems and Arch	VLSI laboratory	Design Laboratory

TECHNICAL SKILLS

Languages: Verilog, C, C++, Python, Shell script
Methodologies: Universal Verification Methodology (UVM)
Tools: vcs (Synopsis), Modelsim (Siemens), irun (Cadence), Jaspergold (Cadence), Vivado (Xilinx)

PUBLICATIONS

- C. Chen, **R. Kande**, N. Nguyen, F. Anderson, A. Tyagi, A.-R. Sadeghi, and J. Rajendran, *HyPFuzz: Formal-Assisted Processor Fuzzing*, USENIX Security Symposium'23 **(Prev. year acceptance rate: 18%)** (Accepted)
- **R. Kande**, A. Crump, G. Persyn, P. Jauernig, A.-R. Sadeghi, A. Tyagi, and J. Rajendran, *TheHuzz: Instruction Fuzzing of Processors Using Golden-Reference Models for Finding Software-Exploitable Vulnerabilities*, USENIX Security Symposium'22 (**Acceptance rate: 18%**)
- A.-R. Sadeghi, J. Rajendran, **R. Kande**, C. Chen, A. Tyagi, P. Jauernig, and P. Mahmoody, *Organizing The World's Largest Hardware Security Competition: Challenges, Opportunities, and Lessons Learned*, in the Proceedings of the 2021 on Great Lakes Symposium on VLSI, pp. 95-100
- C. Chen, **R. Kande**, J. Rajendran, A.-R. Sadeghi, *Trusting the Trust Anchor: Towards Detecting Cross-Layer Vulnerabilities with Hardware Fuzzing*, in 2022 59th ACM/IEEE Design Automation Conference (DAC)

EXPERIENCE

Hardware Security Group, Texas A&M University — Sept. 2018 – Present
Guide: Dr. Jeyavijayan Rajendran, Department of Electrical and Computer Engineering
Graduate Research Student

- I am developing hardware fuzzing tools to detect security vulnerabilities in processor designs.
- As an organizer of Hack@EVENT, a set of hardware security CTF competitions (1000+ participants so far), I added security features (like AES crypto engine, register locks and FUSE memory) and inserted more than 200 security bugs in open source RISC-V SoCs like Ariane, OpenPiton, and OpenTitan.

Intel, Hillsboro, Oregon — Dec. 2020 – May 2021
Intern as Offensive Security Researcher

- Worked in the Offensive Security Research (OSR) team of the Intel Product Assurance and Security (IPAS) organization.
- Developed an automated static analysis tool to aid the design and verification engineers in detecting the vulnerabilities in the reset logic of Intel processors using Synopsys Verdi Interoperable Apps (VIA) interface.

Samsung Research Institute, Delhi, India — July 2017 – Aug. 2018
RTL Design and Verification Engineer

- CODEC IP project:
  - Enhanced the Verilog RTL design to reduce the design area. The gate count has been reduced by 10%.
  - Upgraded a bash script and a Verilog based test bench to automate the process of design verification.
- Security IP project:
  - Modified a C model of the IP to obtain a reference model for verification.
  - Developed a UVM based verification environment to verify the IP; Identified the functional coverage points, generated the corresponding test cases and verified the IP for all the test cases.

Department of Electronics and Communication Engineering, IIT Guwahati July 2016 – May 2017
Undergraduate Research Student

- Designed a 5-stage 32-bit Microprocessor with support for Co-processor, burst mode memory transfer, separate Instruction and Data cache, branch prediction and early branch evaluation.
- Verified the working of the processor design on a Xilinx based Virtex-6 FPGA evaluation kit for 100 programs each having 50-100 instructions.

Semi-Conductor Laboratory, Punjab, India May 2016 – June 2016
Intern

- Developed a hardware design IP for the UDP and Ethernet internet protocols with support for ARP protocol and an internal cache for temporary MAC address storage using Xilinx ISE Design and simulation tool.

AWARDS & ACHIEVEMENTS

- Third place, in Hardware Demonstration, IEEE Hardware Oriented Security and Trust, 2022.
- IEEE Hardware Oriented Security and Trust Student Travel Grant in 2020, 2022, and 2023.
- ACM/IEEE Design Automation Conference, Young Fellowship award in 2020 and 2021.
- USENIX Security Symposium Student Grant award in 2020 and 2021.
- ACM/IEEE Design Automation Conference, best Research Video Award in 2020.
- Department Graduate Merit scholarship, TAMU 2018.
- Qualified the 'Professional' programming test organized by Samsung (Only around 20% of the Samsung employees are Professional qualified world-wide).

TALKS/TOOL DEMONSTRATIONS/WORKSHOPS

- *TheHuzz, Hardware Fuzzer to Detect Security Vulnerabilities in Processors*, poster presentation at the Network and Distributed System Security Symposium (NDSS), 2023.
- *TheHuzz, Hardware Fuzzer to Detect Security Vulnerabilities in Processors*, CAD Tool Demo at 1st edition of CAD4SEC Workshop, 2022.
- *TheHuzz, Hardware Fuzzer to Detect Security Vulnerabilities in Processors*, Hardware Demonstration at IEEE Hardware Oriented Security and Trust, 2022.
- *Insights and Lessons Learnt during Hack@DAC 2021*, special session, ACM/IEEE Design Automation Conference, 2022.

LEADERSHIP & ACTIVITIES

Mentorship Activities at Texas A&M University

- Assisted a junior PhD student, Aneesh Dixit, with setting up the FPGA experiments for his project.
- Assisted masters students, Georges Alsankary, Arjun Muralidharan, and Garrett Persyn with their thesis projects on fuzzing processors to detect security vulnerabilities.
- Mentored an undergraduate student, Nicholas Heinrich-Barna, with the "PLC Fuzzing" and "Black-box Fuzzing" projects.

Academic Activities at Texas A&M University

Assisted my advisor with teaching and managing the *Hardware Security* and *Introduction to Digital Design* courses during Fall'19, Spring'20, Spring'21, Fall'21, and Fall'22.

- Designed class projects *Logic Locking Processors*, *Identifying Hidden Instructions in Processors*, & *Hardware Fuzzing;* class demonstrations *Hacking into coffee-maker* & *Exploiting the vulnerabilities in hardware designs.*

- Mentored 50+ undergraduate and graduate students.

Samsung Research Institute Aug. 2017 – Aug. 2018

Great Work Place (GWP) Agent

- Planned and organized various fun and team building activities on monthly and quarterly basis aimed to make Samsung a better work place.

Indian Institute of Technology, Guwahati April 2015 – April 2016

Head of Entrepreneurship Development Cell

- Lead a team of around 150 members to organize various lecture series and workshops in our campus including *UDGAM*, the Annual E-summit of IIT Guwahati.
- Organized TEDx for the first time in IIT Guwahati along with a team of Post Graduate students.

SERVICE

- Volunteer at Aggieland Humane Society, TX, USA Dec. 2022 to Present
- Member of National Sports Organization (NSO), Athletics.
- Volunteered in LED (Learn.Explore.Discover) an initiative by the Annual Tech Festival of IITG in which we demonstrated simple experiments to the school students nearby our campus so as to explain them the basic principles of science.
- Volunteered as a member of Academic Initiatives club of our college to conduct remedial classes for the freshers of our department.

WORK AUTHORZATION

Eligible to work in the U.S for a period of 12 months under Curricular Practical Training (CPT) program.