Rahul Karthik Sunder

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Education

Texas A&M University, College Station, Texas May 2027
Master of Science in Computer Engineering | GPA: 3.67/4
Coursework: Digital Integrated Circuit Design, Computer Architecture, Intro to Hardware Design Verification, Advanced Hardware Design Verification, Formal Verification, Microprocessor System Design.

Vellore Institute of Technology, Chennai, India May 2025
Bachelors of Technology in Electronics and Communication Engineering | GPA: 8.67/10
Coursework: Digital System Design, Analog Circuits, VLSI System Design, Microprocessor and Microcontrollers, Artificial Intelligence and Machine Learning.

Skills

Technical Skills: RTL to GDSII Flow, FPGA Prototyping, High-Speed Digital Logic, Microarchitecture, Circuit Design, Design For Test, Pre and Post-Silicon Verification.
Design Verification: UVM, Assertions (SVA), Verification Planning, Constrained Random Verification, Coverage Analysis, Scoreboard and Monitors.
Formal Verification: Model Checking, Property Specification, Safety and Liveness Properties
Physical Design: Logic Synthesis, Floorplanning, Placement, CTS, Routing, Setup & Hold Analysis, Slack Analysis, Timing Closure, OCV/AOCV, Clock Skew & Latency, PPA Optimization.
Programming and Scripting: Verilog, SystemVerilog, C/C++, Python, Perl, Tcl, Shell Scripting.
EDA and Simulation Tools: Cadence (Virtuoso, Genus, Innovus, Xcelium, Liberate), Synopsys (Design Compiler, PrimeTime, HSPICE), Siemens (Calibre DRC/LVS), Xilinx Vivado, ModelSim.

Projects

Evaluation of Modern Cache Replacement Policies, *ZSim Simulator* Nov 2025 - Dec 2025
- Implemented LRU, LFU, SRRIP, CARE and IPV cache replacement policies into the ZSim simulator and evaluating using SPEC CPU2006 (single-threaded) and PARSEC (multi-threaded) benchmarks.
- Analyzed performance metrics (Cycles, IPC, MPKI) to evaluate CARE and IPV and compare them against baseline policies (LRU, LFU, SRRIP), highlighting improvements in cache utilization and miss reduction across diverse workloads.

Cruise Control ASIC Design & Implementation, *Synopsys Design Compiler, Primetime, Cadence Innovus* Nov 2025 - Dec 2025
- Performed RTL logic synthesis of a cruise control design using Synopsys Design Compiler, targeting a 180 nm standard-cell library, and generated a synthesized Verilog netlist for downstream implementation
- Conducted pre-layout Static Timing Analysis (STA) using Synopsys PrimeTime by defining clock, input/output delay, drive strength, and load constraints, and analyzed setup and hold timing paths using timing reports
- Executed automatic Place and Route using Cadence Innovus, including floorplanning, power ring and stripe creation, standard-cell placement, and timing-driven routing
- Performed parasitic extraction (SPEF) and evaluated physical design metrics such as total wirelength, number of vias, and standard-cell count.

Design Verification of HTAX Specification, *Cadence Xcelium* Sep 2025 - Dec 2025
- Created a UVM-based verification environment in SystemVerilog for a HTAX specification with Cadence Xcelium and SimVision.
- Developed multiple constrained-random and directed sequences, SystemVerilog assertions, scoreboards, and functional coverage models, achieving 100% functional coverage.
- Created verification test plans and executed multi-test regressions using Cadence vManager, debugging DUT failures through waveform and assertion analysis.

Design of RISC Processor using Sub-Threshold Standard Cells, *Cadence* Dec 2024 - Apr 2025
- Applied Symmetry Matching and Current-to-Capacitance Ratio (CCR) optimization techniques for transistor sizing, achieving power consumption as low as 0.874 μW and 1.20 μW across two approaches.
- Built and tested 30 custom standard cells (Inverter, MUX, DFF, XOR etc.) and performed parasitic extraction using Calibre.
- Characterized the custom standard cell library with CCS and ECSM models across different process corners and synthesized the RTL design to achieve optimized area and robust timing performance.

RTL Design and Implementation of an 8-bit RISC CPU, *ModelSim* Jul 2024 - Nov 2024
- Engineered an 8-bit RISC CPU in Verilog HDL with single-cycle execution.
- Integrated ALU, Program Counter, Memory, Decoder, Accumulator and validated functionality in ModelSim.
- Executed core arithmetic, logic, and memory instructions efficiently utilizing RISC principles.