COA - Quiz 1 (CSN 221 - CAM Aut 2020-21)

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Q.1. Size of ISA = 12

⇒ We need 4 bits to store all opcodes.

Total of 64 registers = (2^6)

⇒ 6 bits for representing a register

⇒ Memory for 1 instruction = 4 + 6 + 6 + 6 + 12

= 34

= 34/8 bytes

= 4.25 bytes

⇒ 1 instruction takes 5 bytes

100 instructions ⇒ **500 bytes**

Q.2. Size of instruction format = 2 bytes (given)

= 16 bits

→ Total encodings = 2^{16}

16 integer regs ⇒ 4 bits $(=2^4)$

64 float regs ⇒ 6 bits (2^6)

⇒ Used encodings-

Type 1: $4 \times (2^4)^3 = 2^{14}$

Type 2: $8 \times (2^6)^2 = 2^{15}$

Type 3: $14 \times (2^4)(2^6) = 7 \times 2^{11}$

⇒ Encodings for Type 4 = $2^{16} - [2^{15} + 2^{14} + 7 \times 2^{11}]$

$= 2^{11}[32 - 16 - 8 - 7]$

$= 2^{11}$

∴ Total no. of instructions of type 4 = $\frac{2^4}{2^6} = 2^5 = 32$.

$N_{max} = 32$

Q.3 → Iconic feature of RISC machine is having a branch delay slot.

→ Also, RISC has reduced number of addressing modes. (Not an iconic feature)

→ RISC needs more memory

⇒ Option: (C) : Having a branch delay slot.

Q.4. RISC is more complicated than CISC : False

Since CISC has more transistors.

Option: (b) → False

Q.5. Option (B) : RISC

Q.6. Option (B) → RISC

Hence the name "Reduced" Instruction Set Computer.

Q.7. CISC = Complex Instruction Set Computer

Option (D)

Q.8. Both the CISC & RISC have been developed to—

→ Semantic gap – between high & low level language.

Option (C) → Semantic gap

Q.9. Motorola A567

Option(d)

Q.10. Pipelining is a unique feature of

Option (A) → RISC

Q.11. In CISC architecture most of the complex instructions are stored in Transistors.

Option (D)

Q.12. Which of these is power efficient?

Option (B) – RISC

Q.13. All of the above are used in the design of a RISC processor

⇒ Option (D) → I, II & III

Q.14 All of the above

Option (D) → a, b, c, d

Q.15 Option (C): Both I & II are true.

Q.16 All belong to RISC family.

→ Option (D): All of the above

Q.17. A bus cycle request that transfers to or from an address which is unrelated to the address used in preceding cycle is called a Non-sequential cycle.

Option: (C)

Q.18.

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ADDS r4, r0, r2;
ADCS r5, r1, r3;
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Option (B)

Q.19. Option (B): It may halt by changing the input.

Q.20. → All of I, II & III are correct about a Turing Machine. None of the given options satisfy.

Answer: None of these

Q.21. **Option (D): Initiation of interrupt service**

1st inst. → PC ⇒ MBR

2nd instr → add. of X → MAR

3rd instr → add. of Y → PC (Interrupt sequence initializes)

4th instr → (old PC values → Memory

Q.22. **Option (D) → 2 kbits**

No. of combinations = $2^4 \times 2^4 = 2^8$

o/p = 8 bits

Total ROM = $2^8 \times 8 = 2^{11}$ = 2k bits

Q.23. **Option (C): Memory address register.**

Q.24 **Option (D): Memory Data Register**

Q.25 **Option (D): Accumulator**

Q.26. B = input ⇒ TM halts

⇒ TM never halts in case of $(0+1)^+$.

⇒ **Option (A) ⇒ M does not halt on any string in $(0+1)^+$**
