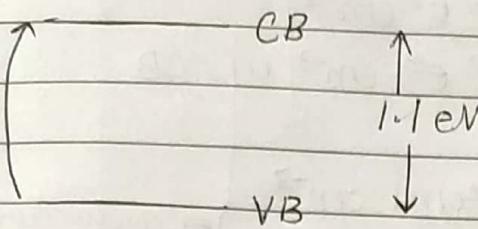


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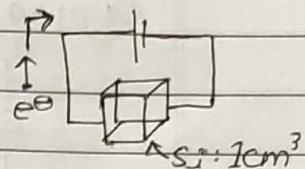
Silicon



e^- jumps from VB to CB at room T by acquiring reqd. energy, creating holes in VB

In conduction band @ room T, there are $\sim 1.5 \times 10^{10} \text{ cm}^{-3} e^-$ in silicon.

$$\boxed{\begin{matrix} \# e^- \\ \text{in CB} \end{matrix} = \begin{matrix} \# \text{ holes} \\ \text{in VB} \end{matrix}}$$



- e^- immobile in VB (attached to atom)
- e^- mobile in CB, and conduct electricity.

Si (semiconductor)

- $5 \times 10^{22} \text{ atoms/cm}^3$
- CB e^- : $1.5 \times 10^{10} \text{ cm}^{-3}$ \ll current very low (compared to conductor)

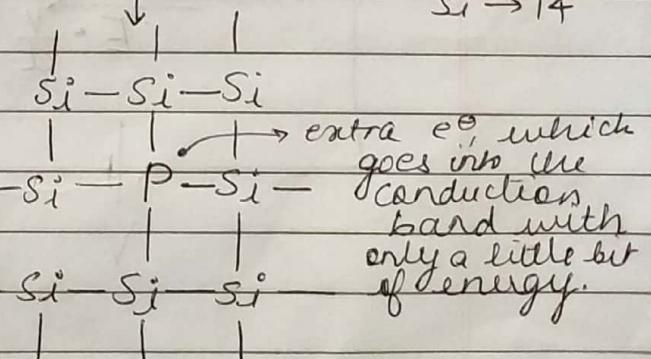
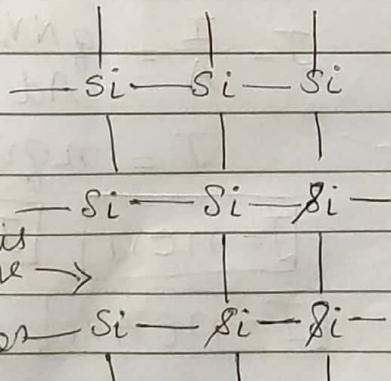
Al (conductor)

- $5 \times 10^{22} \text{ atoms/cm}^3$
- CB e^- : $5 \times 10^{22} \text{ cm}^{-3}$

Doping using P

Intrinsic Silicon \rightarrow introduce P atom

P \rightarrow 15
Si \rightarrow 14



suppose this
 e^- has gone
into the
conduction
band

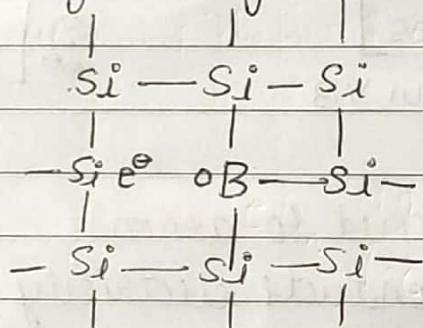
Holes are faster
than electrons

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without P: 5×10^{22} Si atoms cm^{-3}
 $\hookrightarrow 2 \times 10^{23} e^{\circ} \text{cm}^{-3}$
 $\hookrightarrow 1 \times 10^{10} e^{\circ} \text{cm}^{-3}$ in CB

w/ P: 10^{16} P atoms cm^{-3}
 $\hookrightarrow 10^{16} e^{\circ} \text{cm}^{-3}$ in CB \Rightarrow conductivity ↑

Doping using B



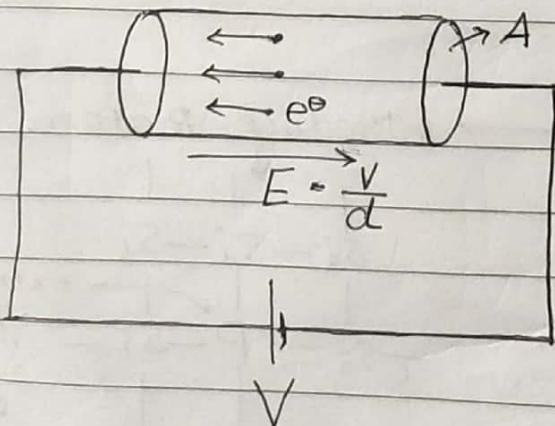
Hole is created due to lack of e°
 number of holes are same as above.

$$E = \frac{V}{d}$$

$$V_d = \mu E$$

↑ mobility
drift velocity

n = doping conc',
or, # of e° /vol^m
in device.



$$I = \frac{Q}{t} = \frac{q N V_d}{d}$$

$$J = \frac{I}{A} = \frac{q N V_d}{A d}$$

$$J = n q v_d$$

$$J = n e v_d$$

$$J = n e \mu E$$

$$[I = n e A v_d]$$

Holes are slower than free e^-

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$$J = neV_d$$

$$V_d = -UE$$

$$J = neUE$$

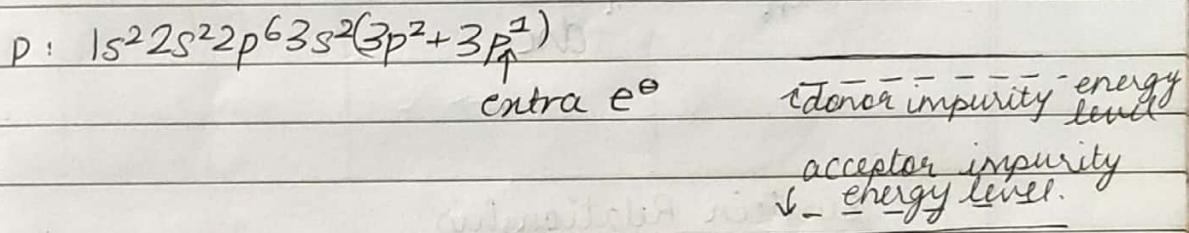
$$J = \sigma E \Rightarrow \sigma = neU$$

$$\sigma_{\text{total}} = neU_n + peU_p \quad (e \text{ is charge of } e^-)$$

$$10^{15} \leq n \leq 10^{17} \text{ (generally)} \quad J_{\text{drift}} = (neU_n + peU_p)E = \sigma E$$

↑ conc' of holes
and electrons

** All electrons donated by phosphorus in silicon will have a same and unique energy level known as donor energy level.



Fermi Level

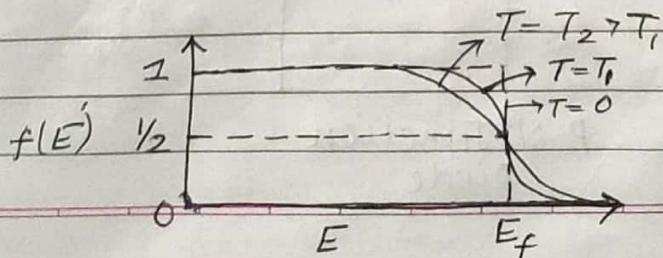
↳ Energy level below which all bands are filled and above which all bands are empty at 0K.

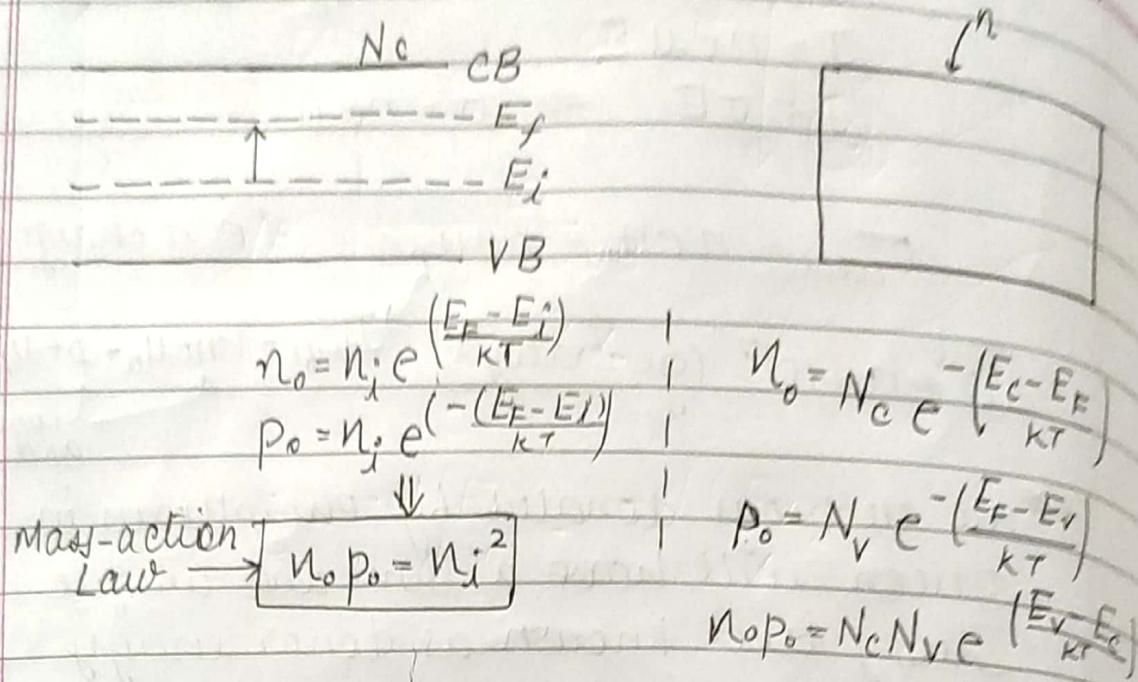
↳ Probability of finding an e^- is $1/2$ at fermi level

$$f(E) = \frac{1}{1 + e^{\frac{E-E_f}{kT}}} \quad \left. \begin{array}{l} \text{Probability of finding} \\ \text{electron at energy} \\ \text{level } E \text{ and temperature } T \end{array} \right\}$$

E_f = Fermi Level.

$$@ E = E_f, T = \text{anything} : f(E) = 1/2$$



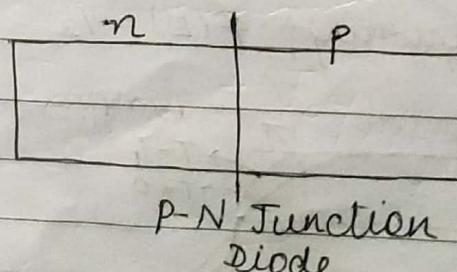
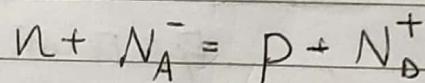


$$J_{\text{diff}} = e D_n \frac{dn}{dx}$$

Einstein Relationship

Diffusivity $\rightarrow D_n = \frac{D_p}{\mu_p} = V_T = 258 \text{ meV}$ at 300K / room T.

- Mass Action Law
- Einstein Relationship
- Drift current, diffusion current

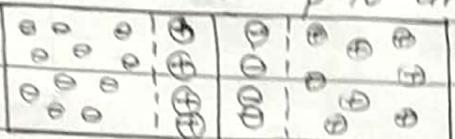


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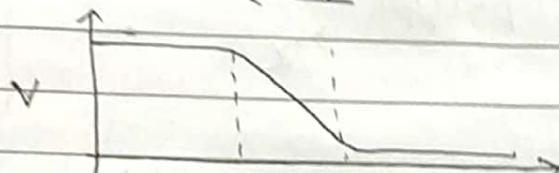
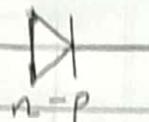
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Junction Diode $\rightarrow \vec{E}$

$$n = 10^{15} \text{ cm}^{-3} \quad p = 10^{15} \text{ cm}^{-3}$$

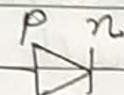


diffusion
drift



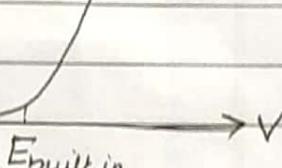
Junction (Depletion region)

Voltage drop @ junction = Junction Potential / Built-in potential
 $\approx 0.6 - 0.7 \text{ V for Si}$



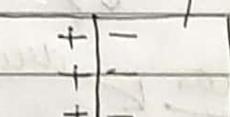
Forward Bias, $p \rightarrow +, n \rightarrow -$

$I \uparrow$



E_{built-in}

+ | -
 V_F

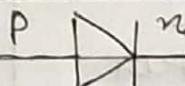


when $E_{ext} = E_j^n$,

large current is allowed to flow.

$E_j^n \approx 0.6 - 0.7$

$E_{ext} \approx (Si)$



Neg Reverse Bias

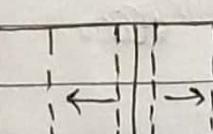
$I \leftarrow$ Breakdown voltage

Reverse saturation current
(due to minority charge carriers)

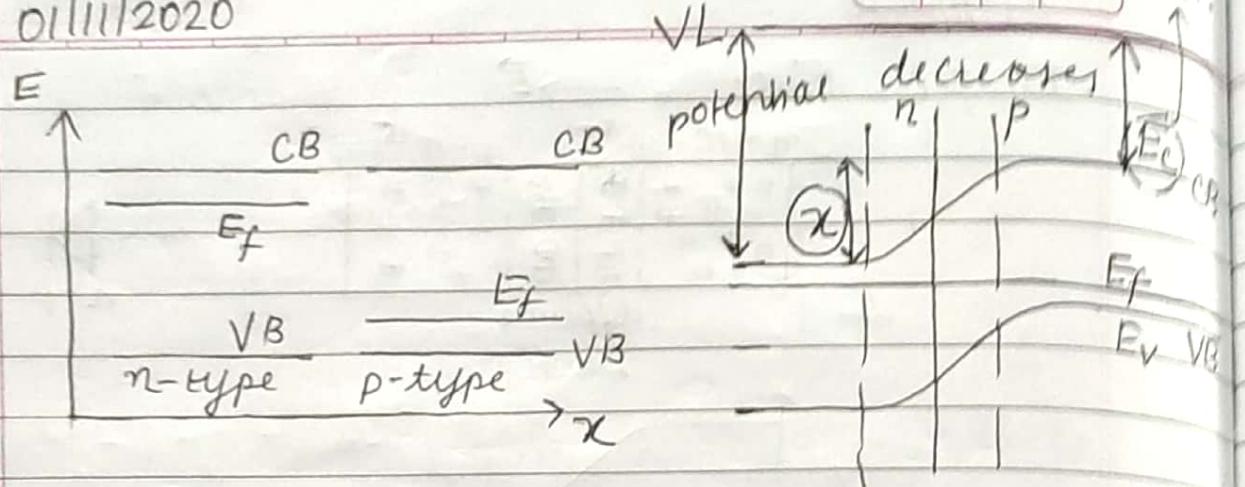
- | +
 V_R

At first, as we increase V , size of depletion region increases such that $\frac{V_1}{d_1} = \frac{V_2}{d_2}$ such that E remains constant.

When d reaches its maximum limit, E increases, causing breakdown.



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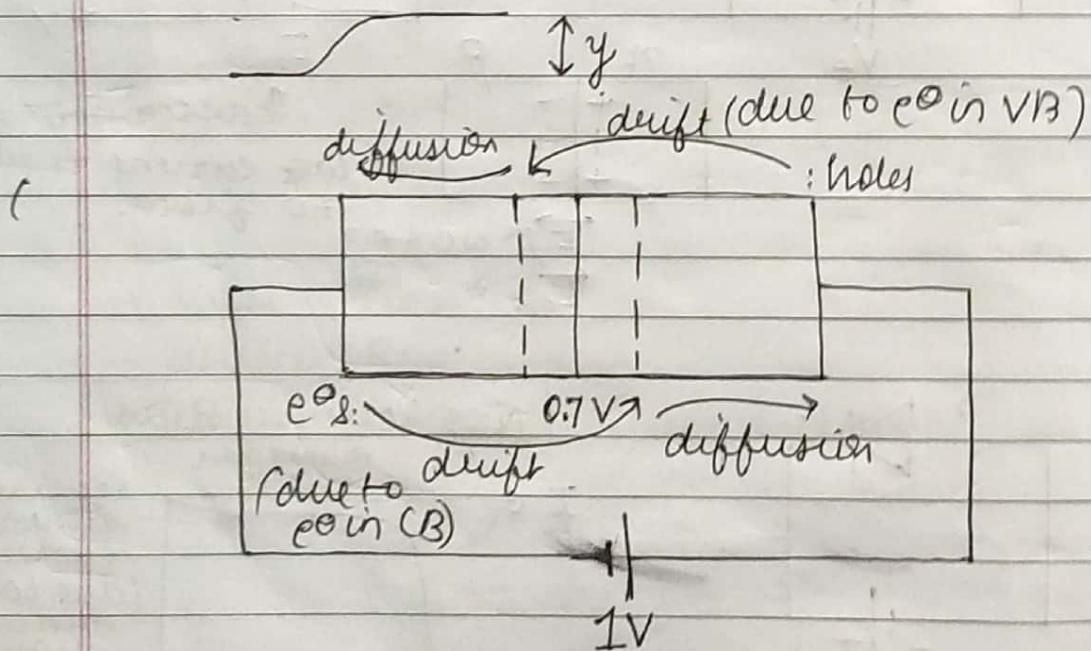


$$\epsilon = -\frac{d(E_c)}{dx} = -\frac{d(E_v)}{dx}$$

x : junction potential without bias

y : junction potential with fwd. bias

$$y \ll x$$



$$J = J_{e^-/\text{drift}} + J_{e^-/\text{diffusion}}$$

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Let I_o = reverse saturation current

$$I = I_o (e^{\frac{V}{nV_T}} - 1) \quad \text{Shockley's Equation}$$

V_T = thermal voltage $\approx 25.8 \text{ mV}$ $\Rightarrow \frac{kT/q}{V_T} = \frac{T}{11600}$

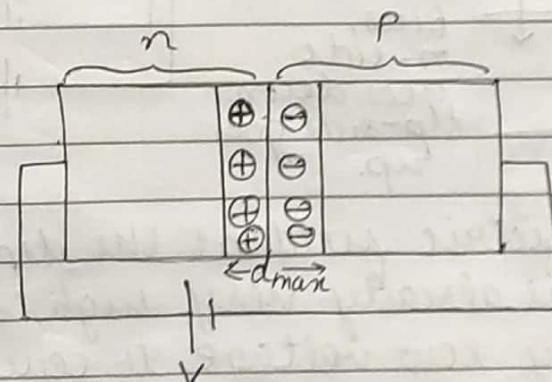
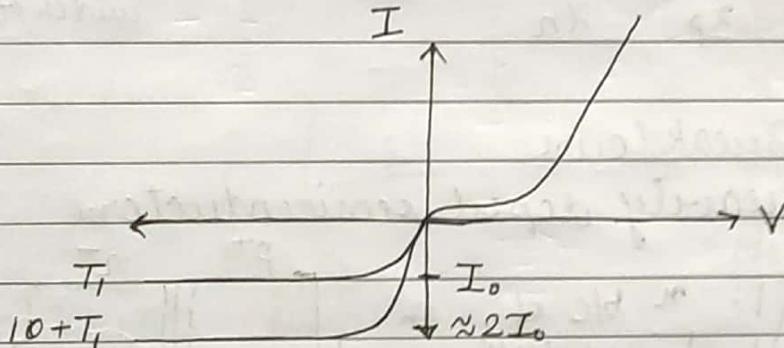
n = ideality factor = 1 for Ge, 2 for Si.
"best value"

$$I_o \approx 10^{-10} \text{ A (generally)}$$

Temperature Dependence of V/I characteristics

The reverse saturation current approximately doubles every time we increase the current by 10°C .

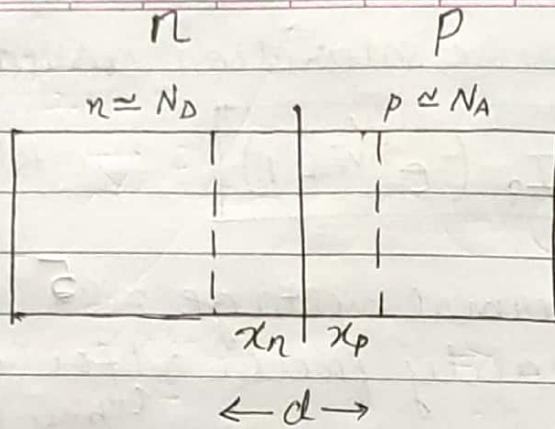
$$I_s(T) = I_{s1} (2^{\frac{T-T_1}{10}})$$



"Avalanche Breakdown"
when V passes d_{\max} ,

01/13/2019

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If $N_D > N_A \Rightarrow x_p > x_n$ and vice versa

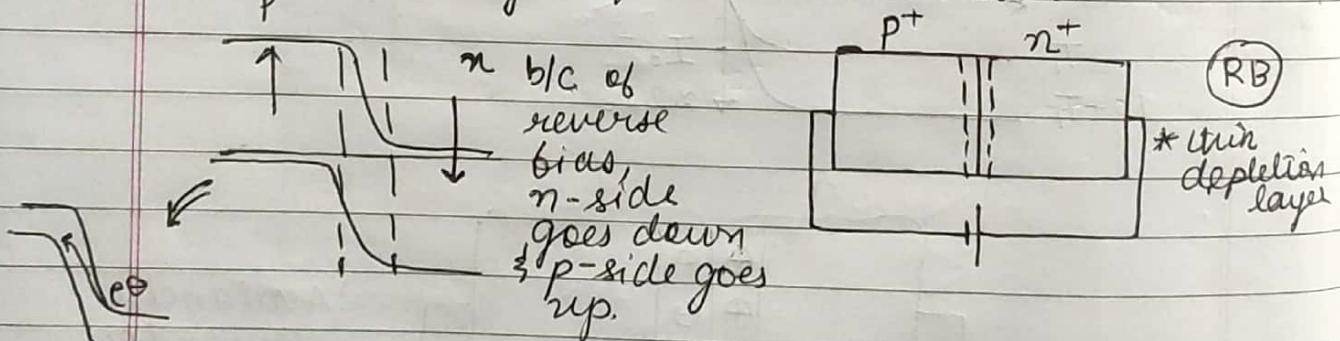
because, if doping concentration is less, the same number of majority charge carriers will take more space than the side with higher doping concentration

$$\Rightarrow \frac{N_D}{x_p} = \frac{N_A}{x_n} \quad \text{and} \quad x_p + x_n = d$$

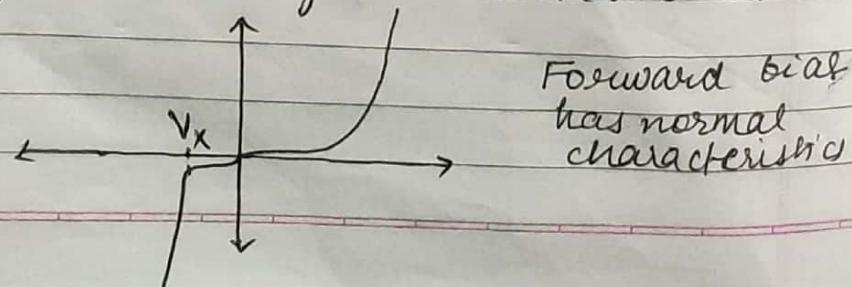
width of depletion layer.

Zener Breakdown

For heavily doped semiconductors



The electric field at the depletion layer is already very high, so it takes a very low voltage to cause a breakdown.

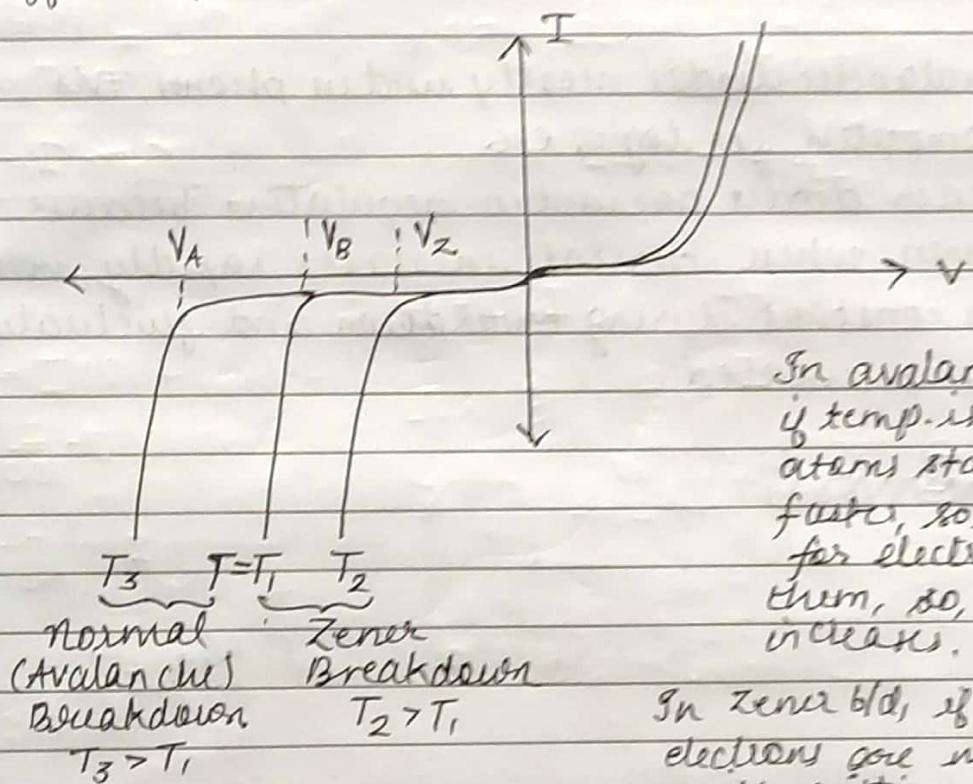


01/13/2019

* Avalanche breakdown is harmful because you are forcing the electrons to be pulled out of the valence band. \Rightarrow CAUSE PERMANENT DAMAGE TO ATOMS *

* Zener breakdown is safe because the diode is heavily doped

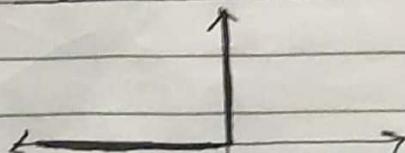
Effects of Temperature on Zener Breakdown



In avalanche b/d, if temp. is increased, atoms start to oscillate faster, so it is harder for electrons to hit them, so, B/D voltage increases.

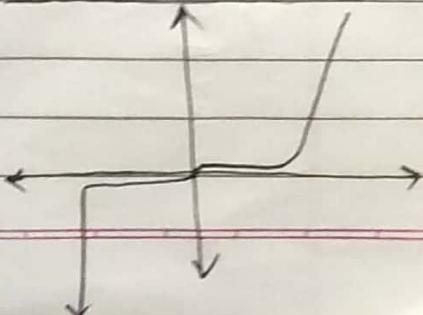
In Zener b/d, if temp. is ↑, electrons are not concerned with hitting atoms, so it helps cross the barrier, decreasing the voltage.

Ideal Diode

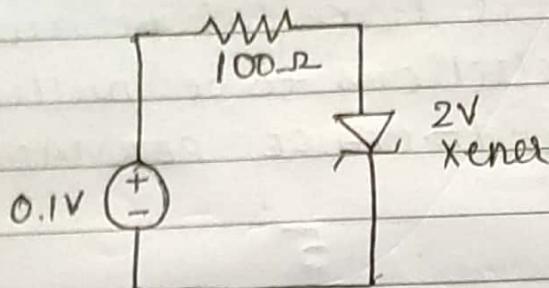


FB: short circuit
RB: ∞ Resistance

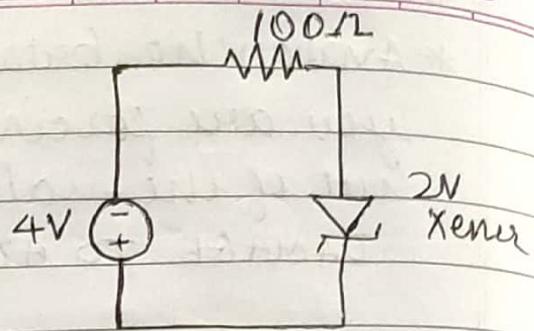
Practical Diode



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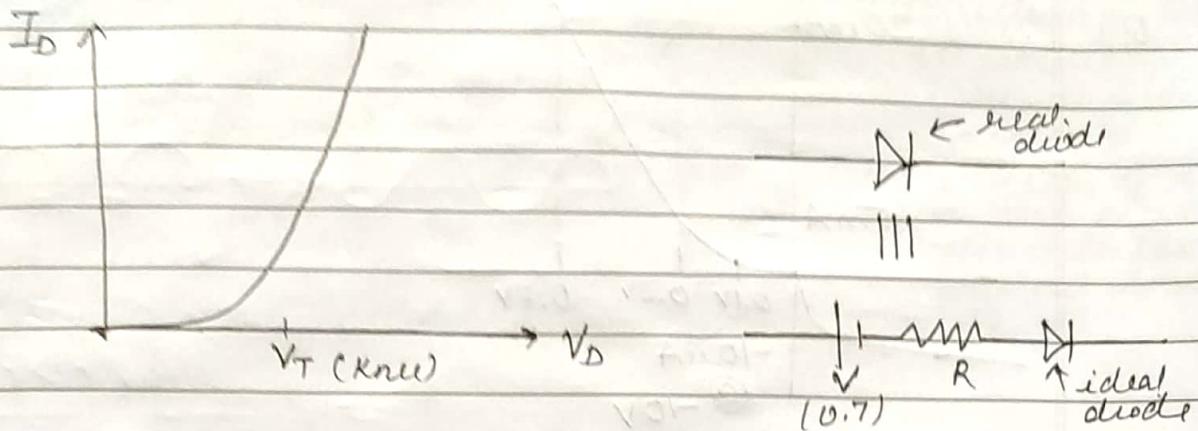
Zener diode behaves like an ideal diode in FWD Bias



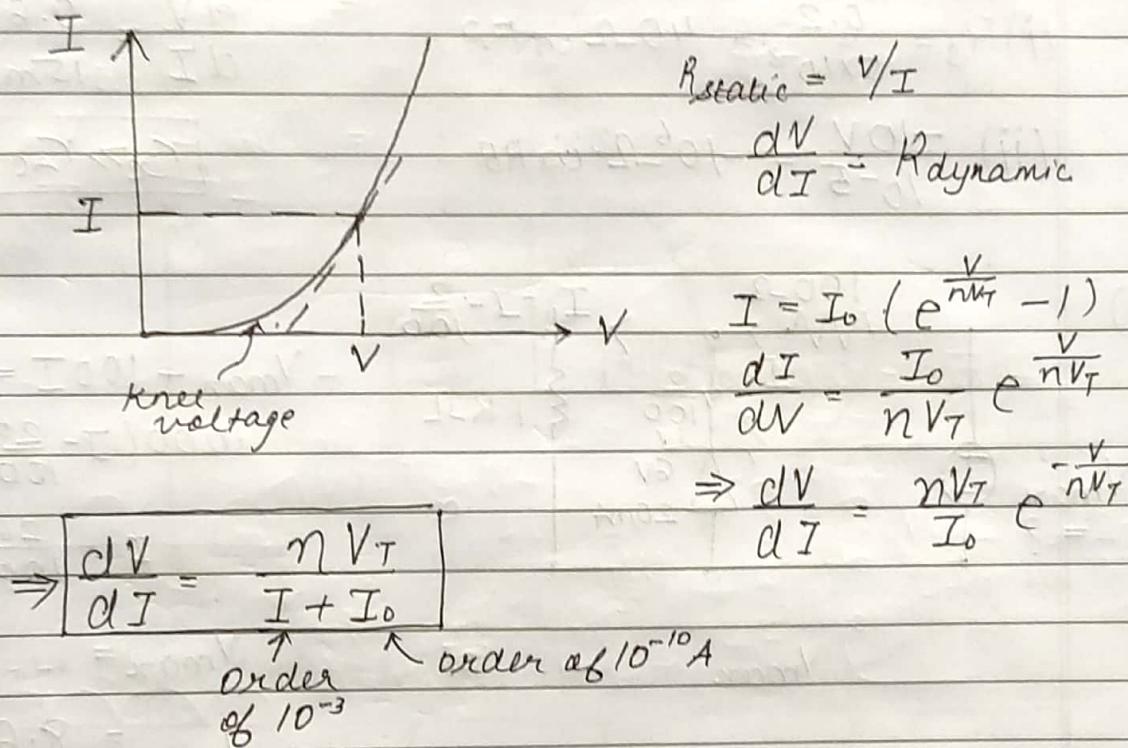
$\Rightarrow 2V$ drop across Xener
b/c $4V > 2V$ in REVERSE
BIAS $\Rightarrow 2V$ drop across
resistance $\Rightarrow i = 20mA$.

- Avalanche diodes mostly used in phones, TVs, computers, for logic, etc.
- Zener diodes are used in regulators because even when current increases rapidly, voltage is constant during breakdown and fluctuation is prevented.

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Diode Resistance: Static and Dynamic



$$\Rightarrow \left[\frac{dV}{dI} = \frac{nV_T}{I + I_0} \right] \quad \begin{matrix} \uparrow \text{order} \\ \text{of } 10^{-3} \end{matrix} \quad \begin{matrix} \nwarrow \text{order of } 10^{-10} \text{ A} \\ \text{of } 10^{-3} \end{matrix}$$

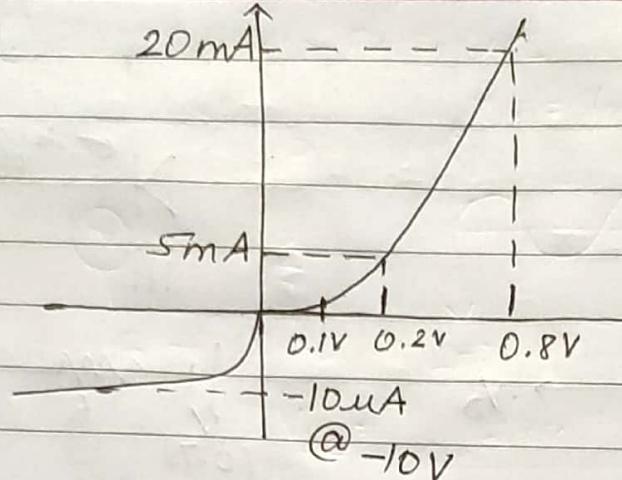
$$\frac{dV}{dI} = R_d \approx \frac{nV_T}{I} \rightarrow (\text{AC resistance})$$

* capacitor blocks DC voltage *

$$\text{For Ge: } n=1 \Rightarrow R_d \propto \frac{V_T}{I} = \frac{26}{I} \text{ m}\Omega$$

01/14/2020

Q)



DC Resistance

$$(i) R_s = \frac{0.2}{5 \times 10^{-3}} = 40 \Omega \text{ in FB}$$

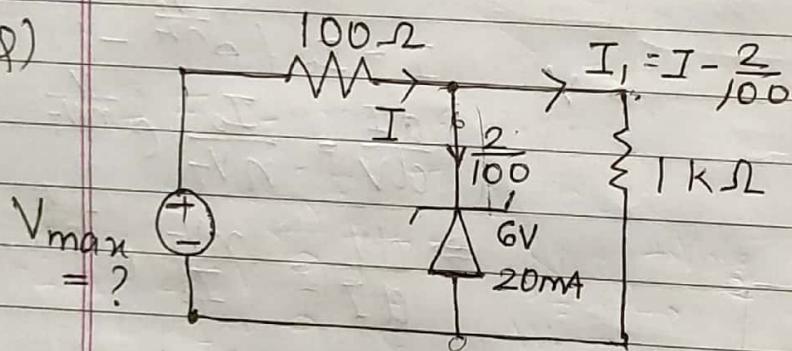
$$(ii) \frac{-10V}{10^{-5}} = -10^6 \Omega \text{ in RB}$$

AC Resistance

$$\frac{dV}{dI} = \frac{0.6V}{15mA} = 40 \Omega$$

$$R_{DC} \gg R_{AC}$$

Q)



$$-V_{max} + 100I = 6$$

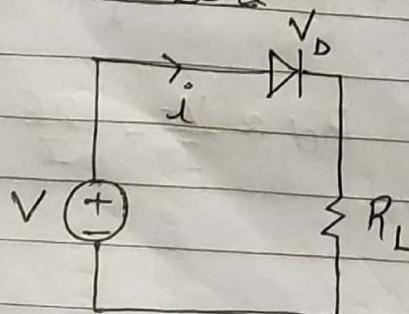
$$1000\left(I - \frac{20}{1000}\right) = 6$$

$$I = \frac{26}{1000}$$

$$V_{max} = \dots$$

$$V_{max} = 8.6 ??$$

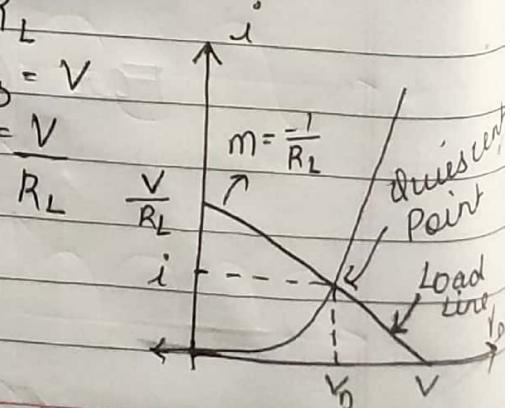
Load Line



$$V = V_D + iR_L$$

$$\text{if } i = 0 \Rightarrow V_D = V$$

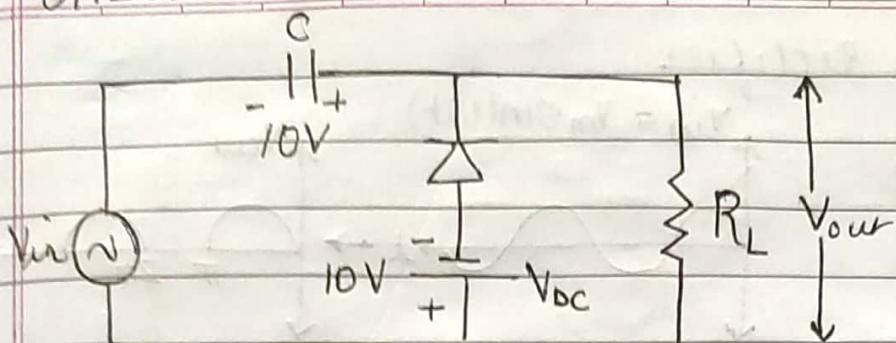
$$\text{if } V_D = 0 \Rightarrow i = \frac{V}{R_L}$$



*Clamper circuits
from Boylestead*

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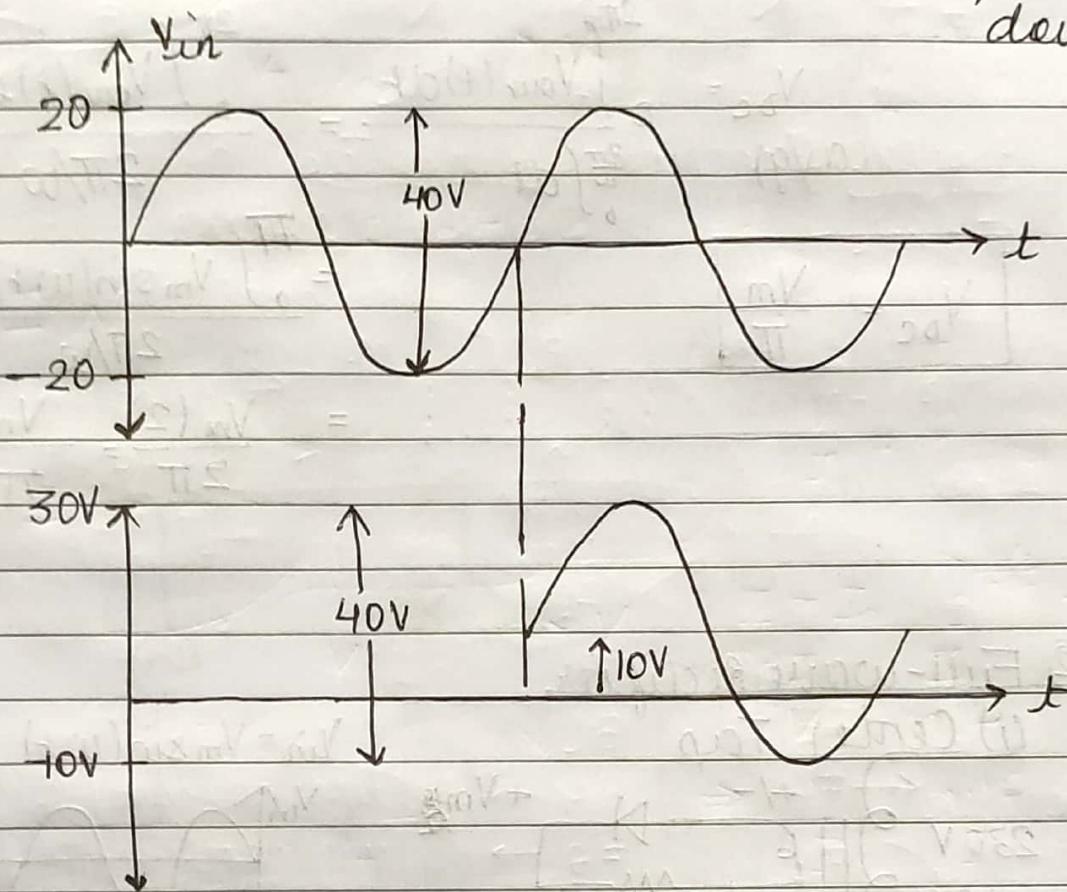
01/23/2020



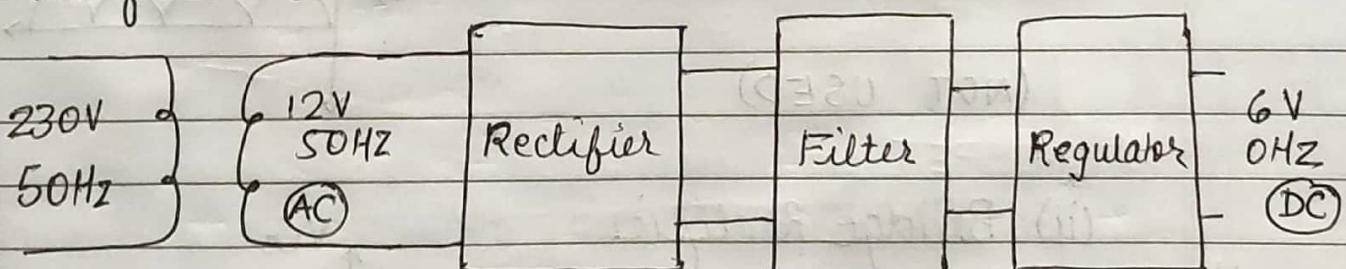
① Direction of diode to decide whether pushed up or down.

② Direction of battery to decide whether further pushed up or down.

*UNITS

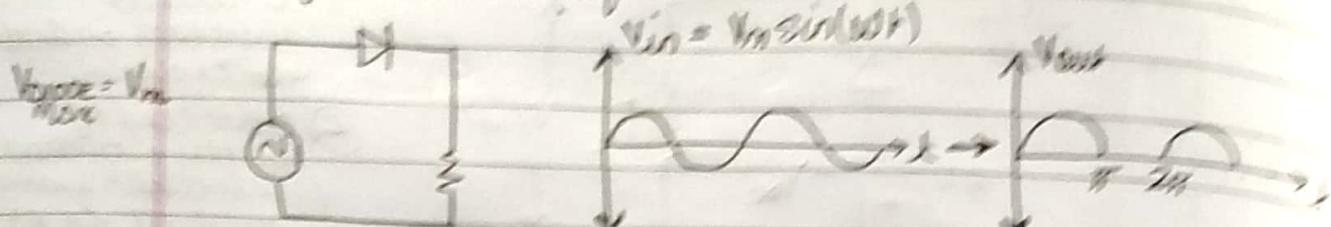


Rectifier (AC \rightarrow DC)



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① Half Wave Rectifier

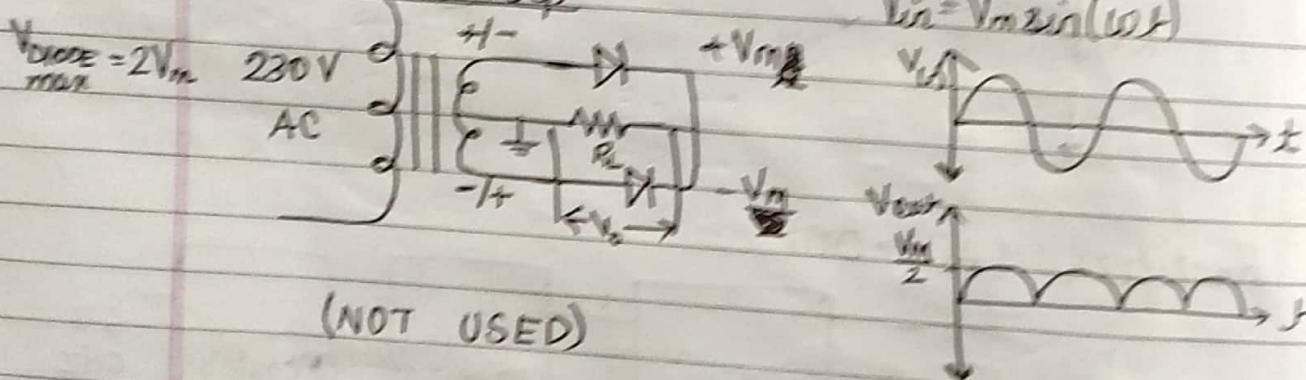


$$V_{DC} = \frac{1}{2\pi} \int_{0}^{2\pi} V_{out}(t) dt = \frac{1}{2\pi} \int_{0}^{2\pi} V_m \sin(\omega t) dt$$

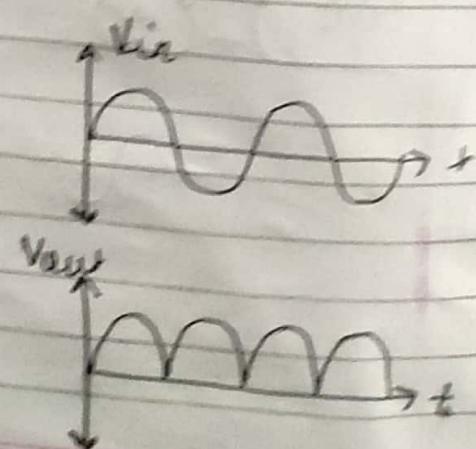
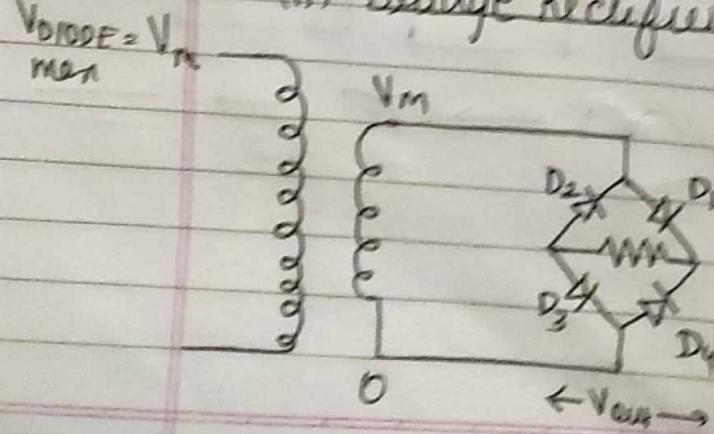
$$= \frac{V_m}{2\pi} \int_{0}^{\pi} \sin(\omega t) dt = \frac{V_m}{2\pi} \cdot \frac{2\pi}{\omega} = \frac{V_m}{\omega} = \frac{V_m}{2\pi f_0}$$

② Full-wave Rectifier

(i) Center Tap



(ii) Bridge Rectifier



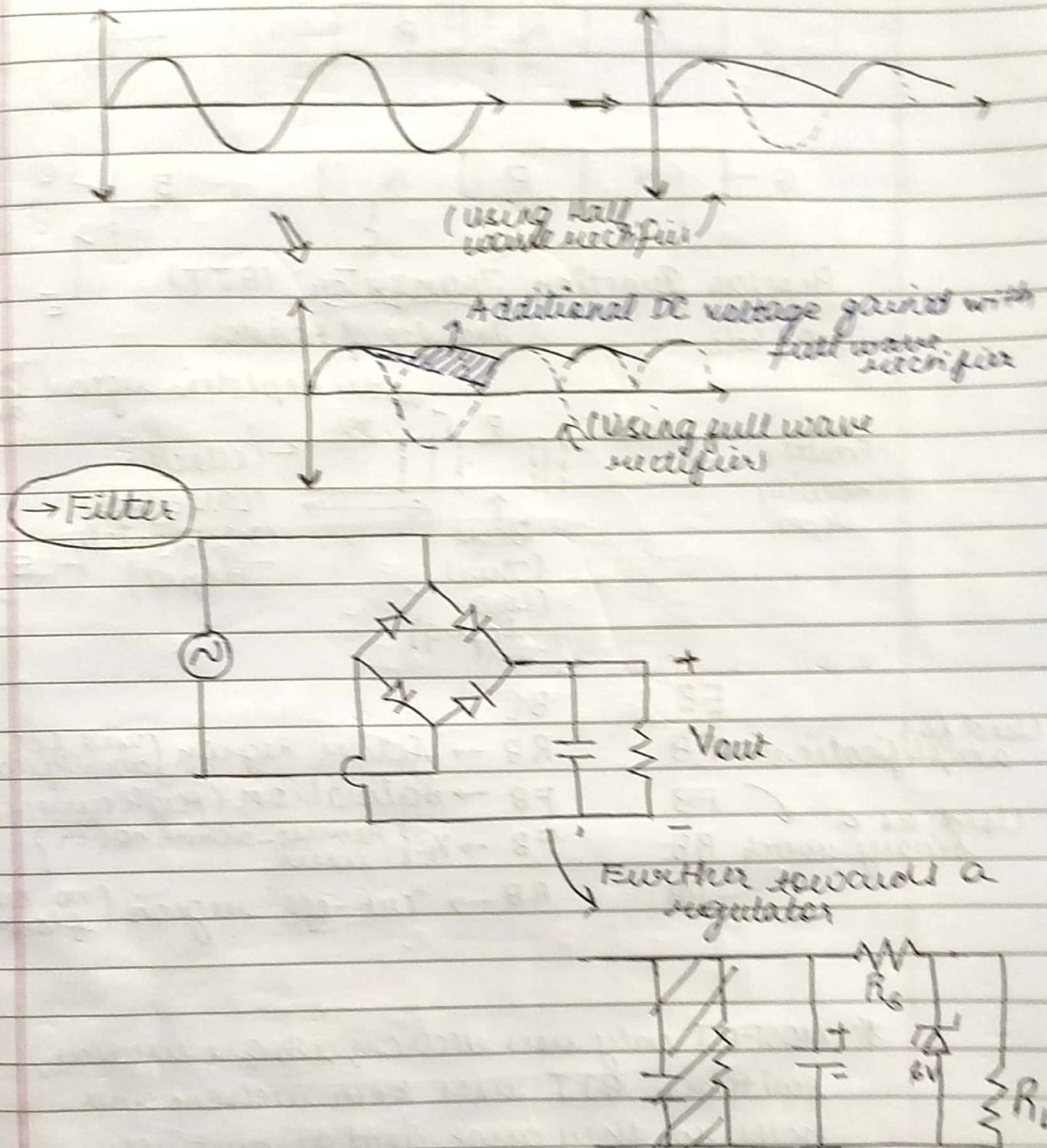
NO VOLTAGE DROP IN BRIDGE RECTIFIER

* Read terminologies from
Book *

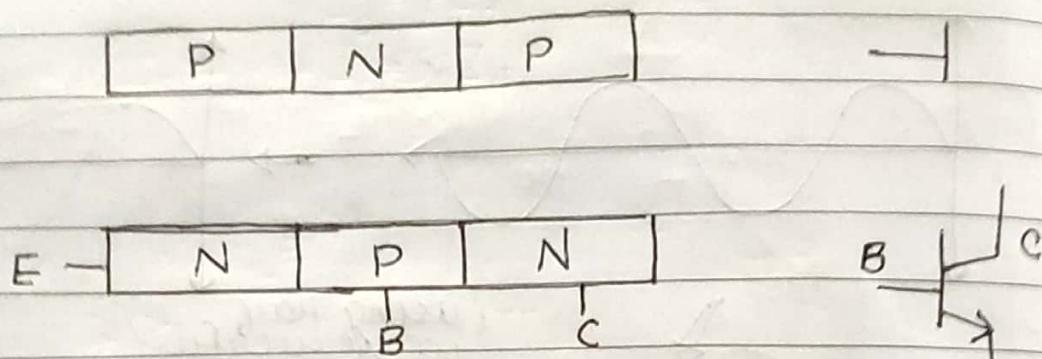
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Converting AC to DC



01/27/2020 Transistor

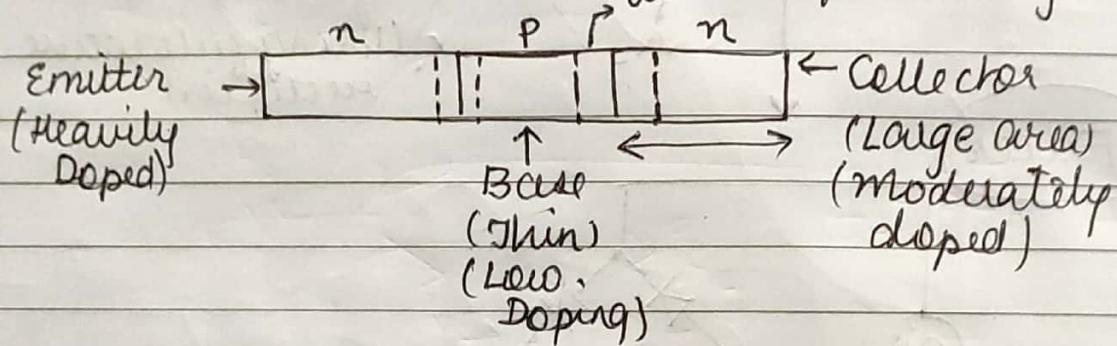


Bipolar Junction Transistor (BJT)

e^+ & hole

Transfer of resistor

wider depletion region (not so heavily depleted)



Used for amplification \leftarrow FB

BC

RB \rightarrow Active Region (used for amplification)

FB \rightarrow Saturation (high current flow)

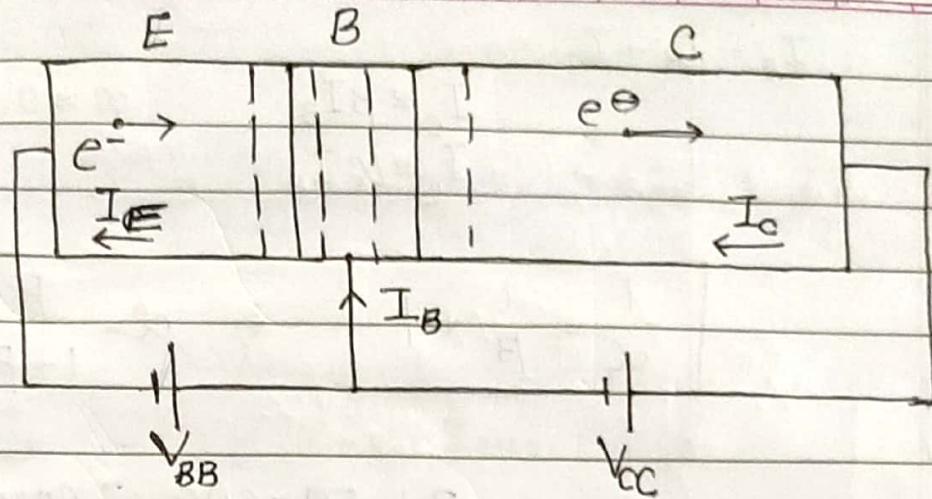
FB \rightarrow X { Reverse-active, never }

RB \rightarrow cut-off region (no current flowing)

Used as a binary switch RB

RB

* MOSFET only uses electrons, so, are used as switches. BJT uses both electrons and holes, so, they aren't used as switches.
HOLES ARE very slow *



$$I_E = I_B + I_C$$

$$\frac{I_C}{I_B} = \beta$$

$$\frac{I_C}{I_E} = \alpha$$

$$\Rightarrow \frac{I_E}{I_C} = \frac{I_B}{I_C} + 1$$

$$\frac{1}{\alpha} = \frac{1}{\beta} + 1$$

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$$I_E = I_B + I_C$$

$$I_C \approx \beta I_B$$

$$\alpha \approx 0.9$$

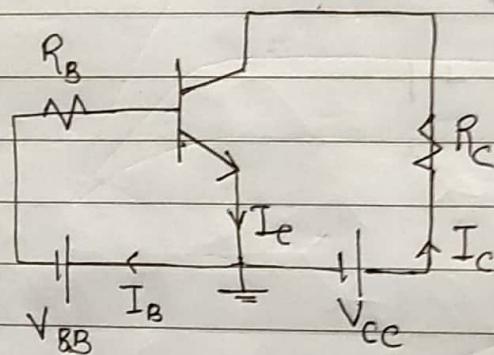
$$I_C \approx \alpha I_E$$

$$\frac{I}{\alpha} = \frac{I}{\beta} + \frac{I}{1+\beta} \Rightarrow \alpha = \frac{\beta}{1+\beta}$$

$\beta: 50 - 600$ normally, this is
 $\alpha: \text{almost } 1$ the range.

Common Emitter

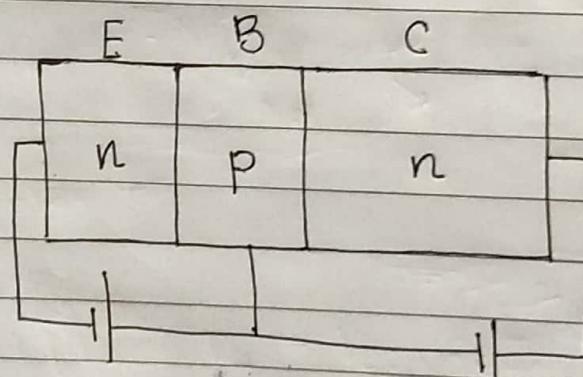
*180° phase change (shift)



$$I_C = \beta I_B + I_{CBO}$$

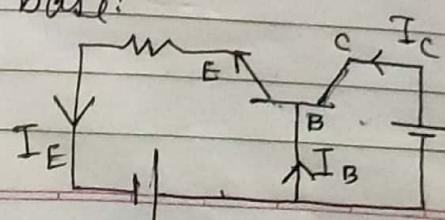
never see current ↑

$$I_C \approx \beta I_B \quad \left. \begin{array}{l} I_C \text{ is} \\ \text{actually} \\ \text{larger.} \end{array} \right\}$$



must have
Reverse Bias saturation
current (negligible)

In common base:



$$I_C = \alpha I_E + I_{CBO}$$

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$$I_C = \beta I_B + I_{CEO} = \alpha I_E + I_{CBO}$$

$$I_C = \frac{\beta}{\alpha} I_B + \frac{I_{CEO}}{\alpha} = \alpha \left(\frac{I_E}{\alpha} \right) + \frac{I_{CBO}}{\alpha} = I_E + \frac{I_{CBO}}{\alpha}$$

~~X = X +~~

$$\beta I_B + I_{CEO} = \alpha I_E + I_{CBO}$$

~~I_{CEO}~~ =

$$I_C = \alpha (I_E + I_B) + I_{CBO}$$

$$I_C (1 - \alpha) = \alpha I_B + I_{CBO}$$

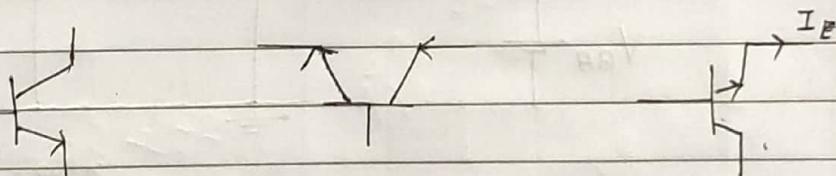
$$I_C = \frac{\alpha}{1 - \alpha} I_B + \frac{I_{CBO}}{1 - \alpha}$$

$$I_C = \frac{\beta I_B + I_{CBO}}{1 - \alpha}$$

$$I_C = \beta I_B + I_{CBO}$$

$$\Rightarrow I_{CEO} = \frac{I_{CBO}}{1 - \alpha}$$

(Input from Base) (Input from
CE CB collector) CC



A_I: Medium Low High

A_V: Medium ~~Very~~ High Low

Impedance { Z_{in}: Low Low Medium

Z_{out}: High, Medium [Low] why?

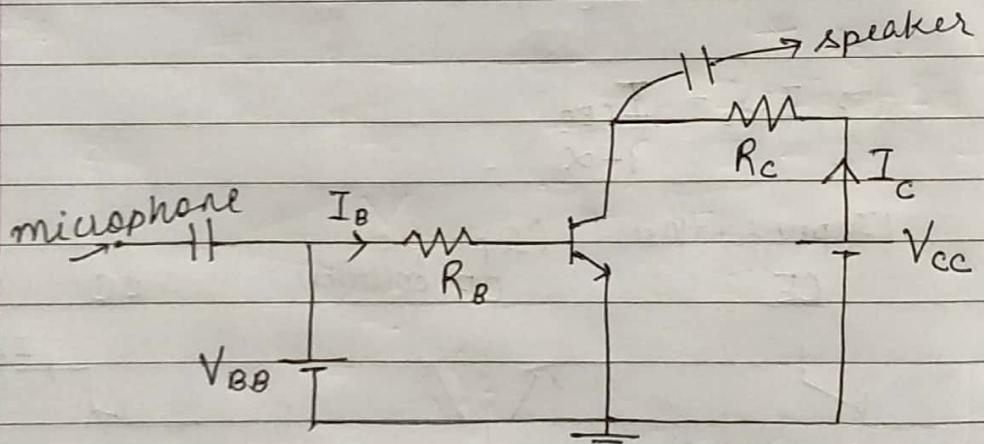
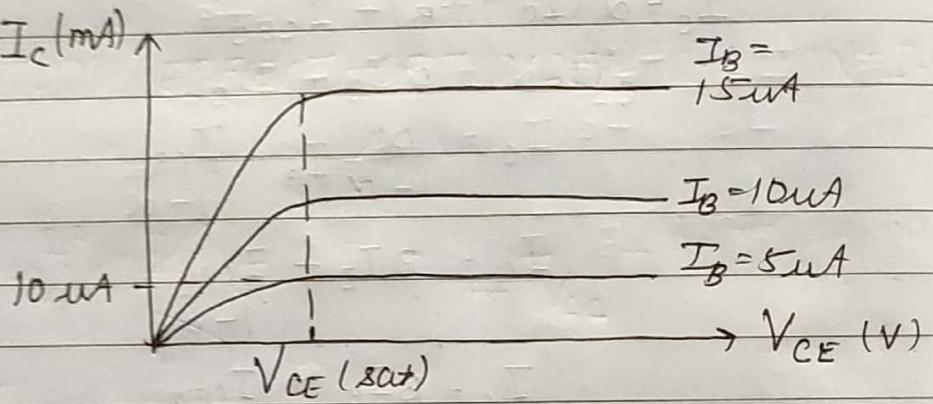
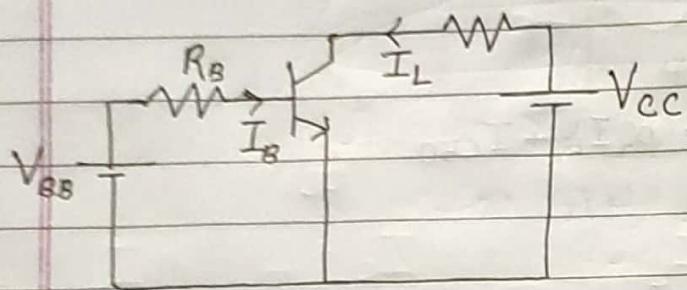
Both current gain and voltage gain \rightarrow commonly used.

POWER GAIN

02/09/2020

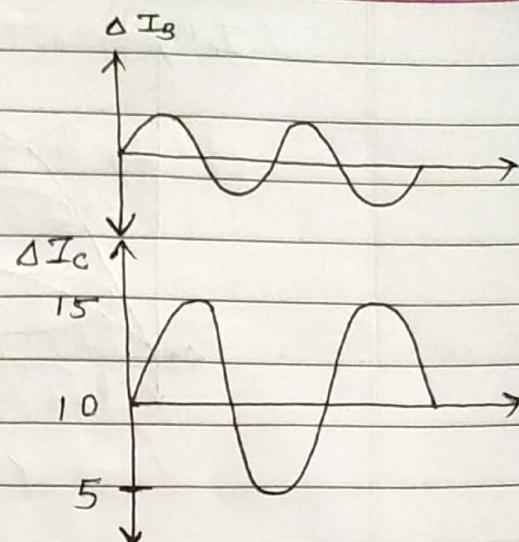
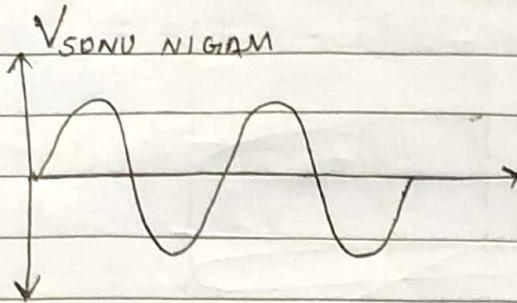
BJT as an Amplifier

$$I_E = \beta I_B + (1+\beta) I_{CBO} \quad \} \text{ where did this come from?}$$

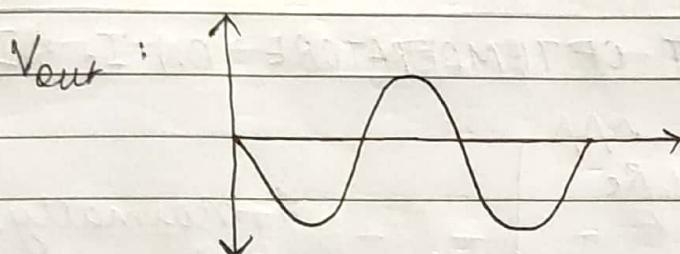


$$V_L = V_{CC} - R_C I_C \quad \left. \begin{array}{l} \text{Max value of} \\ V_L = V_{CC} \text{ when} \\ R_C = 0 / I_C = 0. \end{array} \right\}$$

$$\text{due to } \begin{cases} \text{input } I_B' = I_B + \Delta I_B \\ \text{AC } I_C' = I_C + \Delta I_C \end{cases} \left. \begin{array}{l} \text{Sat} \\ \text{y/Ant} \end{array} \right\} \Delta I_C = \beta \Delta I_B$$



* Adding capacitor b/w V_L and speaker only lets AC signal pass through.



* Input/Output have a phase difference of π in common emitter configuration

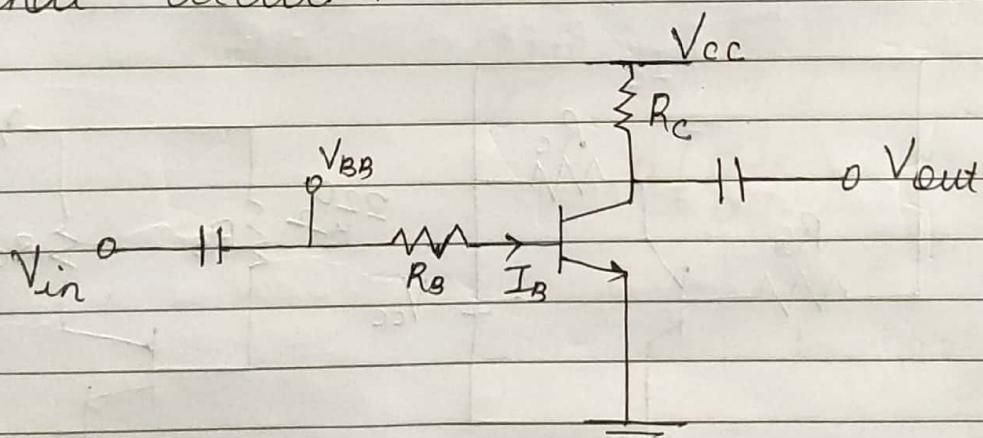
$$V_L = -I_C R_C \quad (\text{say } V_C = 0)$$

$$\Delta V_L = -\Delta I_C \cdot R_C$$

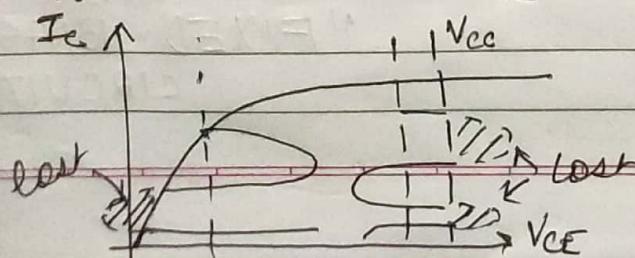
$$V_L \text{ max} = 12 \text{ V}$$

$$V_L \text{ min} = 4 \text{ V}$$

Final circuit :



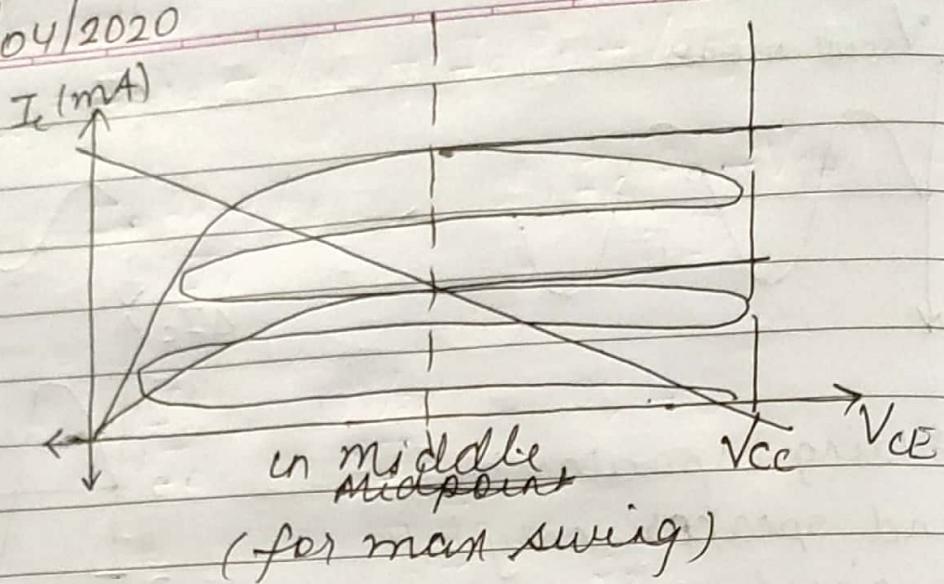
Choose values so V_{CE} is somewhere in the middle.



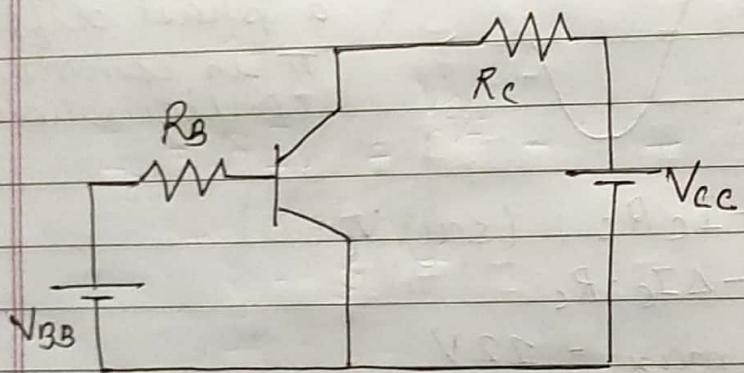
If I_C changes by the slightest amount, Q point changes significantly

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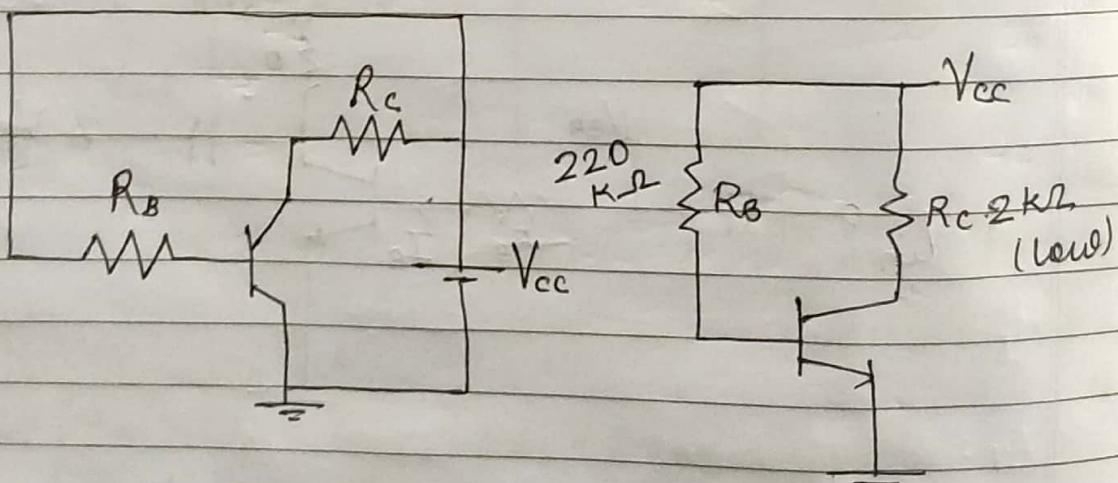
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STUDY EFFECT OF TEMPERATURE ON I_c & I_B



- * Normally, only one battery is used, so here we will remove V_{bb} .
- * i_B is very low, so is V_{bb} .



"FIXED BIAS
CIRCUIT"

02/04/2020

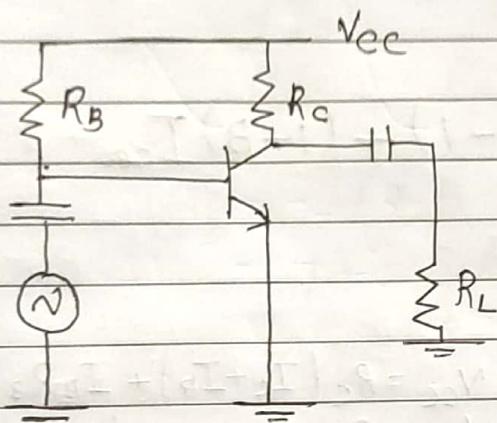
$$I_a = \beta I_B + (1+\beta) I_{CBO} \quad ??$$

Stability Factors

$$S = \frac{dI_c}{dI_{CBO}} \Big|_{V_{BE}} \quad S' = \frac{dI_c}{dV_{BE}} \Big|_{\beta, I_{CBO}} \quad S'' = \frac{dI_c}{d\beta} \Big|_{V_{BE}, I_{CBO}}$$

most important.

Fixed Bias Circuit For Amplification



$$S = \frac{dI_c}{dI_{CBO}}, \quad I_c = \beta I_B + (1+\beta) I_{CBO}$$

$$\frac{dI_c}{dI_c} = \beta \left(\frac{dI_B}{dI_c} \right) + (1+\beta) \left(\frac{dI_{CBO}}{dI_c} \right)$$

$$1 = \beta \left(\frac{dI_B}{dI_c} \right) + \frac{(1+\beta)}{S}$$

$$S = \frac{1 + \beta}{1 - \beta \frac{dI_B}{dI_c}}$$

very small



$$S \approx 1 + \beta$$

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$$V_{ce} = I_B R_B + V_{BE} = I_C R_C + V_{CE}$$

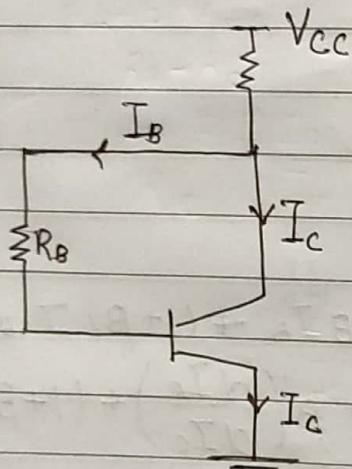
$$\frac{d(I_B R_B + V_{BE})}{dI_C} = \frac{d(I_C R_C + V_{CE})}{dI_C}$$

$$R_B \frac{dI_B}{dI_C} + \frac{dV_{BE}}{dI_C} = R_C + 0$$

$$\frac{dI_B}{dI_C} = \frac{R_C}{R_B}$$

$$S \approx 1 + \beta \quad \} \text{ LARGE } \rightarrow \text{not stable}$$

$$I_C = \beta I_B (e^{\frac{V_{BE}}{nV_T}} - 1) + (1 + \beta) I_{CQ0}$$



$V_{CC} = R_C (I_C + I_B) + I_B R_B + V_{BE}$
 $V_{CC} = \cancel{R_C} I_C + I_B (R_C + R_B) + V_{BE}$
 constant if increased must go down
 ↓ ↓ ↓
 Ib must down Ic comes back down

Collector Feedback Bias

→ That is why this configuration is very stable (considering $\beta \rightarrow \text{constant}$)

$$S = \frac{1 + \beta}{1 - \beta \frac{dI_B}{dI_C}}$$

$$V_{CC} = I_C R_C + I_B R_B + I_B R_C + V_{BE}$$

$$\frac{d(V_{CC})}{dI_C} = R_C + \frac{dI_B}{dI_C} (R_B + R_C) + \frac{dV_{BE}}{dI_C}$$

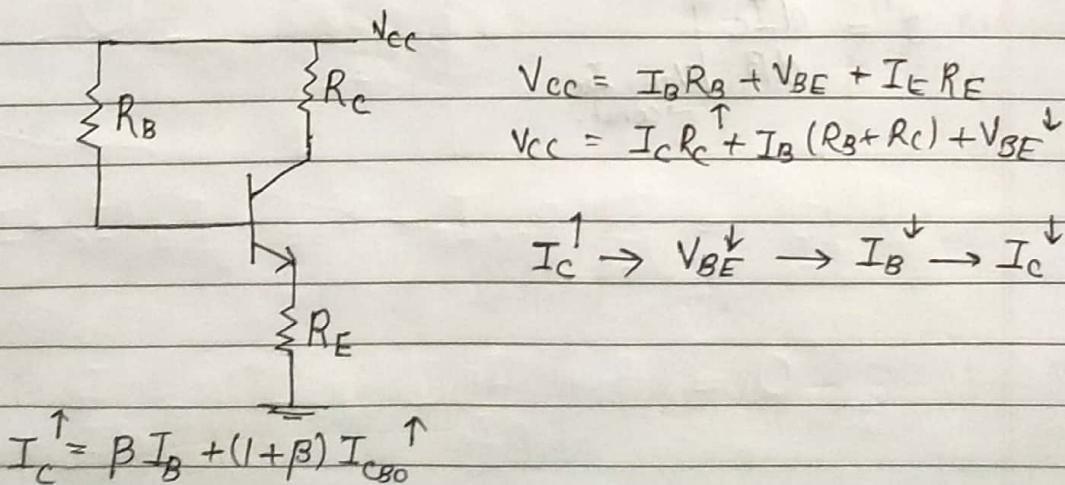
$$0 = R_C + \frac{dI_B}{dI_C} (R_B + R_C)$$

$$\frac{dI_B}{dI_C} = \frac{-R_C}{R_B + R_C}$$

$$\Rightarrow S = \frac{1 + \beta}{1 + \frac{\beta R_C}{R_B + R_C}} \quad \left. \begin{array}{l} S < 1 + \beta \\ \text{Denominator High} \\ \rightarrow \text{more stable than previous circuit.} \end{array} \right\}$$

$$S'' = \frac{dI_C}{d\beta} \quad \left. \begin{array}{l} \text{only occurs when} \\ \text{transistor dies} \Rightarrow \beta \text{ changes.} \end{array} \right\}$$

Emitter feedback



* R_B is very large,
theoretically *

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$$\frac{d}{dI_C} (V_{ce}) = \frac{d}{dI_C} (I_B R_B + V_{BE} + I_E R_E)$$

$$0 = (R_B + R_E) \left(\frac{dI_B}{dI_C} \right) + R_E$$

$$\frac{dI_B}{dI_C} = \frac{-R_E}{R_B + R_E}$$

$$\Rightarrow S = \frac{1 + \beta}{1 + \beta R_E}$$

C

E

$$S_c = \frac{1 + \beta}{1 + \beta R_c}$$

$$R_B + R_c$$

$$S_E = \frac{1 + \beta}{1 + \beta R_E}$$

$$R_B + R_E$$

R_c

R_E

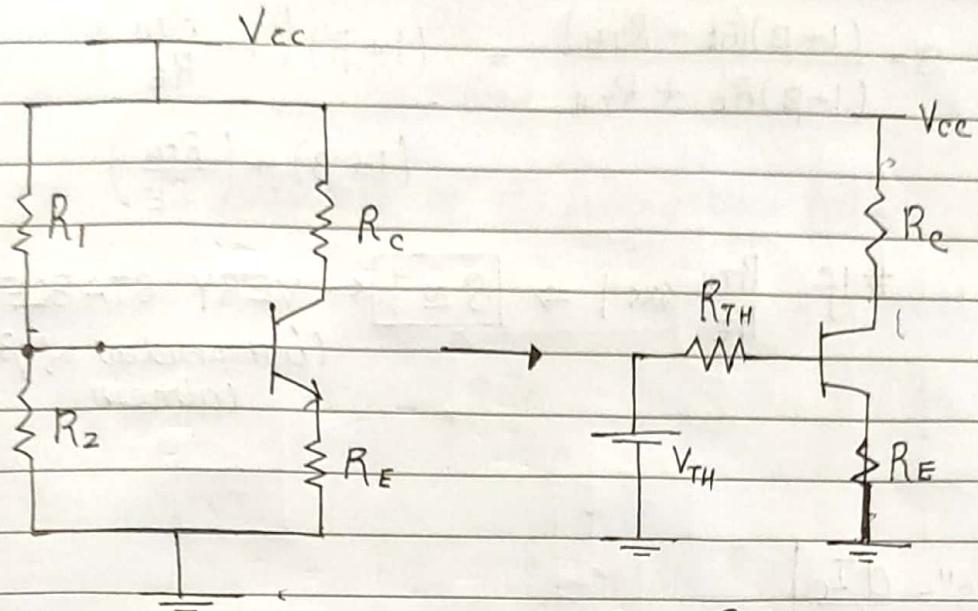
$R_c > R_E \Rightarrow S_c < S_E$ ↗
 $R_c < R_E \Rightarrow S_c > S_E$ ↗ which case is practical here?

$$S'' - \frac{dI_C}{d\beta} \left|_{V_{BE}, I_B \rightarrow \text{const.}}$$

* Resistances have tolerances of 10%, which means
 ΔI_B is large if Resistance is large.
So, high R_E

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$$R_{TH} = \frac{R_1 R_2}{R_1 + R_2} \quad V_{TH} = \frac{V_{CC} R_E}{R_1 + R_2}$$

$$V_{TH} = I_B R_{TH} + V_{BE} + I_E R_E$$

$$V_{TH} = I_B (R_{TH} + R_E) + V_{BE} + I_C R_E \quad \because I_C = I_B + I_E$$

$$V_{CC} = (I_c + I_b)R_c + I_b R_b + V_{BE}$$

$$\frac{d(I_c)}{dI_c} = \frac{d}{dI_c} (\beta I_b + (1+\beta) I_{C(s)})$$

$$1 = \beta \left(\frac{dI_b}{dI_c} \right) + \frac{(1+\beta)}{S}$$

generally
 $R_B \gg R_C$ so

v. unstable.

$$\frac{(1+\beta)(1 + \frac{R_b}{R_c})}{(1+\beta + R_b/R_c)} = S \Leftrightarrow S = \frac{1 + \beta}{1 - \beta \frac{dI_b}{dI_c}}$$

} In original circuit

$$\frac{d(V_{TH})}{dI_c} = \frac{d}{dI_c} (I_b R_{TH} + V_{BE} + I_E R_E)$$

$$0 = R_{TH} \frac{dI_b}{dI_c} + 0 + R_E \frac{dI_b}{dI_c} + R_E \Rightarrow S = \frac{1 + \beta}{1 + \beta R_E / (R_E + R_{TH})}$$

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$$S = \frac{(1+\beta)(R_E + R_{TH})}{(1+\beta)R_E + R_{TH}} = \frac{(1+\beta)\left(1 + \frac{R_{TH}}{R_E}\right)}{(1+\beta) + \left(\frac{R_{TH}}{R_E}\right)}$$

If $\frac{R_{TH}}{R_E} \ll \mid \Rightarrow S \approx 1 \leftarrow \text{VERY STABLE}$
 (independent of β)
 (almost)

$$S'' = \frac{dI_C}{d\beta} \Big|_{I_B, V_{BE} \rightarrow \text{const.}}$$

$$\frac{d(I_C)}{dI_c} = \frac{d(\beta I_B + (1+\beta)I_{CBO})}{dI_c}$$

$$1 = \beta \frac{dI_B}{dI_c} + I_B \frac{d\beta}{dI_c} + I_{CBO} \frac{d\beta}{dI_c}$$

$$1 - \beta \frac{dI_B}{dI_c} = (I_B + I_{CBO}) \frac{d\beta}{dI_c}$$

$$S'' = - \frac{I_B + I_{CBO}}{1 - \beta \frac{dI_B}{dI_c}}$$

$$1 - \beta \frac{dI_B}{dI_c}$$

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$$\frac{d(V_{TH})}{dI_c} = \frac{d}{dI_c} (R_{TH} I_B + V_{BE} + R_E (I_c + I_B))$$

$$O = R_{TH} \frac{dI_B}{dI_c} + R_E + R_E \frac{dI_B}{dI_c}$$

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$$\Rightarrow \frac{dI_B}{dI_C} = \frac{-R_E}{R_E + R_{TH}} \quad (2)$$

↳ evaluate eq? (1) using this value

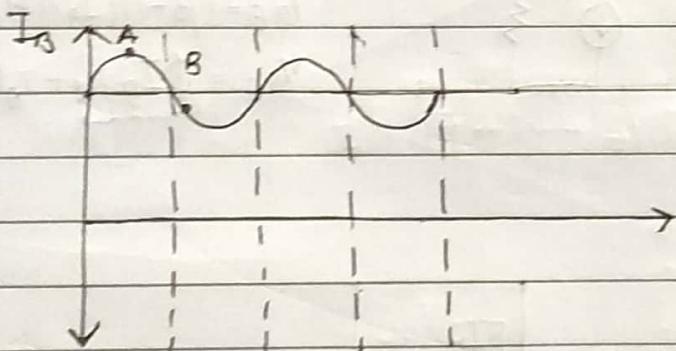
$$\Rightarrow S'' = \frac{I_B + I_{CBO}}{1 + \frac{\beta R_E}{R_E + R_{TH}}}$$

$$\Rightarrow S'' = \frac{(I_B + I_{CBO})(1 + R_{TH}/R_E)}{(1 + \beta + \frac{R_{TH}}{R_E})}$$

If $\frac{R_{TH}}{R_E} \ll 1 \Rightarrow S'' = \frac{(I_B + I_{CBO})}{(1 + \beta)}$

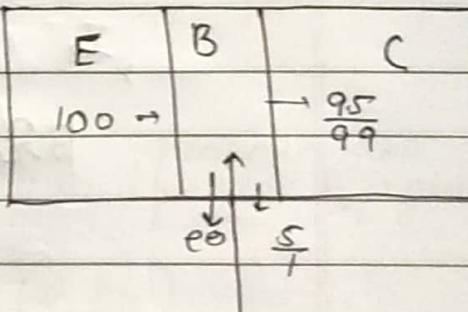
← VERY STABLE
⇒ $\beta \rightarrow$ in the denominator

BJT AC ANALYSIS

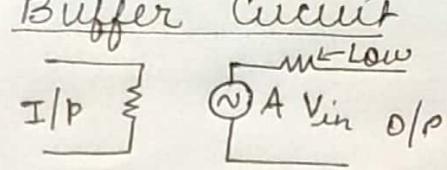


At point A: I_B is high, say $5 e^- s$ come out

At point B: I_B is low, say $1 e^- s$ comes out

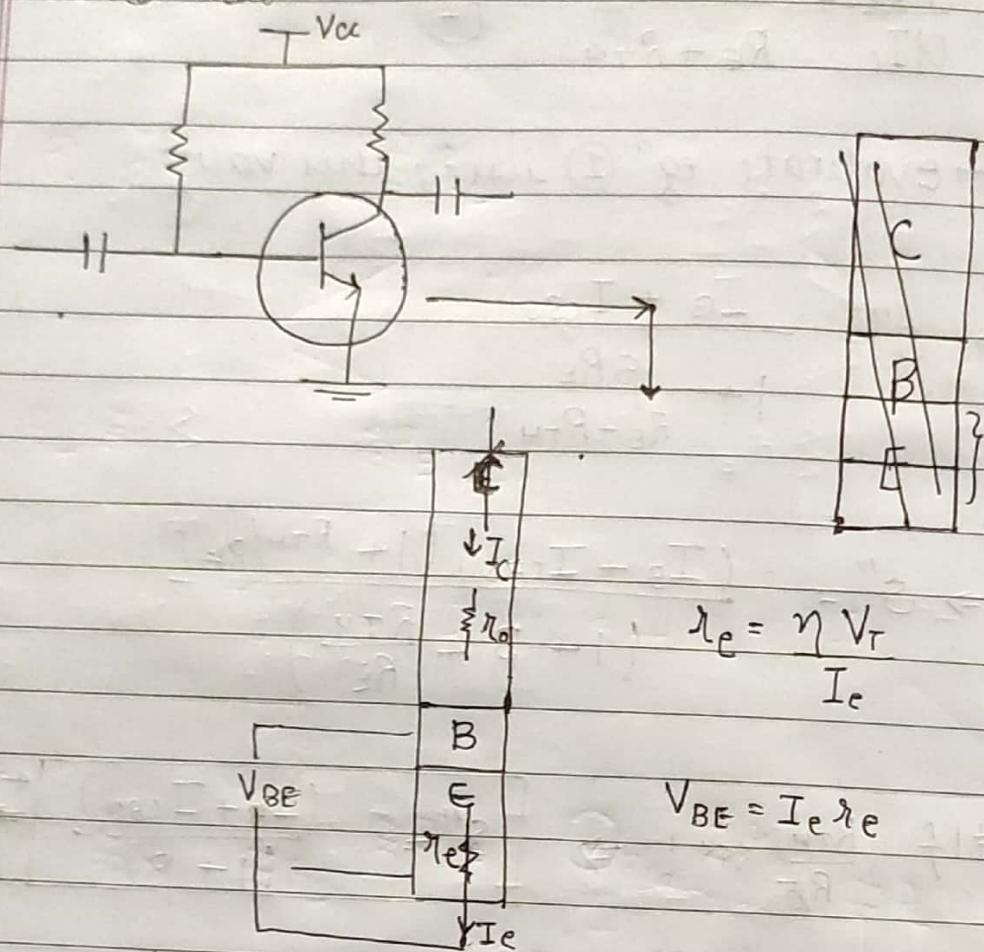


⇒ If frequency of I_B is very high, speed of $e^- s$ is being varied very quickly, they may not be able to physically cope up with it. Hence, I_C of transistor may not correctly represent the input signal.



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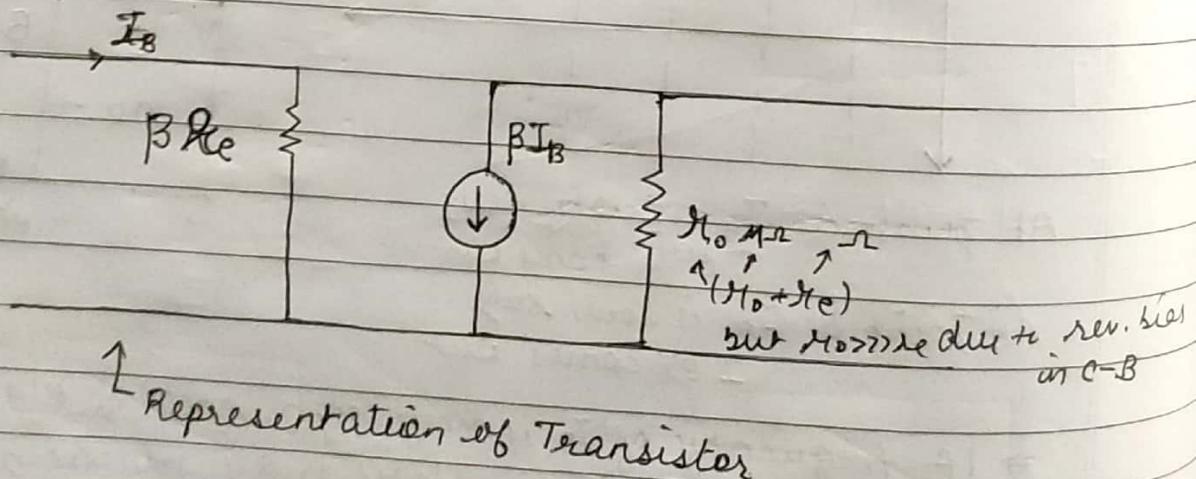
Fixed Bias:



$$V_{BE} = (I_c + I_B) r_e$$

$$V_{BE} = (\beta + 1)(I_B)(r_e)$$

$$V_{BE} = \beta I_B r_{fe} + I_B r_e$$

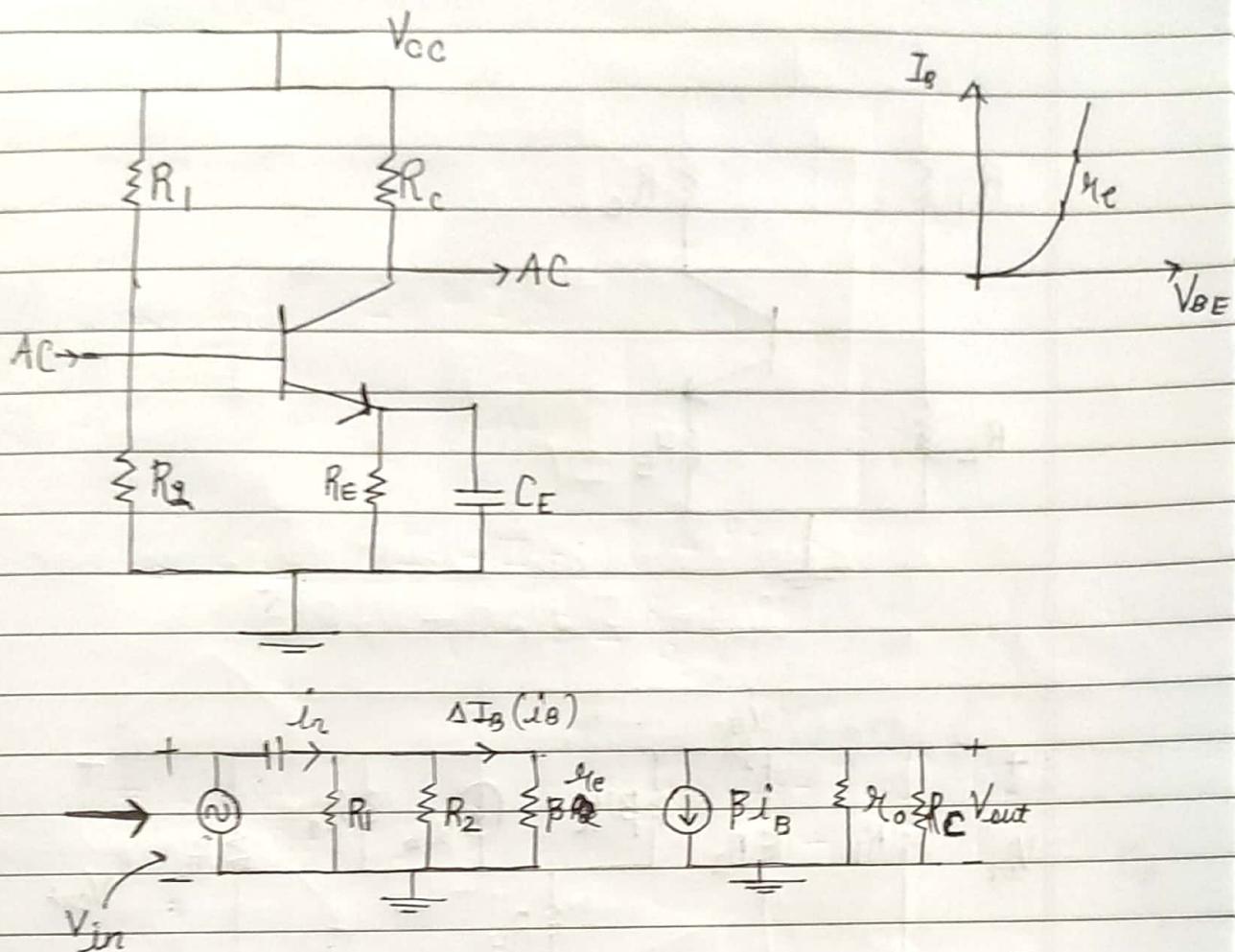


Representation of Transistor

// Actual transistor also has some capacitance ??

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$$Z_{in} = R_1 \parallel R_2 \parallel \cancel{R_e} \beta R_e$$

$$Z_{out} = R_c \parallel R_0$$

$$A_v = \frac{V_{out}}{V_{in}}$$

} since we have assumed both as the same polarity

$$V_{out} = -\beta i_B (R_0 \parallel R_0)$$

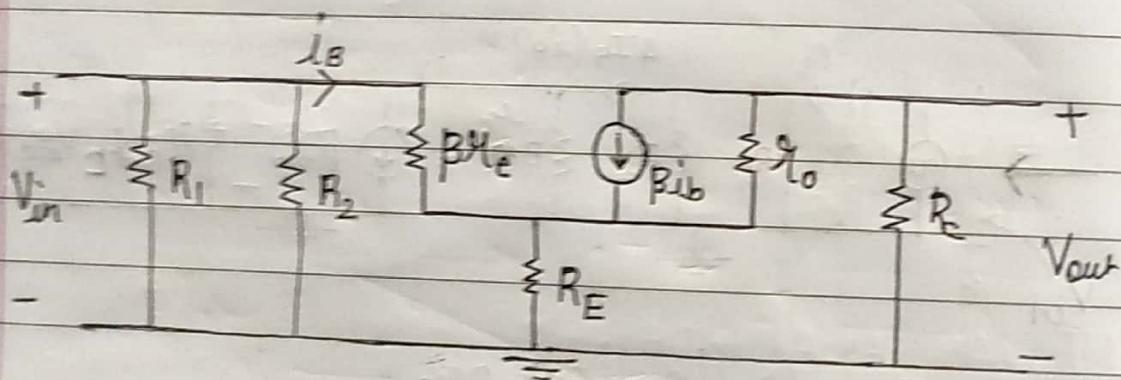
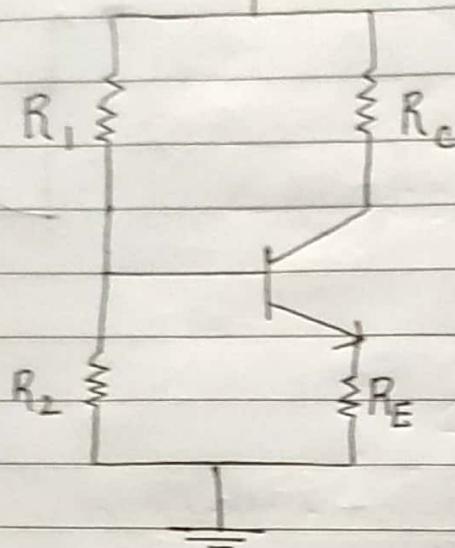
or $-\beta i_B (R_c \parallel R_0 \parallel R_L)$ } only in case when R_L is given

However, take $V_{out} = -\beta i_B (R_c \parallel R_0)$

$$A_v = \frac{-\beta i_B (\cancel{R_e} \parallel R_c)}{i_B \beta R_e}$$

$$= \frac{-R_0 \parallel R_c}{R_e} \approx \frac{-R_c}{R_e}$$

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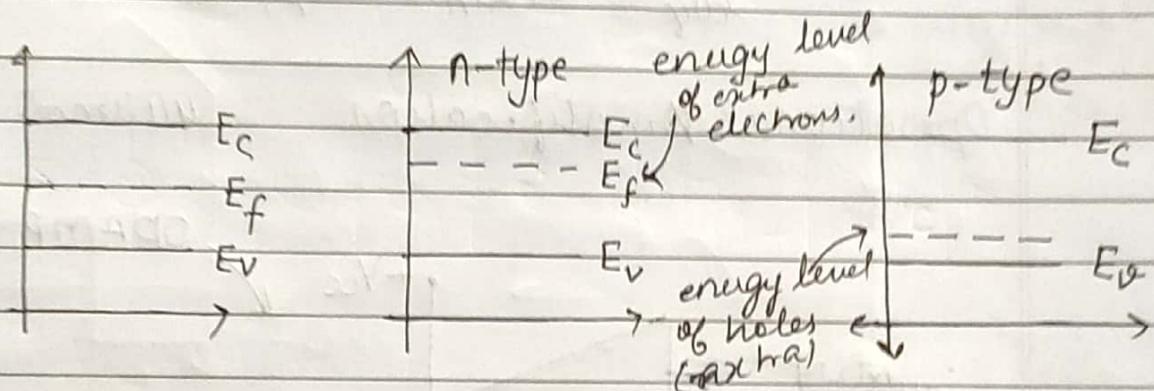
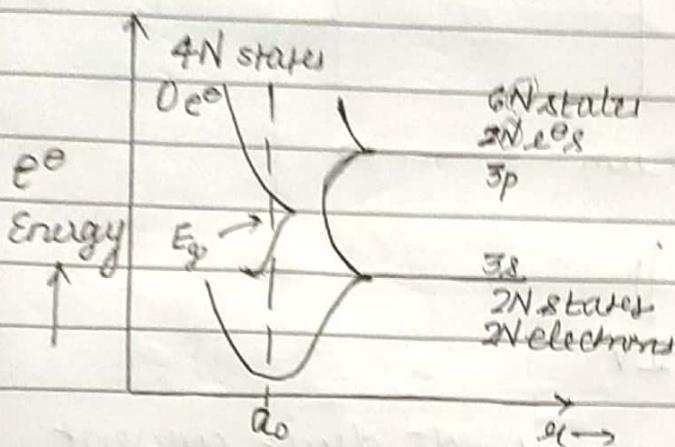
$$\therefore Z_{in} = \beta R_E + (1 + \beta) R_E$$

$$Z_{out} = ?$$

$$V_{out} = ?$$

$$V_{in} = ?$$

REVISION



$$n_0 p_0 = n_i^2$$

$$n_0 = n_i \exp \left[\frac{E_F - E_{F_i}}{kT} \right]$$

$E_F \rightarrow$ Doped E_F
 $E_{F_i} \rightarrow$ Intrinsic E_F

$$p_0 = n_i \exp \left[\frac{-(E_F - E_{F_i})}{kT} \right]$$

$$J_{dry} = e(n\mu_n + p\mu_p)E = \sigma E$$

$$\rho = \frac{1}{\sigma}$$

$$J_{n \times |dx|} = e D_n \frac{dn}{dx}$$

$$J_{p \times |dx|} = -e D_p \frac{dp}{dx}$$