(OA - Quiz 1 (CSH 221-CAM Aut 2020-21)

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9.1. Size of ISA=12

=> We need 4 bits to store all opcodes.

Total of 64 registers=(26)

=> 6 bits for representing a register

→ Memory for 1 instruction = 4+6+6+6+12
= 34/8 bytes
= 4.25 bytes

\$ 1 instruction takes 5 bytes

100 instructions \$ \frac{500 \text{ bytes}}{}

Q-2, Size of instruction format = 2 bytes (given) = 16 bits

-> Total encodings = 216

> Used encodings-Type 1: Lix(24)3 = 214 16 integer regs >> 4 bits (=24)

64 float regs => 6 bits

(26)

Type2: 8x (26)2=215

Type3: 14x (24)(26) = 7x2"

 \Rightarrow Encodings for Type $4 = 2^{16} - (2^{15} + 2^{14} + 7 \times 2^{11})$ = $2^{16} (32 - 16 - 8 - 7)$

= 2"

: Total no. of instructions of type $u = \frac{2^{i}}{26} = 2^5 = 32$.	
Nmax = 32	
Jeonic feature of RISC machine is having a branched slot. Also, RISC has reduced number of addressing nodes. (Not an iconic feature)	1
=> RESC needs more memory => Option:(c): Having a branch delay slot.	
J Opinion of	

O-4. PLSC is more complicated than CISC: False Since CISC has more transistors.

Option: (b) > False

Q. E. Option (B): RISC]

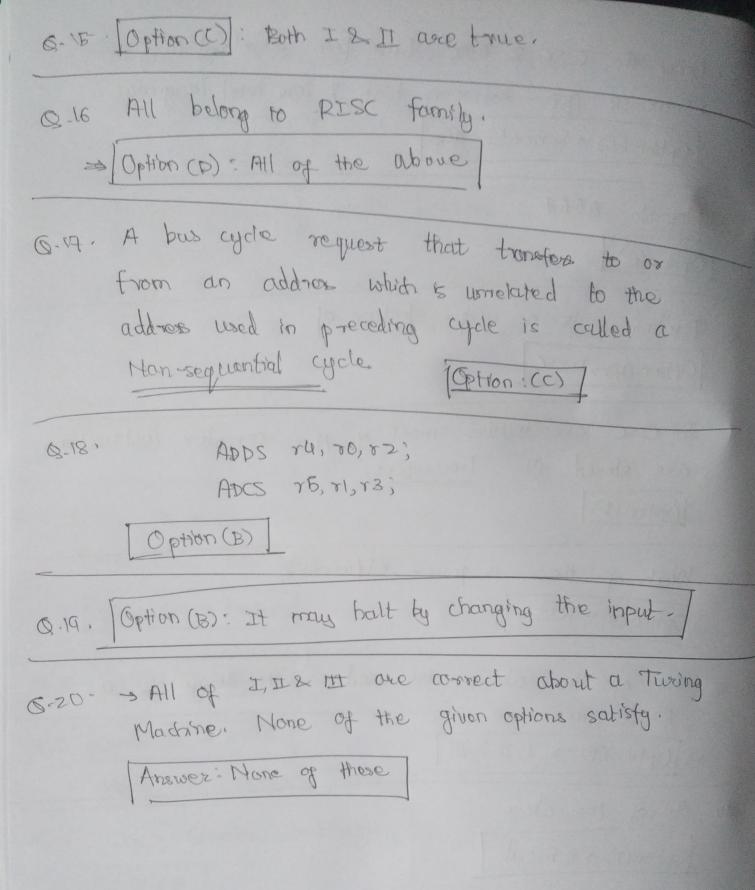
G.6. Option (B) -> RISC

Hence the name "Reduced" Instruction Set Computer.

87. CISCE Complex Instruction Set Computer

Option (b)

6.8	Both the CISC & RISC have been developed to-
	- Semantic gap - between high & low level language.
	Obtion (c) > Sementic gap
6.9.	Motorola A567
1	Option(d)
	The de Marian forten of
Q-10.	Pipelining is a unique feature of
	Option (A) > RISC
Q-11.	In CISC architecture most of the complex instructions are stored in Transistors.
	are stored in Transistors,
	Option (D)
Q-15.	Which of these is power efficient?
	Option(B) - RISC
A 12	, All of the above are used in the design of a
	RISC processor
	=> [Option (D) -> III & III]
Q-(4	All of the above
	(Option (D) -> a,b,c,d



6 21. Option (D): Initiation of intercapt service 1st inst. > PC > MBR 2nd instr -> add - of X -> MAR god instr - add of Y -> PC (Interrupt requence initializes) 4th instr > (old Pc values > Memory Q.22. Option (D) > 2 kbits No of combinations = 24 x24 = 28 of= 8 bits Total ROM= 28x8=2" = 2kbits 0.23. Option (C): Mornory address register. 8-24 Option (D): Memory Data Register 6-26 Option (b): Accumulator 0-26, B=input => TTM halbs TM never halts in case of (0+1)t. 3 Option (A) >> M does not halt on any string in (0+3)+