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Tutorial 2

Q1) ASCII : A → 65 → 1000001

ANS: (B) 1000001

Q2) $\overline{(\bar{A}+B)}+\bar{C} = A = (A+B)(C)$

$\overline{x+y} = \bar{x}\,\bar{y}$

$\therefore \overline{(\bar{A}+B)}+\bar{C} = (A+B)(C)$

Q3) (D) All of the above.

However, we only use 2's complement with computers because of technical reasons.

Q4) (B) 16

128 × 8 RAM ⇒ 1024 ~~bytes~~ bits

⇒ $\frac{1024}{8}$ = 128 Bytes.

Since 1 chip = 128 Bytes

x chip = 2048 Bytes

⇒ $x = 16$

Q5) (D) All of the above

FOR: $A \oplus B \oplus C$ for

A	B	C	
0	0	0	= 1
1	1	1	= 1
1	0	1	= 1

$A \odot B \odot C$

0	1	0	= 1
1	1	1	= 1
1	0	1	= 1

Q6) 256

11 bits ⇒ total 2^{11} instructions = 2048

⇒ # of instructions for 2-address encoding

⇒ each address ⇒ 4 bits

⇒ 2^4 possibilities for 1 address

⇒ 5 2-address instructions

$= 5 \times 2^4 \times 2^4 = 1280$ encodings

$32 \times 2^4 = 512$ one address instructions

⇒ remaining instructions, we can assume are 0-address

= 2048 − 1280 − 512 = 256

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Q7) (C) Instruction opcode.

It is instruction for which operation must be performed

Q8) $(1111111111)_2 = (2^{10} - 1)_{10} = (1023)_{10}$

128 instructions $\Rightarrow 2^7 \Rightarrow$ 7 bits for opcode

Given: 7 bits for operand.

Remaining: 24 - (7+7) = 10 bits for register.

max value = 1111111111

Q9)

~~16 bits = 7 bits for address~~ 16 bits for instructions

~~Total: 2^9 = 512 possible instructions~~

~~① 2, two address instructions =~~

Q9) (C) ~~256~~ 768

$2^{16} = 65536$

2x 2 address instructions = $2 \times 2^7 \times 2^7 = 32768$

250x 1 address instructions = $250 \times 2^7 =$ ~~32000~~ 32000

remaining for 0 address instructions

$= 65536 - 32768 - 32000 = 768$