COA-Quiz1 (CSN-221-CAM Aut2020-21)

* This form will record your name, please fill your name.

1

Consider a processor with 64 registers and an instruction set of size twelve. Each instruction has five distinct fields, namely, opcode, two source register identifiers, one destination register identifier, and a twelve-bit immediate value. Each instruction must be stored in memory in a byte-aligned fashion. If a program has 100 instructions, the amount of memory (in bytes) consumed by the program text is _____(Don't write any units, only value in the answer bar).

2

A processor has 16 integer registers (R0, R1, …, R15) and 64 floating point registers (F0, F1, …, F63). It uses a 2-byte instruction format. There are four categories of instructions: Type-1, Type-2, Type-3, and Type 4. The type-1 category consists of four instructions, each with 3 integer register operands (3Rs). The type-2 category consists of eight instructions, each with 2 floating-point register operands (2Fs). The type-3 category consists of fourteen instructions, each with one integer register operand and one floating-point register operand (1R+1F). The type-4 category consists of N instructions, each with a floating-point register operand (1F). The maximum value of N is _____.

3

The iconic feature(s) of the RISC machine among the following is/are .....

- ◯ Reduced number of addressing modes
- ◯ Increased memory size
- ◯ Having a branch delay slot
- ◯ All of the mentioned

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The RISC processor has a more complicated design than CISC

- ◯ True
- ◯ False

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The Sun microsystems processors usually follow ..... architecture

- CISC
- RISC
- ISA
- ULTRA SPARC

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The computer architecture aimed at reducing the time of execution of instructions is.....

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The CISC stands for .....

- Computer Instruction Set Compliment
- Complete Instruction Set Compliment
- Computer Indexed Set Components
- Complex Instruction set computer

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Both the CISC and RISC architectures have been developed to reduce the .....

- Time delay
- Cost
- Semantic gap
- All

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Out of the following which is not a CISC machine

- IBM 370/168
- VAX 11/780
- Intel 80486
- Motorola A567

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Pipe-lining is a unique feature of .....

- RISC
- CISC
- ISA
- IANA

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In CISC architecture most of the complex instructions are stored in .....

- Register
- Diodes
- CMOS
- Transistors

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Which of the architecture is power efficient?

- CISC
- RISC
- ISA
- IANA

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Consider the following processor design characteristics.

I. Register-to-register arithmetic operations only
II. Fixed-length instruction format
III. Hardwired control unit

Which of the characteristics above are used in the design of a RISC processor?

- I and II only
- II and III only
- I and III only
- I, II and III

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The main difference(s) between a CISC and a RISC processor is/are that a USC processor typically:

a) has fewer instructions
b) has fewer addressing modes
c) has more registers
d) is easier to implement using hardwired control logic

- ◯ a and b
- ◯ b and c
- ◯ a and d
- ◯ a, b, c and d

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Evaluate the following statements and select the appropriate answer given from the choices below.

I. Von Neumann Architecture shares common memory for Data and Instructions
II. Harvard Architecture has separate physical memories for Data and Instructions

- ◯ Only I is true
- ◯ Only II is true
- ◯ Both I and II are true
- ◯ None of them is true

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Which of the following processors belong to Reduced Instruction Set Computers (RISC) family?

- ◯ ARM
- ◯ AVR
- ◯ MIPS
- ◯ All of the above

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A bus cycle request that transfers to or from an address which is unrelated to the address used in the preceding cycle is called a _____

- ◯ Sequential Cycle
- ◯ Internal Cycle
- ◯ Non-Sequential Cycle
- ◯ Coprocessor Register Transfer Cycle

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Using only two instructions, add a 64-bit integer contained in R2 and R3 to another 64-bit integer contained in R0 and R1, and place the result in R4 and R5.

- ADD r4, r0, r2 ; ADC r5, r1, r3 ;
- ADDS r4, r0, r2 ; ADCS r5, r1, r3 ;
- ADD r4, r0, r2 ; ADD r5, r1, r3 ;
- ADD r4, r0, r2 ; ADCS r5, r1, r3 ;

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Which of the following is False with respective to possible outcomes of executing a TM over a given input?

- it may halt and accept the input
- it may halt by changing the input
- It may halt and reject the input
- It may never halt

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Which of the following is wrong?

- TM is a simple mathematical model of general purpose computer
- TM is more powerful than finite automata
- TM can be simulated by a general purpose computer
- All of these

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Consider the following sequence of micro-operations.

MBR ← PC
MAR ← X
PC ← Y
Memory ← MBR

Which one of the following is a possible operation performed by this sequence?

- Instruction fetch
- Operand fetch
- Conditional branch
- Initiation of interrupt service

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The amount of ROM needed to implement a 4 bit multiplier is

- 64 bits
- 128 bits
- 1 Kbits
- 2 Kbits

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The register which holds the address of the location to or from which data are to be transferred is called

- Index register
- Instruction register
- Memory address register
- Memory data register

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The register which contains the data to be written into or readout of the addressed location is called

- Index register
- Instruction register
- Memory address register
- Memory data register

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The register used as a working area in CPU is

- Program counter
- Instruction register
- Instruction decoder
- Accumulator

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A single tape Turing Machine M has two states q0 and q1, of which q0 is the starting state. The tape alphabet of M is {0, 1, B} and its input alphabet is {0, 1}. The symbol B is the blank symbol used to indicate the end of an input string. The transition function of M is described in the following table.

The table is interpreted as illustrated below. The entry (q1, 1, R) in row q0 and column 1 signifies that if M is in state q0 and reads 1 on the current tape square, then it writes 1 on the same tape square, moves its tape head one position to the right and transitions to state q1. Which of the following statements is true about M?

	0	1	B
q0	q1,1,R	q1,1,R	Halt
q1	q1,1,R	q0,L,R	q0,B,L

- ◯ M does not halt on any string in (0 + 1)+
- ◯ M does not halt on any string in (00 + 1)*
- ◯ M halts on all string ending in a 0
- ◯ M halts on all string ending in a 1