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QUIZ-1

1) 500

- Instruction set size = 12 (# of instructions)
  ⇒ $2^3 < 12 < 2^4$
  we need 4 bits here

- Two source register identifiers, and 64 total registers
  $2^6 = 64$ } Each Registers can be represented by max 6 bits
  ⇒ 2 registers for source
  = 6 + 6 = 12 bits

- Destination register: 6 bits

- 12-bit immediate value: 12 bits

Total = 4 + 6 + 6 + 6 + 12
= 34
= 4.25 bytes $\left(\frac{34}{8} = 4.25\right)$

However, ~~4.25~~ storage cannot have a fractional part
⇒ 5 bytes required per instruction

⇒ 100 instructions × 5 = 500

2) (32)

2-byte instruction format means we can describe an instruction using $2 \times 8 = 16$ bits.

$\Rightarrow 2^{16}$ possible instructions

For integer operands, we need 4 bit because $2^4 = 16$ (16 int. registers)
Similarly, $2^6 = 64$ (64 float registers)
$\Rightarrow$ 6 bits

Type-1: 4 instructions $\times\ 2^{(3 \times 4)}$ (3 integer, 4 bits for integer) $= 2^{14}$

Similarly:

Type-2: $8 \times 2^{(2 \times 6)} = 2^{15}$

~~Type-3: $14 \times 2^{(1 \times 4)} = 7 \times 2^5$~~

Type-3: $14 \times 2^{(4+6)} = 7 \times 2^{11}$

Type-4: $N \times (2^6) = N(2^6)$

$\Rightarrow 2^{16} = 2^{15} + (2^{14}) + 7 \times 2^{11} + N(2^6)$

$2^{14} = 7(2^{11}) + N(2^6)$

$2^8 = 7(2^5) + N$

$8(2^5) = 7(2^5) + N$

$2^5 = N$

$\boxed{N = 32}$

3) ~~All of the mentioned~~

Having a branch Delay Slot

4) False

Complex v/s Reduced
more complicated — less complicated

5) RISC

Sun Microsystems follow RISC architecture

6) RISC

RISC (Reduced Instruction Set computer) is designed to perform a smaller number of computer instructions

7) CISC : Complex Instruction Set Computer

8) **Semantic Gap**

They were designed with the ~~ope~~ objective of improving efficiency of software development, and hence reduce the gap b/w high level language and low level language.

9) **Motorola A567**

10) **RISC**

11) **Transistors**

12) **RISC**

Instructions are reduced, and since it use pipelining, lesser amount of computing time is needed.

13) **I, II, and III**

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14) a, b, c, d

15) Both I and II are true

16) All of the above (All are RISC architecture)

17) Non-Sequential Cycle

A bus cycle that transfers to or from a memory address which is unrelated to previous addres is non sequential

18)
```
ADDS r4, r0, r2;
ADCS r5, r1, r3;
```

19) It may halt by changing the input

A turing machine can halt in many ways (either after receiving/rejecting input) but not after changing input.

It can change value on tape and move to an adjacent square/cell.

20) Turi
mo
Th

21) Init

22) 2 Kb

23) Mem

20) Turing Machine is a simple mathematical model of a general purpose computer

That is false b/c TM performs a specific set of instructions, unlike a general-purpos computer

21) **Initiation of Interrupt service**

22) 2 Kbits

A × B ⇒ $(2^4)(2^4)$ possibilities
4bits 4bits ⇒ 2^8

output: A × B = C requires 8 bits too
4 4 8 ← bits

total needed
⇒ $2^8 \times 8 = 2^{11} = 2(2^{10})$
= 2 Kbits

23) **Memory Address Register**

MAR stores address from which data is to be fetched or where it is to be stored.

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24) **Memory Data Register**

MDR is used to store the information which is moved to and from storage and CPU.

25) **Accumulator**

26) M does not halt on any string in $(0+1)+$