	19114079
	Shreyous Dodamand Page: Date: / /
	QU/2-1
- 1) (5DO) (->a (a) (
	The state of the s
	· Instruction set size = 12 (# of instructions) = 23<12<27
	· Instruction set size = 12 (# of instructions)
	$\Rightarrow 2^3 < 12 < 2^+$
	we need + biti here
	. [() \
	Two source negister identifiers, and 64 total negisters
	total registers
	Each (district)
	26 = 64 & Register can be 1 represented by man 65 to
	represented by max 65 to
	=> 2 registers par source
	= 2 registers par source = 6+6=[2 bits]
	Tally borreis to the states you was
	· Destination register: [6 bits]
	· 12-bit immediate value (12 bit)
	The second of th
	OFTE PART FOR
	Total = 4+6+6+6+12
	= 34 m 10: [Alv 10 11 10 1 10 10 10 10 10 10 10 10 10 1
	= 4.25 bytes $\left(\frac{34}{5}, 4.25\right)$
	However, 4.25 to storage cannot have
	a fractional parl
	instruction
	=) 100 instructions x 5 = 500
	The continuity of the same of

2-byte instruction format means we can describe an instruction using 2x8=16bits.

=> 216 possible instructions

For integer eperands, we need 4 bits

because $2^4 = 16$ (16 int. registers)

Similarly, $2^6 = 64$ (64 float registers) $\Rightarrow 6 \text{ bits}$ instructions

Type-1: 4 × 2^(8 × 4) = 2¹⁴

Similarly:

Type-2: $8 \times 2^{(2\times 6)} = 2^{15}$ Type-3: $14 \times 2^{(1\times 4)} = 7\times 2^{5}$ Type-3: $14 \times 2^{(4+6)} = 7\times 2^{7}$

Type-4: N x (26) = N(26)

 $2^{16} = 2^{15} + (2^{14}) + 7 \times 2^{11} + N(2^{11})$

 $\frac{2^{14} = 7(2^{11}) + N(2^{6})}{2^{8} = 7(2^{5}) + N}$ $8(2^{5}) = 7(2^{5}) + N$

N=32

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3)	AU of the mentioned

Having a branch Delay Slot

4) False

more less complicated complicated

5) RISC

Sun Microsystems follow RISC architecture

6) RISC

RISC (Reduced Instruction Set computer) is designed to perform a smaller number of computer instructions

7) CISC: Complex Instruction Set Computes

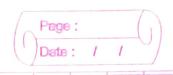
8) Semantic Gap

They were designed with the oper objective of improving efficiency of software development and hence reduce the gap b/w high level language and low level language.

- 9) Motorda A567
- ro) RISC
- 11) Transistors
- Instructions are reduced, and since is use pipelining, lesser amount of computing time is needed.

13) I, II, and III.

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14)	[a,b,c,d]	20)	Turi
			77
		21)	Ini
15)	(Both I and II are true)		
16)	(All of the about) (All are RISCarchitecture)	22)	2 Kb
17)	Non-Sequential Cycle		
	A bus cycle that transfers to a from a mimory address which is unrelated to previous addres is non signerical		
18)	ADDS 24, 20, 2; ADCS 25, 21, 23;		
19)	It may halt by changing the input	23)	Mem
	A turing machine can halt in many ways (either after receiving/ rejecting input) but not after changing input.		
	It can change value on tape and move to an adjacent square/cell.		1



20) Turing Machine is a simple mathematical model of a general purpose computer

That is false b/c TM performs à specific set of instructions, unlike a general purpos compuser

21) Initiation of Interrupt service

22) 2 Kbits

 $A \times B \Rightarrow (2^{+})(2^{+})$ passibilities 4bits 4bits $\Rightarrow 2^{8}$

output: $A \times B = C$ requires 8 bits too

4 4 8 \in \text{bits}

total nucled $\Rightarrow 2^8 \times 8 = 2^{11} = 2(2^{10})$

23) Memory Address Register

MAR stores address from subich data is to be stored.

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24) [Memory Data Register]

MOR is used to store the information which is moved to and from storage and CPT

25) (Accumulator)

26) M does not halt on any string in (0+1)+