Chapter
27
Electronics

Semiconductor electronics

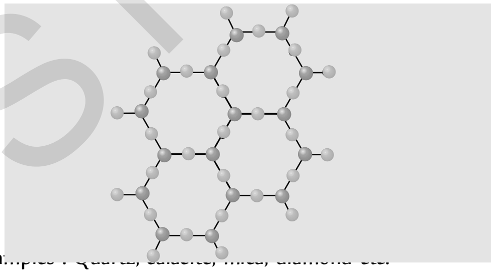
Solids

It is a state of matter which has a definite shape and a definite volume. The characteristic properties of the solid depends upon the nature of forces acting between their constituent particles (*i.e.* ions, atoms or molecules). Solids are divided into two categories.

Crystalline solids

(1) These solids have definite external geometrical form.

(2) Ions, atoms or molecules of these solid are arranged in a definite fashion in all it's three dimensions.



(3) Examples : Quartz, calcite, mica, diamond etc.

(4) They have well defined facets or faces.

(5) They are ordered at short range as well as at long range.

(6) They are anisotropic, *i.e.* the physical properties like elastic modulii, thermal conductivity, electrical conductivity, refractive index have different values in different direction.

(7) They have sharp melting point.

(8) Bond strengths are identical throughout the solid.

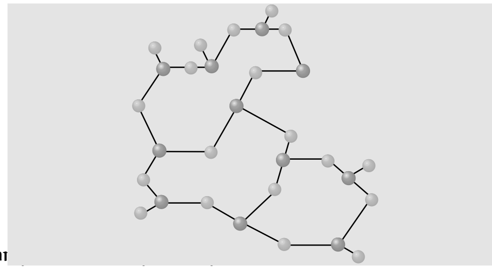
(9) These are considered as true solids.

(10) An important property of crystals is their symmetry.

Amorphous or glassy solids

(1) These solids have no definite external geometrical form.

(2) Ions, atoms or molecules of these solids are not arranged in a definite fashion.



(3) Exa

(4) They do not possess definite facets or faces.

(5) These have short range order, and there is no long range order.

(6) They are isotropic.

(7) They do not have a sharp melting point.

(8) Bond strengths vary.

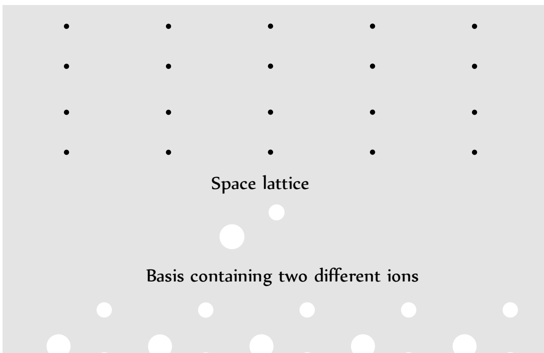
(9) These are considered as pseudo-solids or super cooled liquids.

(10) Amorphous solids do not have any symmetry.

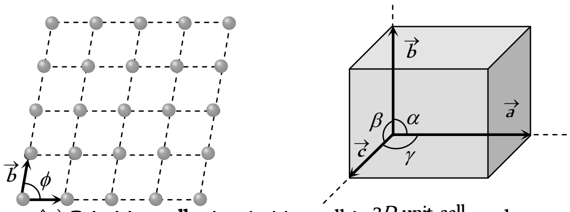
Terms Related with Crystal Structure

(1) **Crystal lattice :** It is a geometrical arrangement of points in space where if atoms or molecules of a solid are placed, we obtain an actual crystal structure of the solid.

(2) **Basis :** The atoms or molecules attached with every lattice point in a crystal structure is called the basis of crystal structure.



(3) **Unit cell :** Is defined as that volume of the solid from which the entire crystal structure can be constructed by the translational repetition in three dimensions. The length of three sides of a unit cell (3*D*) are called primitives or lattice constant they are denoted by *a, b, c*



2*D* unit cell 3*D* unit cell

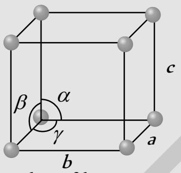
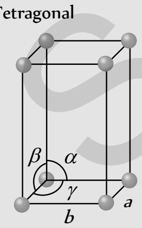
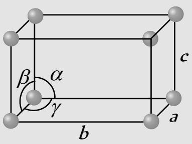
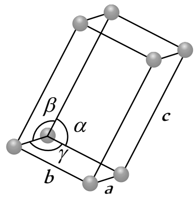
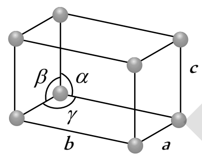
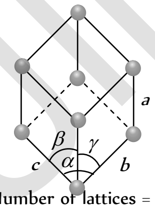
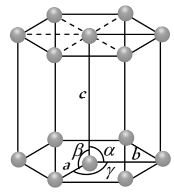
Fig. 27.1

(4) **Primitive cell :** A primitive cell is a minimum volume unit cell or the simple unit cell with particles only at the corners is a primitive unit cell and other types of unit cells are called non-primitive unit cells. There is only one lattice point per primitive cell.

(5) **Crystallographic axis :** The lines drawn parallel to the lines of intersection of the faces of the unit cell are called crystallographic axis.

All the crystals on the basis of the shape of their unit cells, have been divided into seven crystal systems as shown in the following table.

Table 27.1 : Different crystal systems

System	Lattice constants	Angle between lattice constants	Examples
Cubic  Number of lattices = 3	$a = b = c$	$\alpha = \beta = \gamma = 90°$	Diamond, *NaCl, Li, Ag, Cu,* NH_4Cl, *Pb etc.*
Tetragonal  Number of lattices = 2	$a = b \neq c$	$\alpha = \beta = \gamma = 90°$	White tin, $NiSO_4$ *etc.*
Orthorhombic  Number of lattices = 4	$a \neq b \neq c$	$\alpha = \beta = \gamma = 90°$	$HgCl_2$, KNO_3, gallium *etc.*
Monoclinic  Number of lattices = 2	$a \neq b \neq c$	$\alpha = \gamma = 90°$ and $\beta \neq 90°$	$KClO_3$, $FeSO_4$ *etc.*
Triclinic  Number of lattices = 1	$a \neq b \neq c$	$\alpha \neq \beta \neq \gamma \neq 90°$	$K_2Cr_2O_7$, $CuSO_4$ *etc.*
Rhombo-hedral or Trigonal  Number of lattices = 1	$a = b = c$	$\alpha = \beta = \gamma \neq 90°$	Calcite, *As, Sb, Bi etc.*
Hexagonal  Number of lattices = 1	$a = b \neq c$	$\alpha = \beta = 90°$ and $\gamma = 120°$	*Zn, Cd, Ni etc.*

Different Types of Symmetry in Cubic Lattices

(1) **Centre of symmetry :** An imaginary point within the crystal such that any line drawn through it intersects the surface of the crystal at equal distances in both directions.

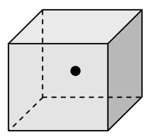
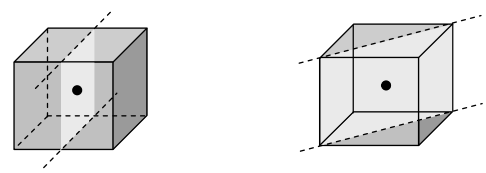


Fig. 27.2

(2) **Plane of symmetry :** It is an imaginary plane which passes through the centre of a crystal and divides it into two equal portions such that one part is exactly the mirror image of the other.



(A) Rectangular plane of symmetry

(B) Diagonal plane of symmetry

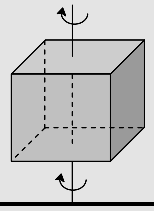
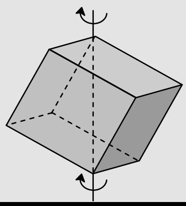
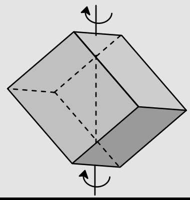
Fig. 27.3

A cubical crystal possesses six diagonal plane of symmetry and three rectangular plane of symmetry.

(3) **Axis of symmetry** : It is an imaginary straight line about which, if the crystal is rotated, it will present the same appearance more than once during the complete revolution.

In general, if the same appearance of a crystal is repeated on rotating through an angle $\frac{360^o}{n}$, around an imaginary axis, the axis is called an *n*-fold axis.

Table 27.2 : A cubical crystal possesses in all 13 axis of symmetry

Axis of four-fold symmetry = 3 (Because of six faces)	Axis of three-fold symmetry = 4 (Because of eight corners)	Axis of two-fold symmetry = 6 (Because of twelve edges)
		

(4) **Elements of symmetry :** The total number of planes, axes and centre of symmetry possessed by a crystal are termed as elements of symmetry. A cubic crystal possesses a total of 23 elements of symmetry.

Planes of symmetry $= (3+6) = 9$,

Axes of symmetry $= (3+4+6) = 13$,

Centre of symmetry = 1.

Total number of symmetry elements = 23

More About Cubic Crystals

(1) **Different lattice in cubic crystals :** There are three lattice in the cubic system.

(i) The simple cubic (*sc*) lattice.

(ii) The body-centered cubic (*bcc*).

(iii) The face-centered cubic (*fcc*).

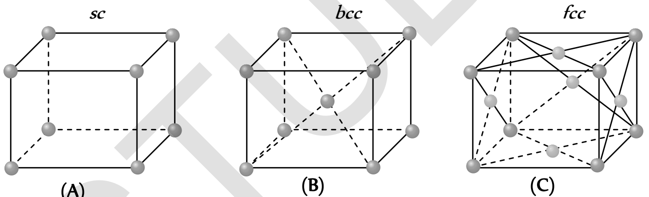
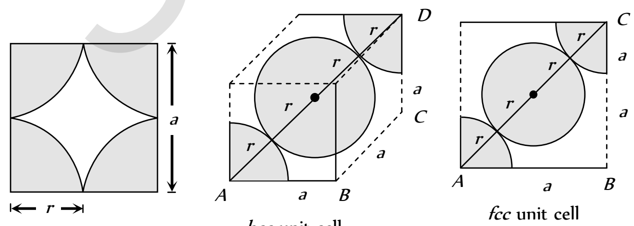


Fig. 27.4

(2) **Atomic radius :** The half of the distance between two atoms in contact is defined as atomic radius.



sc unit cell
$r = a/2$

bcc unit cell
$r = \sqrt{3}\,a/4$

fcc unit cell
$r = a/2\sqrt{2}$

Fig. 27.5

(3) **Atoms per unit cell :** An atom located at the corner of a unit cell of a lattice is shared equally by eight other unit cells in the three dimensional lattice. Therefore, each unit cell has 1/8th share of an atom at its each corner. Similarly, a face of the unit cell is common to the two unit cells in the lattice. Therefore, each unit cell has 1/2 share of an atom at its each face. The atom located at the centre of the unit cell belongs completely to the unit cell.

Let N_c, N_b and N_f be the number of atoms at the corners, centre and face of the unit cell respectively. Therefore the number of atoms per unit cell is given by $N = N_b + \frac{N_f}{2} + \frac{N_c}{8}$

(i) In *sc* lattice : $N_b = 0,\ N_f = 0,\ N_c = 8$ so $N = 1$

(ii) In *bcc* lattice : $N_b = 1,\ N_f = 0,\ N_c = 8$ so $N = 2$

(iii) In *fcc* lattice : $N_b = 0,\ N_f = 6,\ N_c = 8$ so $N = 4$

(4) **Co-ordination number :** It is defined as the number of nearest neighbours that an atom has in a unit cell. It depends upon structure.

(i) Simple cubic structure : Each atom has two neighbours along *X*-axis, two along *Y*-axis and two along *Z*-axis so co-ordination number = 6.

(ii) Face-centred cubic structure: Every corner atom has four neighbours in each of the three planes *XY*, *YZ*, and *ZX* so co-ordination number = 12

(iii) Body-centred cubic structure: The atom of the body of the cell has eight neighbours at eight corner of the unit cell so co-ordination number = 8.

(5) **Atomic packing fraction (or packing factor or relative packing density)**

The atomic packing fraction indicates how close the atoms are packed together in the given crystal structure or the ratio of the volume occupied by atoms in a unit cell in a crystal and the volume of unit cell is defined as APF.

(i) **For *sc* crystal :** Volume occupied by the atom in the unit cell $= \frac{4}{3}\pi r^3 = \frac{\pi a^3}{6}$. Volume of the unit cell $= a^3$

$$\text{Thus P.F.} = \frac{\pi a^3/6}{a^3} = \frac{\pi}{6} = 0.52 = 52\%$$

(ii) **For *bcc* :** P.F. $= \frac{\sqrt{3}\pi}{8} = 68\%$

(iii) **For *fcc* :** P.F. $= \frac{\pi}{3\sqrt{2}} = 74\%$

(6) **Density of unit cell :** Density of unit cell $= \frac{\text{Mass of the unit cell}}{\text{Volume of the unit cell}} = \frac{nA}{NV} = \frac{nA}{Na^3}$

where *n* = Number of atoms in unit cell (For *sc* lattice *n* = 1, for *bcc* lattice *n* = 2, for *fcc* lattice *n* = 4), *A* = atomic weight, *N* = Avogadro's number, *V* = Volume of the unit cell.

(7) **Bond length :** The distance between two nearest atoms in a unit cell of a crystal is defined as bond length.

(i) In a *sc* lattice : Bond length = *a* (ii) In a *bcc* lattice : Bond length $= \frac{\sqrt{3}a}{2}$ (iii) In a *fcc* lattice : Bond length $= \frac{a}{\sqrt{2}}$

Hexagonal Close Packed (HCP) Structure

The HCP structure also maximizes the packing fraction

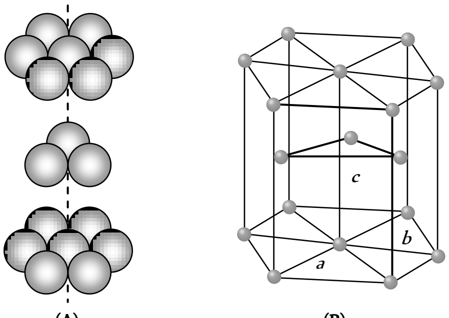


Fig. 27.6

(1) $a = b \neq c$

(2) Number of atoms per unit cell = 6

(3) The volume of the hexagonal cell = $3\sqrt{2}\,a^3$

(4) The packing fraction $= \dfrac{\pi\sqrt{2}}{6}$

(5) Coordination number = 12

(6) Magnesium is a special example of HCP lattice structure.

Bonding Forces in Crystals

The properties of a solid are mainly determined by the type of bonding that exists between the atoms. According to bonding in crystals they are classified into following types.

(1) **Ionic crystal :** This type of bonding is formed due to transfer of electrons between atoms and consequent attraction between them.

(i) In *NaCl* crystal, the electron of *Na* atom is transferred to chlorine atom. In this way *Na* atom changes in to *Na* ion and *Cl* atom changes into *Cl* ion.

(ii) Cause of binding is electrostatic force between positive and negative ion.

(iii) These crystal are usually hard, brittle and possesses high melting and boiling point.

(iv) These are bad conductor of electricity.

(v) Common example are *NaCl, CsCl, LiF etc.*

(2) **Covalent crystal :** Covalent bonding is formed by sharing of electrons of opposite spins between two atoms

(i) The conductivity of these solids rise with rise in temperature.

(ii) These crystal posses high melting point.

(iii) Bonding between H_2, Cl_2 molecules *Ge*, *Si*, Quartz, diamond *etc.* are common example of covalent bonding

(3) **Metallic bonds :** This type of bonding is formed due to attraction of valence (free) electrons with the positive ion cores

(i) Their conductivity decreases with rise of temperature.

(ii) When visible light falls on a metallic crystal, the electrons of atom absorb visible light, so they are opaque to visible light. However some orbital electrons absorb energy and reach in excited state. They then return to their normal states, remitting light of same frequency.

Common examples are *Na, Li, K, Cs, Au, Hg etc.*

(4) **Vander waal's crystal :** These crystal consists of neutral atoms or molecules bonded together in solid phase by weak, short range attractive forces called vander Waal's forces.

(i) This bonding is weakest and occurs in solid CO_2, methane, paraffin, ice, etc.

(ii) They are normally insulator, they are soft, easily compressible and posses low melting point.

(5) **Hydrogen bonding :** Hydrogen bonding is due to permanent dipole interaction.

(i) This bond is stronger than vander Waal's bond but much weaker than ionic and covalent bond.

(ii) They possesses low melting point.

(iii) Common examples are H_2O, *HF etc.*

Single, Poly and Liquid Crystals

(1) **Single crystal :** The crystals in which the periodicity of the pattern extends throughout the piece of the crystal are known as single crystals. Single crystals have anisotropic behaviour *i.e.* their physical properties (like mechanical strength, refractive index, thermal and electrical conductivity) are different along different directions. The small sized single crystals are called mono-crystals.

(2) **Poly-crystals :** A poly-crystal is the aggregate of the monocrystals whose well developed faces are joined together so that it has isotropic properties. Ceramics are the important illustrations of the poly-crystalline solids.

(3) **Liquid crystals :** The organic crystalline solid which on heating, to a certain temperature range becomes fluid like but its molecules remain oriented in a particular directions, showing that they retain their anisotropic properties, is called liquid crystal. These crystals are used in a liquid crystal displays (L.C.D.) which are commonly used in electronic watches, clocks and micro-calculators *etc.*

Energy Bands

This theory is based on the Pauli exclusion principle.

In isolated atom the valence electrons can exist only in one of the allowed orbitals each of a sharply defined energy called energy levels. But when two atoms are brought nearer to each other, there are alterations in energy levels and they spread in the form of bands.

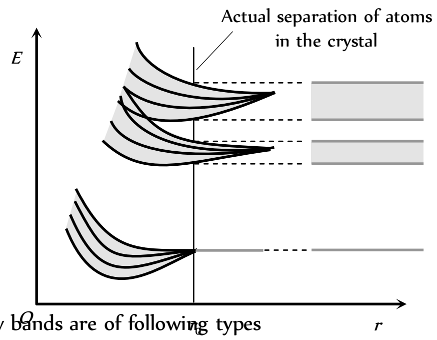


Fig. 27.7 Origin of energy bands in a solid

Energy bands are of following types

(1) **Valence band :** The energy band formed by a series of energy levels containing valence electrons is known as valence band. At 0 *K*, the electrons fills the energy levels in valence band starting from lowest one.

(i) This band is always filled with electrons.

(ii) This is the band of maximum energy.

(iii) Electrons are not capable of gaining energy from external electric field.

(iv) No flow of current due to electrons present in this band.

(v) The highest energy level which can be occupied by an electron in valence band at 0 *K* is called fermi level.

(2) **Conduction band :** The higher energy level band is called the conduction band.

(i) It is also called empty band of minimum energy.

(ii) This band is partially filled by the electrons.

(iii) In this band the electrons can gain energy from external electric field.

(iv) The electrons in the conduction band are called the free electrons. They are able to move any where within the volume of the solid.

(v) Current flows due to such electrons.

(3) **Forbidden energy gap (ΔE) :** Energy gap between conduction band and valence band $\Delta E_g = (C.B.)_{\min} - (V.B.)_{\max}$

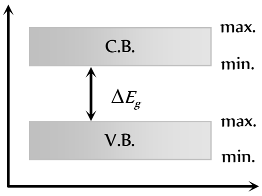


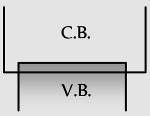
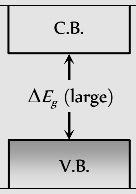
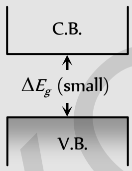
Fig. 27.8

(i) No free electron is present in forbidden energy gap.

(ii) Width of forbidden energy gap depends upon the nature of substance.

(iii) As temperature increases (↑), forbidden energy gap decreases (↓) very slightly.

Table 27.3 : Types of solid

Properties	Conductors	Insulators	Semiconductors
Electrical conductivity	10^2 to 10^8 ℧$/m$	10^{-8} ℧$/m$	10^{-5} to 10^0 ℧$/m$
Resistivity	10^{-2} to 10^{-8} Ω-m (negligible)	10^8 Ω-m	10^5 to 10^0 Ω-m
Band structure			
Energy gap (E_g)	Zero or very small	Very large; for diamond it is 6 *eV*	*Ge* → 0.7 *eV* *Si* → 1.1 *eV* *GaAs* →1.3 *eV* GaF_2 → 2.8 *eV*
Current carriers	Free electrons	––	Free electrons and holes
Condition of V.B. and C.B. at ordinary temperature	V.B. and C.B. are completely filled or C.B. is some what empty	V.B. – completely filled C.B. – completely unfilled	V.B. – somewhat empty C.B. – somewhat filled
Temperature co-efficient of resistance	Positive	Zero	Negative
Effect of temperature on conductivity	Decreases	—	Increases
Effect of temperature on resistance	Increases	—	Decreases
Examples	*Cu, Ag, Au, Na, Pt, Hg* etc.	Wood, plastic, mica, diamond, glass etc.	*Ge, Si, Ga, As* etc.
Electron density	$10^{29}/m^3$	—	*Ge* ~ 10^{19} $/m^3$ *Si* ~ 10^{16} $/m^3$

Holes in Semiconductors

(1) When an electron is removed from a covalent bond, it leaves a vacancy behind. An electron from a neighbouring atom can move into this vacancy, leaving the neighbour with a vacancy. In this way the vacancy formed is called hole (or cotter), and can travel through the material and serve as an additional current carriers.

(2) A hole is considered as a seat of positive charge, having magnitude of charge equal to that of an electron.

(3) Holes acts as virtual charge, although there is no physical charge on it.

(4) Effective mass of hole is more than electron.

(5) Mobility of hole is less than electron.

Intrinsic Semiconductors

(1) A pure semiconductor is called intrinsic semiconductor. It has thermally generated current carriers

(2) They have four electrons in the outermost orbit of atom and atoms are held together by covalent bond

(3) Free electrons and holes both are charge carriers and n_e (in C.B.) $= n_h$ (in V.B.)

(4) The drift velocity of electrons (v_e) is greater than that of holes (v_h)

(5) For them fermi energy level lies at the centre of the C.B. and V.B.

(6) In pure semiconductor, impurity must be less than 1 in 10^8 parts of semiconductor.

(7) In intrinsic semiconductor

$n_e^{(o)} = n_h^{(o)} = n_i$; where $n_e^{(o)} =$ Electron density in conduction band, $n_h^{(o)} =$ Hole density in V.B., $n_i =$ Density of intrinsic carriers.

(8) The fraction of electrons of valance band present in conduction band is given by $f \propto e^{-E_g/kT}$; where E_f = Fermi energy or k = Boltzmann's constant and T = Absolute temperature

(9) Because of less number of charge carriers at room temperature, intrinsic semiconductors have low conductivity so they have no practical use.

(10) Number of electrons reaching from valence band to conduction band $n = AT^{3/2}e^{-E_g/2kT}$

Extrinsic Semiconductor

(1) An impure semiconductor is called extrinsic semiconductor

(2) When pure semiconductor material is mixed with small amounts of certain specific impurities with valency different from that of the parent material, the number of mobile electrons/holes drastically changes. The process of addition of impurity is called doping.

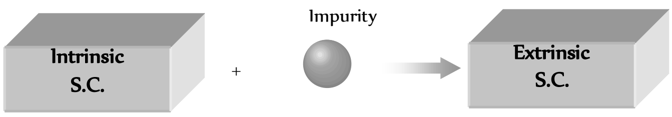


Fig. 27.9

(3) **Pentavalent impurities :** The elements whose atom has five valance electrons are called pentavalent impurities e.g. *As, P, Sb etc.* These impurities are also called donor impurities because they donate extra free electron.

(4) **Trivalent impurities :** The elements whose each atom has three valance electrons are called trivalent impurities e.g. *In, Ga, Al, B, etc.* These impurities are also called acceptor impurities as they accept electron.

(5) The compounds of trivalent and pentavalent elements also behaves like semiconductors *e.g. GaAs, InSb, In P, GaP etc.*

(6) The number of atoms of impurity element is about 1 in 10^8 atoms of the semiconductor.

(7) In extrinsic semiconductors $n_e \neq n_h$

(8) In extrinsic semiconductors fermi level shifts towards valence or conduction energy bands.

(9) Their conductivity is high and they are used for practical purposes.

(10) In a doped extrinsic semiconductor, the number density of e^- of the conduction band (n) and the number density of holes in the valence band (n) differs from that in a pure semiconductor. If n_i is the number density of electron in conduction band or the number density of holes in valence band in a pure semiconductor then $\boldsymbol{n_e n_h} = \boldsymbol{n_i^2}$ (mass action law)

(11) Extrinsic semiconductors are of two types

(i) *N*-type semiconductor (ii) *P*-type semiconductor

N-Type Semiconductor

These are obtained by adding a small amount of pentavalent impurity to a pure sample of semiconductor (Ge).

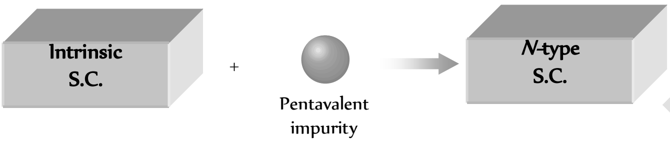


Fig. 27.10

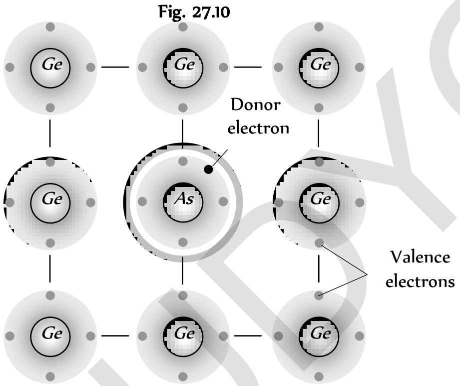


Fig. 27.11

(1) Majority charge carriers – electrons

Minority charge carriers – holes

(2) $n_e >> n_h$; $i_e >> i_h$

(3) Conductivity $\sigma \approx n_e \mu_e e$

(4) *N*-type semiconductor is electrically neutral (not negatively charged)

(5) Impurity is called Donar impurity because one impurity atom generate one electron.

(6) Donor energy level lies just below the conduction band.

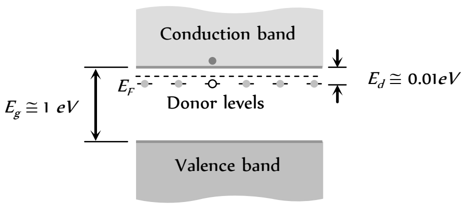
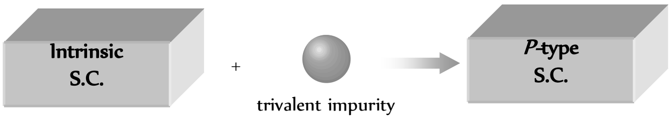


Fig. 27.12

P-Type Semiconductor

These are obtained by adding a small amount of trivalent impurity to a pure sample of semiconductor (Ge).



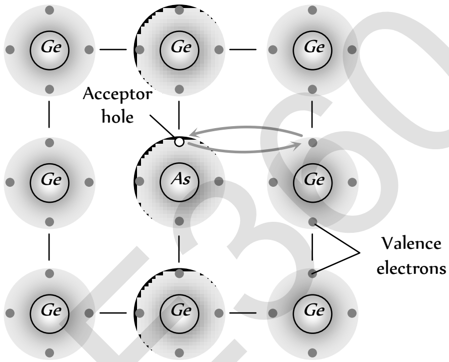


Fig. 27.13

(1) Majority charge carriers – holes

Minority charge carriers – electrons

(2) $n_h >> n_e$; $i_h >> i_e$

(3) Conductivity $\sigma \approx n_h \mu_h e$

(4) *P*-type semiconductor is also electrically neutral (not positively charged)

(5) Impurity is called Acceptor impurity.

(6) Acceptor energy level lies just above the valence band.

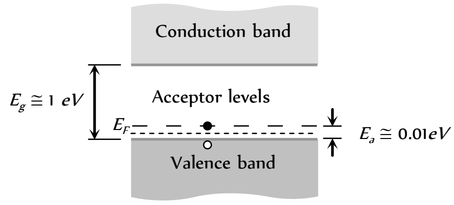


Fig. 27.14

Density of Charge Carriers

Due to thermal collisions, an electron can take up or release energy. Thus, occasionally a valence electron takes up energy and the bond is broken. The electron goes to the conduction band and a hole is created. And occasionally, an electron from the conduction band loses some energy, comes to the valence band and fills up a hole. Thus, new electron-hole pairs are formed as well as old electron-hole disappear. A steady-state situation is reached and the number of electron-hole pairs takes a nearly constant value. For silicon at room temperature (300 *K*), the number of these pairs is about $7 \times 10^{15}\ m$. For germanium, this number is about $6 \times 10^{19}\ /m$.

Table 27. 4 : Densities of charge carriers

Material	Type	Density of conduction electrons (m^{-3})	Density of holes (m^{-3})
Copper	Conductor	9×10^{28}	0
Silicon	Intrinsic semiconductor	7×10^{15}	7×10^{15}
Silicon doped with phosphorus (1 part in 10^6)	*N*-type semiconductor	5×10^{22}	1 $\times 10^9$

Silicon doped with aluminium (1 part in 10^6	P-type semiconductor	1×10^9	5×10^{22}

Conductivity of Semiconductor

(1) In intrinsic semiconductors $n_e = n_h$. Both electron and holes contributes in current conduction.

(2) When some potential difference is applied across a piece of intrinsic semiconductor current flows in it due to both electron and holes *i.e.* $i = i_e + i_h \Rightarrow i = eA[n_e v_e + n_h v_h]$

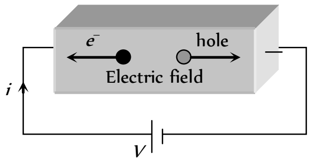


Fig. 27.15

(3) As we know $\sigma = \frac{J}{E} = \frac{i}{AE}$. Hence conductivity of semiconductor

$\sigma = e[n_e \mu_e + n_h \mu_h]$; where v_e = drift velocity of electron, v_h = drift velocity of holes, E = Applied electric field $\mu_e = \frac{v_e}{E}$ = mobility of electron and $\mu_h = \frac{v_h}{E}$ = mobility of holes

(4) Motion of electrons in the conduction band and of holes the valence band under the action of electric field is shown below

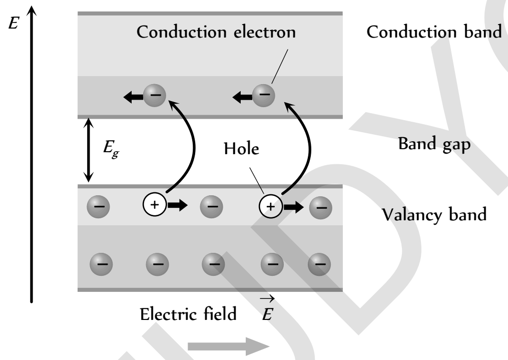


Fig. 27.16

(5) At absolute zero temperature (0 K) conduction band of semiconductor is completely empty *i.e.* $\sigma = 0$. Hence the semiconductor behaves as an insulator.

P-N Junction Diode

When a P-type semiconductor is suitably joined to an N-type semiconductor, then resulting arrangement is called P-N junction or P-N junction diode

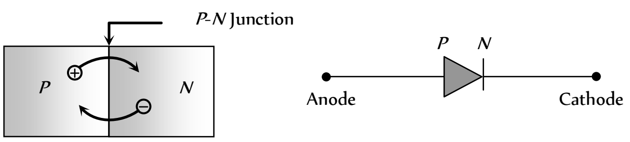


Fig. 27.17

(1) **Depletion region :** On account of difference in concentration of charge carrier in the two sections of P-N junction, the electrons from N-region diffuse through the junction into P-region and the hole from P region diffuse into N-region.

Due to diffusion, neutrality of both N and P-type semiconductor is disturbed, a layer of negative charged ions appear near the junction in the P-crystal and a layer of positive ions appears near the junction in N-crystal. This layer is called depletion layer

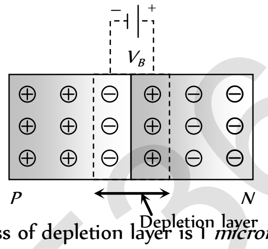


Fig. 27.18

(i) The thickness of depletion layer is 1 *micron* = 10^{-6} *m*.

(ii) Width of depletion layer $\propto \frac{1}{\text{Dopping}}$

(iii) Depletion is directly proportional to temperature.

(iv) The P-N junction diode is equivalent to capacitor in which the depletion layer acts as a dielectric.

(2) **Potential barrier :** The potential difference created across the P-N junction due to the diffusion of electron and holes is called potential barrier.

For *Ge* $V_B = 0.3V$ and for silicon $V_B = 0.7V$

On the average the potential barrier in P-N junction is ~ 0.5 V and the width of depletion region ~ 10^{-6} *m*.

So the barrier electric field $E = \frac{V}{d} = \frac{0.5}{10^{-6}} = 5 \times 10^5 \ V/m$

(3) **Some important graphs**

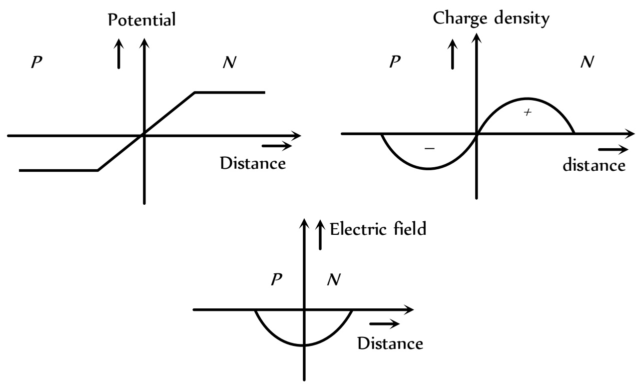


Fig. 27.19

(4) **Diffusion and drift current :** Because of concentration difference holes/electron try to diffuse from their side to other side. Only those holes/electrons crosses the junction, which have high kinetic energy. This diffusion results in an electric current from the P-side to the N-side known as diffusion current (i_{df})

As electron hole pair (because of thermal collisions) are continuously created in the depletion region. There is a regular flow of electrons towards the N-side and of holes towards the P-side. This makes a current from the N-side to the P-side. This current is called the drift current (i_{dr}).

Biasing

It means the way of connecting emf source to *P-N* junction diode. It is of following two types

(1) **Forward biasing :** Positive terminal of the battery is connected to the *P*-crystal and negative terminal of the battery is connected to *N*-crystal

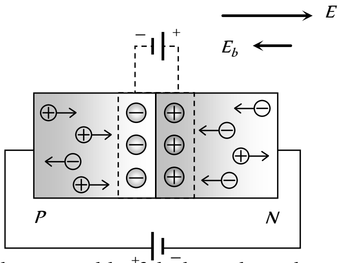


Fig. 27.20

(i) In forward biasing width of depletion layer decreases

(ii) In forward biasing resistance offered $R_{forward} \approx 10\Omega$ - 25Ω

(iii) Forward bias opposes the potential barrier and for $V > V_B$ a forward current is set up across the junction.

(iv) The current is given by $i = i_s(e^{eV/kT} - 1)$; where

$i_s =$ Saturation current, In the exponent $e = 1.6 \times 10^{-19}$ *C*,

k = Boltzmann's constant

(v) Cut-in (Knee) voltage : The voltage at which the current starts to increase rapidily. For *Ge* it is 0.3 *V* and for *Si* it is 0.7 *V*.

(vi) *df* – diffusion

dr – drift

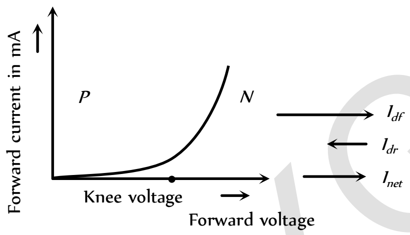


Fig. 27.21

(2) **Reverse biasing :** Positive terminal of the battery is connected to the *N*-crystal and negative terminal of the battery is connected to *P*-crystal

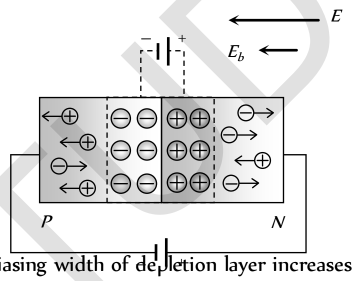


Fig. 27.22

(i) In reverse biasing width of depletion layer increases

(ii) In reverse biasing resistance offered $R_{Reverse} \approx 10\Omega$

(iii) Reverse bias supports the potential barrier and no current flows across the junction due to the diffusion of the majority carriers.

(A very small reverse currents may exist in the circuit due to the drifting of minority carriers across the junction)

(iv) Break down voltage : Reverse voltage at which break down of semiconductor occurs. For *Ge* it is 25 *V* and for *Si* it is 35 *V*.

(v)

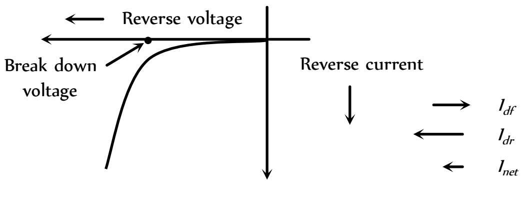


Fig. 27.23

Reverse Breakdown

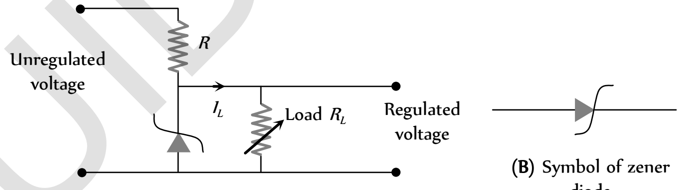
If the reverse biased voltage is too high, then breakdown of *P-N* junction diode occurs. It is of following two types

(1) **Zener breakdown :** When reverse bias is increased the electric field across the junction also increases. At some stage the electric field becomes so high that it breaks the covalent bonds creating electron, hole pairs. Thus a large number of carriers are generated. This causes a large current to flow. This mechanism is known as **Zener breakdown.**

(2) **Avalanche breakdown :** At high reverse voltage, due to high electric field, the minority charge carriers, while crossing the junction acquires very high velocities. These by collision breaks down the covalent bonds, generating more carriers. A chain reaction is established, giving rise to high current. This mechanism is called **avalanche breakdown.**

Special Purpose Diodes

(1) **Zener diode :** It is a highly doped *p-n* junction which is not damaged by high reverse current. It can operate continuously, without being damaged in the region of reverse background voltage. In the forward bias, the zener diode acts as ordinary diode. It can be used as voltage regulator



(A) Zener diode as a voltage regulator

(B) Symbol of zener diode

Fig. 27.24

(2) **Light emitting diode (LED :** Specially designed diodes, which give out light radiations when forward biases. LED'S are made of *GaAsp*, *Gap etc*.

These are forward biased *P-N*-junctions which emits spontaneous radiation.

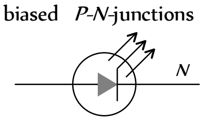


Fig. 27.25

(3) **Photo diode:** Photodiode is a special type of photo-detector. Suppose an optical photons of frequency ν is incident on a semiconductor, such that its energy is greater than the band gap of the semiconductor (*i.e.* $h\nu > E_g$) This photon will excite an electron from the valence band to the conduction band leaving a vacancy or hole in the valence band.

Which obviously increase the conductivity of the semiconductor. Therefore, by measuring the change in the conductance (or resistance) of the semiconductor, one can measure the intensity of the optical signal.

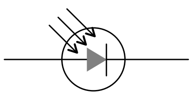


Fig. 27.26

(4) **Solar cells :** It is based on the photovoltic effect. One of the semiconductor region is made so thin that the light incident on it reaches the *P-N*-junction and gets absorbed. It converts solar energy into electrical energy.

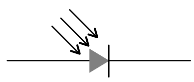


Fig. 27.27

P-N Junction Diode as a Rectifier

Rectifier is a circuit which converts *ac* to unidirectional pulsating output. In other words it converts *ac* to *dc*. It is of following two types

(1) **Half wave rectifier :** When the *P-N* junction diode rectifies half of the *ac* wave, it is called half wave rectifier

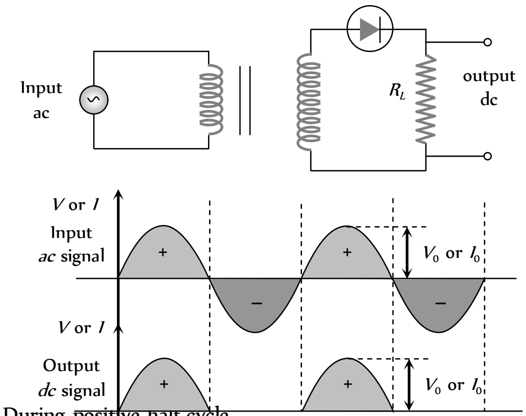


Fig. 27.28

(i) During positive half cycle

Diode $\longrightarrow$ forward biased

Output signal $\longrightarrow$ obtained

(ii) During negative half cycle

Diode $\longrightarrow$ reverse biased

Output signal $\longrightarrow$ not obtained

(iii) Output voltage is obtained across the load resistance R_L. It is not constant but pulsating (mixture of *ac* and *dc*) in nature .

(iv) Average output in one cycle

$$I_{dc} = \frac{I_0}{\pi} \text{ and } V_{dc} = \frac{V_0}{\pi};\ I_0 = \frac{V_0}{r_f + R_L}$$

(r_f = forward biased resistance)

(v) r.m.s. output : $I_{rms} = \frac{I_0}{2}, V_{rms} = \frac{V_0}{2}$

(vi) The ratio of the effective alternating component of the output voltage or current to the *dc* component is known as ripple factor.

$$r = \frac{I_{ac}}{I_{dc}} = \left[\left(\frac{I_{rms}}{I_{dc}}\right)^2 - 1\right]^{1/2} = 1.21$$

(vii) Peak inverse voltage (PIV) : The maximum reverse biased voltage that can be applied before commoncement of Zener region is called the PIV. When diode is not conducting PIV across it = V_0

(viii) Efficiency : It is given by $\%\eta = \frac{P_{out}}{P_{in}} \times 100 = \frac{40.6}{1 + \frac{r_f}{R_L}}$

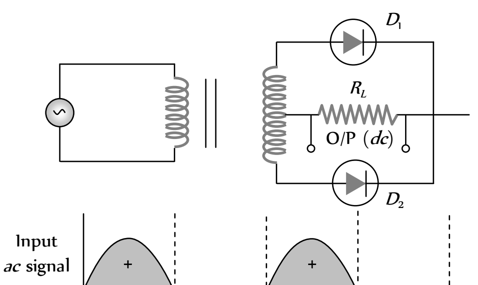
If $R_L >> r_f$ then η = 40.6%

If $R_L = r_f$ then η = 20.3%

(ix) Form factor = $\frac{I_{rms}}{I_{dc}} = \frac{\pi}{2} = 1.57$

(x) The ripple frequency (ω) for half wave rectifier is same as that of *ac*.

(2) **Full wave rectifier :** It rectifies both halves of *ac* input signal.



(i) During positive half cycle

Diode : D_1 $\longrightarrow$ forward biased

D_2 $\longrightarrow$ reverse biased

Output signal $\longrightarrow$ obtained due to D_1 only

(ii) During negative half cycle

Diode : D_1 $\longrightarrow$ reverse biased

D_2 $\longrightarrow$ forward biased

Output signal $\longrightarrow$ obtained due to D_2 only

(iii) Fluctuating *dc* $\longrightarrow$ Filter $\longrightarrow$ constant *dc*.

(iv) Output voltage is obtained across the load resistance R_L. It is not constant but pulsating in nature.

(v) Average output : $V_{av} = \frac{2V_0}{\pi}, I_{av} = \frac{2I_0}{\pi}$

(vi) *r.m.s.* output : $V_{rms} = \frac{V_0}{\sqrt{2}}, I_{rms} = \frac{I_0}{\sqrt{2}}$

(vii) Ripple factor : r = 0.48 = 48%

(viii) Ripple frequency : The ripple frequency of full wave rectifier = 2 × (Frequency of input *ac*)

(ix) Peak inverse voltage (PIV) : It's value is $2V_0$

(x) Efficiency : $\eta_{\%} = \frac{81.2}{1 + \frac{r_f}{R_L}}$ for $r_f << R_L$, $\eta = 81.2\%$

(3) **Full wave bridge rectifier :** Four diodes D_1, D_2, D_3 and D_4 are used in the circuit.

During positive half cycle D_1 and D_3 are forward biased and D_2 and D_4 are reverse biased

During negative half cycle D_2 and D_4 are forward biased and D_1 and D_3 are reverse biased

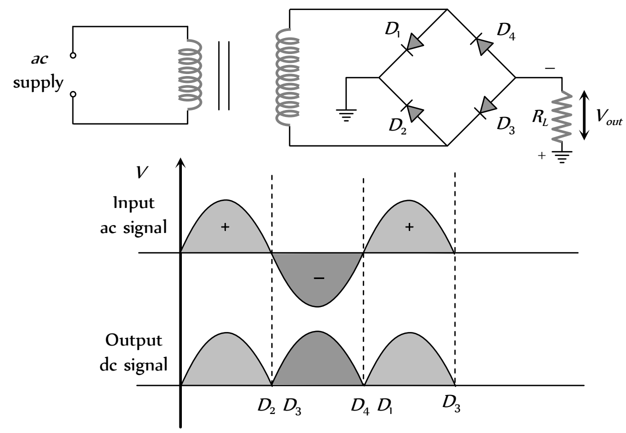


Fig. 27.30

Transistor

(1) The name of this electronic device is derived from it's fundamental action transfer resistor.

(2) Transistor does not need any heater or hot filament, transistor is small in size and light in weight.

(3) Transistor in general is known as bipolar junction transistor.

(4) Transistor is a current operated device.

(5) It consists of three main regions

(i) **Emitter (*E*) :** It provides majority charge carriers by which current flows in the transistor. Therefore the emitter semiconductor is heavily doped.

(ii) **Base (*B*) :** The based region is lightly doped and thin.

(iii) **Collector (*C*) :** The size of collector region is larger than the two other regions.

(6) Junction transistor are of two types :

(i) *NPN* transistor : It is formed by sandwiching a thin layer of *P*-type semiconductor between two *N*-type semiconductors

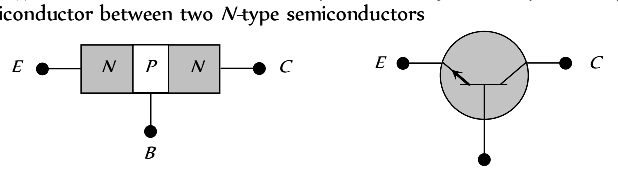


Fig. 27.31

In *NPN* transistor electrons are majority charge carriers and flow from emitter to base.

(ii) *PNP* transistor : It is formed by sandwiching a thin layer of *N*-type semiconductor between two *P*-type semiconductor

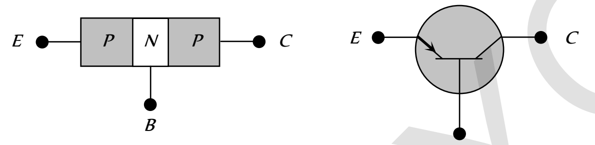


Fig. 27.32

In *PNP* transistor holes are majority charge carriers and flow from emitter to base.

In the symbols of both *NPN* and *PNP* transistor, arrow indicates the direction of conventional current.

Working of Transistor

(1) There are four possible ways of biasing the two *P-N* junctions (emitter junction and collector junction) of transistor.

(i) Active mode : Also known as linear mode operation.

(ii) Saturation mode : Maximum collector current flows and transistor acts as a closed switch from collector to emitter terminals.

(iii) Cut-off mode : Denotes operation like an open switch where only leakage current flows.

(iv) Inverse mode : The emitter and collector are inter changed.

Table 27.5 : Different modes of operation of a transistor

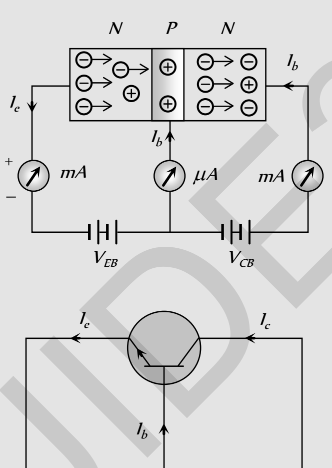
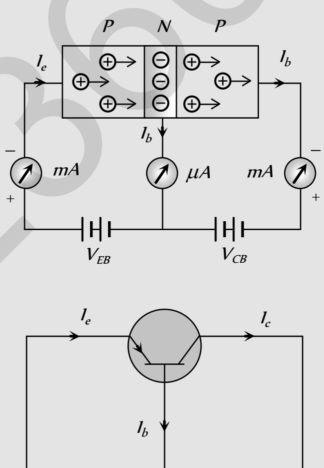
Operating mode	Emitter base bias	Collector base bias
Active	Forward	Reverse
Saturation	forward	Forward
Cut off	Reverse	Reverse
Inverse	Reverse	Forward

(2) A transistor is mostly used in the active region of operation *i.e.* emitter base junction is forward biased and collector base junction is reverse biased.

(3) From the operation of junction transistor it is found that when the current in emitter circuit changes. There is corresponding change in collector current.

(4) In each state of the transistor there is an input port and an output port. In general each electrical quantity (*V* or *I*) obtained at the output is controlled by the input.

Table 27.6 : Circuit diagram of *PNP*/*NPN* transistor

NPN – transistor	*PNP* – transistor
	
5% emitter electron combine with the holes in the base region resulting in small base current. Remaining 95% electrons enter the collector region.	5% emitter holes combine with electrons in the base region resulting in small base current. Remaining 95% holes enter the collector region.
$I_e > I_c$, and $I_e = I_b + I_c$	$I_e > I_c$, and $I_e = I_b + I_c$

Transistor Configurations

A transistor can be connected in a circuit in the following three different configurations.

Common base (CB), Common emitter (CE) and Common collector (CC) configuration.

(1) **CB configurations :** Base is common to both emitter and collector .

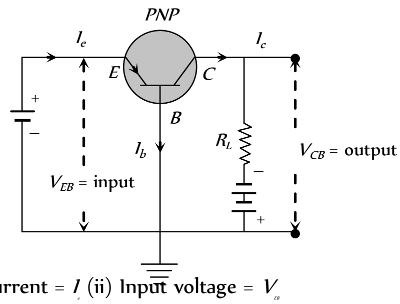


Fig. 27.33

(i) Input current = I_e (ii) Input voltage = V_{EB}

(iii) Output voltage = V_{CB} (iv) Output current = I_c

With small increase in emitter-base voltage V_{EB}, the emitter current I_e increases rapidly due to small input resistance.

(v) **Input characteristics :** If V_{CB} = constant, curve between I_e and V_{EB} is known as input characteristics. It is also known as emitter characteristics

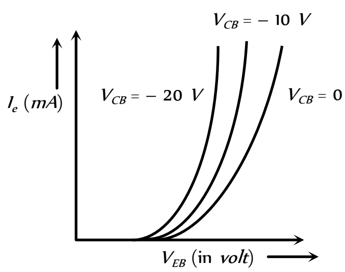


Fig. 27.34

Input characteristics of *NPN* transistor are also similar to the above figure but I_e and V_{eb} both are negative and V_{cb} is positive.

Dynamic input resistance of a transistor is given by

$$R_i = \left(\frac{\Delta V_{EB}}{\Delta I_e}\right)_{V_{CB} = \text{constant}} \qquad \{ R_i \text{ is of the order of } 100\ \Omega\}$$

(vi) **Output characteristics :** Taking the emitter current i_e constant, the curve drawn between I_c and V_{cb} are known as output characteristics of *CB* configuration.

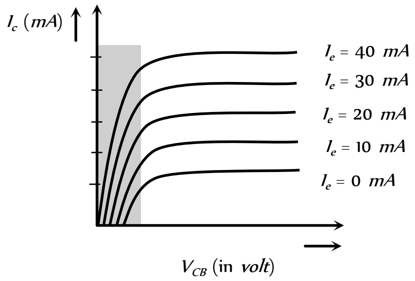


Fig. 27.35

Dynamic output resistance $R_o = \left(\frac{\Delta V_{CB}}{\Delta i_C}\right)_{i_e = \text{constant}}$

(2) **CE configurations :** Emitter is common to both base and collector.

The graphs between voltages and currents when emitter of a transistor is common to input and output circuits are known as CE characteristics of a transistor.

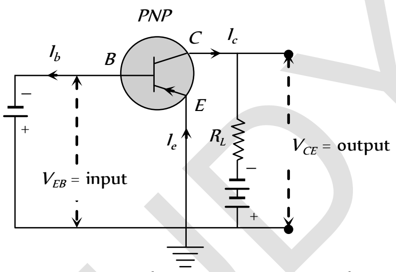


Fig. 27.36

Input characteristics : Input characteristic curve is drawn between base current I_b and emitter base voltage V_{eb}, at constant collector emitter voltage V_{ce}.

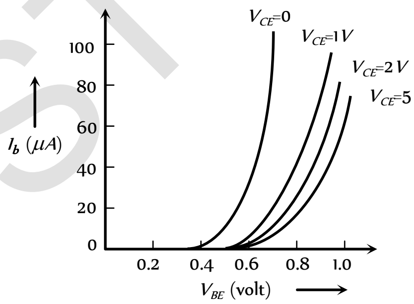


Fig. 27.37

Dynamic input resistance $R_i = \left(\frac{\Delta V_{BE}}{\Delta I_B}\right)_{V_{CE} \to \text{constant}}$

Output characteristics : Variation of collector current I_c with V_{ce} can be noticed for V_{ce} between 0 to 1 *V* only. The value of V_{ce} up to which the I_c changes with V_{ce} is called knee voltage. The transistor are operated in the region above knee voltage.

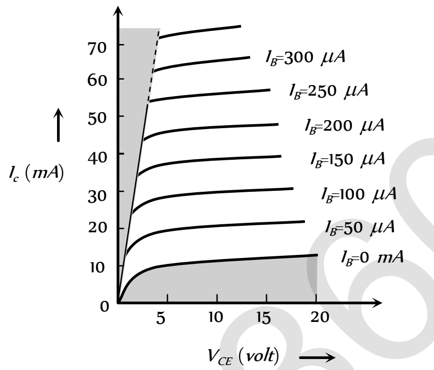


Fig. 27.38

Dynamic output resistance $R_0 = \left(\frac{\Delta V_{CE}}{\Delta I_C}\right)_{I_B \to \text{constant}}$

Field-Effect Transistor

The low input impedance of the junction transistor is a handicap in certain applications. In addition, it is difficult to incorporate large numbers of them in an integrated circuit and they consume relatively large amounts of power. The field-effect transistor (FET) lacks these disadvantages and is widely used today although slower in operation than junction transistors.

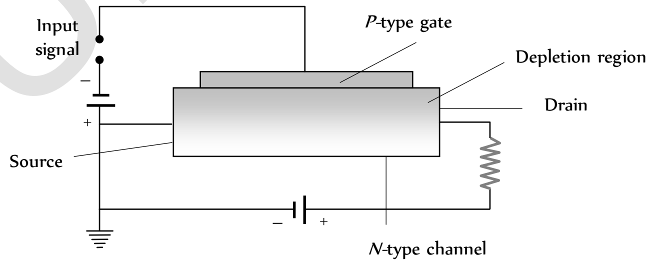


Fig. 27.39

An *n*-channel FET consists of a block of *N*-type material with contacts at each end together with a strip of *P*-type material on one side that is called the gate. When connected as shown, electrons move from the source terminal to the drain terminal through the *N*-type channel. the *PN* junction is given a reverse bias, and as a result both the *N* and *P* materials near the junction are depleted on charge carriers. The higher the reverse potential on the gate, the larger the depleted region in the channel and the fewer the electrons available to carry the current. Thus the gate voltage controls the channel current. Very little current passes through the gate circuit owing to the reverse bias, and the result is an extremely high input impedance. FET is uni-polar.

Transistor as an Amplifier

A device which increases the amplitude of the input signal is called amplifier.

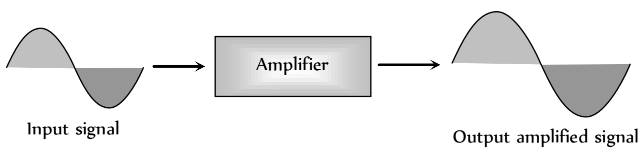


Fig. 27.40

The transistor can be used as an amplifier in the following three configuration

(i) CB amplifier (ii) CE amplifier (iii) CC amplifier

(1) ***NPN* transistor as CB amplifier**

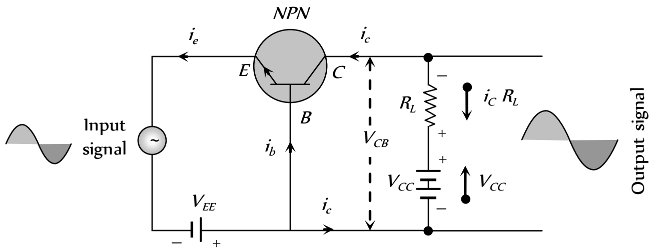


Fig. 27.41

(i) $i_e = i_b + i_C$; i_b = 5% of i_e and i_C = 95% of i_e

(ii) $V_{EE} < V_{CC}$

(iii) Net collector voltage $V_{CB} = V_{CC} - i_C R_L$

When the input signal (signal to be amplified) is fed to the emitter base circuit, it will change the emitter voltage and hence emitter current. This in turn will change the collector current (i_c). This will vary the collector voltage V_{CB}. This variation of V_{CB} will appear as an amplified output.

(iv) Input and output signals are in same phase

(2) ***NPN* transistor as *CE* amplifier**

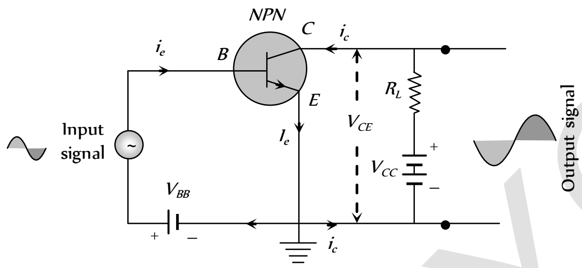


Fig. 27.42

(i) $i_e = i_b + i_C$; i_b = 5% of i_e and i_C = 95% of i_e

(ii) $V_{CC} > V_{BB}$

(iii) Net collector voltage $V_{CE} = V_{CC} - i_C R_L$

(iv) Input and output signals are 180° out of phase.

Different Gains in CE/CB Amplifiers

(1) **Transistor as CB amplifier**

(i) *ac* current gain $\alpha_{ac} = \dfrac{\text{Small change in collector current } (\Delta i_c)}{\text{Small change in collector current } (\Delta i_e)}$

V_{B} (constant)

(ii) *dc* current gain $\alpha_{dc} (\text{or } \alpha) = \dfrac{\text{Collector current} (i_c)}{\text{Emitter current } (i_e)}$

valve of α_{dc} lies between 0.95 to 0.99

(iii) Voltage gain $A_v = \dfrac{\text{Change in output voltage} (\Delta V_o)}{\text{Change in input voltage} (\Delta V_i)}$

$\Rightarrow$ $A_v = \alpha_{ac} \times$ Resistance gain

(iv) $\text{Power gain} = \dfrac{\text{Change in output power} (\Delta P_o)}{\text{Change in input power} (\Delta P_c)}$

$\Rightarrow \text{Power gain} = \alpha_{ac}^2 \times \text{Resistance gain}$

(2) **Transistor as CE amplifier**

(i) *ac* current gain $\beta_{ac} = \left(\dfrac{\Delta i_c}{\Delta i_b}\right)$ V_{CE} = constant

(ii) *dc* current gain $\beta_{dc} = \dfrac{i_c}{i_b}$

(iii) Voltage gain : $A_v = \dfrac{\Delta V_o}{\Delta V_i} = \beta_{ac} \times \text{Resistance gain}$

(iv) $\text{Power gain} = \dfrac{\Delta P_o}{\Delta P_i} = \beta_{ac}^2 \times \text{Resistance gain}$

(v) Trans conductance (g_m) : The ratio of the change in collector current to the change in emitter base voltage is called trans conductance. *i.e.* $g_m = \dfrac{\Delta i_c}{\Delta V_{EB}}$. Also $g_m = \dfrac{A_V}{R_L}$; R_L = Load resistance

(3) **Relation between α and β** : $\beta = \dfrac{\alpha}{1-\alpha}$ or $\alpha = \dfrac{\beta}{1+\beta}$

Transistor as an Oscillator

(1) It is defined as a circuit which generates an *ac* output signal without any externally applied input signal.

Audio frequency oscillators generates signals of frequencies ranging from a few *Hz* to 20 *kHz* and radio frequency oscillators have a range from few *kHz* to *MHz*.

(2) In an oscillator the frequency, waveform, and magnitude of *ac* power generated is controlled by circuit itself.

(3) An oscillator may be considered as amplifier which provides it's own input signal.

(4) The essential of a transistor oscillator are

(i) **Tank circuit :** Parallel combination of *L* and *C*. This network resonates at a frequency $\nu_0 = \dfrac{1}{2\pi}\sqrt{\dfrac{1}{LC}}$.

(ii) **Amplifier :** It receives *dc* power from the battery and converts into *ac* power.

The amplifier increases the strength of oscillations.

(iii) **Feed back circuit :** This circuit supplies a part of the collector energy to the tank circuit.

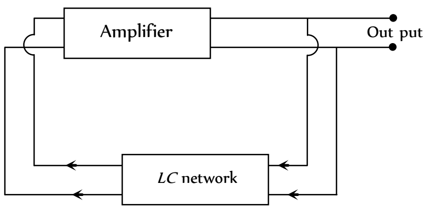


Fig. 27.43

(5) A basic common-emitter *NPN* oscillator is shown in the figure.

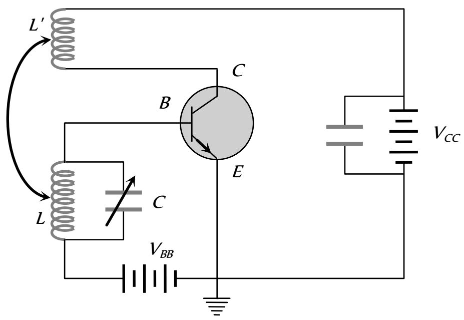


Fig. 27.44

A tank circuit (*L-C* circuit) is connected in the base-emitter circuit, in which the capacitance C is kept variable. By changing C oscillations of a desired frequency can be obtained. An inductance coil L' connected in the collector-emitter circuit is coupled to coil L.

On completion of the circuit electrical oscillations are developed in the tank circuit. The circuit amplifies these oscillations. A part of the amplifies signal in the collector circuit is fed back in the base circuit by the coupling between L and L'. Due to this feed back amplitude of oscillation builds up till power dissipation in the oscillatory circuit becomes equal to power fed-back. In this state the amplitude of oscillations becomes constant.

The oscillations can be transferred to an external circuit by mutual induction in a coil connected in that circuit.

(6) **Need for positive feedback :** The oscillations are damped due to the presence of some inherent electrical resistance in the circuit. Consequently, the amplitude of oscillations decreases rapidly and the oscillations ultimately stop. Such oscillations are of little practical importance. In order to obtain oscillations of constant amplitude, we make an arrangement for regenerative or positive feedback from the output circuit to the input circuit so that the losses in the circuit can be compensated.

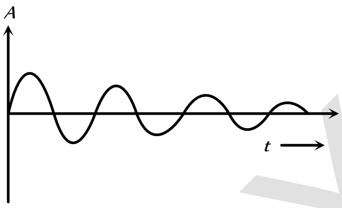


Fig. 27.45

Table 27.7: Comparison between CB, CE and CC amplifier

Characteristic	Amplifier		
	CB	CE	CC
Input resistance (R_i)	≈ 50 to 200 Ω low	≈ 1 to 2 *k*Ω medium	≈ 150 – 800 *k*Ω high
Output resistance (R_o)	≈ 1 – 2 *k*Ω high	≈ 50 *k*Ω medium	≈ *k*Ω low
Current gain	0.8 – 0.9 low	20 – 200 high	20 – 200 high
Voltage gain	Medium	High	Low
Power gain	Medium	High	Low
Phase difference between input and output voltages	Zero	180°	Zero
Used as amplifier for	current	Power	Voltage

Digital Electronics

Decimal and Binary Number System

(1) **Decimal number system :** In a decimal number system, we have ten digits *i.e.* 0, 1, 2, 3, 4, 5, 6, 7, 8, 9.

A decimal number system has a base of ten (10)

e.g. 1971 = 1000 + 900 + 70 + 1

= $1 \times 10^3 + 9 \times 10^2 + 7 \times 10^1 + 1 \times 10^0$

MSD LSD

LSD = Least significant digit

MSD = Most significant digit

(2) **Binary number system :** A number system which has only two digits *i.e.* 0 (Low) and 1 (High) is known as binary system. The base of binary number system is 2.

(i) Each digit in binary system is known as a bit and a group of bits is known as a byte.

(ii) The electrical circuit which operates only in these two state *i.e.* 1 (On or High) and 0 (*i.e.* Off or Low) are known as digital circuits.

Table 27. 8 : Different names for the digital signals

State Code	1	0
Name for the State	On	Off
	Up	Down
	Close	Open
	Excited	Unexcited
	True	False
	Pulse	No pulse
	High	Low
	Yes	No

(3) **Decimal to binary conversion**

(i) Divide the given decimal number by 2 and the successive quotients by 2 till the quotient becomes zero.

(ii) The sequence of remainders obtained during divisions gives the binary equivalent of decimal number.

(iii) the most significant digit (or bit) of the binary number so obtained is the last remainder and the least significant digit (or bit) is the first remainder obtained during the division.

***For Example* :** Binary equivalence of 61

2	61	Remainder
2	30	1 LSD
2	15	0

2	7	1
2	3	1
2	1	1
	0	1 MSD

$\Rightarrow (61)_{10} = (111101)_2$

(4) **Binary to decimal conversion :** The least significant digit in the binary number is the coefficient of 2 with power zero. As we move towards the left side of LSD, the power of 2 goes on increasing.

For Example **:** $(11111100101)_2 = 1 \times 2^{10} + 1 \times 2^9 + 1 \times 2^8 + 1 \times 2^7 + 1 \times 2^6 + 1 \times 2^5 + 0 \times 2^4 + 0 \times 2^3 + 1 \times 2^2 + 0 \times 2^1 + 1 \times 2^0 = 2021$

Voltage Signal

(1) **Analogue voltage signal :** The signal which represents the continuous variation of voltage with time is known as analogue voltage signal

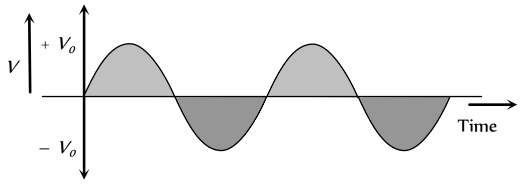


Fig. 27.46

(2) **Digital voltage signal :** The signal which has only two values. *i.e.* either a constant high value of voltage or zero value is called digital voltage signal

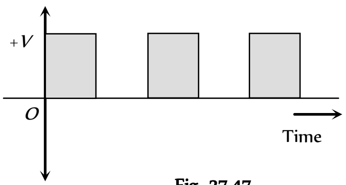


Fig. 27.47

Boolean Algebra

(1) In Boolean algebra only two states of variables (0 and 1) are allowed.

(2) The variables (A, B, C ....) of Boolean Algebra are subjected to three operations.

(i) **OR Operation :** Represented by (+) sign

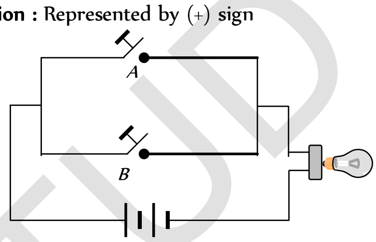


Fig. 27.48

Boolean expression $Y = A + B$

When switch A or B is closed – Bulb glows

(ii) **AND Operation :** Represented by (·) sign

Boolean expression $Y = A \cdot B$

When switches A and B both are closed – Bulb glows

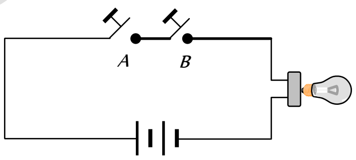
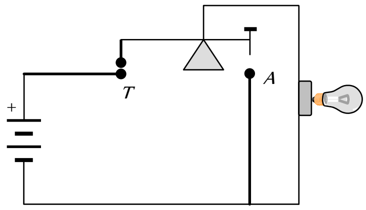


Fig. 27.49

(iii) **NOT Operation :** Represented by bar over the variables

Boolean expression $Y = \overline{A}$



A OFF $\rightarrow$ Lamp ON

A ON $\rightarrow$ Contact at T is broken

$\rightarrow$ Lamp OFF

Fig. 27.50

(3) **Basic Boolean postulates and laws**

(i) Boolean Postulates : $0 + A = A$, $\quad 1 \cdot A = A$,

$1 + A = 1$, $\quad 0 \cdot A = 0$,

$A + \overline{A} = 1$

(ii) Identity law : $A + A = A$, $\quad A \cdot A = A$

(iii) Negation law : $\overline{\overline{A}} = A$

(iv) Commutative law : $A + B = B + A$, $\quad A \cdot B = B \cdot A$

(v) Associative law : $(A+B) + C = A + (B+C)$,

$(A \cdot B) \cdot C = A \cdot (B \cdot C)$

(vi) Distributive law : $A \cdot (B+C) = A \cdot B + A \cdot C$

$(A + B) \cdot (A + C) = A + BC$

(vii) Absorption laws : $A + A \cdot B = A$, $\quad A \cdot (A + B) = A$

$\overline{A} \cdot (A + B) = \overline{A} \cdot B$

(viii) Boolean identities : $A + \overline{A}B = A + B$, $A(\overline{A} + B) = AB$,

$A + BC = (A + B)(A + C)$, $(\overline{A} + B) \cdot (A + C) = \overline{A}C + AB$

(ix) **De Morgan's theorem** : It states that the complement of the whole sum is equal to the product of individual complements and vice versa *i.e.* $\overline{A + B} = \overline{A} \cdot \overline{B}$ and $\overline{A \cdot B} = \overline{A} + \overline{B}$

Logic Gates and Truth Table

(1) **Logic gate :** The digital circuit that can be analysed with the help of Boolean algebra is called logic gate or logic circuit. A logic gate has two or more inputs but only one output.

There are primarily three logic gates namely the OR gate, the AND gate and the NOT gate.

(2) **Truth table :** The operation of a logic gate or circuit can be represented in a table which contains all possible inputs and their corresponding outputs is called the truth table. To write the truth table we use binary digits 1 and 0.

The 'OR' Gate

(1) It has two inputs (A and B) and only one output (Y)

(2) Boolean expression is $Y = A + B$ and is read as "Y equals A **OR** B"

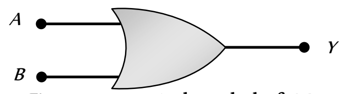
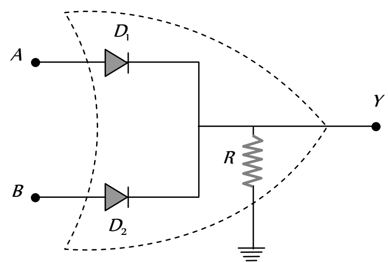


Fig. 27.51 : Logical symbol of OR gate

(3) **Realization of OR gate**



(i) $A = 0$, $B = 0$

Both diodes D_1 and D_2 do not conduct and hence $Y = 0$

(ii) $A = 0$, $B = 1$

D_1 = Does not conducts, D_2 = Conducts, hence $Y = 1$

(iii) $A = 1$, $B = 0$

D_1 = Conducts, D_2 = Does not conduct, hence $Y = 1$

(iv) $A = 1$, $B = 1$

Both D_1 and D_2 conducts, hence $Y = 1$

(4) **Truth table for 'OR' gate**

A	B	$Y = A + B$
0	0	0
0	1	1
1	0	1
1	1	1

The 'AND' Gate

(1) It has two inputs (A and B) and only one output (Y)

(2) Boolean expression is $Y = A \cdot B$ is read as " Y equals A AND B"

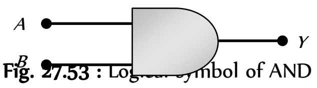


Fig. 27.53 : Logical symbol of AND gate

(3) **Realization of AND gate**

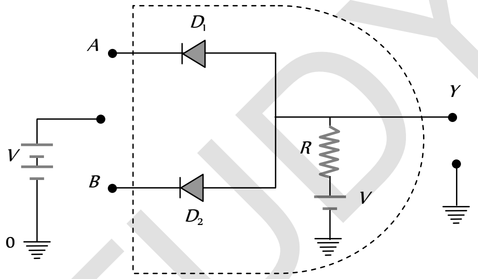


Fig. 27.54

(i) $A = 0$, $B = 0$

The voltage supply through R is forward biasing diodes D_1 and D_2 (offers low resistance) the voltage V would drop across R

The output voltage at Y = the voltage across diode = 0

(ii) $A = 0$, $B = 1$

D_1 = conducts, D_2 = Not Conducts

the out voltage at Y= The voltage across the diode (D) =0

(iii) $A = 1$, $B = 0$

D_1 = Conducts, D_2 = Not conducts

the out voltage at Y= The voltage across the diode (D_1) =0

iv) $A = 1$, $B = 1$

None of the diode conducts

the out voltage at Y= Battery voltage =1

(4) **Truth table for 'AND' gate**

A	B	$Y = A . B$
0	0	0
0	1	0
1	0	0
1	1	1

The 'NOT' Gate

(1) It has only one input and only one output.

(2) Boolean expression is $Y = \overline{A}$ and is read as "y equals not A"

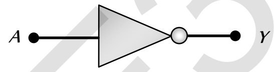


Fig 27.55 : Logical symbol of NOT gate

(3) **Realization of NOT gate :** The transistor is so biased that the collector voltage $V_{cc} = V$ (Voltage corresponding to 1 state)

The resistors R and R_1 are so chosen that if the input is low *i.e.* O, the transistor is in the cut off and hence the voltage appearing at the output will be the same as applied V. Hence $Y = V$ (or state 1)

If the input is high, the transistor current is in saturation and the net voltage at the output Y is 0 (in state 0)

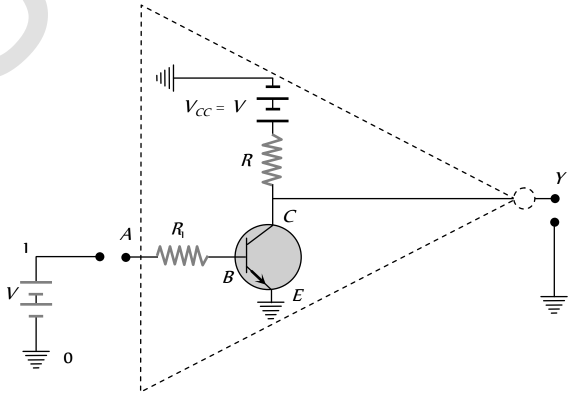


Fig. 27.56

(4) **Truth table for NOT gate :**

A	$Y = \overline{A}$
0	1
1	0

Combination of Logic Gates

(1) **The 'NAND' gate :** From 'AND' and 'NOT' gate

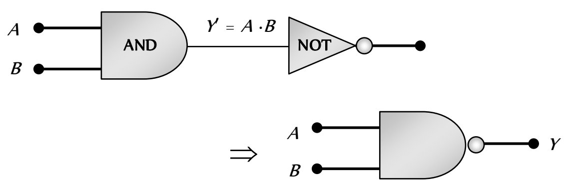


Fig. 27.57

Boolean expression and truth table : $Y = \overline{A \cdot B}$

A	B	$Y' = A \cdot B$	Y
0	0	0	1
0	1	0	1
1	0	0	1
1	1	1	0

(2) **The 'NOR' gate :** From 'OR' and 'NOT' gate

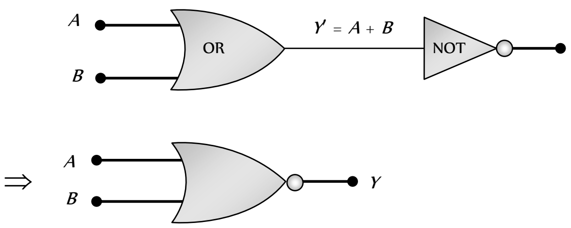


Fig. 27.58

Boolean expression and truth table : $Y = \overline{A + B}$

A	B	$Y' = A + B$	Y
0	0	0	1
0	1	1	0
1	0	1	0
1	1	1	0

(3) **The 'XOR' gate :** From 'NOT', 'AND' and 'OR' gate. Known as exclusive OR gate.

or

The logic gate which gives high output (*i.e.*, 1) if either input A or input B but not both are high (*i.e.* 1) is called exclusive OR gate or the XOR gate.

It may be noted that if both the inputs of the XOR gate are high, then the output is low (*i.e.*, 0).

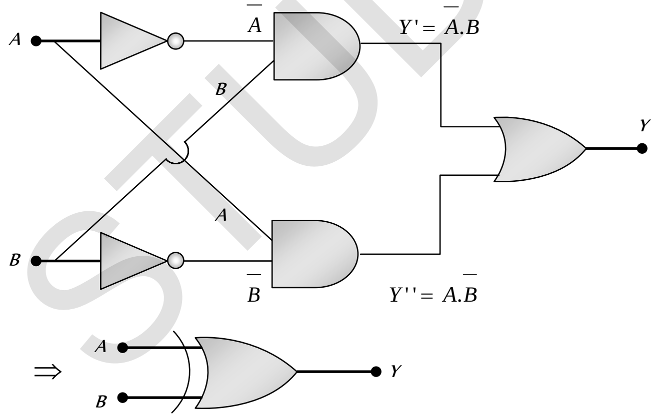


Fig. 27.59

Boolean expression and truth table : $Y = A \oplus B = \overline{A}B + A\overline{B}$

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

(4) **The exclusive nor (XNOR) gate**

XOR + NOT $\longrightarrow$ XNOR

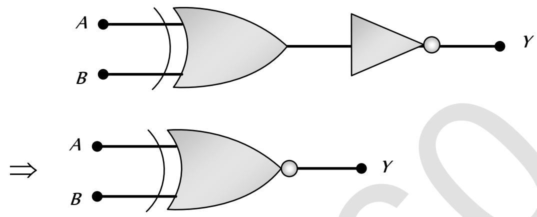


Fig. 27.60

Boolean expression : $Y = A \odot B = \overline{A}\,\overline{B} + AB$

Logic Gates Using 'NAND' Gate

The NAND gate is the building block of the digital electronics. All the logic gates like the OR, the AND and the NOT can be constructed from the NAND gates.

(1) **Construction of the 'NOT' gate from the 'NAND' gate**

(i) When both the inputs (A and B) of the NAND gate are joined together then it works as the NOT gate.

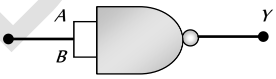


Fig. 27.61

(ii) Truth table and logic symbol

Input	Output
$A = B$	Y
0	1
1	0

(2) **Construction of the 'AND' gate from the 'NAND' gate**

(i) When the output of the NAND gate is given to the input of the NOT gate (made from the NAND gate), then the resultant logic gate works as the AND gate

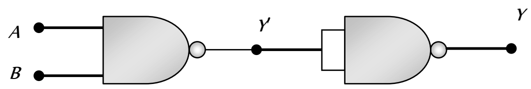


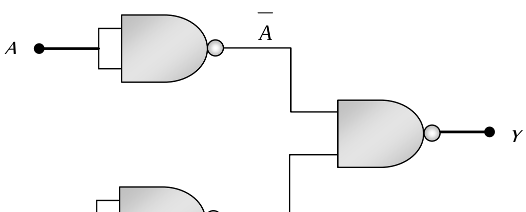
Fig. 27.62

(ii) Truth table and logic symbol

A	B	Y'	Y
0	0	1	0
0	1	1	0
1	0	1	0
1	1	0	1

(3) **Construction of the 'OR' gate by the 'NAND' gate**

(i) When the outputs of two NOT gates (obtained from the NAND gate) is given to the inputs of the NAND gate, the resultant logic gate works as the OR gate



(ii) Truth table and logic symbol

A	B	$\overline{A}$	$\overline{B}$	Y
0	0	1	1	0
0	1	1	0	1
1	0	0	1	1
1	1	0	0	1

Valve Electronics

Electron Emission from Metal

(1) Free electron in metal experiences a barrier on surface due to attractive Coulombian force.

(2) When kinetic energy of electron becomes greater than barrier potential energy (or binding energy E_b) then electron can come out of the surface of metal.

(3) **Fermi energy (E_f) :** Is the maximum possible energy possessed by free electron in metal at $0K$ temperature

(i) In this energy level, probability of finding electron is 50%.

(ii) This is a reference level and it is different for different metals.

(4) **Threshold energy (or work function W_0) :** Is the minimum energy required to take out an electron from the surface of metal. Also $W_0 = E_b - E_f$

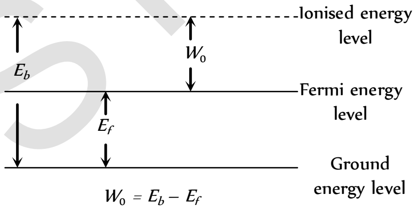


Fig. 27.64

Work function for different materials

$(W)_{\text{Pure tungsten}} = 4.5\ eV$

$(W)_{\text{Thoriated tungsten}} = 2.6\ eV$

$(W)_{\text{Oxide coated tungsten}} = 1\ eV$

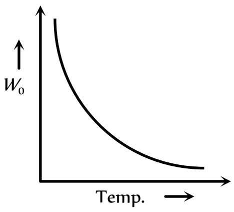


Fig. 27.65

(5) Four processes of electron emission from a metal are

(i) Thermionic emission

(ii) Photoelectric emission

(iii) Field emission

(iv) Secondary emission

Thermionic Emission

(1) The phenomenon of ejection of electrons from a metal surface by the application of heat is called thermionic emission and emitted electrons are called thermions and current flowing is called thermion current.

(2) Thermions have different velocities.

(3) This was discovered by Edison

(4) Richardson – Dushman equation for current density (*i.e.* electric current emitted per unit area of metal surface) is given as

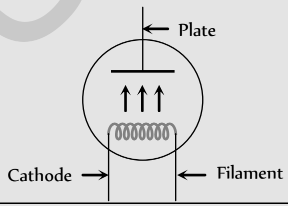
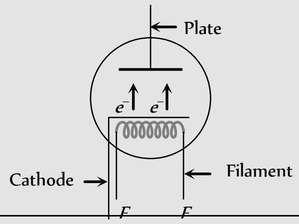
$$J = AT^2 e^{-W_0/kT} = AT^2 e^{-\frac{qV}{kT}} = AT^2 e^{-\frac{11600\,V}{T}}$$

where A = emission constant = 12×10^4 *amp/ m-K*, k = Boltzmann's constant, T = Absolute temp and W_0 = work function.

(5) The number of thermions emitted per second per unit area (J) depends upon following :

(i) $J \propto T^2$ (ii) $J \propto e^{-W_0}$

Table 27.9: Types of thermionic emitters

Directly heated emitter	Indirectly heated emitter
	
Cathode is directly heated by passing current.	Cathode is indirectly heated.
Thermionic current is less.	Thermionic current is more.
Energy consumption and life is small.	Energy consumption and life is more.

Vacuum Tubes and Thermionic Valves

(1) Those tubes in which electrons flows in vacuum are called vacuum tubes.

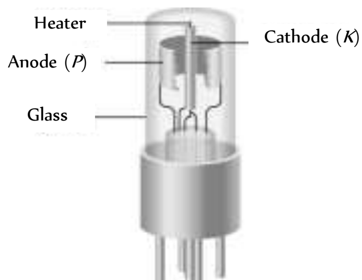
(2) These are also called valves because current flow in them is unidirectional.

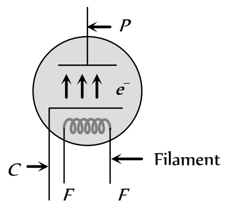
(3) Vacuum in vacuum tubes prevents the emission of secondary electrons and burning of heated filament (which will happen if we use air in place of vacuum)

(4) Every vacuum tube necessarily contains two electrodes out of which one is always electron emitter (cathode) and another one is electron collector (anode or plate).

(5) Depending upon the number of electrodes used the vacuum tubes are named as diode, triode, tetrode, pentode.... respectively, if the number of electrodes used are 2, 3, 4, 5..... respectively.

Diode Valve





(1) **Inventor :** Fleming

(2) **Principle :** Thermionic emission

(3) **Number of electrodes :** Two

(4) **Working :** When plate potential (V_p) is positive, plate current (i_p) flows in the circuit (because some emitted electrons reaches to plate). If $+V_p$ increases i_p also increases and finally becomes maximum (saturation).

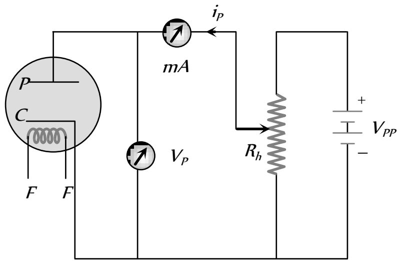


Fig. 27.67

(5) **Space charge :** If V_p is zero or negative, then electrons collect around the plate as a cloud which is called space charge. space charge decreases the emission of electrons from the cathode.

Characteristic Curves of a Diode

A graph represents the variation of i_p with V_p at a given filament current (i_f) is known as characteristic curve.

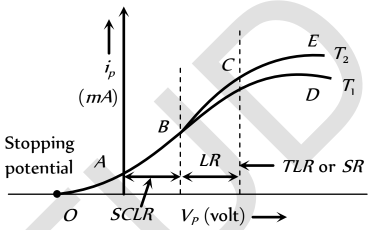


Fig. 27.68

The curve is not linear hence diode valve is a non-ohmic device.

(1) **Space charge limited region (SCLR)** : In this region current is space charge limited current.

Also $i_p \propto V_p^{3/2} \Rightarrow i_p = kV_p^{3/2}$; where k is a constant depending on metal as well as on the shape and area of the cathode. This is called child's law.

(2) **Linear region (LR) :** In this region $i_p \propto V_p$

(3) **Saturated region (SR) or temperature limited region (TLR) :** In this part, the current is independent of potential difference applied between the cathode and anode.

$i_p \neq f(V_p)$, $i_p = f$ (Temperature)

The saturation current follows Richardson Dushman equation *i.e.* $i = AST^2 e^{-\phi_0 / kT}$; Here

A = Emission constant = $\dfrac{4\pi\, mek^2}{h^3}\, amp / m^2 - k^2$

S = Area of emitter in m^2 ; T = Absolute temperature in K

ϕ_0 =Work function of metal in Joule; k =Boltzmann constant

The small increase in i_p after saturation stage due to field emission is known as Shottkey effect.

(4) **Diode resistance**

(i) Static plate resistance or dc plate resistance : $R_p = \dfrac{V_p}{i_p}$.

(ii) Dynamic or ac plate resistance : If at constant filament current, a small change ΔV_p in the plate potential produces a small change Δi_p in the plate current, then the ratio $\Delta V_p / \Delta i_p$ is called the dynamic resistance, or the 'plate resistance' of the diode $r_p = \dfrac{\Delta V_p}{\Delta i_p}$.

(iii) In SCLR : $r_p < R_p$, (iv) In TLR : $R_p < r_p$ and $r_p = \infty$.

(5) **Uses of diode valve**

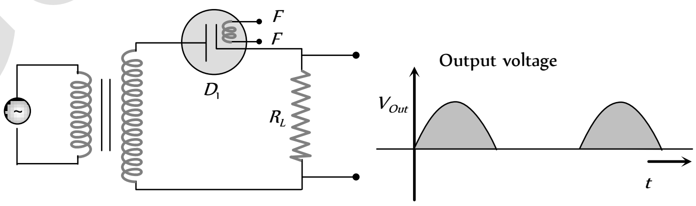
(i) As a rectifier (ii) As a detector

(iii) As a transmitter (iv) As a modulator

Diode Valve as a Rectifier

Rectifier is a device which converts ac into dc

(1) **Half wave rectifier :** The circuit of half wave rectifier is shown below. In the first half cycle of *ac* input the diode conducts and in the second half cycle it does not conducts. Thus half of the input cycle appear as output.



(A) Half wave rectifier (B) Output signal

Fig. 27.69

(i) Output voltage is not constant but pulsating in nature.

(ii) It is a mixture of *ac* and *dc.*

(iii) The *dc* values of the half wave output are given by

$$V_{d.c.} = \frac{V_0}{\pi} \text{ and } i_{d.c.} = \frac{i_0}{\pi}$$

(iv) The *r.m.s.* values of the half wave output are given by

$$V_{rms} = \frac{V_0}{2} \text{ and } i_{rms} = \frac{i_0}{2}$$

(v) The ratio of the effective alternating component to the direct component of the output voltage or current is called ripple factor $r = \dfrac{i_{a.c.}}{i_{d.c.}} = \sqrt{\left(\dfrac{i_{rms}}{i_{d.c.}}\right)^2 - 1} = \sqrt{\left(\dfrac{\pi}{2}\right)^2 - 1} = 1.21 = 121\%$.

(vi) Efficiency of half wave rectifier is given by

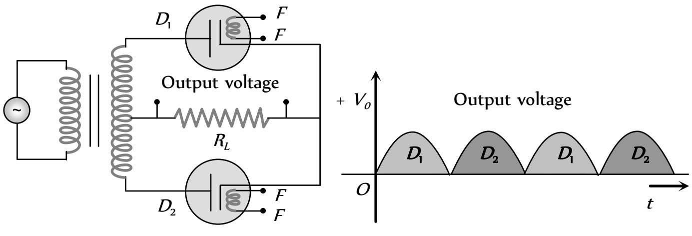
$$\eta = \frac{P_{d.c.}}{P_{a.c.}} \times 100\% = \frac{40.6}{1+\dfrac{r_p}{R_L}}\%$$

The maximum efficiency (for $R_L >> r_p$) = 40.6%

(vii) Form factor $= \dfrac{i_{rms}}{i_{d.c.}} = \dfrac{V_{rms}}{V_{d.c.}} = \dfrac{\pi}{2} = 1.57$

(viii) Ripple frequency = Frequency of input ac = ω

(2) **Full wave rectifier :** It consist of two diodes D_1 and D_2. They conducts alternately during positive and negative half cycle of input *ac* and a unidirectional (or *dc*) current flows in output



(A) Full wave rectifier (B) Output signal

Fig. 27.70

(i) The average or *dc* output values are

$$V_{d.c.} = \frac{2V_0}{\pi} \text{ and } i_{d.c.} = \frac{2i_0}{\pi}$$

(ii) It is a mixture of *ac* and *dc*

(iii) The *r.m.s.* values of the half wave output are given by

$$V_{rms} = \frac{V_0}{\sqrt{2}} \text{ and } i_{rms} = \frac{i_0}{\sqrt{2}}$$

(iv) Ripple factor $r = \sqrt{\left(\dfrac{\pi}{2\sqrt{2}}\right)^2 - 1} = 0.48 = 48\%$.

(v) Efficiency of half wave rectifier is given by

$$\eta = \frac{P_{d.c.}}{P_{a.c.}} \times 100\% = \frac{81.2}{1+\dfrac{r_p}{R_L}}\%$$

The maximum efficiency (for $R_L >> r_p$) = 81.2%

(vii) Form factor $= \dfrac{i_{rms}}{i_{d.c.}} = \dfrac{V_{rms}}{V_{d.c.}} = \dfrac{\pi}{2\sqrt{2}} = 1.11$

(viii) Ripple frequency = Double of frequency of input ac = 2ω

Filter Circuit

Filter circuits smooth out the fluctuations in amplitude of ac ripple of the output voltage obtained from a rectifier.

(i) Filter circuit consists of capacitors or/ and choke coils.

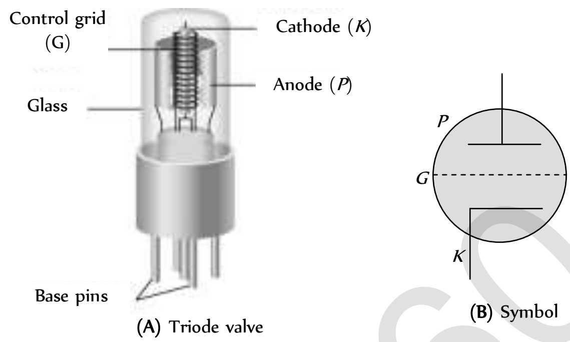
(ii) A capacitor offers a high resistance to low frequency ac ripple (infinite resistance to dc) and a low resistance to high frequency ac ripple. Therefore, it is always used as a shunt to the load.

(iii) A choke coil offers high resistance to high frequency ac, and almost zero resistance to dc. It is used in series.

(iv) π - Filter is best for ripple control.

(v) For voltage regulation choke input filter (*L*-filter) is best.

Triode Valve



(A) Triode valve (B) Symbol

Fig. 27.71

(1) **Inventor :** Dr. Lee De Forest

(2) **Principle :** Thermionic emission

(3) **Number of electrodes :** It consists of three electrodes.

(i) Filament (*F*) : It emits electron on heating.

(ii) Plate or anode (*P*) : It collect the electrons.

(iii) Control grid : It is a third electrode, also known as control grid, which controls the electrons going from cathode to plate. As a result grid controls the plate current. It is kept near the cathode with low negative potential.

When grid is given positive potential then plate current increases but in this case triode cannot be used for amplifier and therefore grid is normally not given positive potential.

When grid is given negative potential then plate current decreases but in this case grid controls plate current most effectively.

(4) **Working :** Plate of triode valve is always kept at positive potential *w.r.t.* cathode. The potential of plate is more than that of grid.

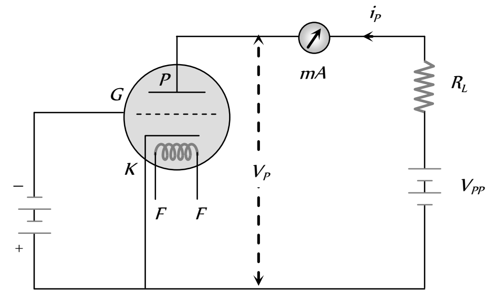


Fig. 27.72

The variation of plate potential affects the plate current as follows $i_p = k\left(V_G + \dfrac{V_p}{\mu}\right)^{3/2}$; where μ = Amplification factor of triode valve, k = Constant of triode valve.

The valve of V_G for which the plate current becomes zero is known as the cut off voltage. For a given V_p, it is given by $V_G = -\dfrac{V_p}{\mu}$.

Characteristics of Triode

The triode characteristics can be obtained under two sets of condition as

Static characteristics and dynamic characteristics

(1) **Static characteristics :** Graphical representation of V_p or V_g and i_p without any load

(i) **Static plate characteristic curve :** Graphical representation of i_p and V_p at constant V_g.

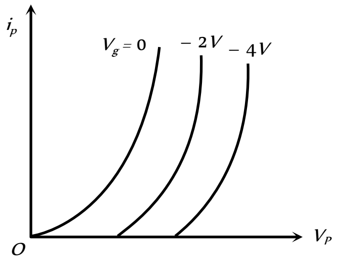


Fig. 27.73

(ii) **Static mutual characteristics curve :** Graphical representation of i_p and V_g when V_p is kept constant

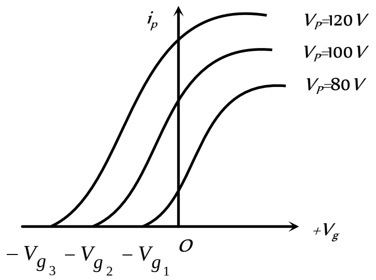


Fig. 27.74

(iii) **Constant current characteristic curve :** Graphical representation between V_p and V_g when i_p is constant.

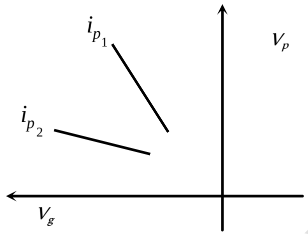


Fig. 27.75

(2) **Dynamic characteristics :** The curve plotted between i_p, V_p and V_g when the triode contains load in the plate circuit are called dynamics characteristics of diode.

(i) **Load line :** Voltage drop iR_L across load R_L which decreases the plate potential will be less then the supply voltage.

Plate voltage $V_p = V_{pp} - i_pR_L \Rightarrow i_p = -\dfrac{1}{R_L}V_p + \dfrac{V_{pp}}{R_L}$

This equation represents a straight line on the static plate characteristics, joining the points (V_{pp} , 0) on plate voltage axis and $(0, V_{pp}/R_L)$ on plate current axis. This line known as load line.

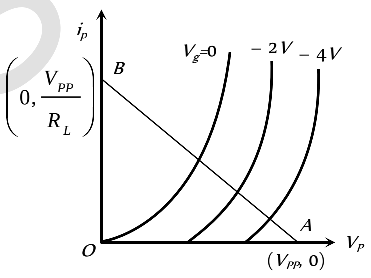


Fig. 27.76

(a) Points at which load line cuts the plate characteristic curves are called operating points.

(b) The slope of load line $AB = \dfrac{di_p}{dV_p} = -\dfrac{1}{R_L}$

(c) In graph, $OA = V_{pp}$ = intercept of load line on V_p axis and $OB = V_{pp}/R_L$ = intercept of load line on i_p axis.

(d) Static plate characteristic + load line

→ Dynamic plate characteristic

Static mutual characteristic + load line

→ Dynamic mutual characteristic

Constants of Triode Valve

(1) **Plate or dynamic resistance (*r*)**

(i) The slope of plate characteristic curve is equal to $\dfrac{1}{\text{plate resistance}}$

or It is the ratio of small change in plate voltage to the change in plate current produced by it, the grid voltage remaining constant. That is, $r_p = \dfrac{\Delta V_p}{\Delta i_p}, V_G = \text{constant}.$

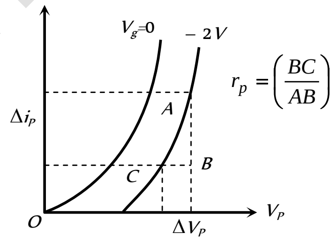


Fig. 27.77

(ii) It is expressed in kilo ohms ($k\Omega$). Typically, it ranges from 8$k\Omega$ to 40$k\Omega$. The r_p can be determined from plate characteristics. It represents the reciprocal of the slope of the plate characteristic curve.

(iii) If the distance between plate and cathode is increased the r_p increases. The value of r_p is infinity in the state of cut off bias or saturation state.

(2) **Mutual conductance (or *trans* conductance) (*g*)**

(i) It is defined as the ratio of small change in plate current (Δi_p) to the corresponding small change in grid potential (ΔV_g) when plate potential V_p is kept constant *i.e.* $g_m = \left(\dfrac{\Delta i_p}{\Delta V_g}\right)_{V_p \text{ is constant}}$

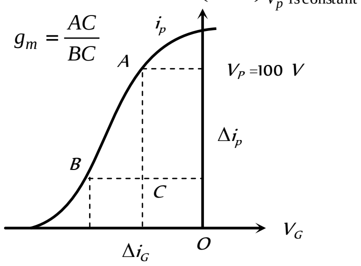


Fig. 27.78

(ii) The value of g_m is equal to the slope of mutual characteristics of triode.

(iii) The value of g_m depends upon the separation between grid and cathode. The smaller is this separation, the larger is the value of g_m and vice versa.

(iv) In the saturation state, the value of $\Delta i_p = 0$, $g_m = 0$

(3) **Amplification factor (μ) :** It is defined as the ratio of change in plate potential (ΔV_p) to produce certain change in plate current (Δi_p) to the change in grid potential (ΔV_g) for the same change in plate current (Δi_p) *i.e.* $\mu = -\left(\frac{\Delta V_p}{\Delta V_g}\right)_{\Delta I_p = \text{a constant}}$; negative sign indicates that V_p and V_g are in opposite phase.

(i) Amplification factor depends upon the distance between plate and cathode (d_{pk}), plate and grid (d_{pg}) and grid and cathode(d_{gk}).

i.e. $\mu \propto d_{pg} \propto d_{pk} \propto \frac{1}{d_{gk}}$

(ii) The value of μ is greater than one.

(iii) Amplification factor is unitless and dimensionless.

(4) **Relation between triode constants :** The triode constants are not independent of each other. They are related by the relation $\mu = r_p \times g_m$

The r_p and g_m depends on i_p in the following manner

$r_p \propto i_p^{-1/3}$, $g_m \propto i_p^{1/3}$, μ does not depend on i_p.

Above three constants may be determined from any one set of characteristic curves.

$$r_p = \frac{V_{P1} - V_{P2}}{I_{PA} - I_{PB}},$$

$$g_m = \frac{I_{PA} - I_{PB}}{V_{G1} - V_{G2}},$$

$$\mu = -\frac{V_{P1} - V_{P2}}{V_{G2} - V_{G1}}$$

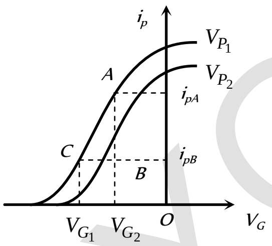


Fig. 27.79

Triode as an Amplifiers

Amplifier is a device by which the amplitude of variation of *ac* signal voltage / current/ power can be increased

(1) The signal to be amplified (V_i) is applied in the grid circuit and amplified output is obtained from the plate circuit

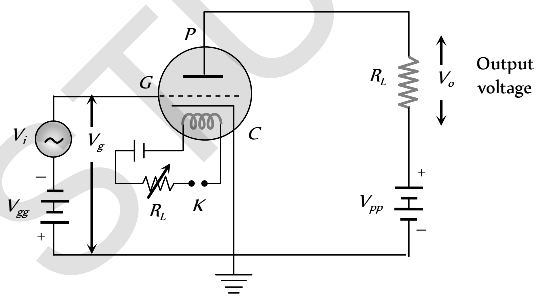


Fig. 27.80

(2) The voltage at grid is the sum of signal V_i and grid bias V_{gg}.

$$V_g = V_{gg} + V_i$$

(3) Small change in grid voltage results in a large change in plate current so results in a large change in voltage across $R_L \; (V_0 = i_p R_L \Rightarrow \Delta V_0 = \Delta i_p R_L)$

(4) The linear portion of the mutual characteristic with maximum slope is chosen for amplification without distortion.

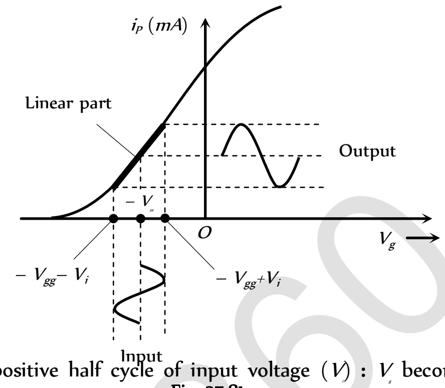


Fig. 27.81

(i) For the positive half cycle of input voltage (V_i) : V_g becomes less negative, so i_p increases

(ii) For the negative half cycle of input voltage (V_i) : V_g becomes more negative, so i_p decreases

(iii) The phase difference between the output signal and input signal is 180° (or π)

(5) **Voltage amplification**

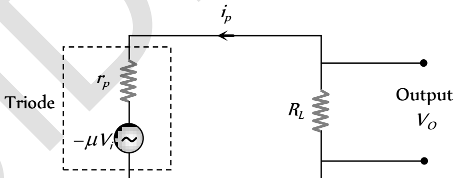


Fig. 27. 82 : Equivalent circuit of triode amplifier

Current through the load resistance is given by $i_p = -\frac{\mu V_i}{r_p + R_L}$

$$\Rightarrow V_0 = i_p R_L = \frac{-\mu V_i R_L}{r_p + R_L} \Rightarrow \text{Voltage gain} = \frac{V_0}{V_i} = -\frac{\mu R_L}{r_p + R_L}$$

Numerically $A = \frac{\mu R_L}{r_p + R_L} = \frac{\mu}{1 + \frac{r_p}{R_L}}$

(i) If $R_L = \infty \Rightarrow A$ will be maximum and $A_{max} = \mu$

(Practically $A < \mu$)

(ii) If $r_p = R_L \Rightarrow A = \frac{\mu}{2}$

(iii) Power at load resistance $P = i_p V_0 = i_p^2 R_L$

Condition for maximum power $R_L = r_p$

$$\therefore P_{max} = \left(\frac{\mu V_i}{R_L + R_L}\right)^2 \times R_L = \frac{\mu^2 V_i^2}{4 R_L}$$

Tips & Tricks

✍ The most efficient packing of atoms in cubic lattice structure occurs for *fcc*.

✍ The lattice for *NaCl* crystal is *fcc*.

✍ The space lattice of diamond is *fcc*. (The diamond structure may be viewed as two *fcc* structures displaced from each other by one quarter of a body diagonal).

✍ Carbon, silicon, germanium, tin can crystallize in the diamond structure.

✍ At room temperature $\sigma_{Ge} > \sigma_{Si}$

✍ $(n_i)_{Ge} \simeq 2.4 \times 10^{19}\ /m^3$ and $(n_i)_{Si} \simeq 1.5 \times 10^{16}\ /m^3$

✍ In a transistor circuit the reverse bias is high as compared to the forward bias. So that it may exert a large attractive force on the charge carriers to enter the collector region.

✍ *Ge* is more sensitive to heat since it's forbidden energy gap is smaller than that of silicon. Electrons from the valence band of *Ge* requires less energy to move from the valence band to conduction band.

✍ Both *N*-type as well as *P*-type semiconductor are neutral.

✍ Semiconductor devices are current control devices.

✍ The semiconductor devices are temperature sensitive devices.

✍ The electric field setup across the potential barrier is of the order of 3×10^5 *V/m* for *Ge* and 7×10^5 *V/m* for *Si*.

✍ An ideal junction diode when forward biased offers zero resistance. Voltage drop across such a junction diode is zero. In reverse biased diode offers infinite resistance and voltage drop across it is equal to voltage applied.

✍ A *P-N* junction diode can be considered to be equivalent to a capacitor with *P* and *N* regions acting as the plates of the capacitors and depletion layer as the dielectric medium.

✍ The mobility of electron is two-three times the mobility of holes. Therefore NPN devices are fast and hence preferred.

✍ If $E_g \simeq 0\,eV$, the material is good conductor or metal and if $E_g \simeq 1\,eV$, the material is a semiconductor. If $E_g \simeq 6\,eV$ then the material is an insulator.

✍ A *P-N* junction or diode acts like a valve or voltage controlled switch. When forward biased, it acts like ON switch. When reverse biased, it acts like an OFF switch.

✍ The current due to minority carriers in the junction diode is independent of the applied voltage. It only depends upon the temperature of the diode.

✍ Voltage obtained from a diode rectifier is a mixture of alternating and direct voltage.

✍ Cross sectional area of base is very large as compared to emitter. Cross sectional area of collector is less than base but greater than emitter.

✍ C.C (common collector) amplifier is called power amplifier or current booster or emitter follower.

✍ Devices like tunnel diode, tetrode and thyrisisters have negative resistance.

✍ Transistor provides good power amplification when they are use in CE configuration.

✍ **MOSFETS :** In a MOSFET, a type of three-terminal transistor, a potential applied to the gate terminal *G* controls the internal flow of electrons from the source terminal *S* to the drain terminal *D*. Commonly, a MOSFET is operated only in its ON (conducting) or OFF (not conducting condition. Installed by the thousands and millions on silicon wafers (chips) to form integrated circuits, MOSFETs form the basis for computer hardware.

✍ When a *PN* junction is forward biased, it can emit light, hence can serve as a light-emitting diode (LED). The wavelength of the emitted light is $\lambda = \dfrac{c}{f} = \dfrac{hc}{E_g}$

✍ The fermi energy of a given material is the energy of a quantum state that has the probability 0.5 of being occupied by an electron.

✍ Number of conduction electrons per unit volume

$$= \frac{\text{(Material's density)}}{(\text{Molar mass } M)/N_A}$$

(N_A = Avogadro's number = 6.02×10^{23} */mol*)

✍ The occupancy probability *P*(*E*) : Electrical conduction of a metal depends on the probability that if an energy level is available at energy *E*, is it actually occupied by an electron.

the expression for occupancy probability *P*(*E*) is given by

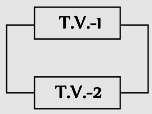
Fermi-Dirac statistics $P(E) = \dfrac{1}{\exp\left(\dfrac{E - E_F}{kT}\right) + 1}$; E_F=Fermi energy

✍ A good emitter should have low work function, high melting point, high working temperature, high electrical and mechanical strength.

✍ When triode amplifier are in series, total voltage gain

$A = A_1 A_2 A_3$ ....

✍ When two triode valve are in parallel



Total plate resistance $\dfrac{1}{r_p} = \dfrac{1}{r_{p_1}} + \dfrac{1}{r_{p_2}}$

Total mutual conductance $G_m = g_{m_1} + g_{m_2}$

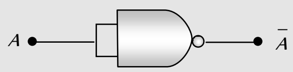
Total amplification factor $\mu = G_m R_p$

Voltage amplification $A = \dfrac{\mu R_L}{r_p + R_L}$

✍ **NOR** gate is a universal gate because it can be used to perform the basic logic function, AND, OR and NOT.

✍ Output in Ex-OR gate is '1' only when inputs are different.

✍ If both inputs of NAND gate are shorted then it will become 'NOT gate



NOT gate