Block level logical diagram

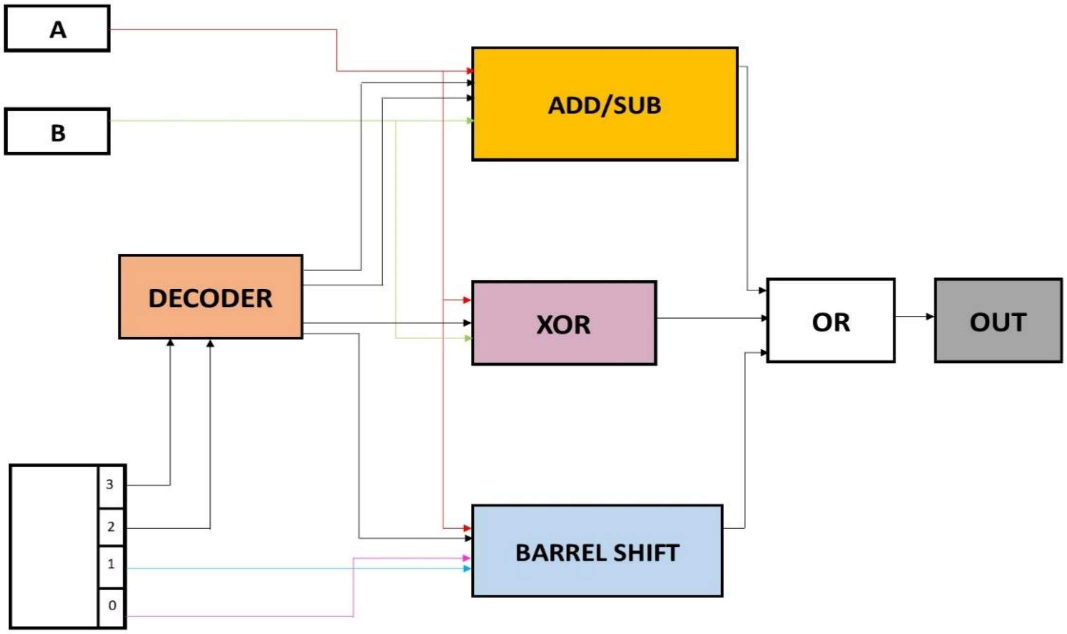


Figure 1 Inside the ALU

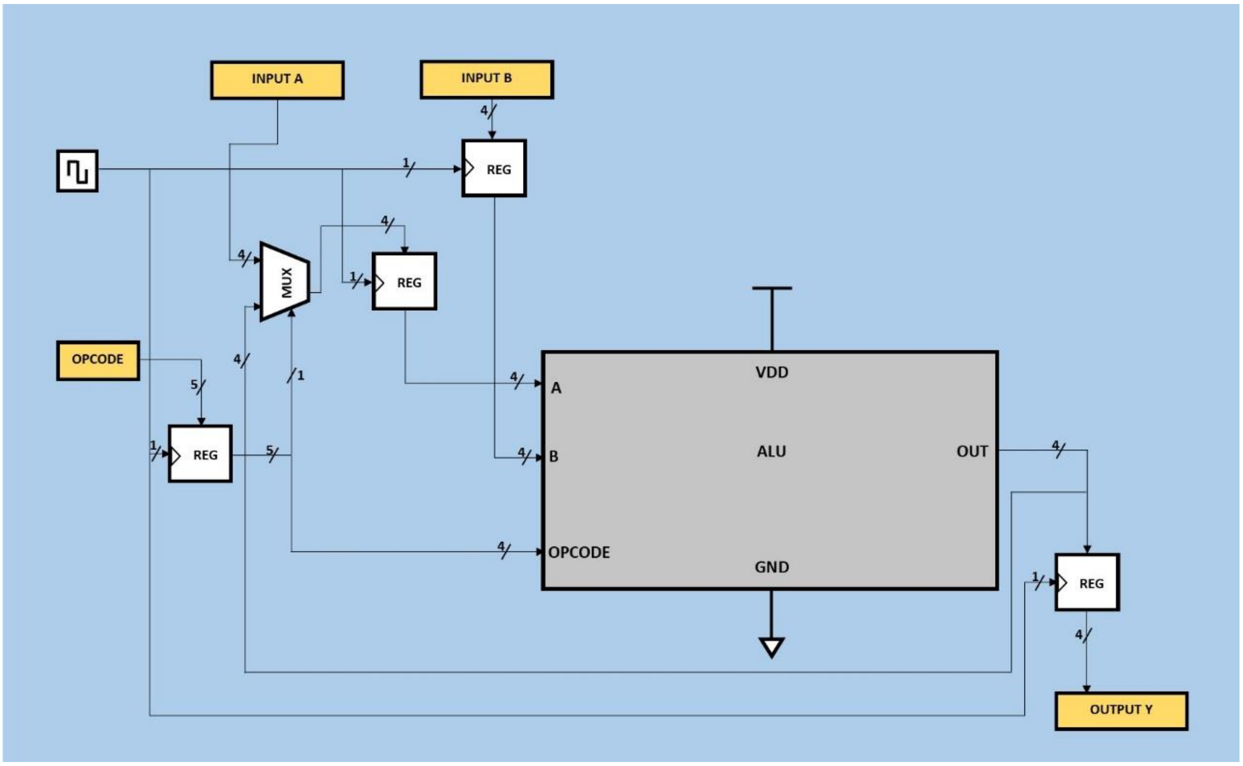


Figure 2 Overview of the exterior control of the ALU

Logical Unit: This only consists of the XOR block that performs a 4-bitwise XOR on the A and B inputs. This requires only 4 XOR 2x1 gates from the gsclib045 library.

Arithmetic Unit: It's composed of the ADD-SUB block and the BARREL-SHIFT REGISTER block. The **Kogge-Stone** adder will be used to perform the addition and subtraction operations and output will be in 2s complement. The Right-Barrel Shifter will be implemented using a cascade of the barrel shifter of 1 and 2 with a 2-bit select linked to the opcode.

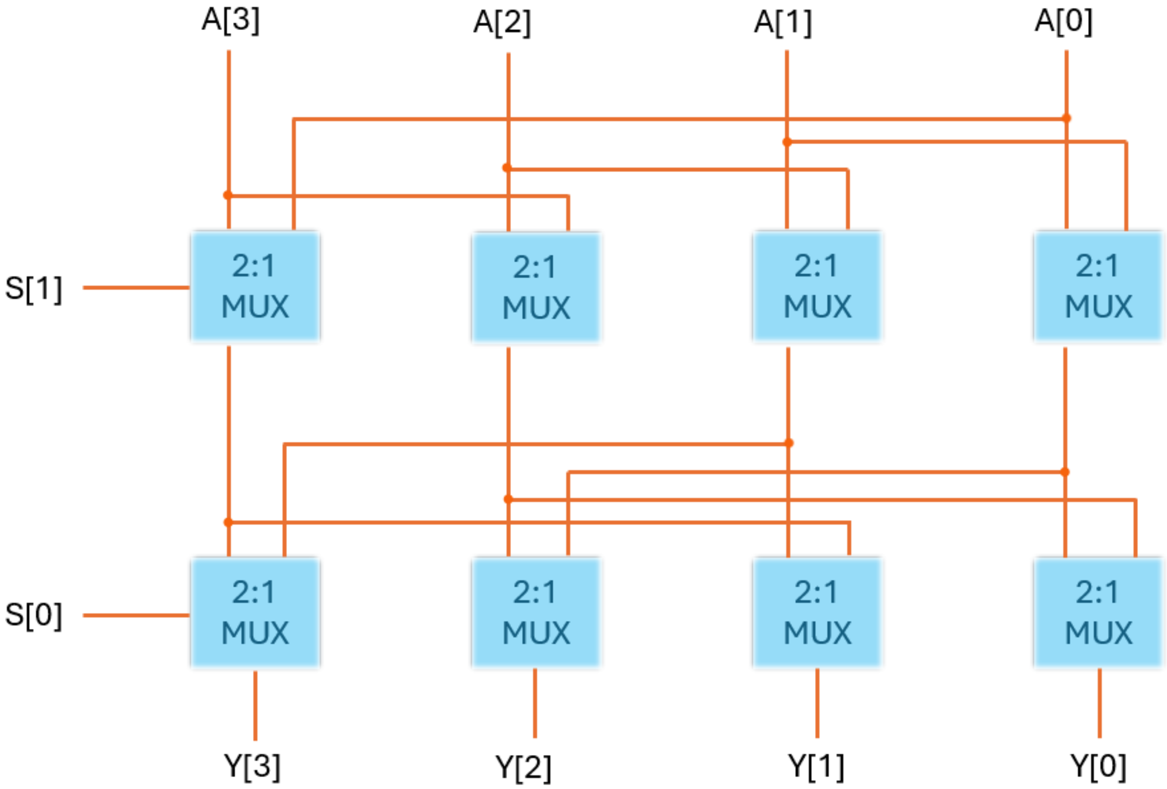
Power optimization

We make use of **data gating or input gating.** We AND the inputs to all the blocks with an enable bit. The enable bit is 0 if the block is inactive and 1 if the block is active. As a result, whenever a block isn't in use its output is set to zero. This doesn't conserve static power, but it does conserve dynamic power.

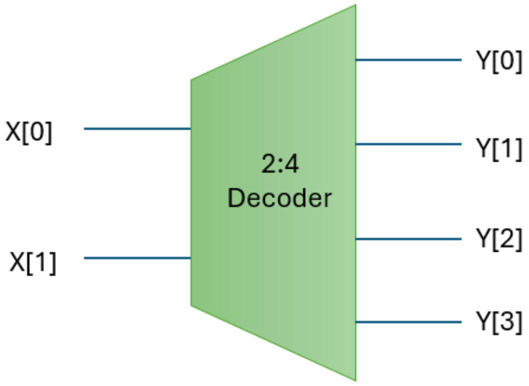
Delay optimization

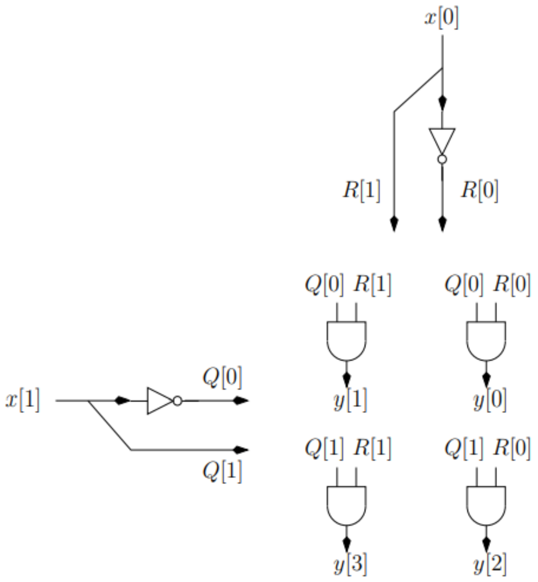
In our circuit, enable signals to adder and XOR blocks has a fan-out of 8. Optimal fanouts are 3.6 ~4 so we use 2 buffers for each block to decrease the max fan-out from 8 to 4. Hence in total 4 buffers have been used.

4-Bit Right Shift Barrel Shifter



2:4 Decoder





Kogge-stone adder

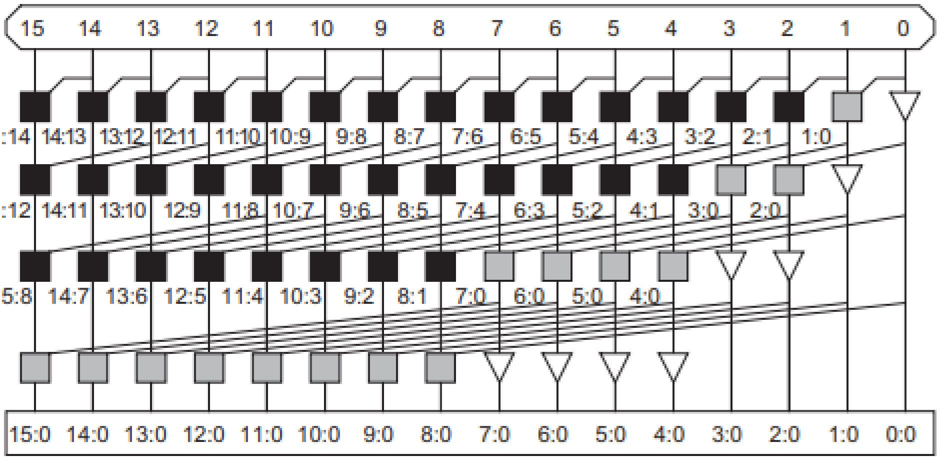


Figure 3: 16-bit Kogge-Stone adder

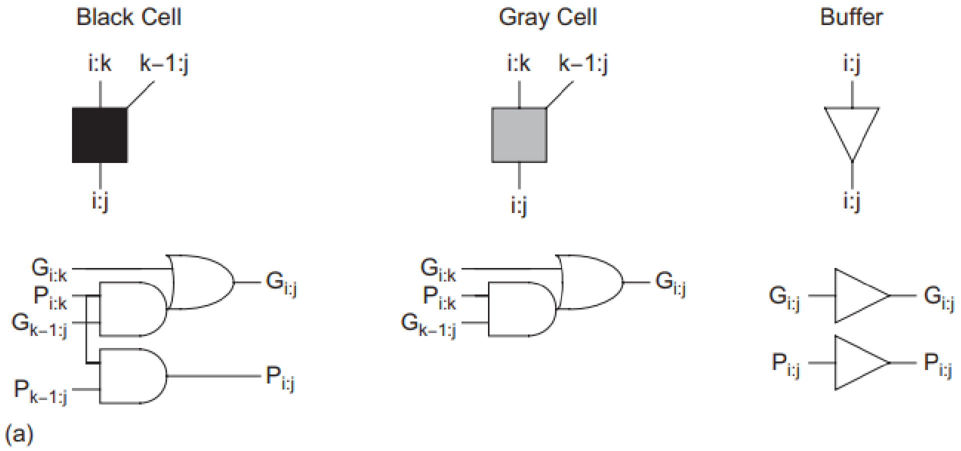


Figure 4: blocks making up the adder.