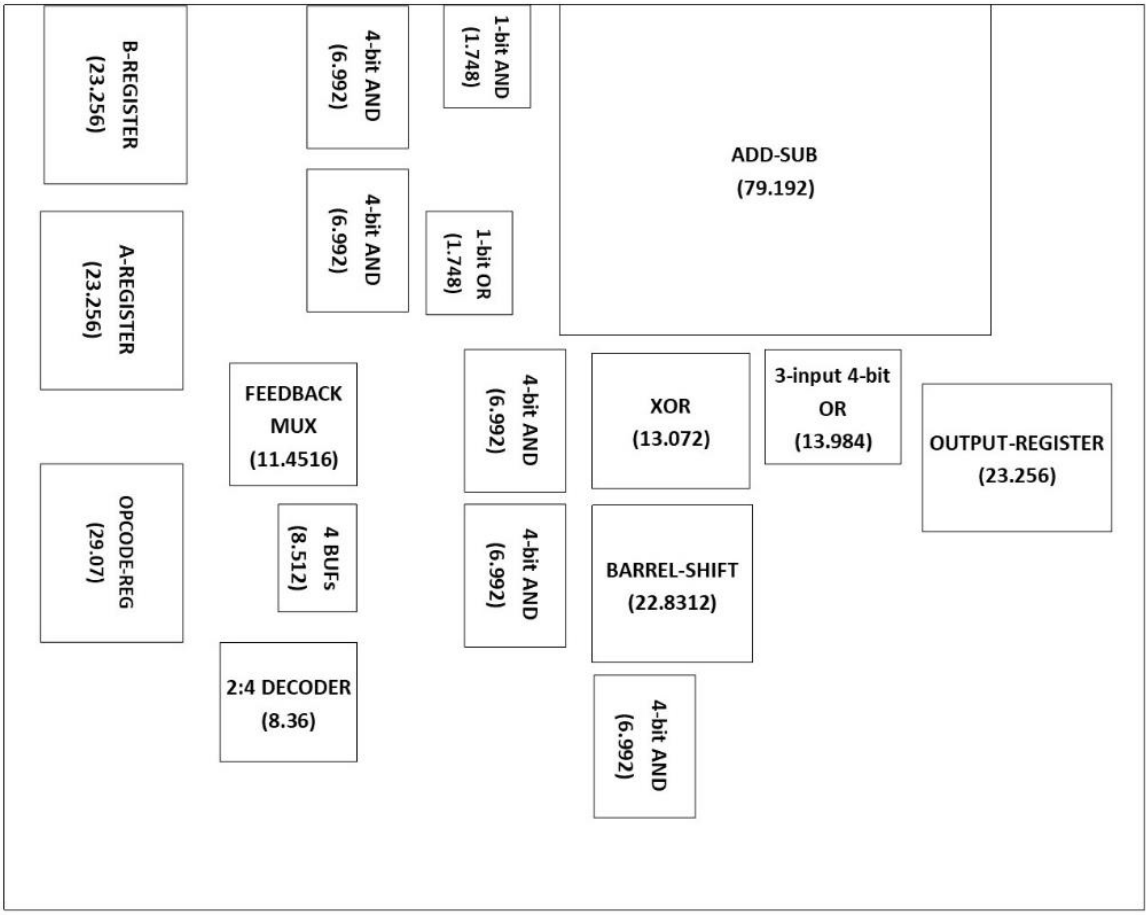

Figure 1: Floorplan for the ALU

Adder

Part Name	# of the parts	Length (μm)	Width (μm)	Area of comp. (μm^2)	Total area (μm^2)
AND (2x2)	12	0.92	1.9	1.748	20.976
OR (2x1)	6	0.92	1.9	1.748	10.488
XOR (2x1)	8	1.72	1.9	3.268	26.144
BUF (1x1)	4	1.12	1.9	2.128	8.512
XOR (2x1) (for SUB)	4	1.72	1.9	3.268	13.072
Total area of the adder					79.192

XOR Block

Part Name	# of the parts	Length (μm)	Width (μm)	Area of comp. (μm^2)	Total area (μm^2)
XOR (2x1)	4	1.72	1.9	3.268	13.072

Barrel Shift Register

Part Name	# of the parts	Length (μm)	Width (μm)	Area of comp. (μm^2)	Total area (μm^2)
MUX (2:1)	8	1.89	1.51	2.8539	22.8312

Control Requirements

2:4 DECODER

Part Name	# of the parts	Length (μm)	Width (μm)	Area of comp. (μm^2)	Total area (μm^2)
INV (X1)	2	1.71	0.4	0.684	1.368
AND (2x2)	4	0.92	1.9	1.748	6.992
Total area					8.36

3x 4-bit register (for A, B and Y)

Part Name	# of the parts	Length (μm)	Width (μm)	Area of comp. (μm^2)	Total area (μm^2)	Total total area (μm^2)
DFF (QX1)	4	3.4	1.71	5.814	23.256	69.768

So, to add to this, we need 3 4-bit registers. 1 to store A, a 2nd to store B and a 3rd to store Y.
Thus, the total area comes to $\underline{69.768\ [\mu m^2]}$

1x 5-bit register (for the opcode)

Part Name	# of the parts	Length (μm)	Width (μm)	Area of comp. (μm^2)	Total area (μm^2)
DFF (QX1)	5	3.4	1.71	5.814	29.07

4-bit MUX

Part Name	# of the parts	Length (μm)	Width (μm)	Area of comp. (μm^2)	Total area (μm^2)
MUX (2:1)	4	1.89	1.51	2.8539	11.4516

3-input 4-bit OR (or the adder output, xor output and bsr output)

Part Name	# of the parts	Length (μm)	Width (μm)	Area of comp. (μm^2)	Total area (μm^2)
OR(2x1)	8	0.92	1.9	1.748	13.984

1-bit OR (to OR the add enable and the sub enable)

Part Name	# of the parts	Length (μm)	Width (μm)	Area of comp. (μm^2)	Total area (μm^2)
OR(2x1)	1	0.92	1.9	1.748	1.748

5x 4-bit AND gates (to AND the inputs with the respective enables, 1 for the BSR, 2 for the ADDER and 2 for the XOR)

Part Name	# of the parts	Length (μm)	Width (μm)	Area of comp. (μm^2)	Total area (μm^2)
AND (2x2)	21	0.92	1.9	1.748	36.708

The extra AND is for when we AND the carry in-bit for subtraction.

4 buffers to reduce the fan-out

Part Name	# of the parts	Length (μm)	Width (μm)	Area of comp. (μm^2)	Total area (μm^2)
BUF (2x1)	4	1.12	1.9	2.128	8.512

The total area comes to $\mathbf{294.7328\ \mu m^2}$.

We agreed on the goal to keep the total area under **150% ($\mathbf{442.0992\ \mu m^2}$)** of total area of the layout of all the components combined as calculated above.

Opcode

The ALU accepts one **5-bit opcode.**

Op4	Op3	Op2	Op1	Op0	Func.
*	0	0	*	*	ADD
*	0	1	*	*	SUB
*	1	0	*	*	XOR
*	1	1	0	0	Shift 4
*	1	1	0	1	Shift 1
*	1	1	1	0	Shift 2
*	1	1	1	1	Shift 3
0	*	*	*	*	Use external input A
1	*	*	*	*	Feedback

The operations are as follows:
Op4 determines if there's feedback or not. 0 for external input and 1 for feedback.
Op3 and Op2 determine the ALU operation. 00 for addition, 01 for subtraction, 10 for XOR and 11 for Barrel-Shifting.
Op1 and Op0 determine by how much we will perform the shift when the barrel-shift register is selected. 00 for shift 4, 01 for shift 1, 10 for shift 2 and 11 for shift 3.