2-to-4 decoder

Schematic print

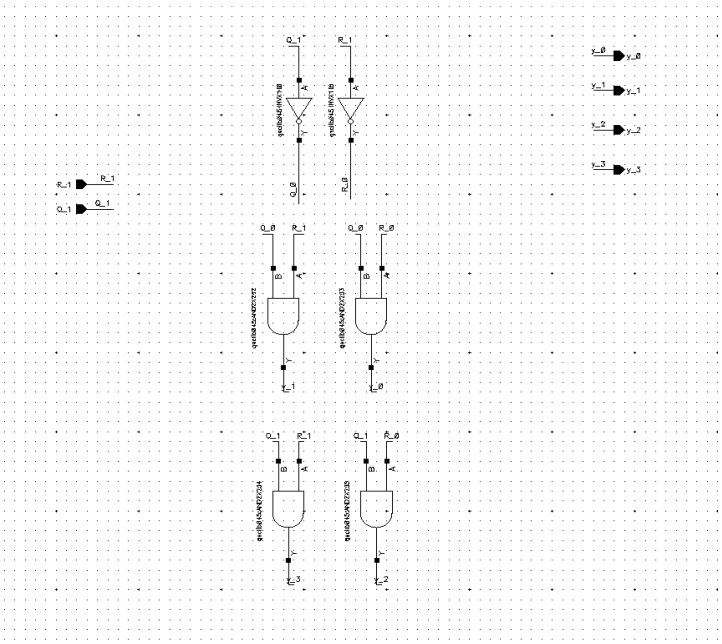

Figure 1: 2-to-4 decoder schematic

Layout print

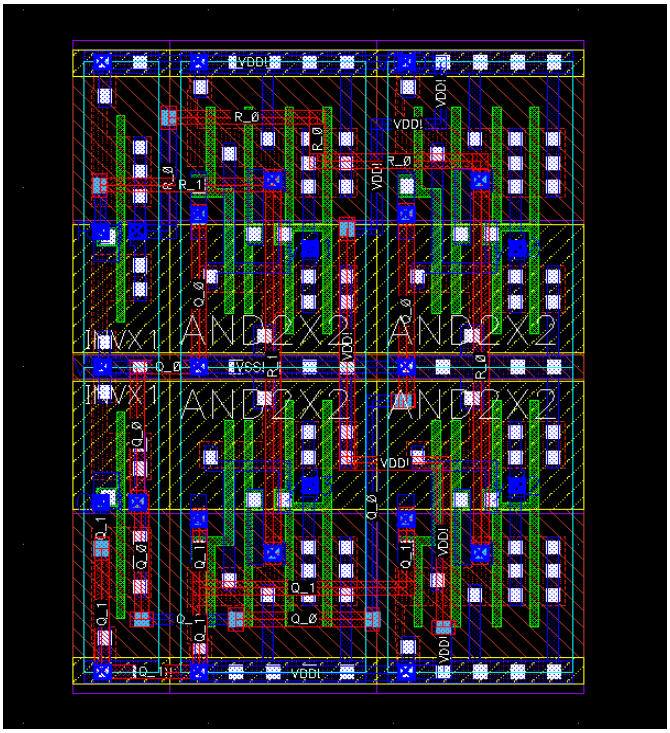

Figure 2: 2-to-4 decoder layout

4-bit 3-input OR

Schematic Print

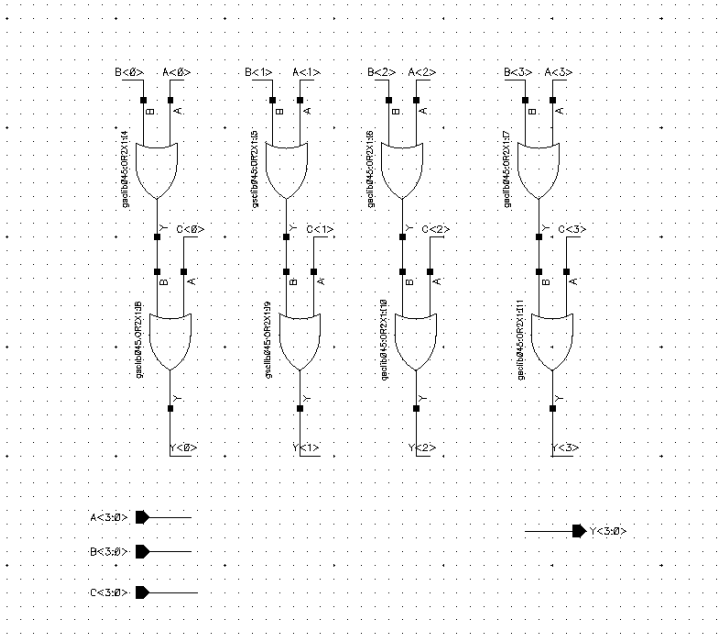

Figure 3: 4-bit 3-input OR schematic

Layout Print

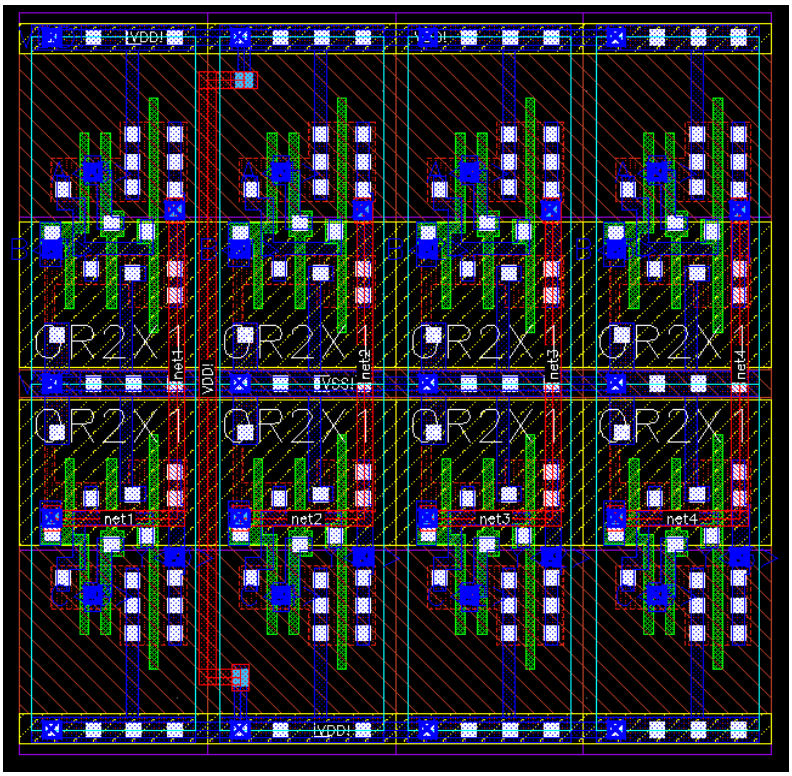

Figure 4: 4-bit 3-input OR layout

4-bit AND

Schematic Print

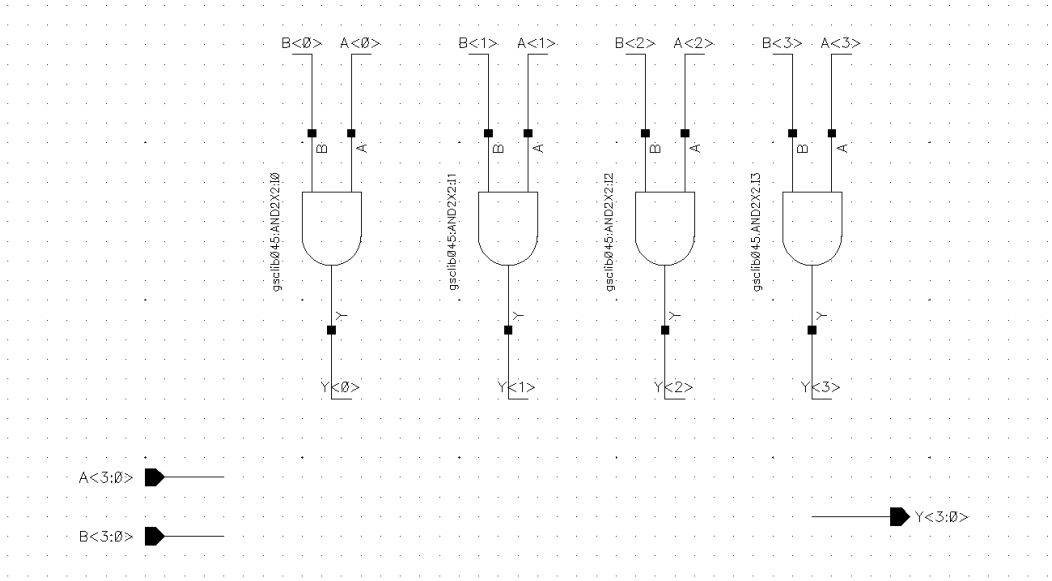

Figure 5: 4-bit AND schematic

Layout Print

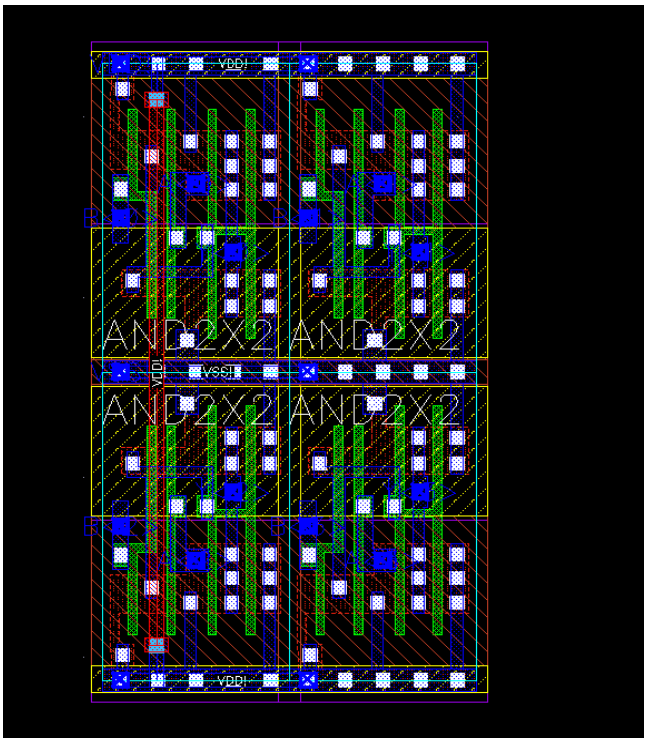

Figure 6: 4-bit AND layout

4-bit MUX

Schematic Print

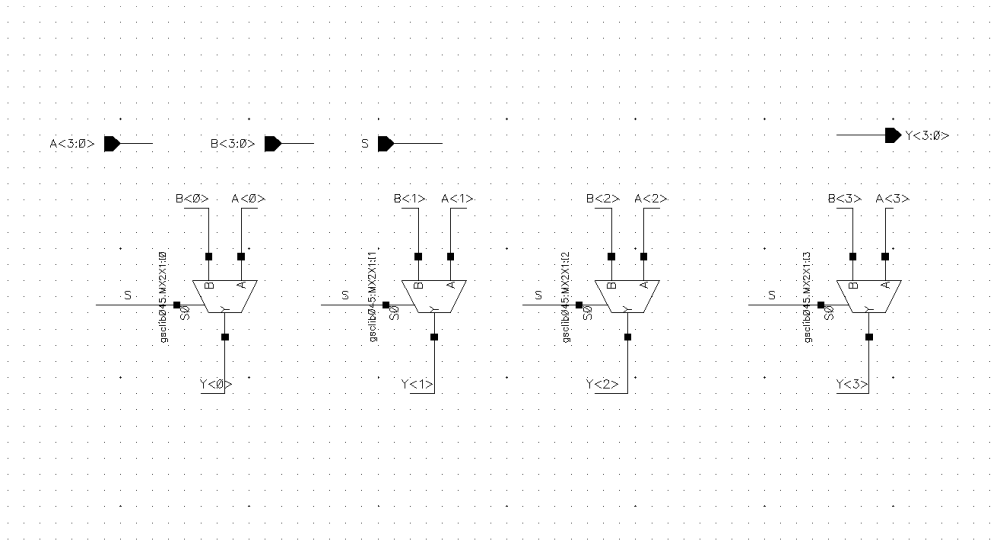

Figure 7: 4-bit MUX schematic

Layout Print

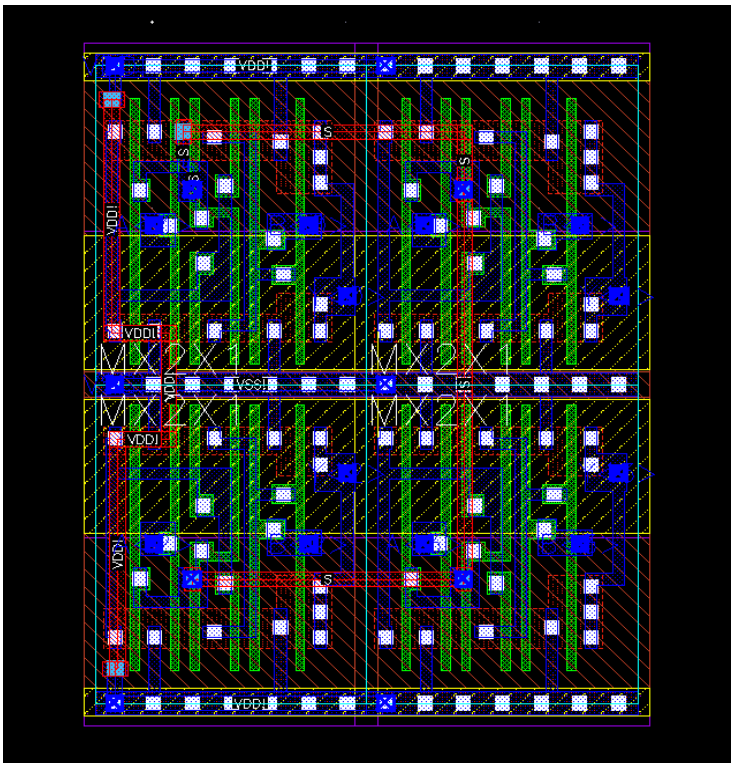

Figure 8: 4-bit MUX layout

4-bit Register

Schematic Print

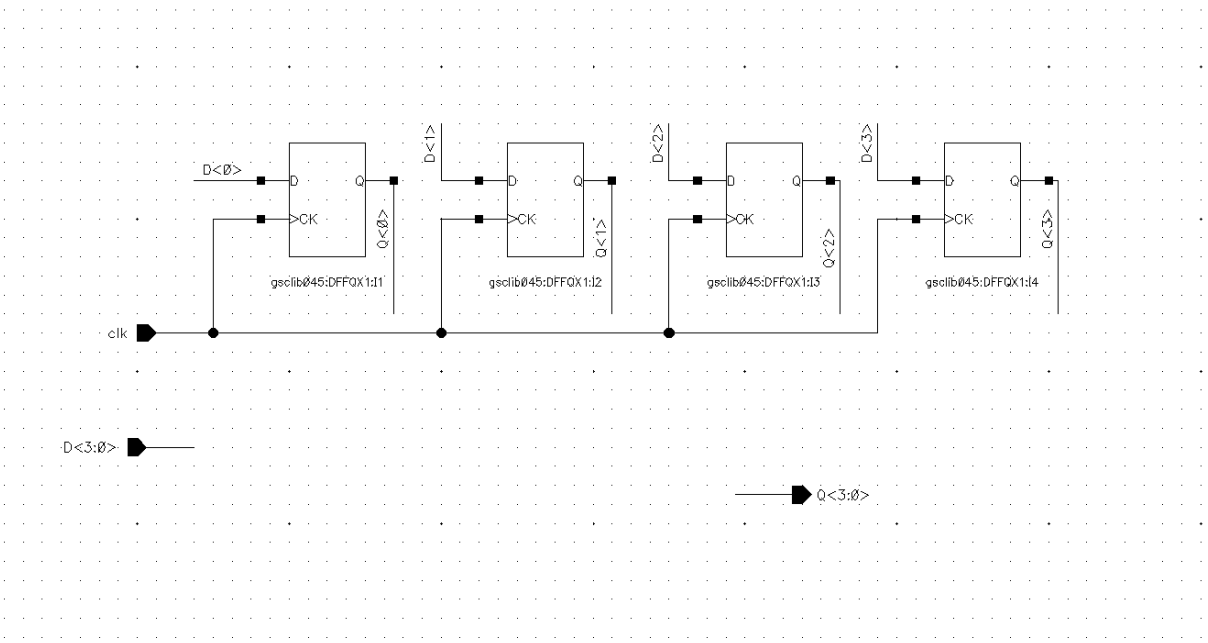

Figure 9: 4-bit register schematic

Layout Print

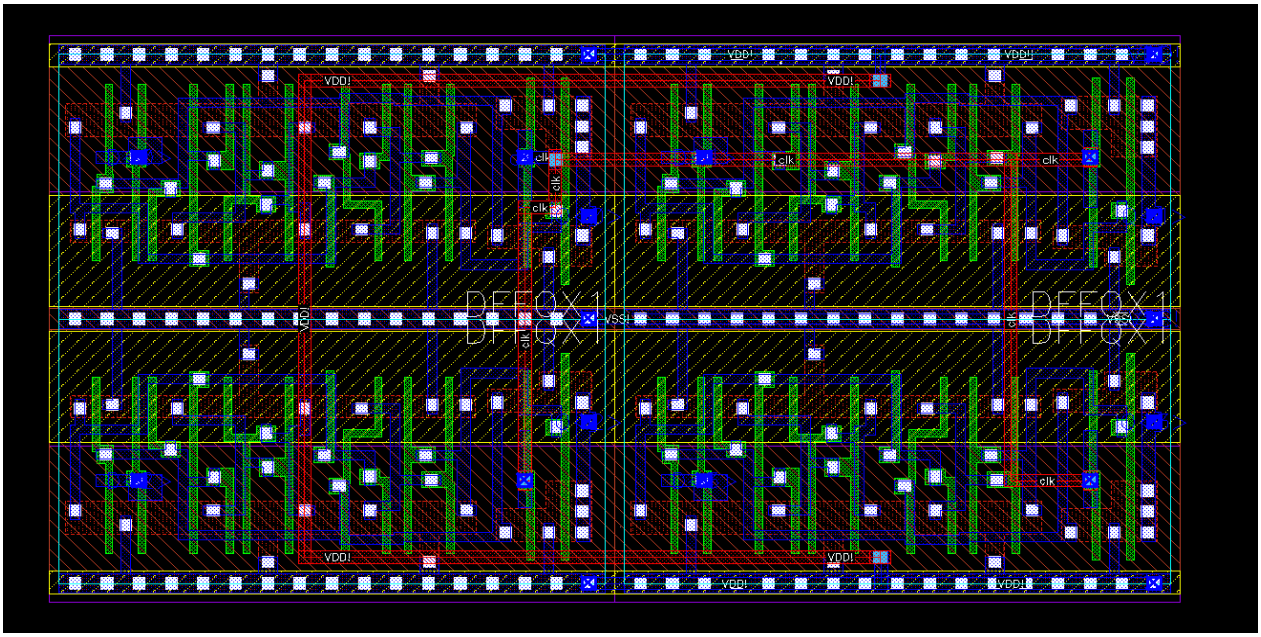

Figure 10: 4-bit register layout

5-bit Register

Schematic Print

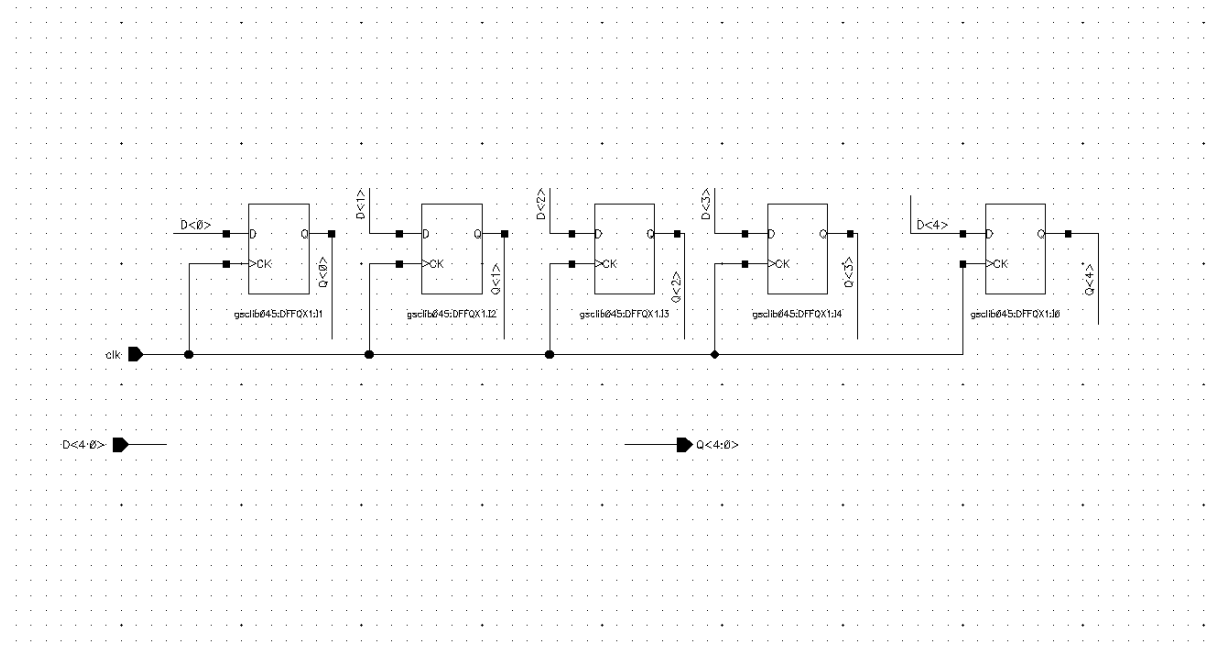

Figure 11: 5-bit register schematic

Layout Print

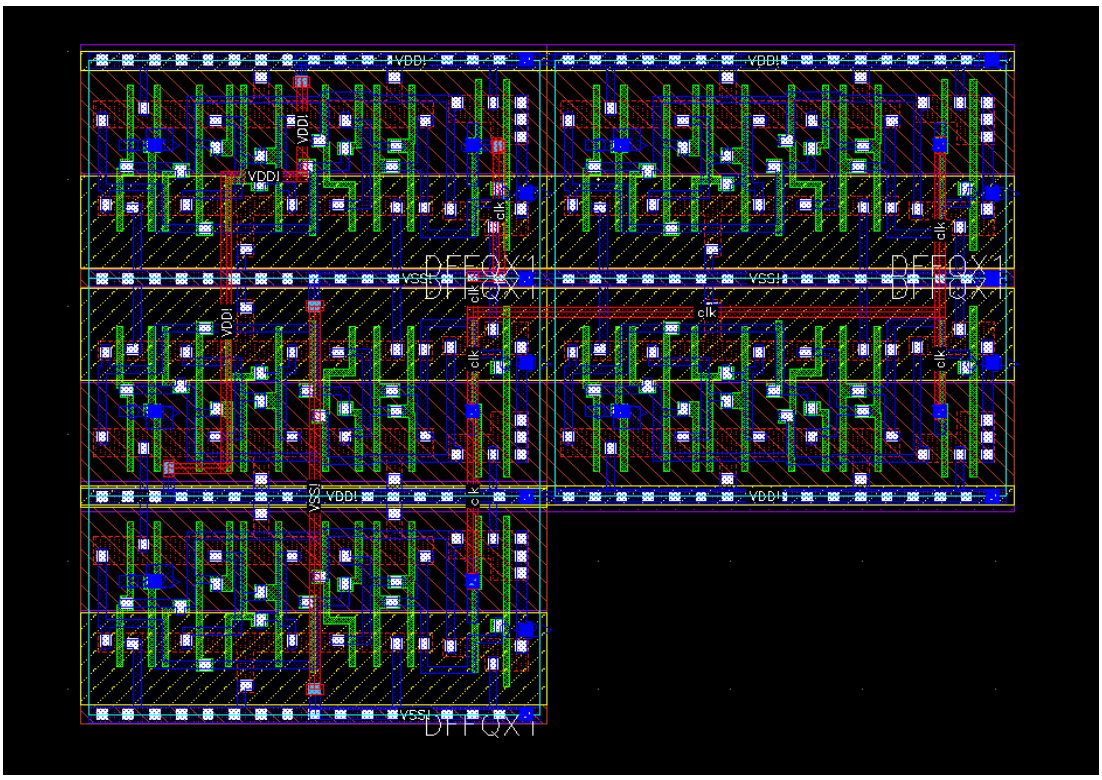

Figure 12: 5-bit register layout

4-bit XOR

Schematic Print

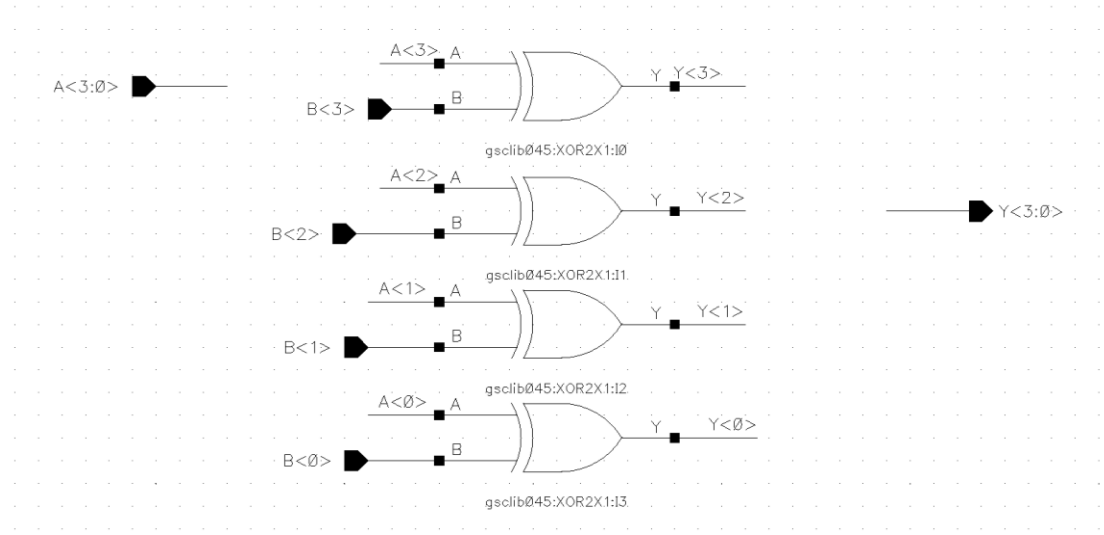

Figure 13: 4-bit XOR schematic

Layout Print

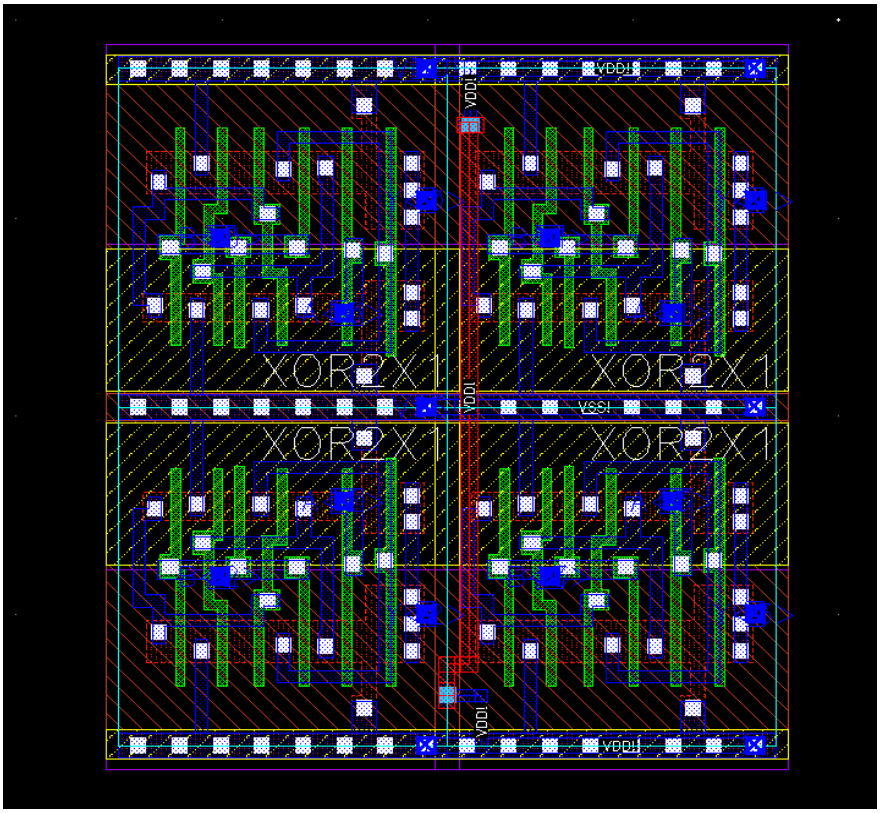

Figure 14: 4-bit XOR layout

Barrel Right-Shift register

Schematic Print

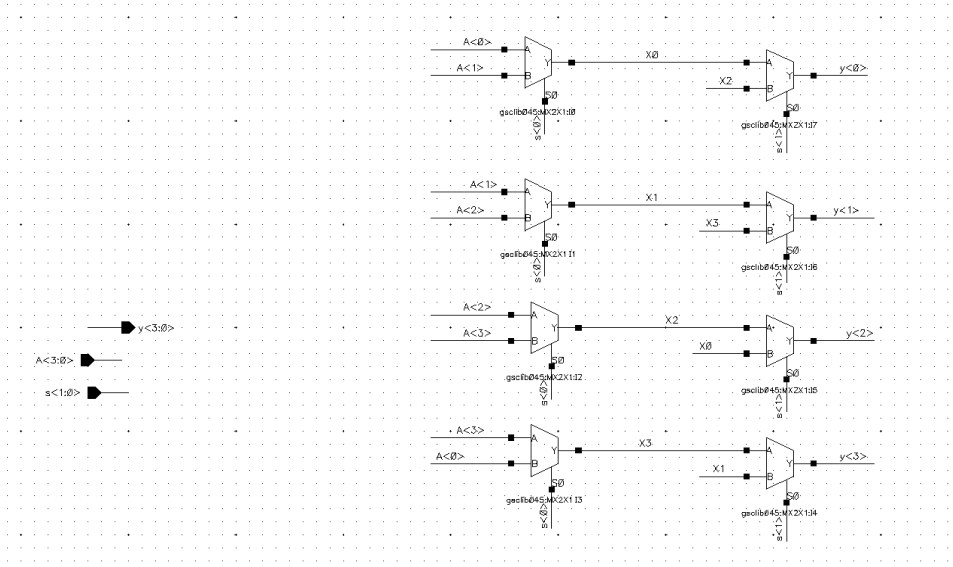

Figure 15: Barrel Shift Register schematic

Layout Print

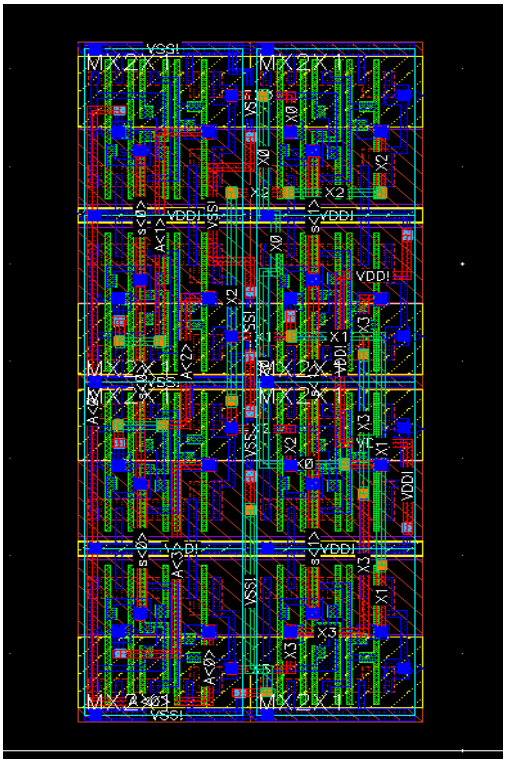

Figure 16: Barrel Shifter Layout

Adder block

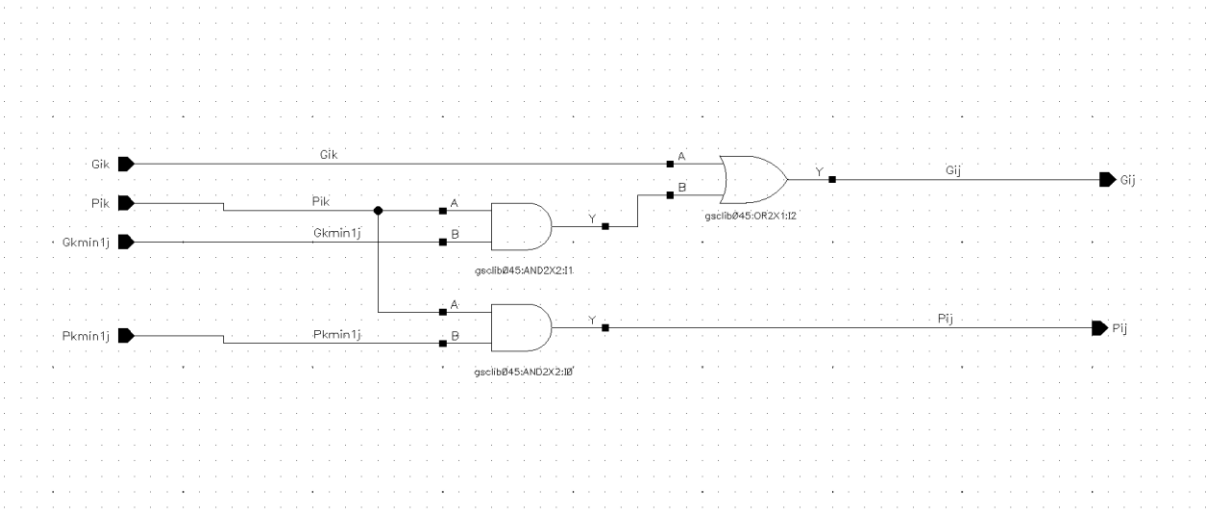

Figure 17: Black cell schematic

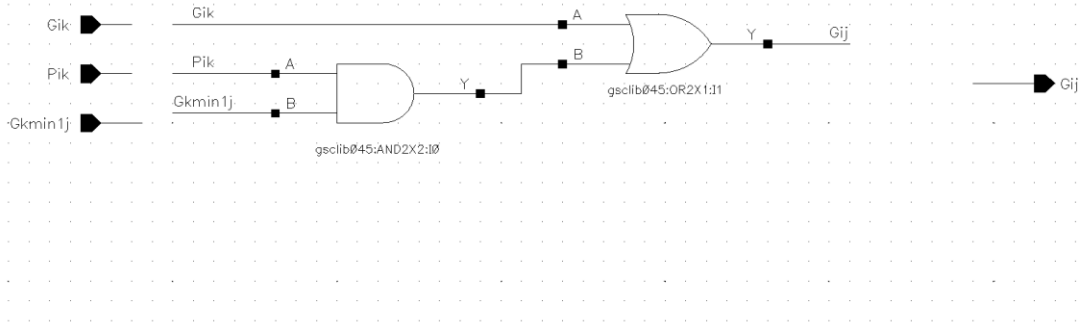

Figure 18: Grey cell schematic

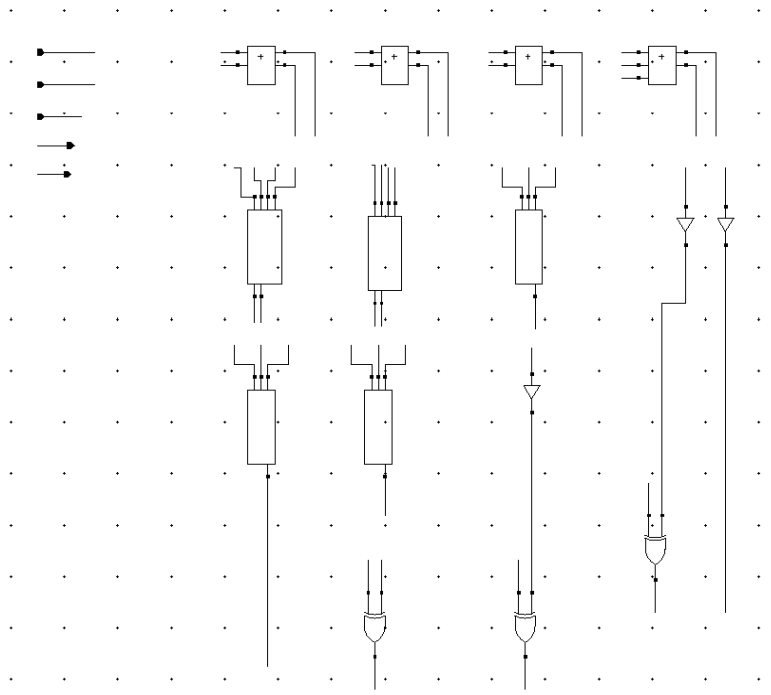

Figure 19: Adder schematic

Layout Print

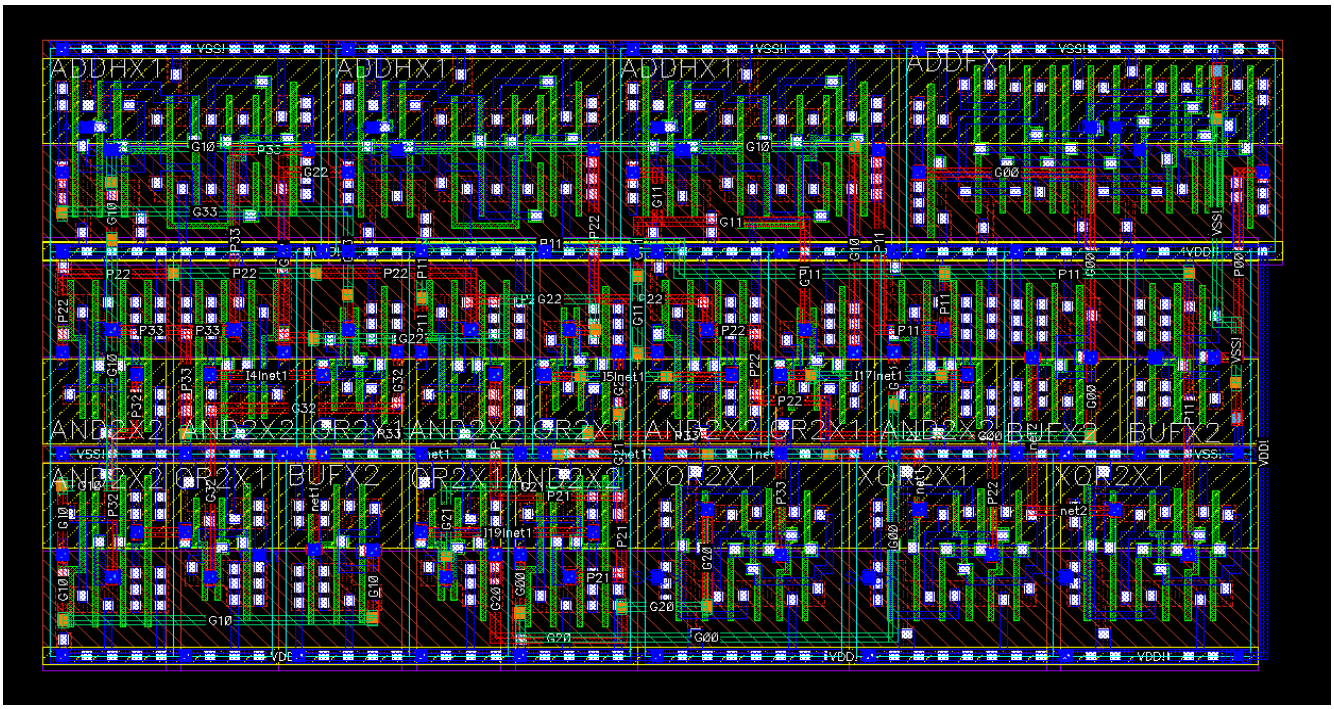

Figure 20: Adder layout

ALU block

Schematic Print

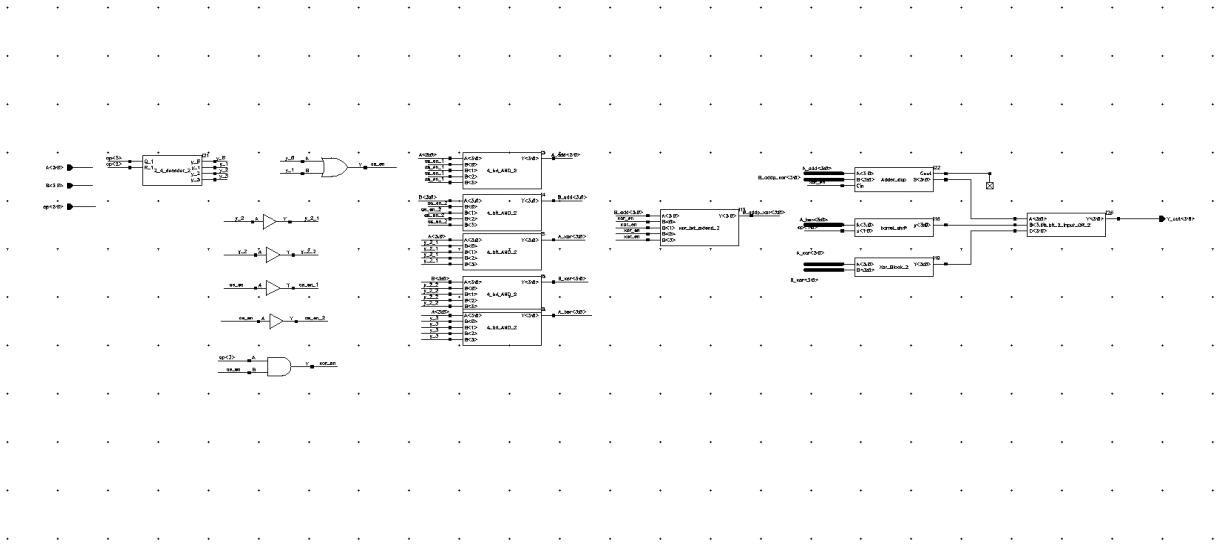

Figure 21: ALU schematic

Layout Print

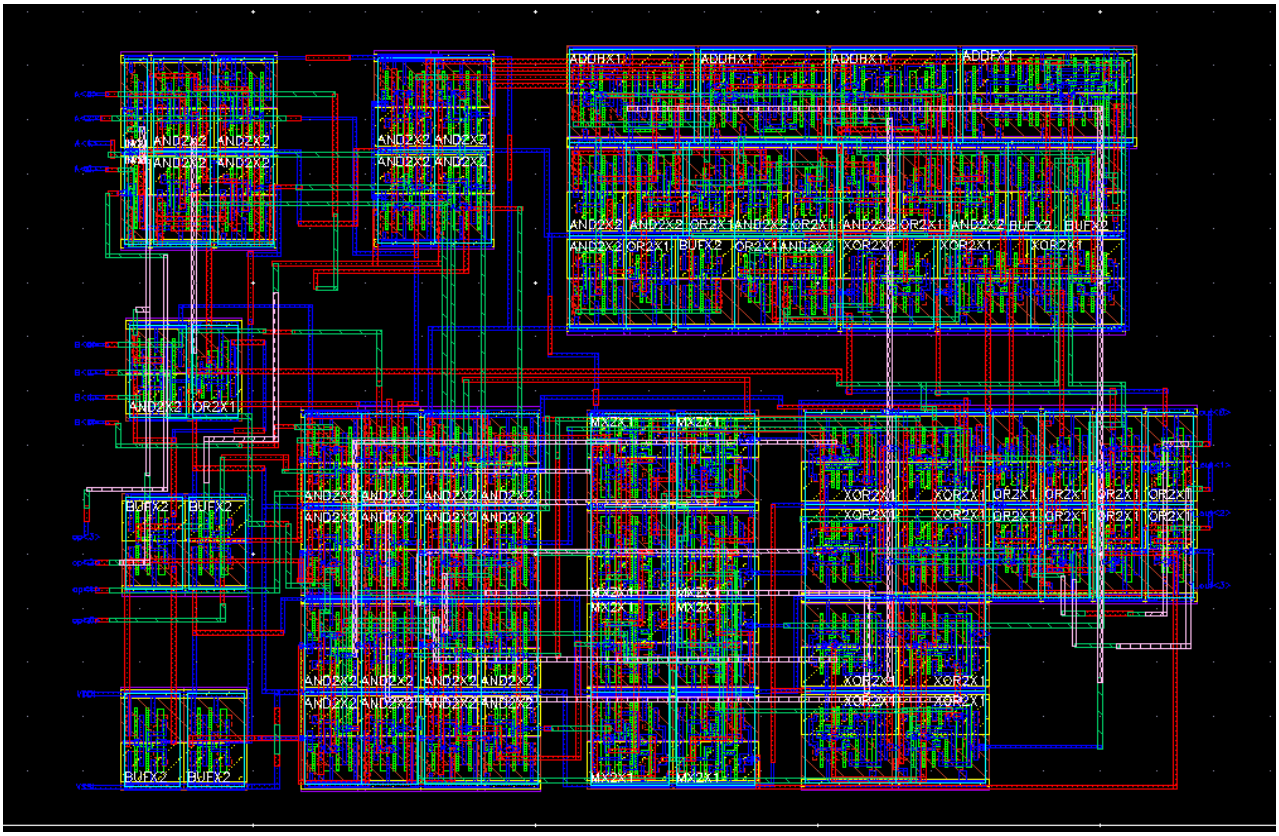

Figure 22: ALU layout

Overview circuit

Schematic Print

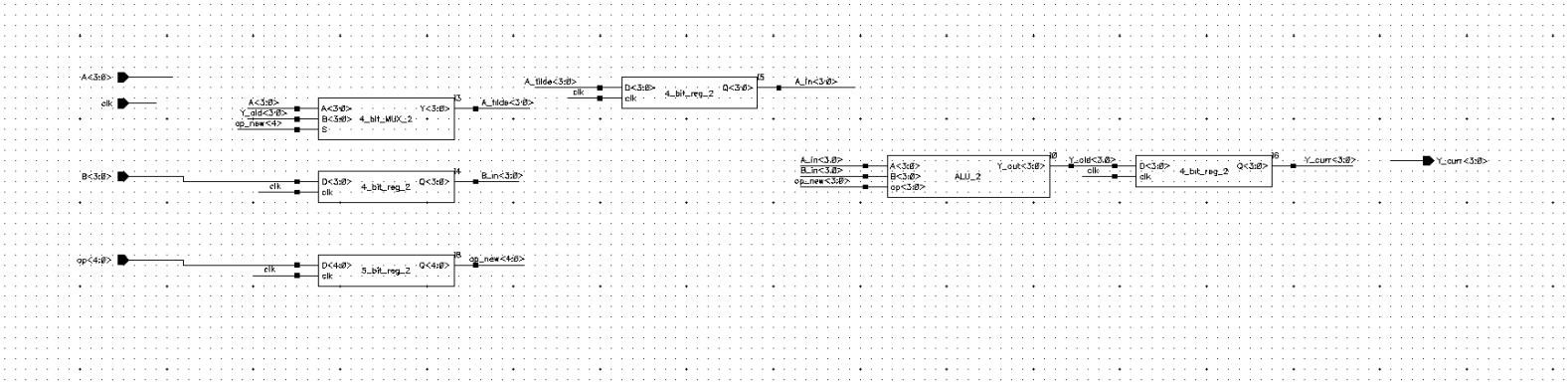

Figure 23: Overview circuit schematic

Layout Print

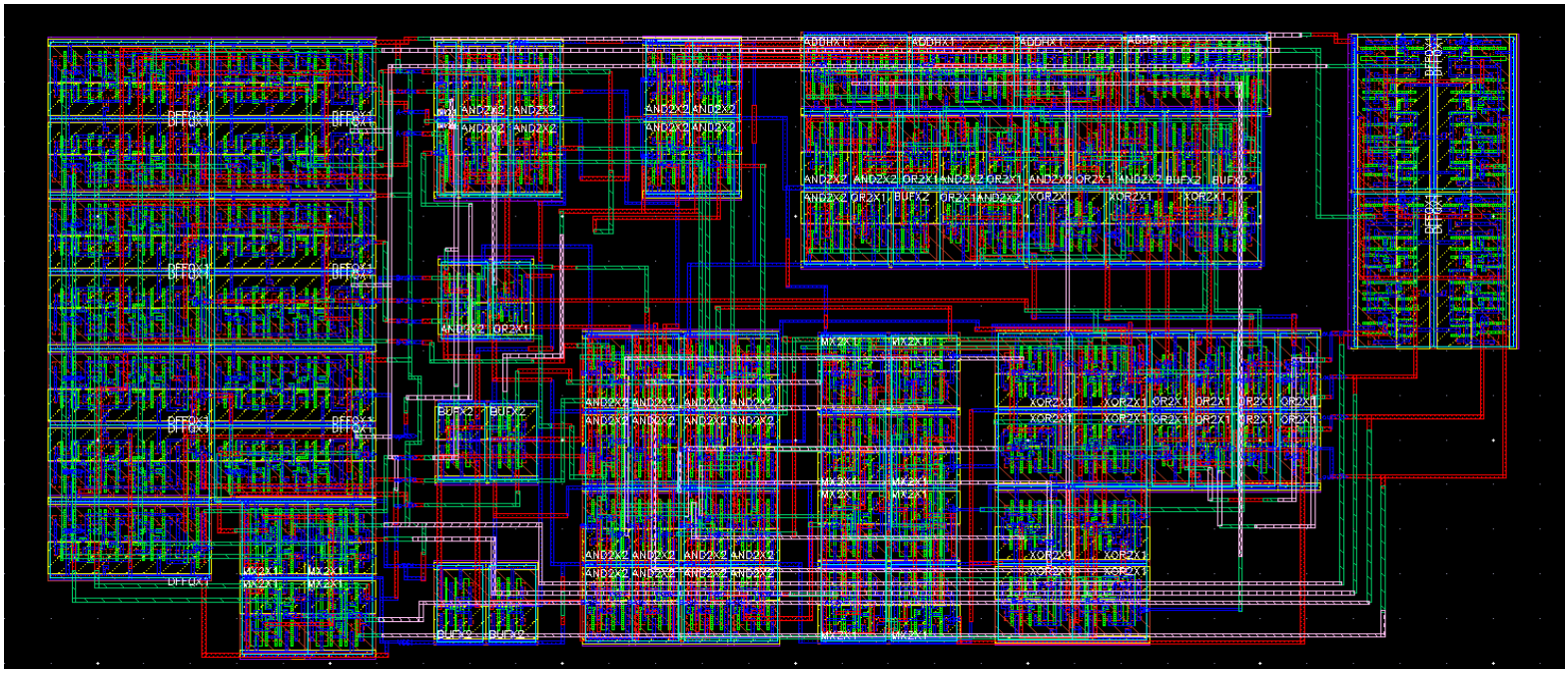

Figure 24: Overview circuit layout

Realization area

The final realization area is 31.615μm by 13.92μm =**440.0808 $\boldsymbol{\mu m^2}$** which is less than the projected area of **442.0992 $\boldsymbol{\mu m^2}$** which thus satisfies the constraint of the realization area not occupying more than 150% of the total area of the cells. In addition to this, only 4 layers of metal were used in the making of the final circuit with every individual block before the ALU using only 3 layers of metal at maximum.