Simulation results of proper working

Top view circuit test with calculated maximal frequencies

operation	feedback	Op<4>	Op<3>	Op<2>	Op<1>	Op<0>
Addition	No	0	0	0	*	*
Subtraction	No	0	0	1	*	*
XOR	No	0	1	0	*	*
Shift by 2	No	0	1	1	1	0
Addition	Yes	1	0	0	*	*
Subtraction	Yes	1	0	1	*	*
XOR	Yes	1	1	0	*	*
Shift by 2	Yes	1	1	1	1	0

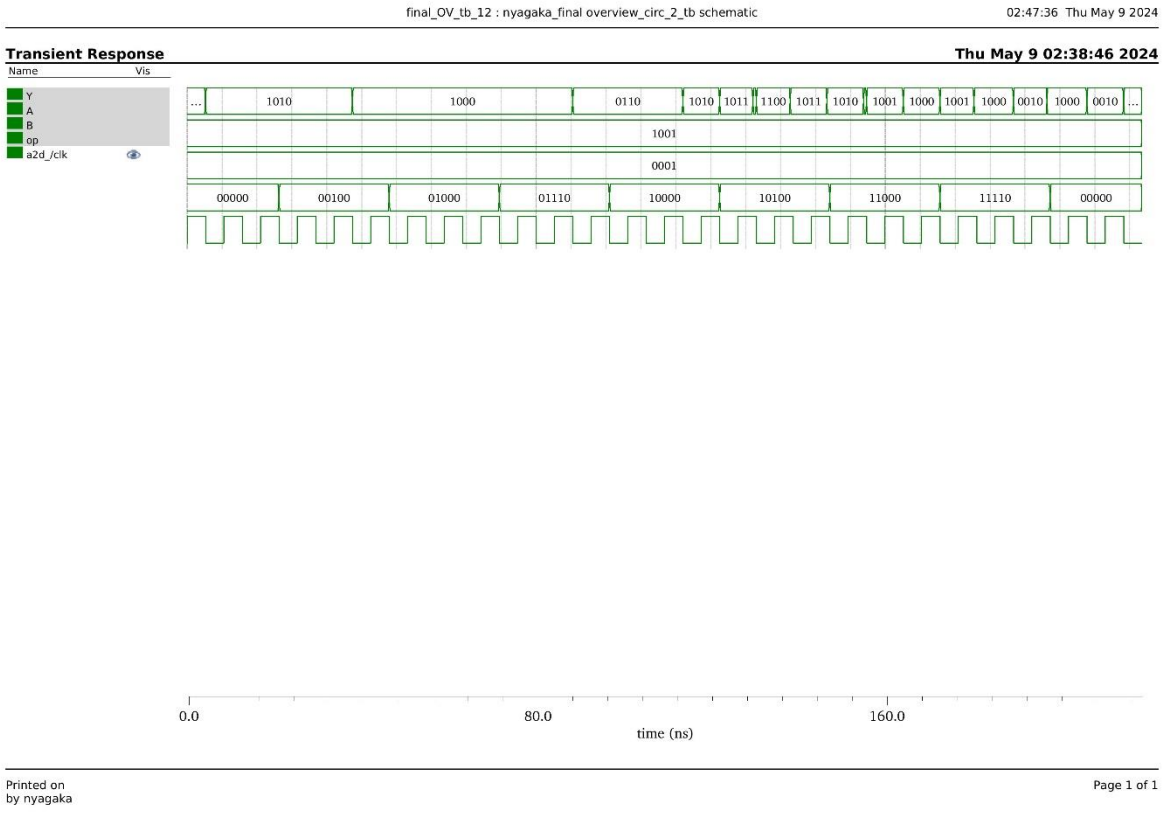

Figure 1: Final circuit functioning for VDD=1.2V

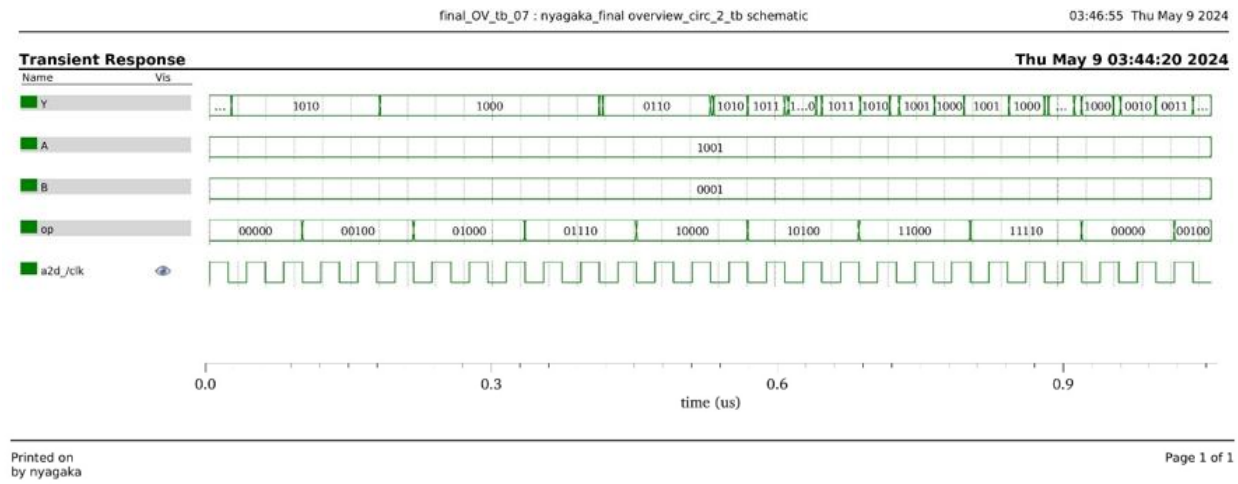

Figure 2: Final circuit functioning for VDD=0.7V

A and **B** are the signals at the input before the registers, **op** is the opcode before the register and **Y** is the output of the circuit at the output register.

The graphs may seem cutoff but that's a result of the way they're extracted from the software. The circuits are functional, and it should be noted that for $V_{DD} = 1.2V$ the clock period is $8.4n$ and for $V_{DD} = 0.7V$ the clock period is $39.3n$ as a result of the differing minimal periods.

The circuits function correctly as it takes 2 clock cycles (2 rising edges) to change output according to opcode for the ALU (without any change in feedback bit) and 3 clock cycles (3 rising edges) to change to and from feedback. This is how we designed our circuit to perform and it works exactly this way. In addition, the outputs subject to the delay after changing operation are in accordance with the opcode.

Steps taken to optimize circuit performance

We make use of **data gating or input gating**. We AND the inputs to all the blocks with an enable bit. The enable bit is 0 if the block is inactive and 1 if the block is active. As a result, whenever a block isn't in use its output is set to zero. This conserves dynamic power. It increased the area of of layout as we had to AND the inputs to every block with a respective select bit but in the long run it proved useful to decreasing power consumption.

In addition to the above, we **made use of 4 buffers to decrease the fan-out** of certain signals from 8 to 4. From the course, we know that the optimal fan-out is 3.6 ~4 thus it was imperative to use these buffers to reduce the fan-out and further reduce the delay of the overall circuit.