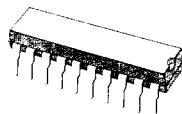


## 8 BIT HCMOS MICROCONTROLLERS WITH A/D CONVERTER

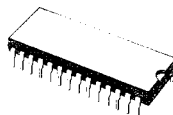
### PRELIMINARY DATA

- 8-BIT ARCHITECTURE
- STATIC HCMOS OPERATION
- 3.0 TO 6.0V SUPPLY OPERATING RANGE
- 3.25 $\mu$ S TCYCLE (with 4MHz clock)
- RUN, WAIT & STOP MODES
- USER ROM : 1828 BYTES
- RESERVED ROM : 220 BYTES
- DATA ROM : 32 BYTES
- DATA RAM : 32 BYTES
- 20-PIN DIP OR SO PLASTIC PACKAGE (ST6010, ST6011, ST6014)
- 28-PIN DIP OR SO PACKAGE (ST6012, ST6013)
- 6 PUSH-PULL BIDIRECTIONAL INPUTS/OUTPUTS WITH 5mA DRIVING CAPABILITY (ST6010)
- 7 PUSH-PULL BIDIRECTIONAL INPUTS/OUTPUTS WITH 5mA DRIVING CAPABILITY (ST6011, ST6012)
- 8 PUSH-PULL BIDIRECTIONAL INPUTS/OUTPUTS WITH 5mA DRIVING CAPABILITY (ST6013, ST6014)
- 8-BIT COUNTER WITH A 7-BIT PROGRAMMABLE PRESCALER (Timer)
- HARDWARE ACTIVATED DIGITAL WATCHDOG FUNCTION (ST6010, ST6012, ST6013, ST6014)
- SOFTWARE ACTIVATED DIGITAL WATCHDOG/TIMER (ST6011)
- 8-BIT A/D CONVERTER WITH 3 (ST6011, ST6014), 7 (ST6010) AND 9 (ST6012, ST6013) ANALOG INPUTS AND SEPARATE ANALOG REFERENCE VOLTAGE (not available in ST6010)
- ONE LEVEL OR EDGE SENSITIVE EXTERNAL INTERRUPT INPUT
- ON-CHIP CLOCK OSCILLATOR
- BYTE EFFICIENT INSTRUCTION SET
- BIT TEST AND JUMP INSTRUCTIONS
- WAIT, STOP (ST6011 only) AND BIT MANIPULATION INSTRUCTIONS
- TRUE LIFO 4 LEVEL STACK
- 9 POWERFUL ADDRESSING MODES
- THE ACCUMULATOR, THE X, Y, V & W REGISTERS, THE PORT AND PERIPHERALS DATA/CONTROL REGISTERS ARE ADDRESSED IN THE DATA SPACE AS RAM LOCATIONS

- THE DEVELOPMENT TOOL OF THE ST601X MICROCONTROLLER FAMILY CONSISTS OF THE EMS6-HW/B1X EMULATION AND DEVELOPMENT PACKAGE CONNECTED VIA A STANDARD RS232 SERIAL LINE TO AN IBM PC. THE ST60P1X PIGGYBACK ROMLESS VERSION IS AVAILABLE



DIP-20



DIP-28

(Order Codes at the end of the datasheet)

Figure 1 : ST6010 - ST6011 - ST6012 Pin Configurations.

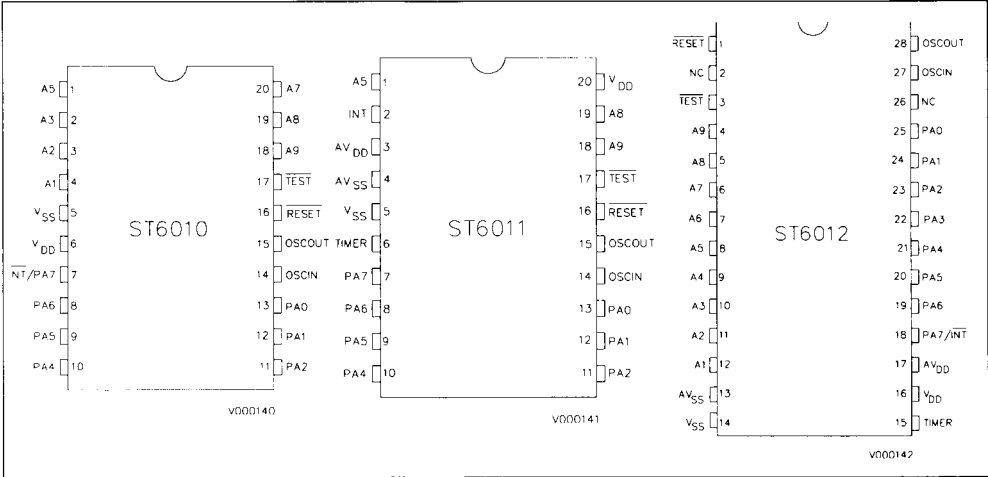
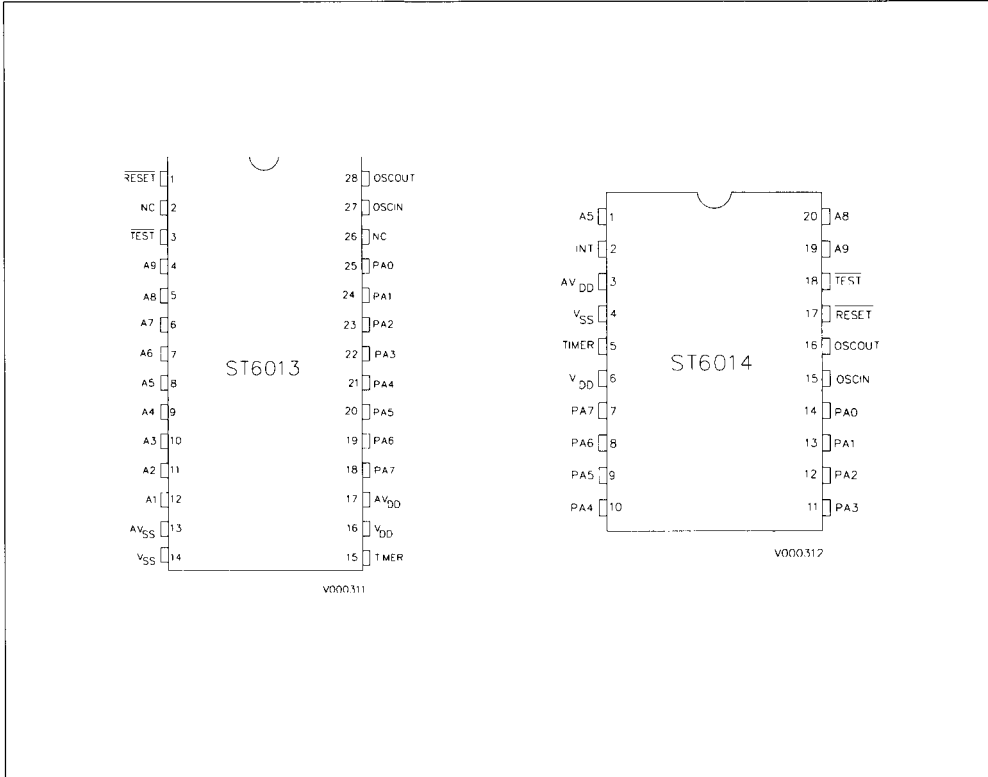


Figure 2 : ST6013 - ST6014 Pin Configurations.

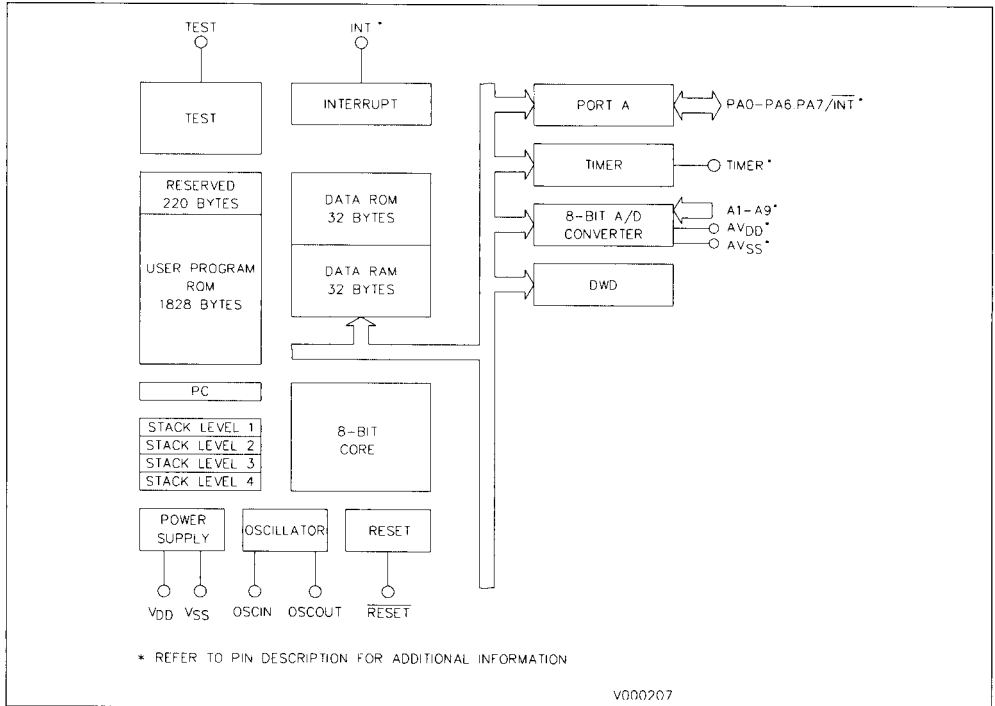


## GENERAL DESCRIPTION

The ST6010, ST6011, ST6012, ST6013 and ST6014 microcontrollers are members of the 8-bit HCMOS ST60XX family, a series of devices oriented to low-medium complexity applications. All ST60XX members are based on a building block approach: to a common core is associated a combination of on-chip peripherals (macrocells) available from a standard library to form around the core all the existing and future ST6 devices. These peripherals are designed with the same core technology giving full compatibility, short design and testing

time. The macrocells of the ST6010/11/12/13/14 are: the Timer that includes an 8-bit counter with a 7-bit software programmable prescaler (Timer), the 8-bit A/D Converter with a different number of analog inputs (ADC) with separate analog reference voltage (ST6012, ST6014 only), the hardware (ST6010/12/13/14) or software (ST6011) activated digital watchdog/timer (DWD). Thanks to these peripherals these devices are well suited for automotive and industrial controls applications.

**Figure 3 : ST601X Block Diagram.**



PIN DESCRIPTION

**VDD and Vss.** Power is supplied to the MCU using these two pins. VDD is power and Vss is the ground connection.

**OSCIN, OSCOUT.** These pins are internally connected to the on-chip oscillator circuit. A crystal quartz or a ceramic resonator has to be connected between these two pins in order to allow a right operating of the MCU. A signal can be also provided to the OSCIN pin as external clock. The OSCIN pin is the input pin, the OSCOUT pin is the output pin.

**RESET.** The active low RESET pin is used to restart the microcontroller at the beginning of its program.

**TEST.** The TEST (mode select) pin is used to place the MCU into special operating mode. If TEST is held at +5V the MCU enters the normal operating mode. If TEST is held at zero when reset is active the test operating mode is automatically selected (the user should connect this pin to VDD for normal operation ).

**INT/PA7 (\*).** The INT pin provides the capability for asynchronous applying an external interrupt to the

MCU. This pin is active low on ST6010, ST6012 and is connected together with the I/O line PA7. On ST6014 is active low but is not connected to I/O line PA7. On ST6011 the interrupt pin is falling edge sensitive while on ST6013 the external interrupt line is not available. (\*) The PA7/INT connection is implemented only on ST6010 and ST6012.

**PA0-PA7.** These 8 lines are organized as one I/O port (A). Each line may be configured as either an input or an output under software control of the data direction register. Port A has a push-pull output configuration with 5mA drive capability and schmitt trigger inputs. (\*) PA3 is not available in ST6010 and ST6011. On ST6010 and ST6012 PA7 and the external interrupt line are connected together.

**A1-A9.** These 9 pins are the analog inputs for the on-chip 8-bit A/D converter. The user can select by software which analog channel has to be converted. The following table summarizes the A/D pins available for the different devices.

Table 1 : A/D Available Inputs for Different ST601X Products.

A/D Input	ST6010	ST6011	ST6012	ST6013	ST6014
A1	Pin 4	NA	Pin 12	Pin 12	NA
A2	Pin 3	NA	Pin 11	Pin 11	NA
A3	Pin 2	NA	Pin 10	Pin 10	NA
A4	NA	NA	Pin 9	Pin 9	NA
A5	Pin 1	Pin 1	Pin 8	Pin 8	Pin 1
A6	NA	NA	Pin 7	Pin 7	NA
A7	Pin 20	NA	Pin 6	Pin 6	NA
A8	Pin 19	Pin 19	Pin 5	Pin 5	Pin 20
A9	Pin 18	Pin 18	Pin 4	Pin 4	Pin 19

**AVDD,AVss.** These pins are used to provide a separate reference voltage to the A/D converter in order to allow high precision conversion. These pins are not available on ST6010. On ST6014 only AVDD is available.

**TIMER.** This is the timer I/O pin. In input mode it is connected to the prescaler and acts as external

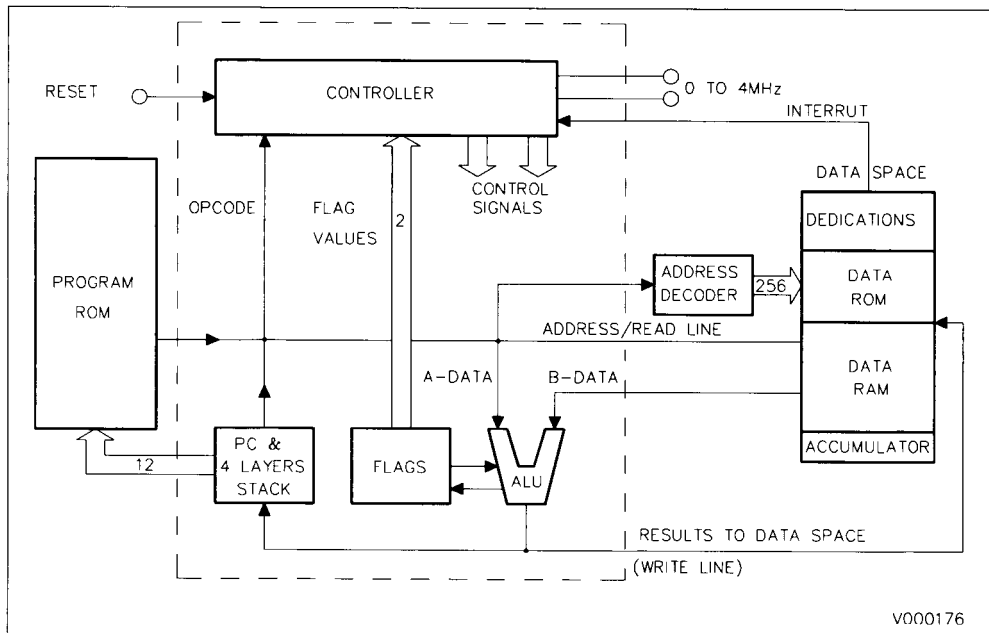
timer clock (DOUT=TOUT=0) or as control gate for the internal timer clock (DOUT=1,TOUT=0). In the output mode the timer pin outputs the data bit when a time out occurs. This pin is not available in ST6010.

## ST60XX CORE

The CORE of the ST60XX Family is implemented independently from the I/O or memory configuration. Consequently, it can be treated as an independent central processor communicating with I/O and memory via internal addresses, data, and control buses. The in-core communications are ar-

ranged as shown in the following block diagram figure; the controller being externally linked to both the reset and the oscillator while the core is linked to the dedicated on-chip macrocells peripherals via the serial data bus and indirectly for interrupt purposes, through the control registers.

**Figure 4 :** ST60XX Core Block Diagram.



## INPUT/OUTPUT PORT

The ST601X has one I/O port (A), each I/O line can be individually programmed either in the input mode or the output mode. ST6010 has 6 I/O lines, while 7 are available on ST6011 and ST6012 and 8 on ST6013 and ST6014. The input mode allows configuring the lines in the high impedance state. The lines are organized in one port (port A). The port occupies two registers in the data space, there being one register, the **DATA register (DR, location 00H)**,

used to read the logic level values of the lines programmed in the input mode or to write the logic value of the signal to be output on the lines configured in the output mode, and another, the **DATA DIRECTION register (DDR, location 04H)**, that allows the selection of the direction of each pin (input or output). In input mode the data register remains unchanged as the logic value at port pins is read directly into the shift register of the port macrocell.

## TIMER

The Timer peripheral consists of an 8-bit counter with a 7-bit programmable prescaler, thus giving a maximum count of  $2^{15}$ , and a control logic that allows configuring the peripheral in three operating modes. The content of the 8-bit counter can be read/written in the Timer/Counter register TCR that can be addressed in the data space as RAM loca-

tion at the 13H address. The state of the 7-bit prescaler can be read in the PSC register at the 12H address. The control logic device can be managed thanks to the TSCR register (14H address). On ST6011, ST6012, ST6013 and ST6014 the external Timer pin is available for the user.

## DIGITAL WATCHDOG/TIMER

The digital watchdog/timer of the ST601X devices consists of a down counter that can be used to provide a controlled recovery from a software upset. On ST6010, ST6012, ST6013 and ST6014 it is automatically initialized after reset so that this function does not need to be activated by the user program. As the watchdog function is always activated this down counter can't be used as a timer. On the ST6011 the watchdog activation can be controlled

by the user software so that the watchdog can be used as a simple 7-bit timer for general purpose counting.

The watchdog is using one data space register (DWDR location 18H) and the watchdog time can be programmed using the 6MSbits in the watchdog register. The check time can be set differently for different routines within the general program.

## 8-BIT A/D CONVERTER

The ST601X A/D converter is an 8-bit analog to digital converter with 3 (ST6011, ST6014), 7 (ST6010), 9 (ST6012, ST6013) analog inputs offering 8-bit resolution with  $\pm 1/2$  bit of linearity and a conversion time of 150uS (clock frequency of 4MHz). The A/D

converter also offers separate analog reference voltage pins. The ST601X A/D peripheral converts by a process of successive approximations using a clock frequency from 100 to 500kHz. The clock is derived from the oscillator with a division factor of

twelve.

## DEVELOPMENT SUPPORT & EMULATION SYSTEM

The ST60XX development system offers powerful in-circuit emulator and easy-to-use sets (dedicated boards) of modular hardware and software tools to

shorten the total system development time of the final application. The ST60XX emulator offers emulation power with plug-in flexibility in the selection of emulation hardware modules for the dedicated macrocells. The emulator can be interfaced with a standard RS232 serial link to industry standard MS-DOS

personal computers. The ST60P1X piggyback version is also available to provide flexibility in prototypes or pre-production.

ABSOLUTE MAXIMUM RATINGS

This product contains devices to protect the inputs against damage due to high static voltages, how-

ever it is advised to take normal precaution to avoid application of any voltage higher than maximum rated voltages. For proper operation it is recommended that  $V_I$  and  $V_O$  must be higher than  $V_{SS}$  and smaller than  $V_{DD}$ . Reliability is enhanced if unused

Symbol	Parameter	Value	Unit
$V_{DD}$	Supply Voltage	- 0.3 to 7.0	V
$V_I$	Input Voltage	$V_{SS} - 0.3$ to $V_{DD} + 0.3$	V
$V_O$	Output Voltage	$V_{SS} - 0.3$ to $V_{DD} + 0.3$	V
$I_O$	Current Drain per Pin Excluding $V_{DD}$ & $V_{SS}$	$\pm 10$	mA
$I_{VDD}$	Total Current into $V_{DD}$ (source)	50	mA
$I_{VSS}$	Total Current out of $V_{SS}$ (sink)	50	mA
PD	Total Power Dissipation	18	mW
ESD	ESD Susceptibility	2000 <sup>(1)</sup>	V
$T_{stg}$	Storage Temperature	- 65 to 150	°C

inputs are connected to an appropriated logic voltage level ( $V_{DD}$  or  $V_{SS}$ ).

Notes : 1. MIL 883B Mode, 100pF through 1.5KΩ.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$T_A$	Operating Temperature	6 Version 7 Version	- 40 - 40		85 110	C C
$V_{DD}$	Operating Supply Voltage		3		6	V
$f_{OSC}$	Oscillator Frequency	$V_{DD} = 4.5 - 6.0V$	0		4	MHz
$f_{OSC}$	Oscillator Frequency	$V_{DD} = 3.5V$	0		1	MHz
$f_{OSC}$	Oscillator Frequency	$V_{DD} = 3.0V$	0		0.5	MHz
$AV_{DD}$ $AV_{SS}$	Analog Supply Voltage		$V_{SS}$		$V_{DD}$	V

2. Stresses above those listed as "absolute maximum ratings" may cause permanent damage to the device. This is a stress

THERMAL CHARACTERISTICS

$R_{th(J-A)}$	Thermal Resistance Plastic DIP 20 Plastic DIP 28 Plastic SO 20 Plastic SO 28	Max.	130 80 160	°C/W
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rating only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

**Note :** On ST6010 AV<sub>DD</sub> and AV<sub>SS</sub> are internally connected to digital V<sub>SS</sub> and V<sub>DD</sub>.

## POWER CONSIDERATIONS

The average chip-junction temperature, T<sub>j</sub>, in Celsius can be obtain from :

$$T_j = T_A + P_D \times R_{thJA}$$

where : T<sub>A</sub> = Ambient Temperature, R<sub>thJA</sub> = Package thermal resistance (junction-to ambient, P<sub>D</sub> = P<sub>int</sub> + P<sub>port</sub>,

P<sub>int</sub> = I<sub>DD</sub> x V<sub>DD</sub> (chip internal power),

P<sub>port</sub> = Port power dissipation (determined by the user).

For most applications, P<sub>port</sub> < P<sub>int</sub> and the former can be neglected. P<sub>port</sub> may become significant if the device is configured to drive darlington bases or sink LED loads. An approximate relationship between P<sub>D</sub> and T<sub>J</sub> (if P<sub>port</sub> is neglected) is :

$$P_D = K (T_J + 273).$$

Solving previous equations gives:

$$K = P_D \times (T_A + 273) + R_{thJA} \times P_D^2$$

## DC ELECTRICAL CHARACTERISTICS

T<sub>A</sub> = - 40 to 85°C unless otherwise specified.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V <sub>P</sub>	Positive Threshold	All I/O Lines V <sub>DD</sub> = 3.0V V <sub>DD</sub> = 4.5V V <sub>DD</sub> = 5.5V	1.8 2.8 3.6	2.0 3.2 4.0	2.2 3.8 4.4	V
V <sub>N</sub>	Negative Threshold	All I/O Lines V <sub>DD</sub> = 3.0V V <sub>DD</sub> = 4.5V V <sub>DD</sub> = 5.5V	1.1 1.6 2.0	1.3 2.0 2.4	1.5 2.4 2.8	V
V <sub>H</sub>	Hysteresis Voltage	All I/O Lines V <sub>DD</sub> = 3.0V V <sub>DD</sub> = 4.5V V <sub>DD</sub> = 5.5V	0.6 0.9 1.1	0.8 1.2 1.6	0.9 1.4 1.8	V
V <sub>IL</sub>	Input Low Level Voltage	RESET PIN V <sub>DD</sub> = 3.0V V <sub>DD</sub> = 4.5V V <sub>DD</sub> = 5.5V			0.90 1.35 1.65	V
V <sub>IL</sub>	Input Low Level Voltage	INT PIN V <sub>DD</sub> = 3.0V V <sub>DD</sub> = 4.5V V <sub>DD</sub> = 5.5V			0.90 1.35 1.65	V
V <sub>IH</sub>	Input High Level Voltage	RESET PIN V <sub>DD</sub> = 3.0V V <sub>DD</sub> = 4.5V V <sub>DD</sub> = 5.5V	2.10 3.15 3.85			V
V <sub>IH</sub>	Input High Level Voltage	INT PIN V <sub>DD</sub> = 3.0V V <sub>DD</sub> = 4.5V V <sub>DD</sub> = 5.5V	2.10 3.15 3.85			V
V <sub>OL</sub>	Low Level Output Voltage	All I/O Lines I <sub>O</sub> < 1μA V <sub>DD</sub> = 3.0V V <sub>DD</sub> = 5.5V			0.1 0.1	V
V <sub>OL</sub>	Low Level Output Voltage	All I/O Lines I <sub>OL</sub> < 5mA V <sub>DD</sub> = 4.5V V <sub>DD</sub> = 5.5V			0.8 0.8	V
V <sub>OH</sub>	High Level Output Voltage	All I/O Lines I <sub>O</sub> < 1μA V <sub>DD</sub> = 3.0V V <sub>DD</sub> = 5.5V	2.9 5.4			V
V <sub>OH</sub>	High Level Output Voltage	All I/O Lines I <sub>OH</sub> = -5mA V <sub>DD</sub> = 4.5V V <sub>DD</sub> = 5.5V	3.0 4.0			V



## DC ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$I_{IL}, I_{IH}$	Input Leakage Current	All Digital Inputs $V_{in} = V_{DD}$ or $V_{SS}$ $V_{DD} = 3.0V$ $V_{DD} = 5.5V$		0.1 0.1	1.0 1.0	$\mu A$
$I_{IL}, I_{IH}$	Input Leakage Current	All A/D Conv. Inputs $V_{in} = V_{DD}$ or $V_{SS}$ $V_{DD} = 3.0V$ $V_{DD} = 5.5V$		0.1 0.1	1.0 1.0	$\mu A$
$V_{ON}$	Trigger Level ON Voltage	RESET $V_{DD} = 3.0V$ $V_{DD} = 4.5V$ $V_{DD} = 5.5V$			1.0 1.5 1.7	V
$V_{OFF}$	Trigger Level OFF Voltage	RESET $V_{DD} = 3.0V$ $V_{DD} = 4.5V$ $V_{DD} = 5.5V$	2.0 3.0 3.8			V
$I_{DD}$	Supply Current RUN Mode	$I_{Load} = 0mA$ $F_{osc} = 0.5MHz$ $V_{DD} = 3.0V$ $F_{osc} = 4.0MHz$ $V_{DD} = 5.5V$			2.0 3.0	mA mA
$I_{DD}$	Supply Current WAIT Mode	$I_{Load} = 0mA$ $F_{osc} = 0.5MHz$ $V_{DD} = 3.0V$ $F_{osc} = 4.0MHz$ $V_{DD} = 5.5V$			1.0 1.5	mA mA
$I_{DD}$	Supply Current STOP Mode	Note 1 $I_{Load} = 0mA$ $V_{DD} = 3.0V$ $V_{DD} = 5.5V$			3 10	$\mu A$ $\mu A$

## AC ELECTRICAL CHARACTERISTICS

$T_A = -40$  to  $85^\circ C$  unless otherwise specified.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$f_{OSC}$	Oscillator Frequency	Crystal or External Clock $V_{DD} = 3.0V$ $V_{DD} = 4.5V$ $V_{DD} = 5.5V$	DC DC DC		0.5 4 4	MHz
$t_{SU}$	Oscillator Start-up Time	$V_{DD} = 3.0V$ $V_{DD} = 4.5V$ $V_{DD} = 5.5V$			15 10 10	mS
$t_{HI}$	Level Interr. Hold Time	$V_{DD} = 3.0V$ $V_{DD} = 4.5V$	$5 \cdot t_{cyc}$			$\mu s$
$C_{IN}$	Input Capacitance	All Inputs Pins			10	pF
$C_{OUT}$	Output Capacitance	All Output Pins			15	pF

A/D CONVERTER CHARACTERISTICS

T<sub>A</sub> = – 40 to 85°C unless otherwise specified.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Res	Resolution		8	8	8	Bit
Lin	Non Linearity	Max Deviation from the Best Straight Line			± 1/2	LSB
Qe	Quantization Error	Uncertainly due to converter resolution.			± 1/2	LSB
ZO	Zero Offset	V <sub>in</sub> = AV <sub>SS</sub>			1	LSB
FSO	Full Scale Offset	V <sub>in</sub> = AV <sub>DD</sub>			1	LSB
t <sub>C</sub>	Conversion Time	f <sub>OSC</sub> = 4MHz <sup>(1)</sup>		150		µs
V <sub>AN</sub>	Conversion Range		AV <sub>SS</sub>		AV <sub>DD</sub>	V
ZIR	Zero Input Reading	Conversion result when V <sub>in</sub> = AV <sub>SS</sub> .	00			Hex
FSR	Full Scale Reading	Conversion result when V <sub>in</sub> = AV <sub>DD</sub> .			FF	Hex
AV <sub>SS</sub> AV <sub>DD</sub>	Analog Reference	(2)	V <sub>SS</sub>		V <sub>DD</sub>	V
AC <sub>IN</sub>	Analog Input Capacitance				5	pF
ASI	Analog Source Impedance				30	KΩ
SSI	Analog Refer. Supply Imped.				2	KΩ

where K is constant pertaining to the particular part. K can be determined from the equation by measuring

TIMER CHARACTERISTICS

T<sub>A</sub> = – 40 to 85°C unless otherwise specified

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
tRes	Timer Resolution		$\frac{1}{f_o} \cdot 12$			s
f <sub>IN</sub>	Input Frequency on TIMER Pin	V <sub>DD</sub> = 3.0V V <sub>DD</sub> = 4.5V		$\frac{1}{4} f_{osc}$		MHz

## ORDERING INFORMATION

The following chapter deals with the procedure for transfer the Program/Data ROM codes to SGS-THOMSON.

**Communication of the ROM content.** To communicate the contents of Program/Data ROM memories to SGS-THOMSON, the customer has to send one 2764 EPROM that must be programmed as follows:

0000H-087FH	Reserved (Should be filled with FFH)
0880H-0F9FH	User program
0FA0H-0FFBH	Reserved (Should be filled with FFH)
0FFCH	Interrupt vector LOW byte
0FFDH	Interrupt vector HIGH byte
0FFEH	Reset vector LOW byte
0FFFH	Reset vector HIGH byte

the Data ROM space (32 Bytes) of the microcontroller must be placed in the EPROM from:

1160H-117FH

All unused bytes must be filled with FFH. For shipment to SGS-THOMSON the EPROM should be placed in a conductive IC carrier and packaged carefully.

**Listing Generation & Verification.** When SGS-THOMSON receives the EPROM a computer listing is generated from the EPROM. This listing corresponds exactly to the mask that will be used to produce the microcontroller. Then the listing is returned to the customer that must thoroughly check, complete, sign and return it to SGS-THOMSON. SGS-THOMSON will also program one 2764 EPROM from the data file corresponding to the listing to help the customer in its verification. The signed listing constitutes a part of the contractual agreement for the creation of the customer mask. SGS-THOMSON sales organization will provide detailed information on contractual points.

## ST601X Part Number

ST60YYB6/XX

Device	_____	_____	Customer ROM Code
Package	_____	_____	Temperature Range

Device : ST6010, ST6011, ST6012, ST6013, ST6014

Package: B:Pin Plastic Dual-in-Line, M:Plastic SO

Temperature range : - 40°C to 85°C 6

Temperature range : - 40°C to 110°C 7

Marking : it is by default equivalent to the sales type (part number). If a special marking is required see attached option list chart.

Temperature range : – 40°C to 85°C 6

Temperature range : – 40°C to 110°C 7

Marking : it is by default equivalent to the sales type (part number). If a special marking is required see attached option list chart.

ST601X MICROCONTROLLER OPTION LIST

Customer .....  
Address .....  
Contact .....  
Phone No .....  
Reference .....

Device [ ] (d)

Package [ ] (p)

Temperature Range [ ] (t)

For marking one line with 11 characters maximum is possible

Special Marking [ ] (y/n) Line 1 "....." (M)

[d] 1 = ST6010, 2 = ST6011, 3 = ST6012, 4 = ST6013, 5=ST6014

[p] B = Plastic Dual in Line, M = Plastic SO

(t) 6 = – 40 to 85°C

7 = – 40 to 110°C