50th Anniversary of Moore's Law

Mr. C

Agenda

- Mr. C 101 in 30 seconds
- Set the Stage
  - A Few Terms, Why Si?, How are ICs made?
- Moore's Law
- Is Moore's Law now dead? What's next?

One Pager – Mr. C

- VP Technology & IP, MonolithIC 3D Inc.
  - Industry Affiliate Partner at the Stanford University Nanofabrication Facility (SNF)
  - Visiting researcher at Rice University Chemistry Department
- CTO Cronquist Consulting
  - 3DIC, Yield, NPI, Foundry Mgmt, Radiation effects on microelectronics
- Sr. Director Technology & Foundry, Actel Corp (FPGAs)
  - PI on 24M$ of government funded research on radiation hardening
- Other Startups: Chartered Semiconductor (now Global Foundries) and Sierra Semiconductor (now PMC-Sierra)
- Also American Microelectronics Inc. (AMI) & Synertek/Honeywell
- 100+ technical papers, 80+ patents held or in application
- BS Chemistry Santa Clara University, cum laude, Chemistry Medal

One Picture – Mr. C

Agenda

- Mr. C 101 in 1 minute
- Set the Stage
  - A Few Terms, Why Si?, How are ICs made?
- Moore's Law
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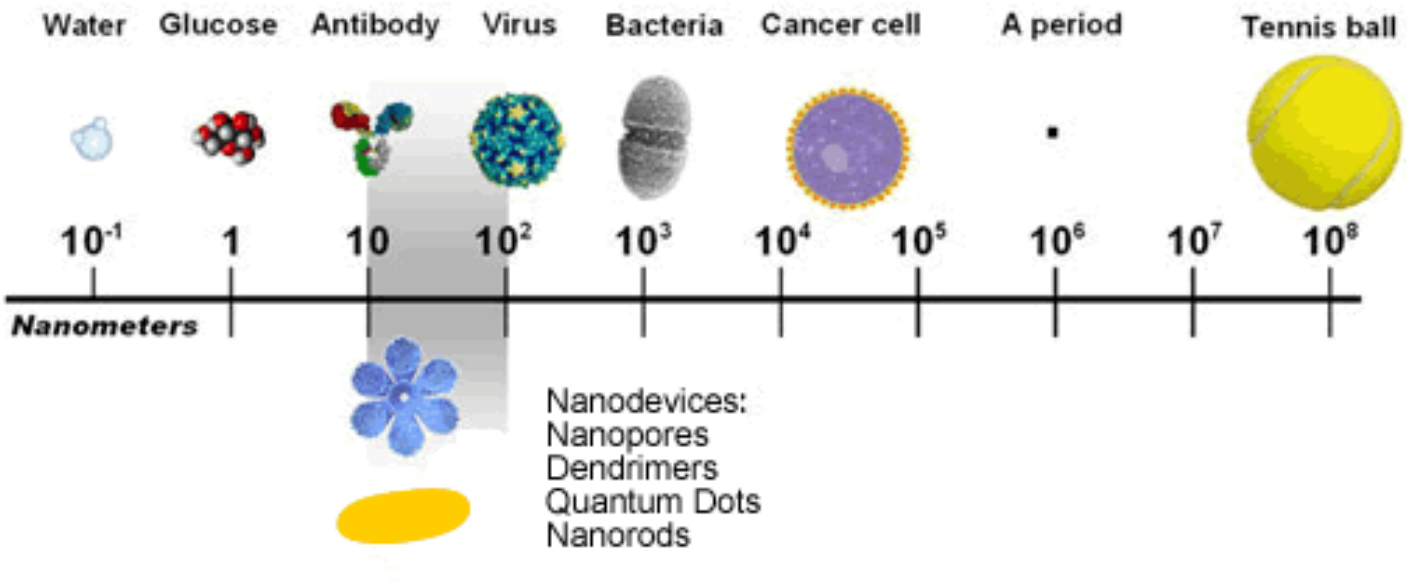
A Few Terms

- Angstrom (10^{-10}m), nanometer (10^{-9}m), micron (10^{-6}m)
- Volts/Amps/Ohms: milli-, micro-, nano-, femto-
- Transistor
- Resistor
- Capacitor



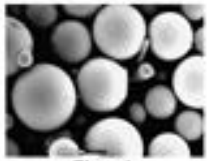
The Scale of Things – Nanometers and More

Things Natural

Dust mite
200 μm

Ant
~ 5 mm

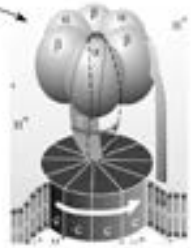
Human hair
~ 60-120 μm wide



Fly ash
~ 10-20 μm

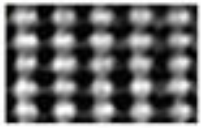
Red blood cells
(~7-8 μm)

~10 nm diameter

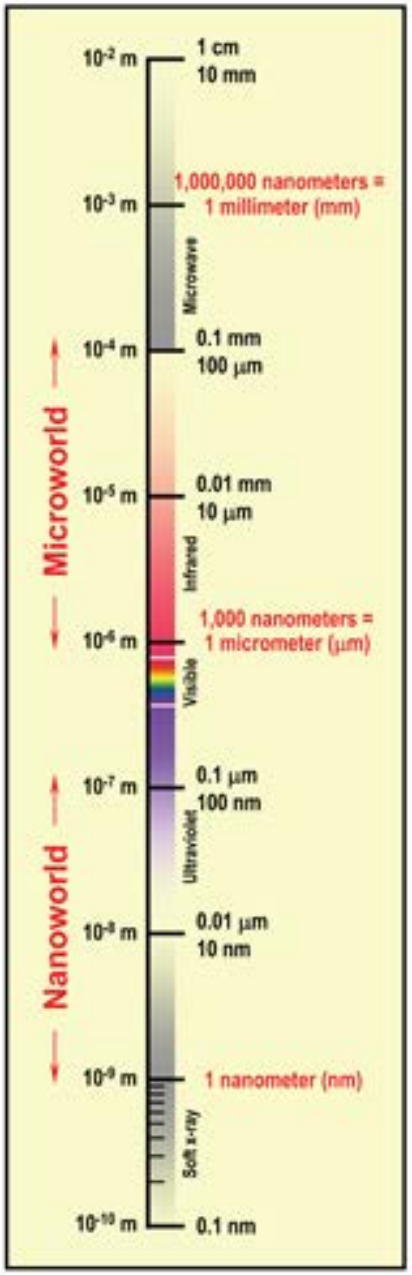


ATP synthase

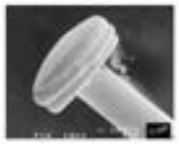
DNA
~2-1/2 nm diameter



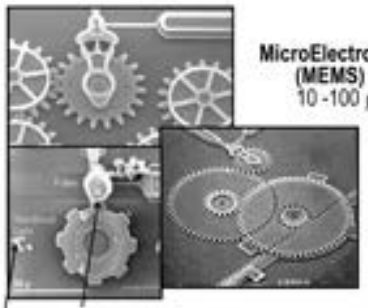
Atoms of silicon
spacing 0.078 nm



Things Manmade

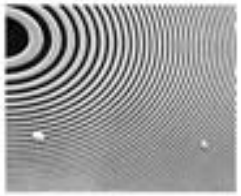


Head of a pin
1-2 mm

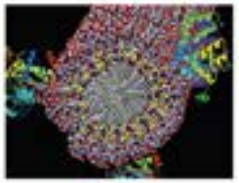


MicroElectroMechanical
(MEMS) devices
10 -100 μm wide

Pollen grain
Red blood cells

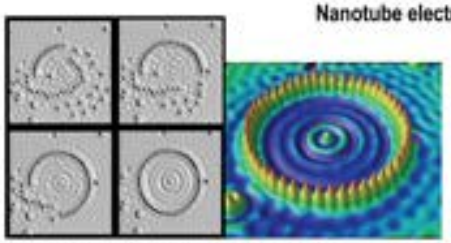


Zone plate x-ray "lens"
Outer ring spacing ~35 nm

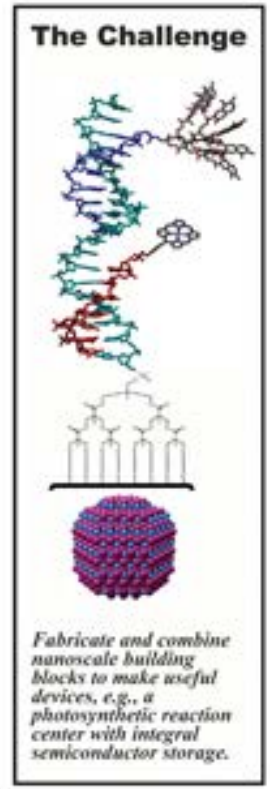


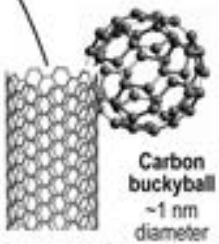
Self-assembled,
Nature-inspired structure
Many 10s of nm

Nanotube electrode



Quantum corral of 48 iron atoms on copper surface
positioned one at a time with an STM tip
Corral diameter 14 nm



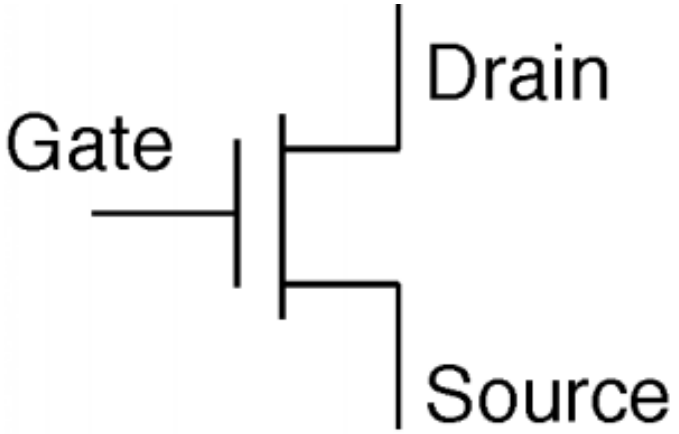


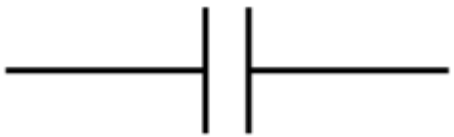
Carbon
buckyball
~1 nm
diameter

Carbon nanotube
~1.3 nm diameter

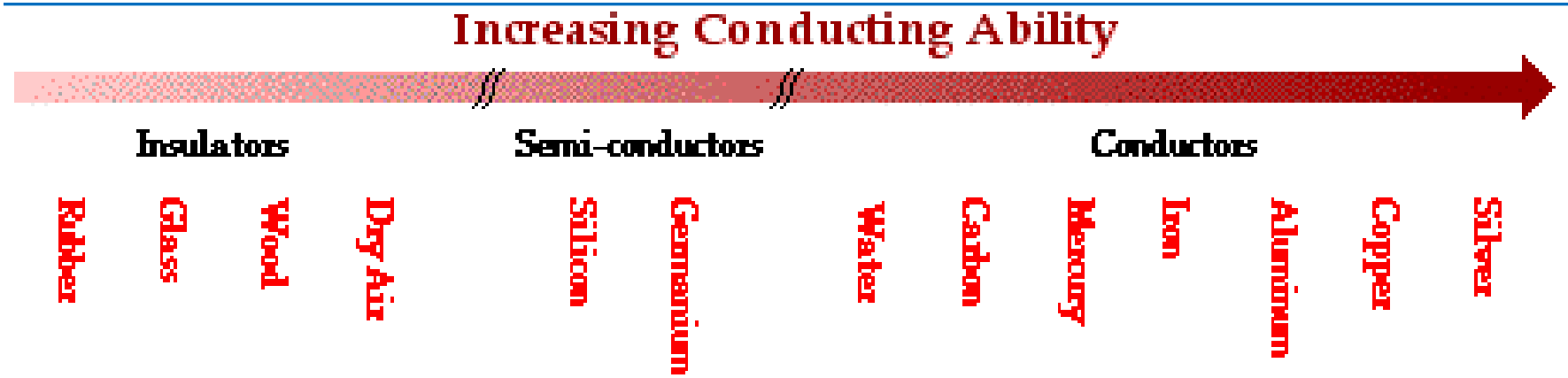
A Few Terms

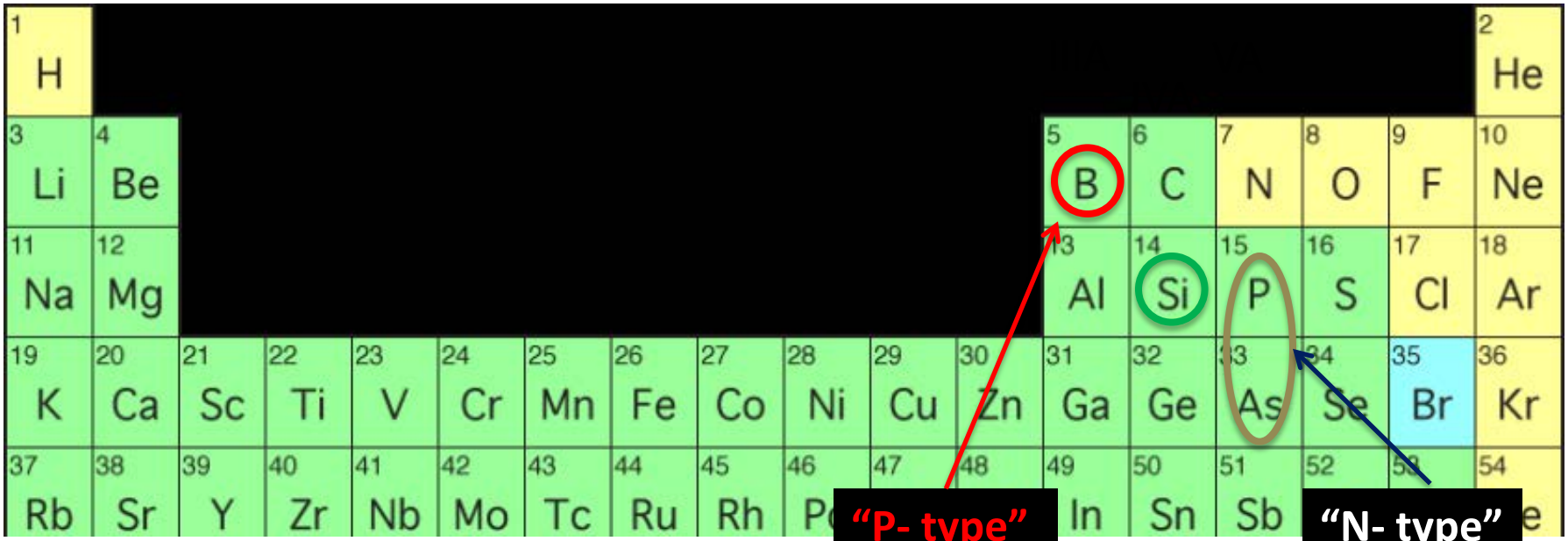
- Transistor – Amplified Switch
- Resistor – Obstructs e^- flow
- Capacitor – stores charge





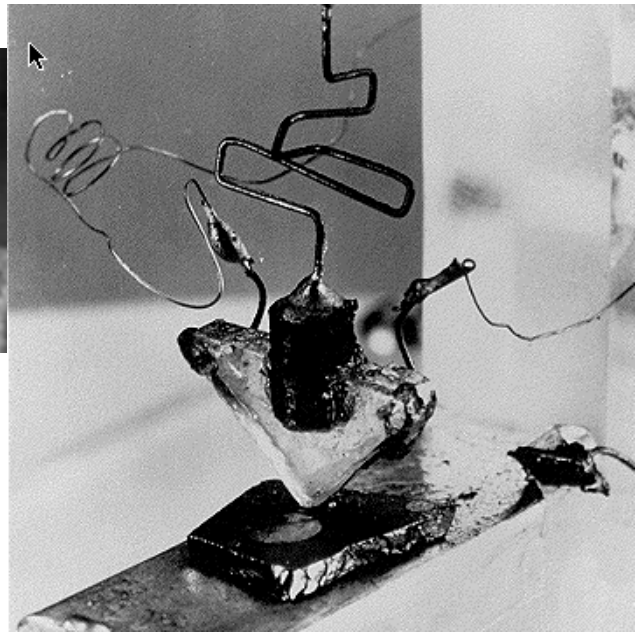
Semiconductors and Doping

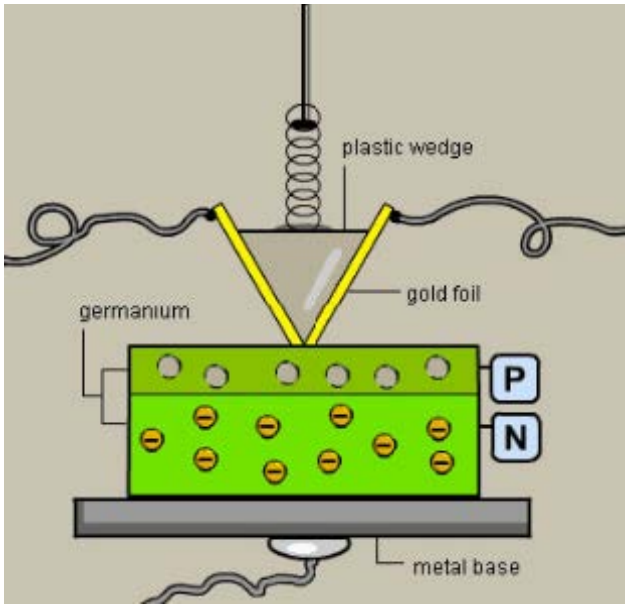




Invention of Transistor

- Julius Lilienfeld
  - Proposed the MESFET & MOSFET but never made
- The Nobel Prize in Physics 1956 was awarded jointly to William Bradford Shockley, John Bardeen and Walter Houser Brattain "*for their researches on semiconductors and their discovery of the transistor effect*"





Silicon (of the Valley)

- Si based devices are >95% of worldwide devices sold
- Bardeen, Brattain, & Shockley used Ge….Why Si?
  - Leaky junctions
    - Ge narrow bandgap (0.66eV); Si is 1.1 eV
  - Oxide Quality/Manufacturing
    - SiO_2 selectively etched to Si (HF); GeO_2 dissolves in H_2O
    - III-V (GaAs): leaves metal at the oxide interface
  - Intrinsic (un-doped) Resistivity
    - Ge = 47 Ω-cm; Si = 230,000 Ω-cm
  - Si: naturally occurring in silica and silicates, plentiful

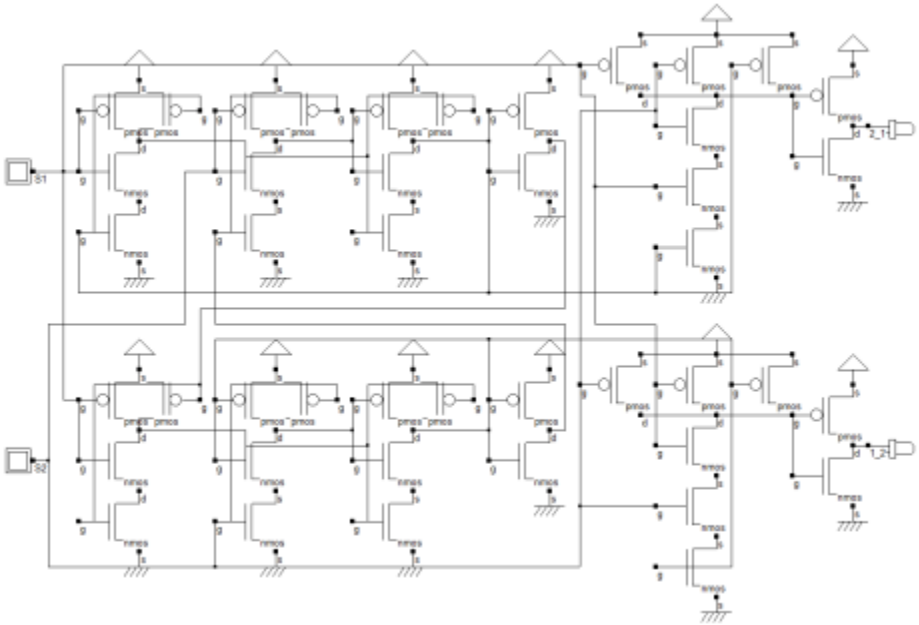
Where are IC's made? – a *Wafer Fab*

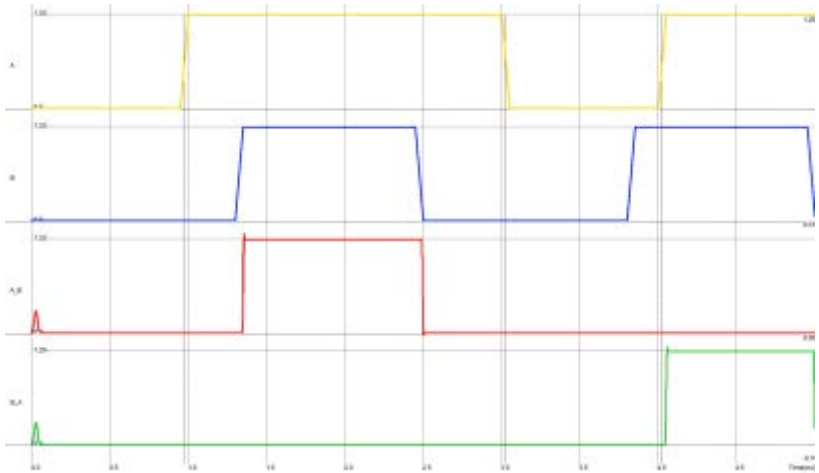
How are ICs made?

- Electrical Design & Simulation
- Physical Layout and Data Conversion to 'mask data'
- In the Wafer Fab Cleanroom:
  - Runsheet ('Cookbook'): 100's to 1000's of individual steps
  - Repetitions of combinations of:
    - Oxidation/Deposition/Diffusion, Lithography, Etching, Ion-Implant
- Assembly and Packaging
- Testing

The MicroChip- TECH Museum 2' Intro

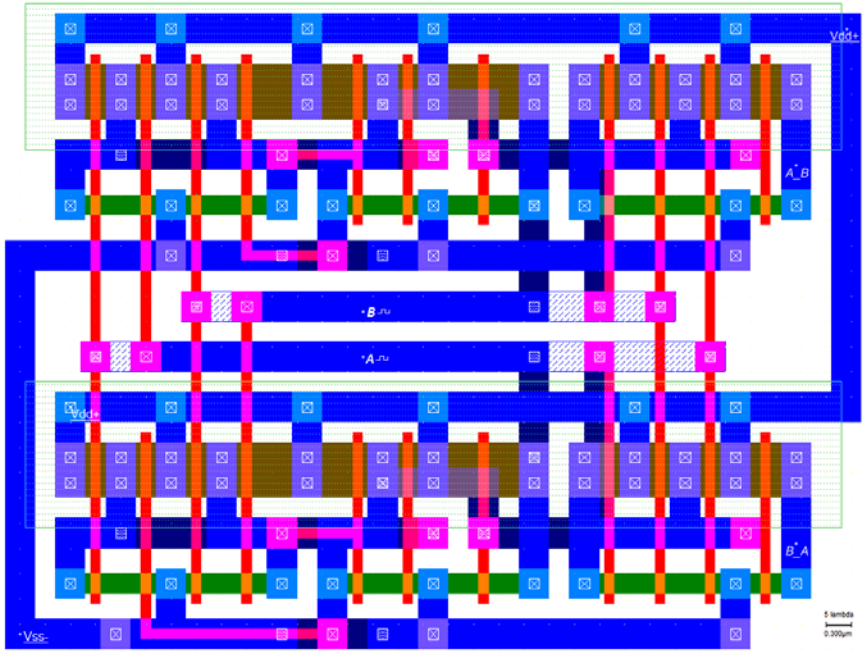
Chip Electrical Design & Simulation

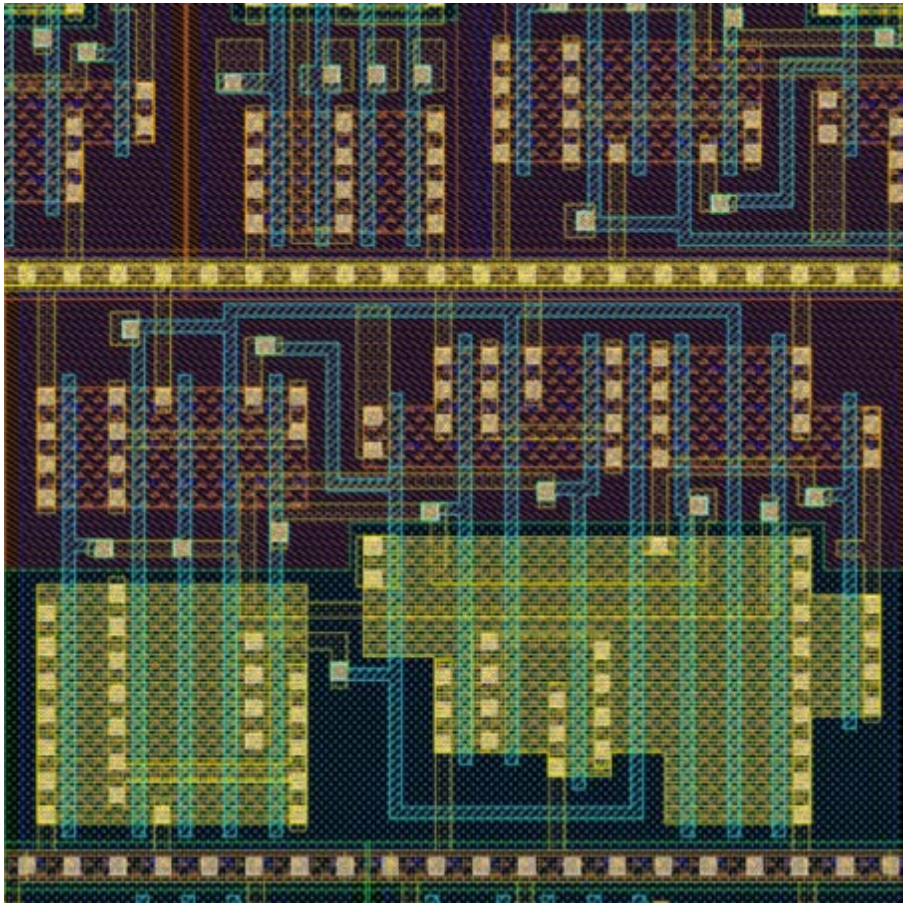




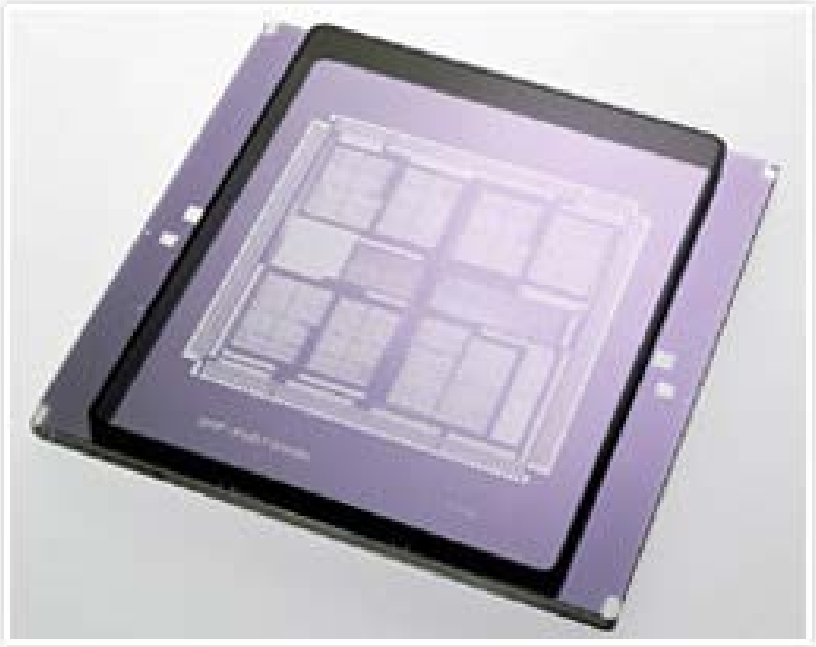
```
public:
        Wave() : fileName("Untitled.wav"), numOfChannels(2),
sampleRate(44100), byteRate(176400), blockAlign(4), bitsPerSample(16),
length(0), data(NULL) {
        }
        Wave(const std::string& fileName) : fileName(fileName),
numOfChannels(2), sampleRate(44100), byteRate(176400), blockAlign(4),
bitsPerSample(16), length(0), data(NULL) {
            load();
        }
        Wave(uint16_t numOfChannels, uint32_t sampleRate, uint32_t byteRate,
uint16_t blockAlign, uint16_t bitsPerSample) : fileName("Untitled.wav"),
numOfChannels(numOfChannels), sampleRate(sampleRate), byteRate(byteRate),
blockAlign(blockAlign), bitsPerSample(bitsPerSample), length(0), data(NULL) {
            create();
        }
        Wave(const Wave& audio) : fileName(audio.fileName),
numOfChannels(audio.numOfChannels), sampleRate(audio.sampleRate),
byteRate(audio.byteRate), blockAlign(audio.blockAlign),
bitsPerSample(audio.bitsPerSample), length(audio.length), data(NULL) {
            create();
            std::copy(audio.data, audio.data + audio.length, this->data);
        }
        ~Wave() {
            delete[] this->data;
        }
        inline uint32_t getNumOfChannels() const {
            return this->numOfChannels;
        }
        inline uint32_t getSampleRate() const {
            return this->sampleRate;
        }
        inline uint32_t getByteRate() const {
            return this->byteRate;
        }
        inline uint16_t getBlockAlign() const {
            return this->blockAlign;
        }
        inline uint32_t getBitsPerSample() const {
            return this->bitsPerSample;
        }
        inline uint32_t getLength() const {
            return this->length;
        }
        inline const uint8_t* getData() const {
            return this->data;
        }
        inline int16_t getSample(uint32_t position, uint32_t channel) const {
            return int16_t((uint16_t(this->data[2 * position * this-
>numOfChannels + 2 * channel + 1]) << 8) | this->data[2 * position * this-
>numOfChannels + 2 * channel]);
        }
        inline int16_t getMaxSample() const {
            int16_t max = 0;
            for (uint32_t i = 0; i < this->getNumOfSamples(); i++) {
                for (uint32_t j = 0; j < this->numOfChannels; j++) {
                    if (abs(this->getSample(i, j)) > max) {
```

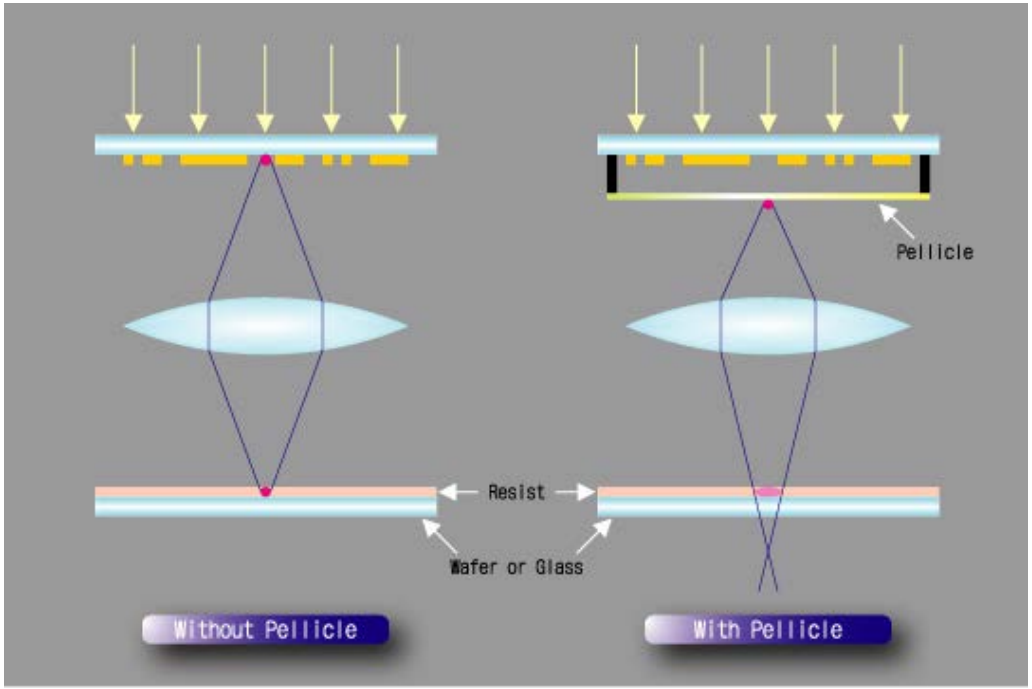
Physical Layout



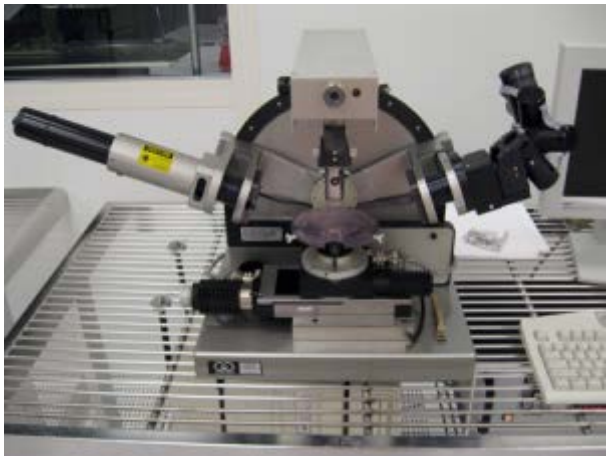


Photomask of each layer & pellicles





In the Wafer Fab Processing

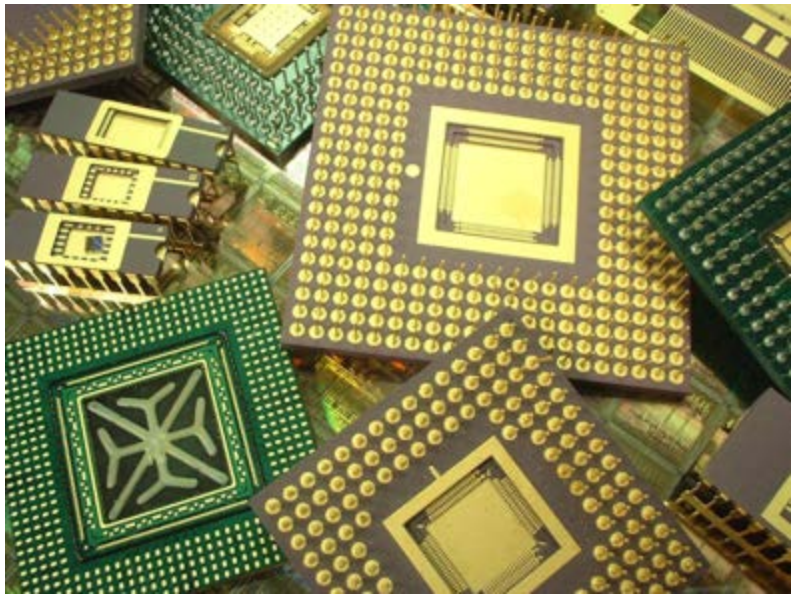


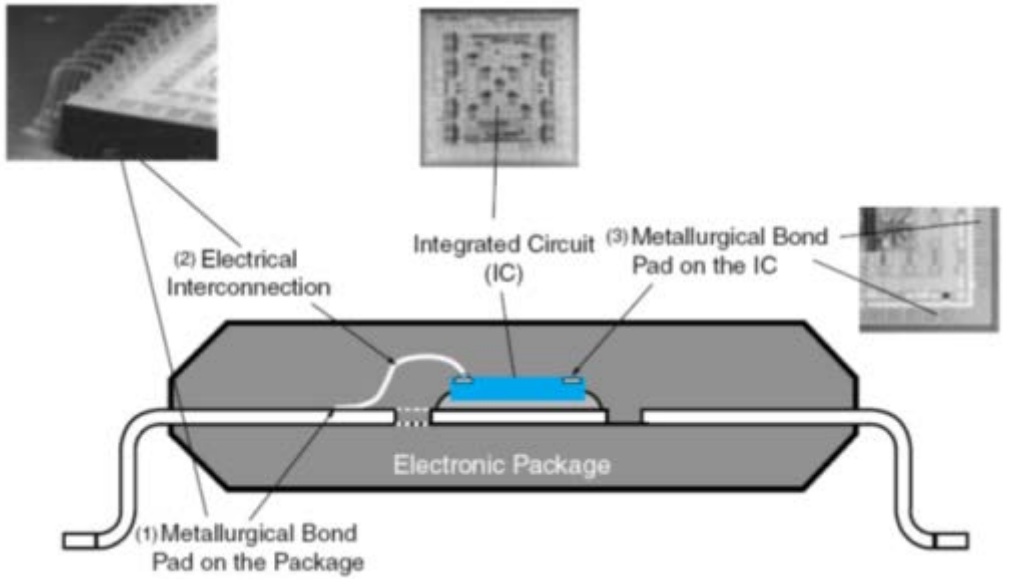
Part 1 Part 2

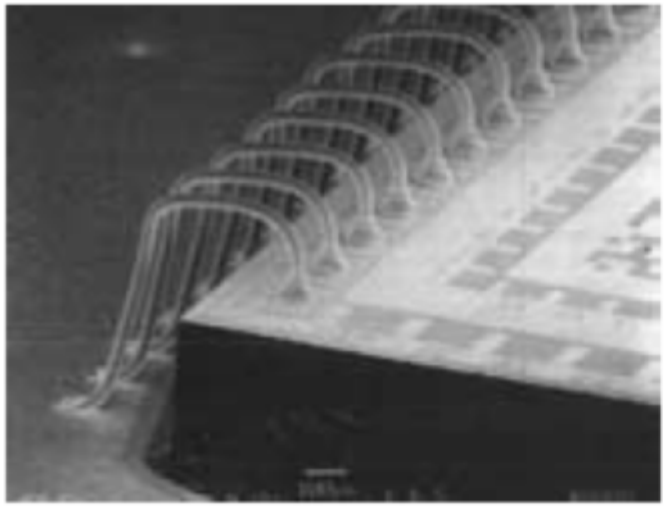
Some Wafer Fab Processes

- Silicon Crystal Growth: Mono-crystalline, Czochralski Silicon
- Oxidation: Thermal SiO_2
- Deposition: CVD (Chemical Vapor Deposition), PECVD (Plasma Enhanced CVD), PVD (Physical Vapor Deposition)
- Lithography: Optical, Electron, X-Ray, Ion
- Etching: Plasma, Ion, Wet chemistry
- Ion Implantation: Precise doping quantity and location
- Diffusion: Thermal, RTA (Rapid Thermal Anneal) LSA (Laser Spike Annealing)

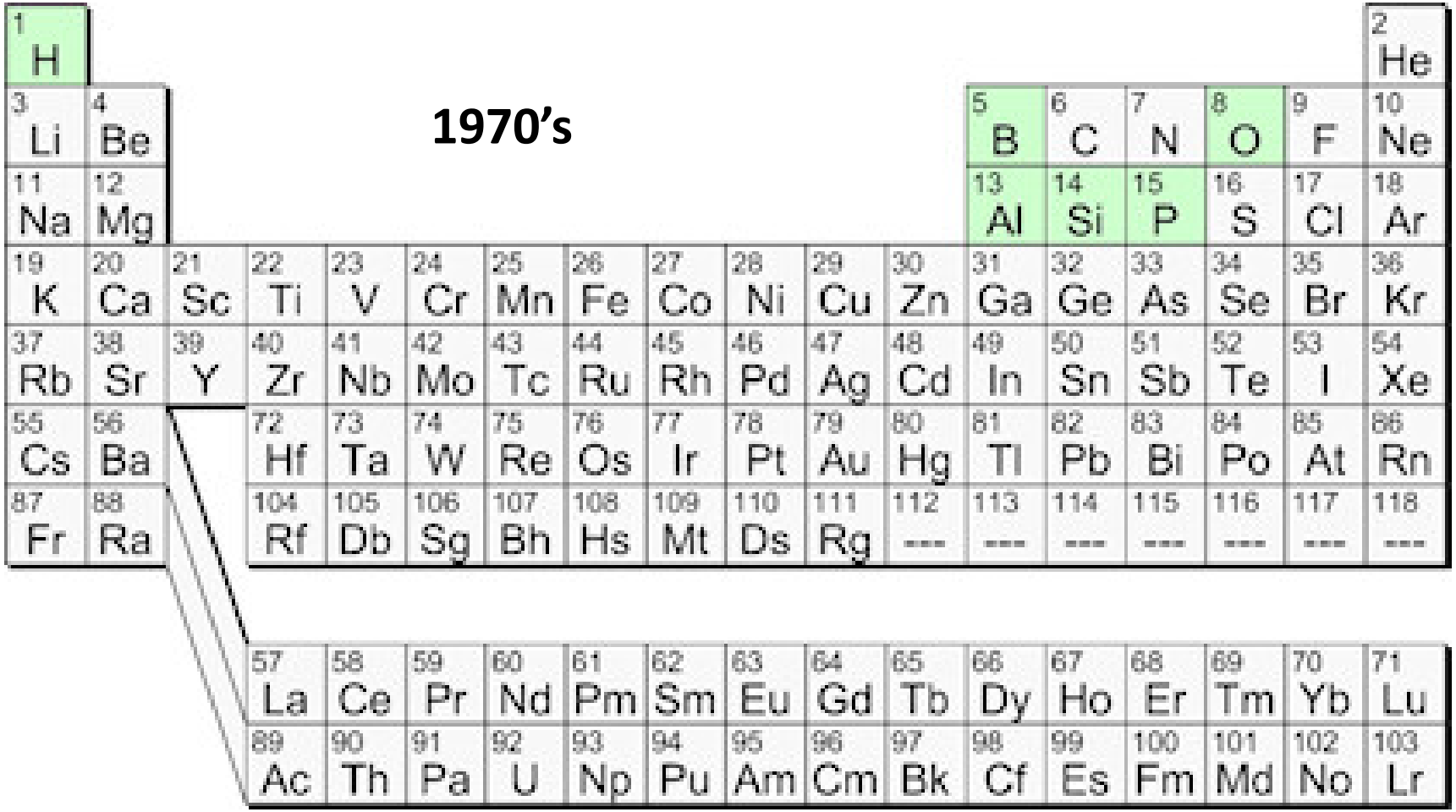
Assembly/Packaging & Testing







Chemistry/Material Science in ICs



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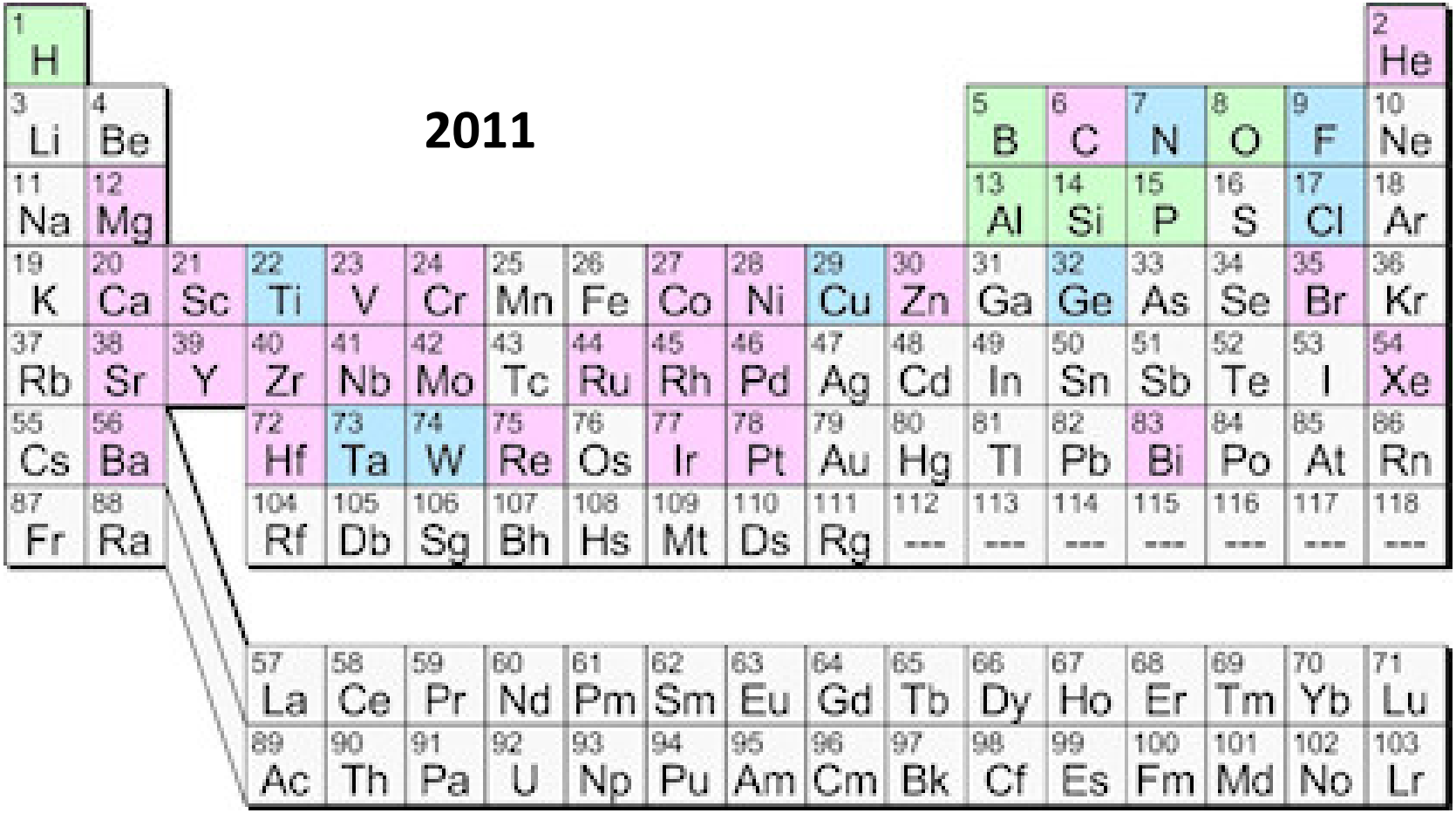

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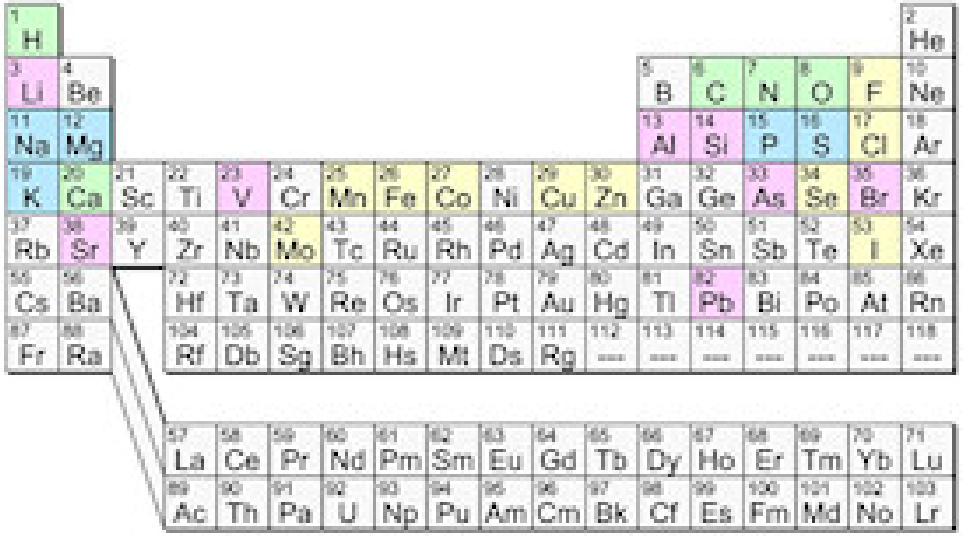
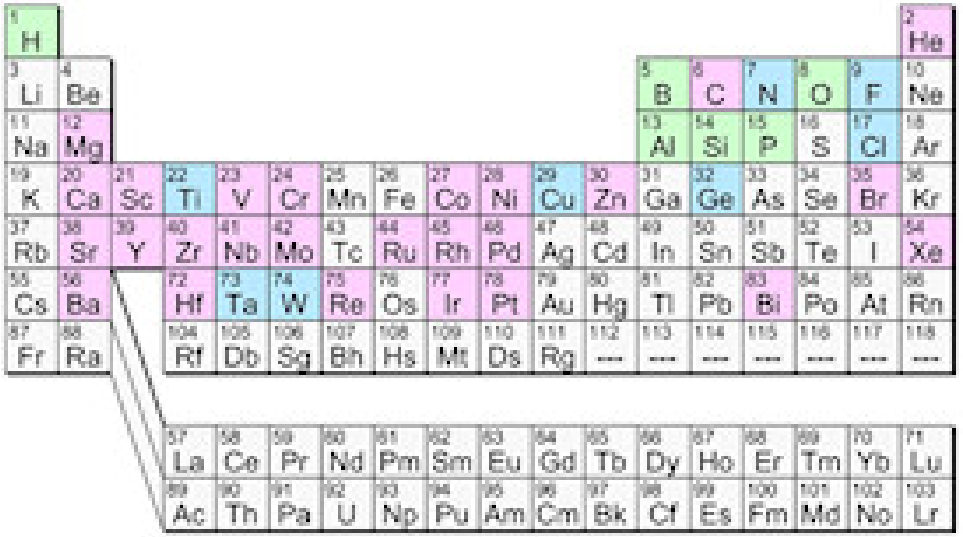


Human Being

"Silicon" Chip



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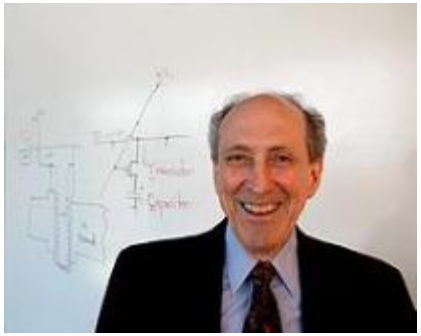
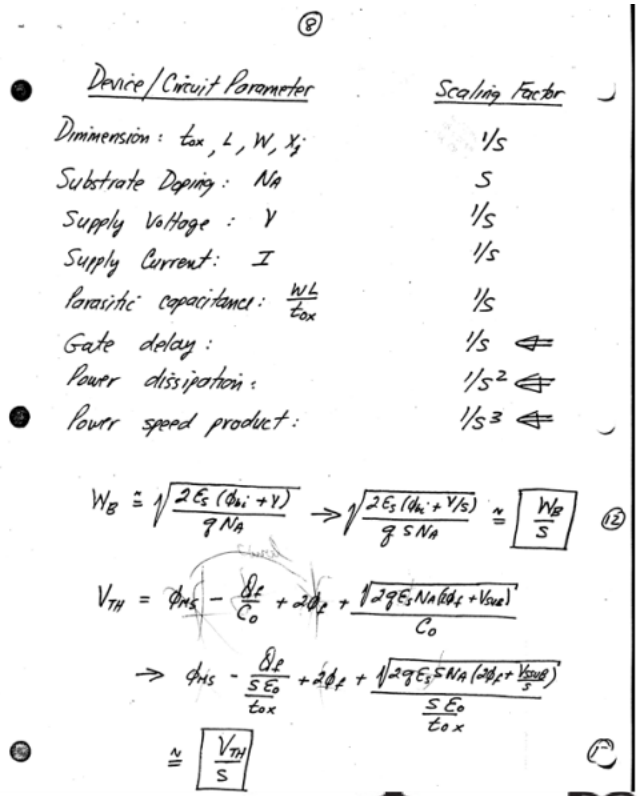
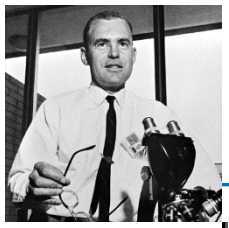
Dennard Scaling

The scaling theory of MOSFETs predicts that the speed of any chip would increase in direct proportion to the decrease in size of its transistors

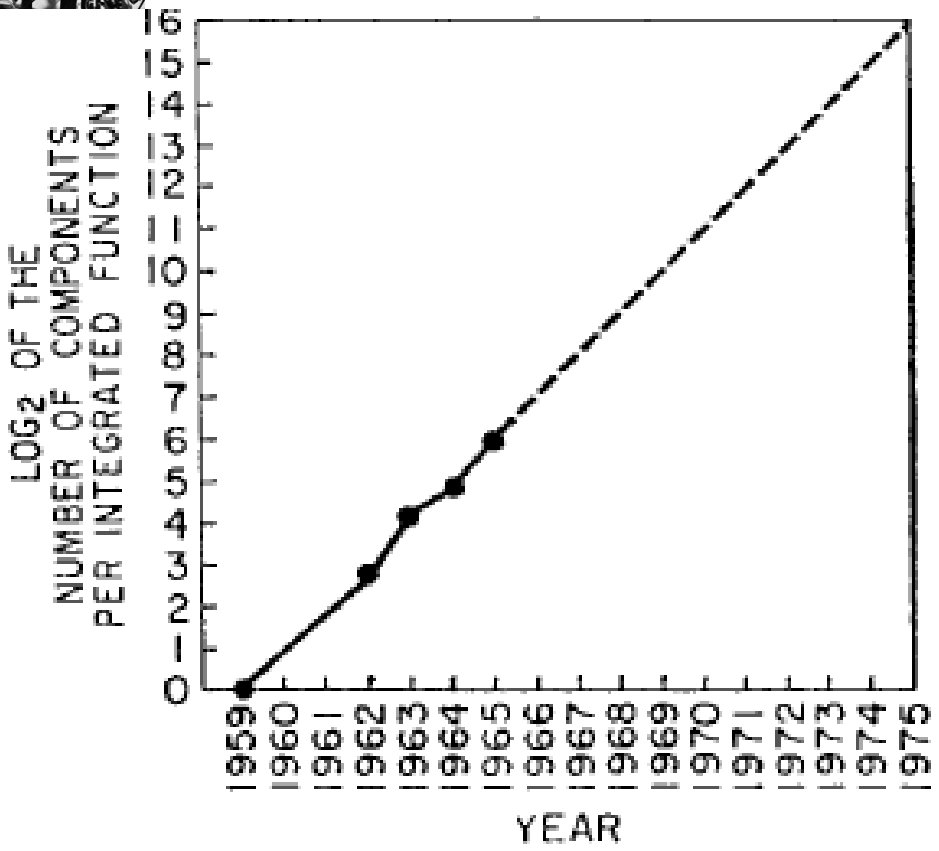


Parameter	Constant field scaling
Physical dimensions (L_{ch}, W, T_{ox})	$1/\alpha$
Power supply voltage	$1/\alpha$
Doping concentration	α
Electrical field in device	1
Gate capacitance	$1/\alpha$
Gate delay	$1/\alpha$
Power consumption	$1/\alpha^2$
Integration density	α^2
Power density	1



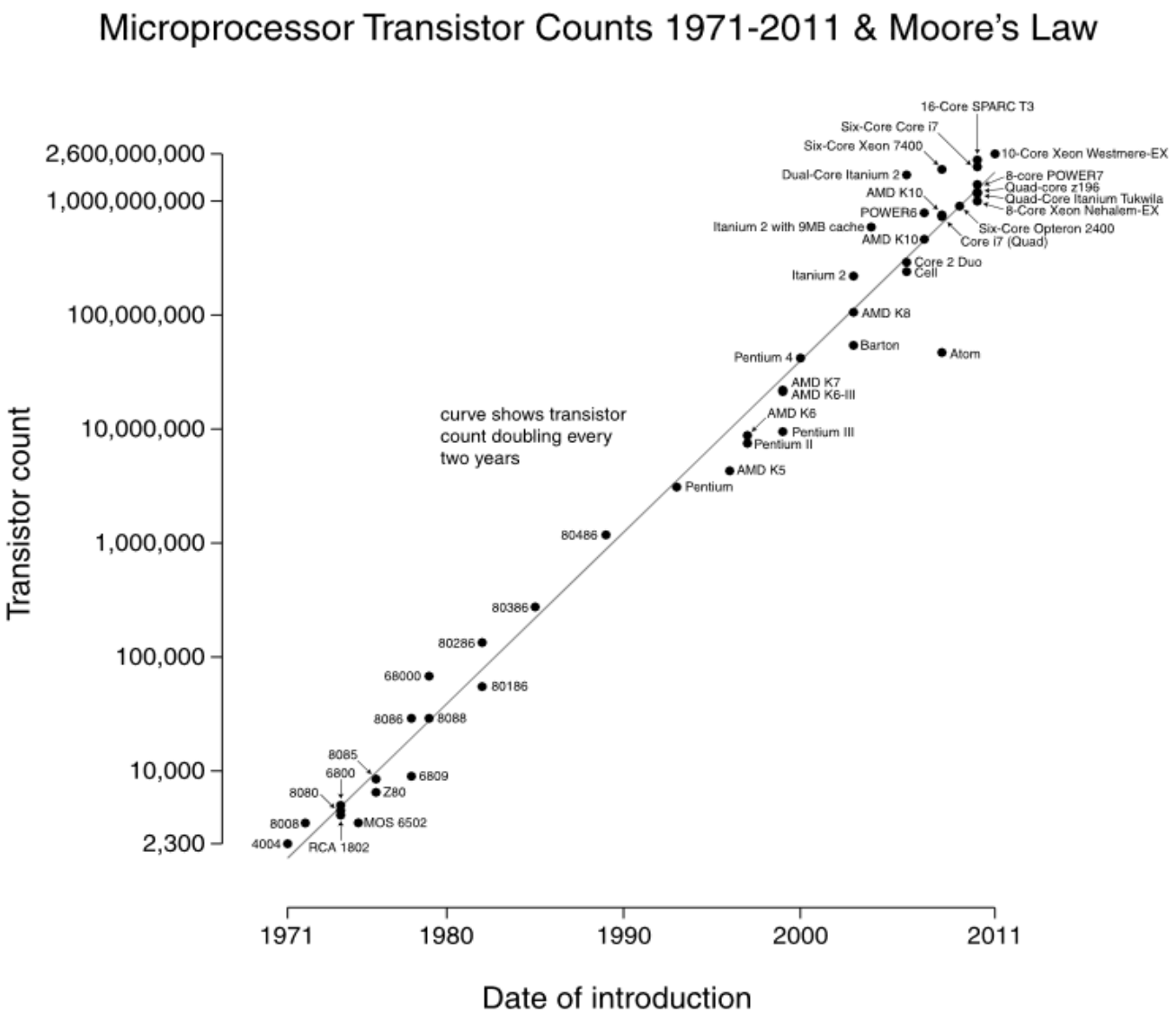


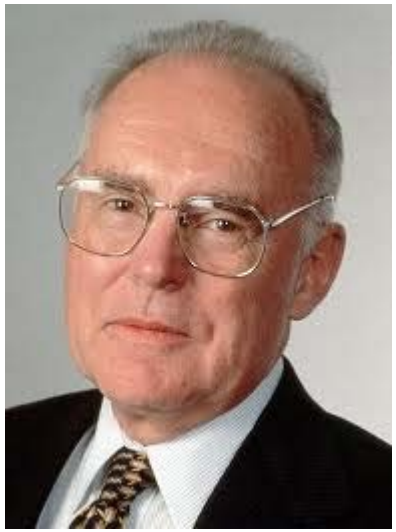
Moore's Law



- Gordon Moore, Fairchild Semiconductor's Director of R&D, wrote an internal paper in which he drew a line through five points representing the number of components per integrated circuit for minimum cost per component developed between 1959 and 1964.
- Extrapolating the trend to 1975 he projected that the number of components per chip would reach 65,000; a doubling every 12 months.
- Edited for publication as a magazine article, "Cramming more components onto integrated circuits" was published in Electronics on April 19, 1965.

Moore's Law



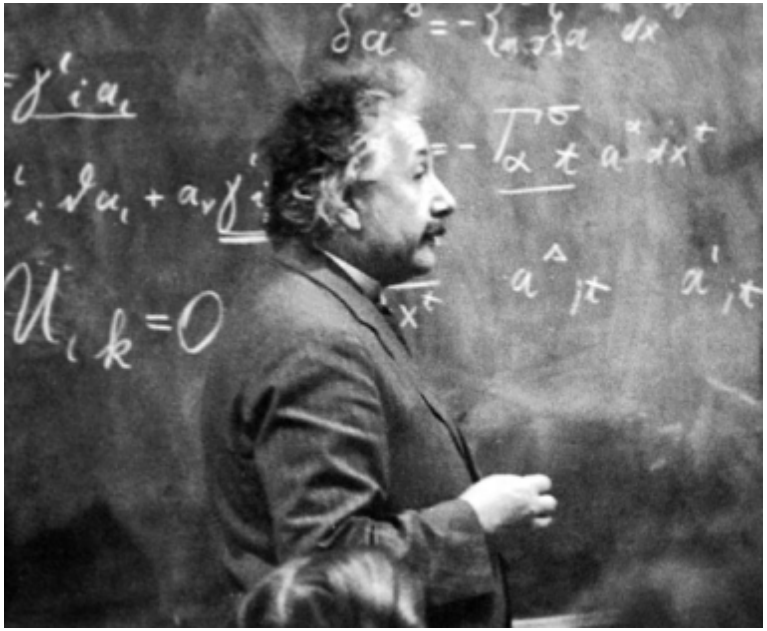


[CES 2015: Intel's Video of Moore's Law]

To Ponder

"The significant problems we face cannot be solved at the same level of thinking we were at when we created them"

- Albert Einstein



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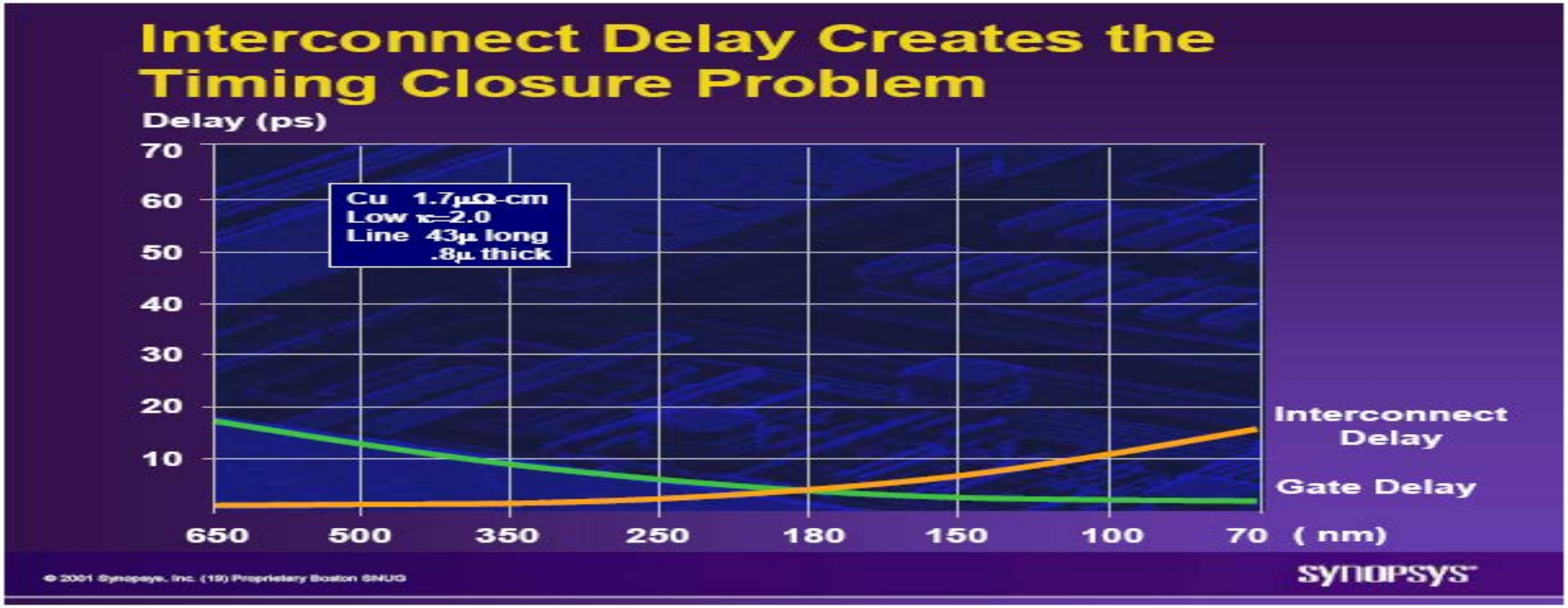
Semiconductor Industry is Facing an Inflection Point

Dimensional Scaling has reached Diminishing Returns

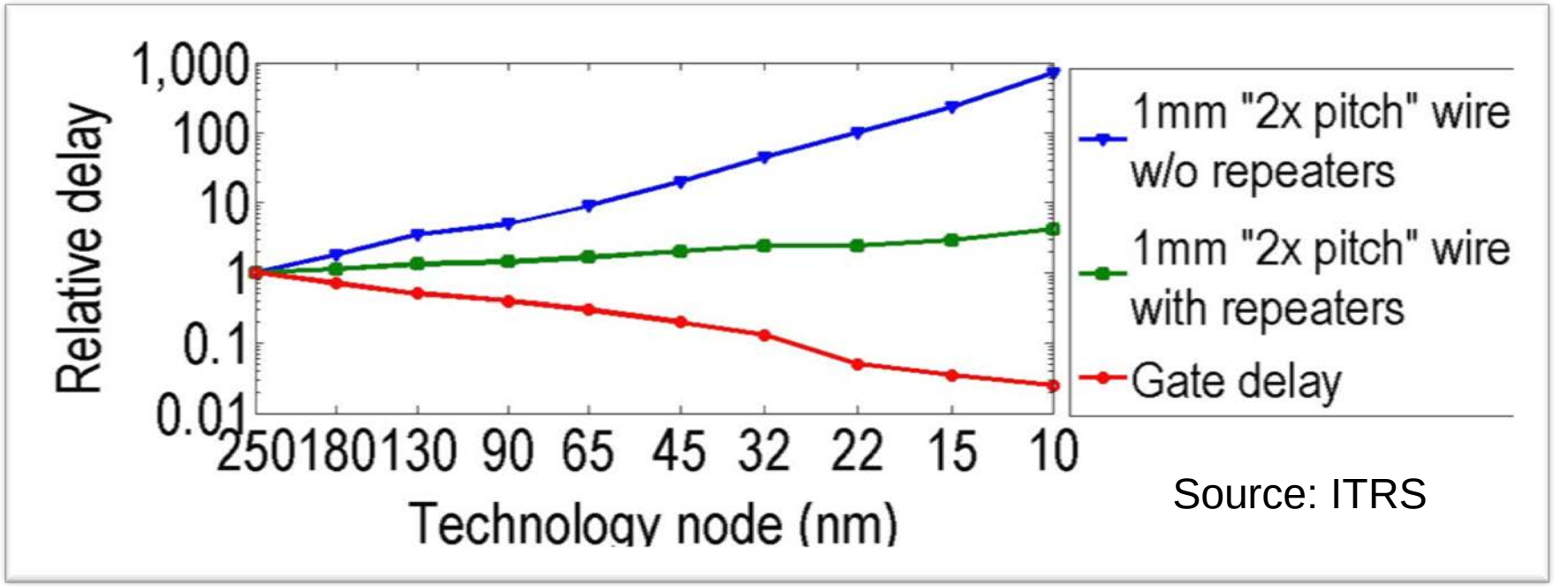
MonolithIC3D™

The Current 2D-IC is Facing Escalating Challenges - I

- On-chip interconnect is
  - Dominating device power consumption
  - Dominating device performance
  - Penalizing device size and cost



Interconnect Delay
A Big Issue with Scaling



- *Transistors improve with scaling, interconnects do not*
- *Even with repeaters, 1mm wire delay ~50x gate delay at 22nm node*

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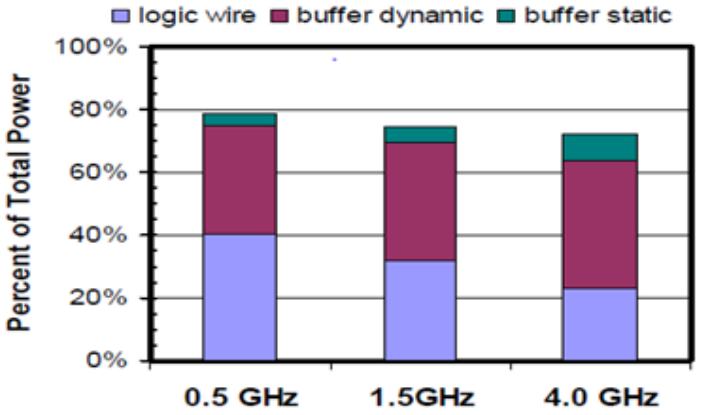
Connectivity Consumes 70-80% of Total Power @ 22nm

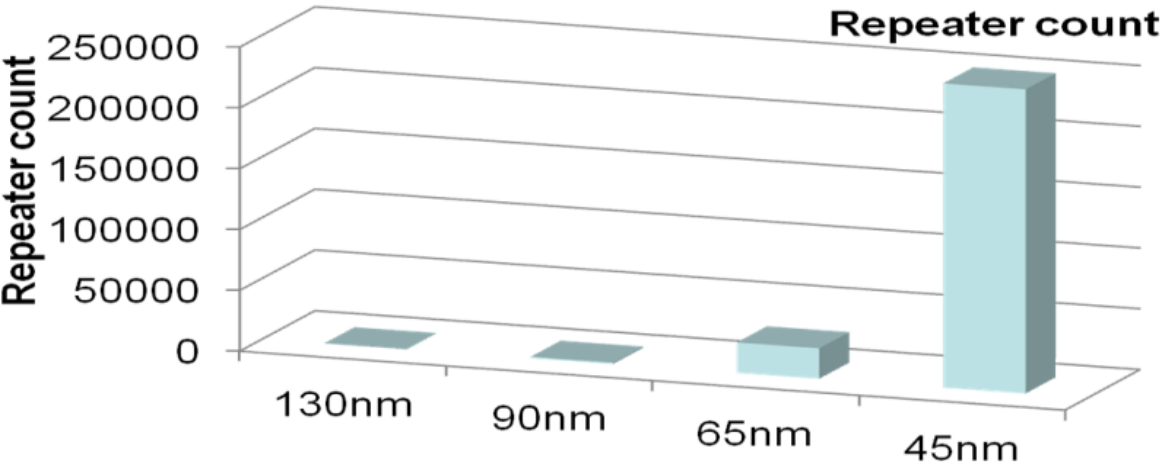
Repeaters Consume Exponentially More Power and Area



- *At 22nm, on-chip connectivity consumes 70-80% of total power*
- *Repeater count increases exponentially*
- *At 45nm, repeaters are > 50% of total leakage*

70-80% of total logic power is for communication
– **Need proper consideration of wires!!**

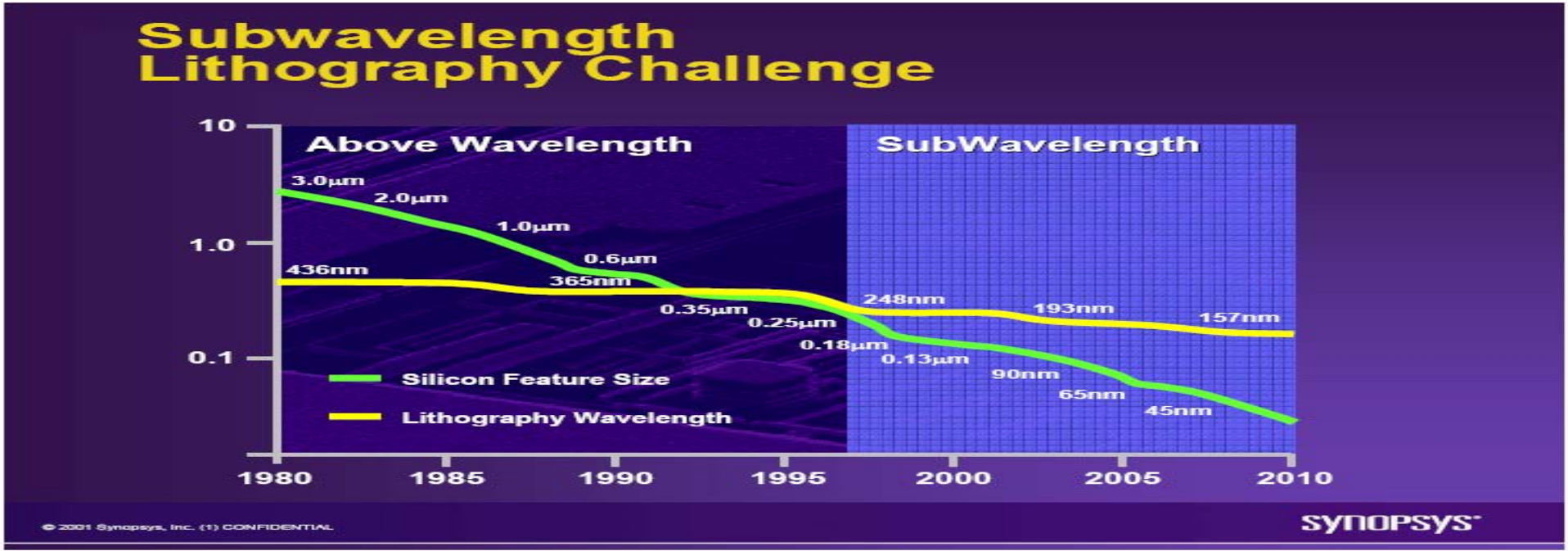
L. Chang, D. J. Frank IEDM 2012 Short Course IBM T. J. Watson Research Cent



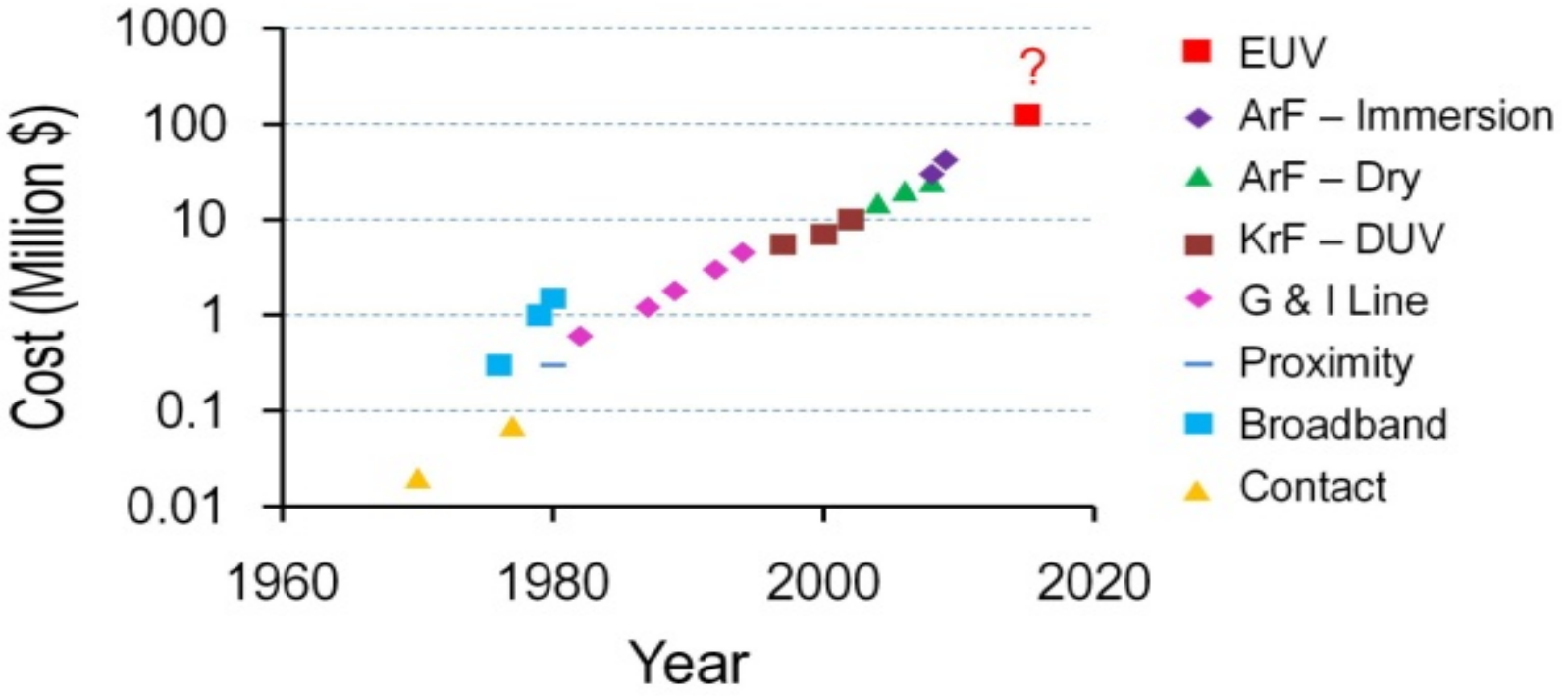
Source: IBM POWER processors
R. Puri, et al., SRC Interconnect Forum, 2006

The Current 2D-IC is Facing Escalating Challenges - II

- Lithography is
  - Dominating Fab cost
  - Dominating device cost and diminishing scaling's benefits
  - Dominating device yield
  - Dominating IC development costs



A Challenge: Lithography



- **Quad-patterning next year → costly. EUV delayed, costly.**
- ***Can we get benefits of scaling without relying on lithography?***

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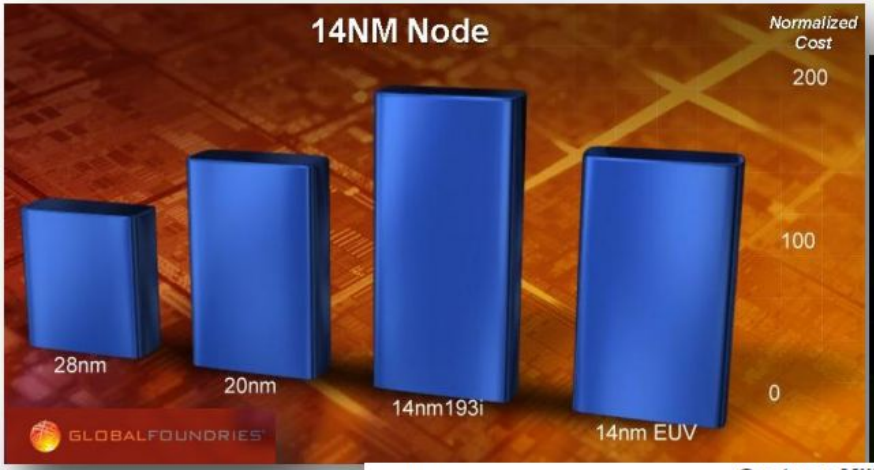
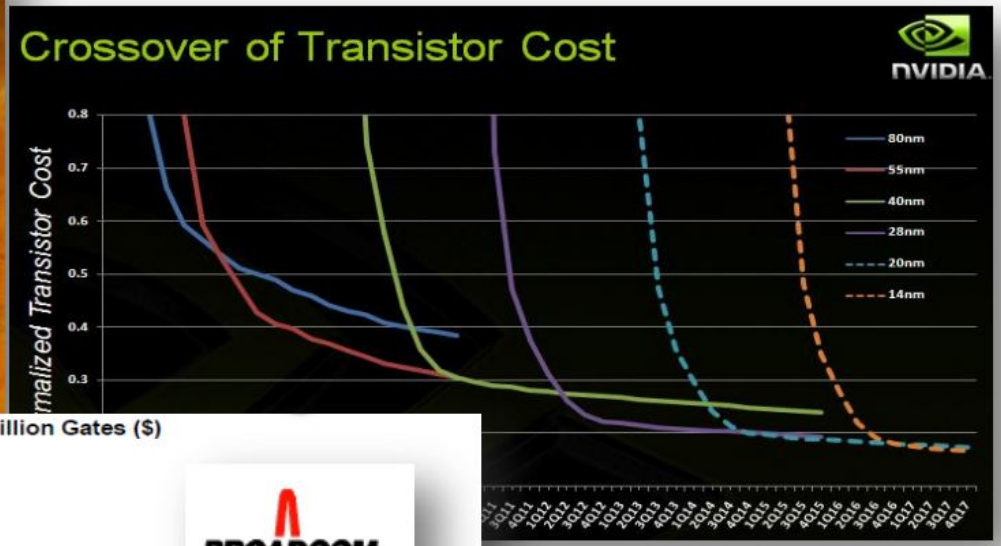
Cost per transistor is no longer scaling

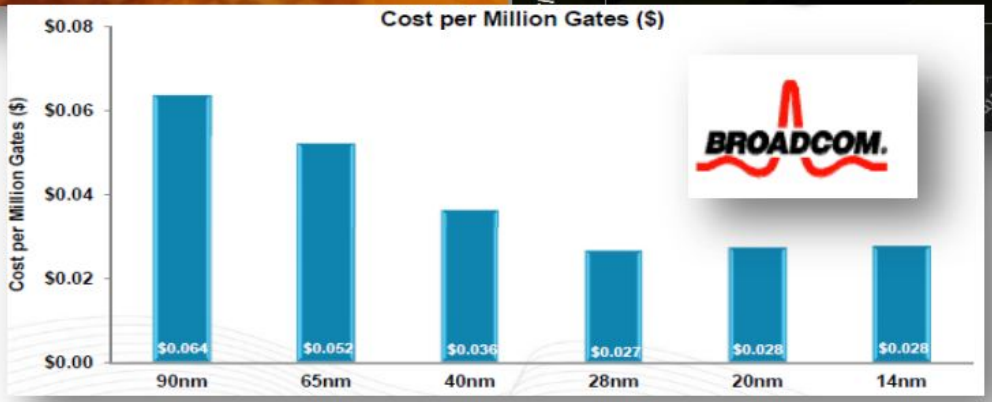
Cost becomes a concern post 28 nm

ASML

Public

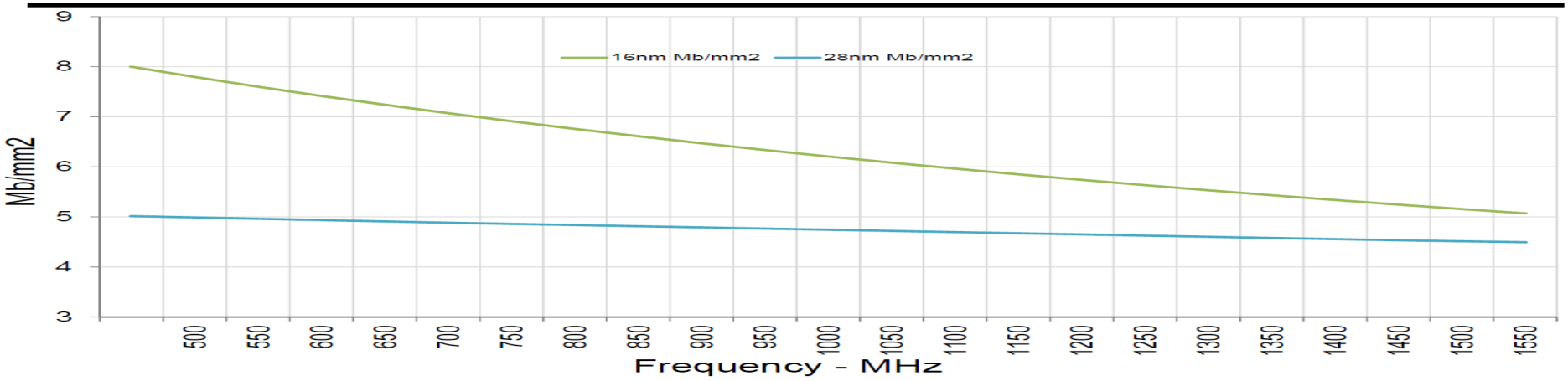






Sources: nVidea, ITPC, nov, 2011
Broadcom, IMEC, may 2012
GF, ISS, jan 2013

Embedded SRAM isn't Scaling Beyond 28nm (1.1x instead off 4x)
eSRAM > 60% of Die Area => End of Dimension Scaling?



Memory density at 1500MHz and above scales by ~1.1x or less from 28nm to 16nm

For 400G ASSP/ASIC, need to double the SRAM density

- But density improvement from process node N to N+1 is not 2x anymore but by 1.1x
- 500mm^2 die in 28nm for 200G with 60% SRAM ported to 16nm for 400G will be ~ 745mm^2
- Die size close to reticle limit - exacerbates yield & cost of lower end segments

At > 400G, embedding all the SRAM would make the die size bigger than reticle limit

Dinesh Maheshwari, CTO, Memory Products Division at Cypress Semiconductors, ISSCC2014

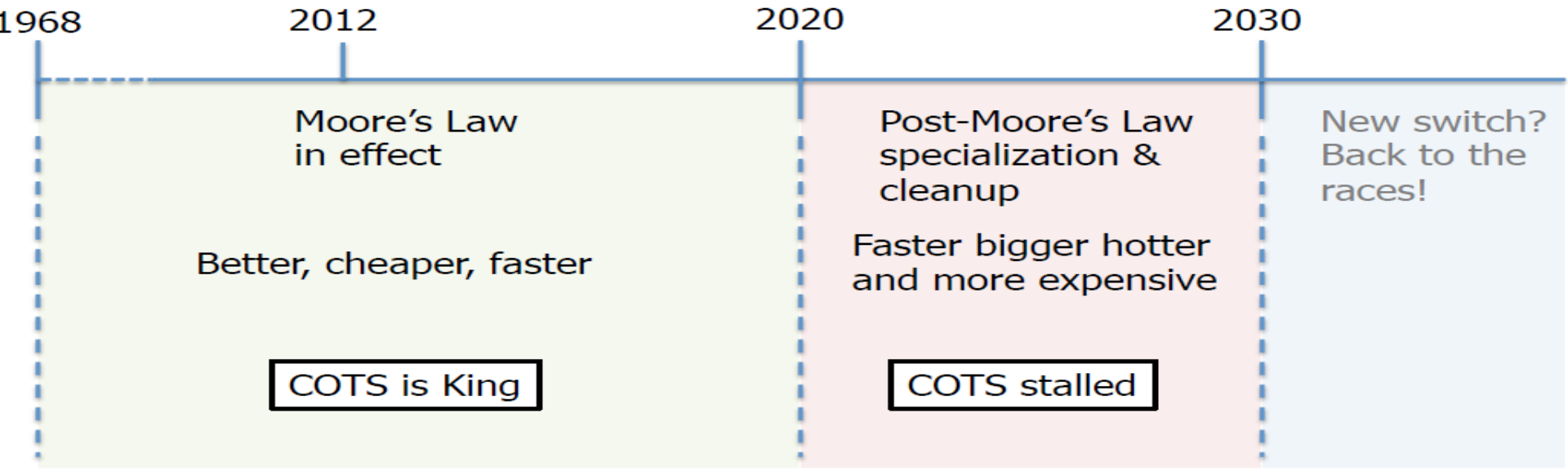
Moore's Law Dead by 2022*

Bob Colwell, Director MTO, DARPA

DARPA

My model: During and After Moore's Law

1. COTS is both problem & opportunity for DoD for next 10 years.
2. Then COTS stalls out. (But DoD doesn't have to!)



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*http://www.eetimes.com/document.asp?doc_id=1319330

*CRA/CCC & ACM SIGDA, Pittsburgh, March 2013

Conclusions:

- Dimensional Scaling (“Moore’s Law”) is already exhibiting diminishing returns
- The road map beyond 2017 (7nm) is unclear
- While the research community is working on many interesting new technologies (see below), none of them seem mature enough to replace silicon for 2019
  - Carbon nanotube
  - Graphene
  - Nanowire
  - Photonics
  - Indium gallium arsenide
  - Spintronics
  - Molecular computing
  - Quantum computing
  - ’2D’ devices: MoS2, etc
- 3D IC is considered, by many, as the near term solution, and **Monolithic 3D IC** is well positioned to be so, as it uses the existing infrastructure
  - **Monolithic 3D is the only alternative that could be ready for high volume in 2019**

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“CEA-Leti Signs Agreement with Qualcomm to Assess Sequential (monolithic)3D Technology”

Business Wire December 08, 2013

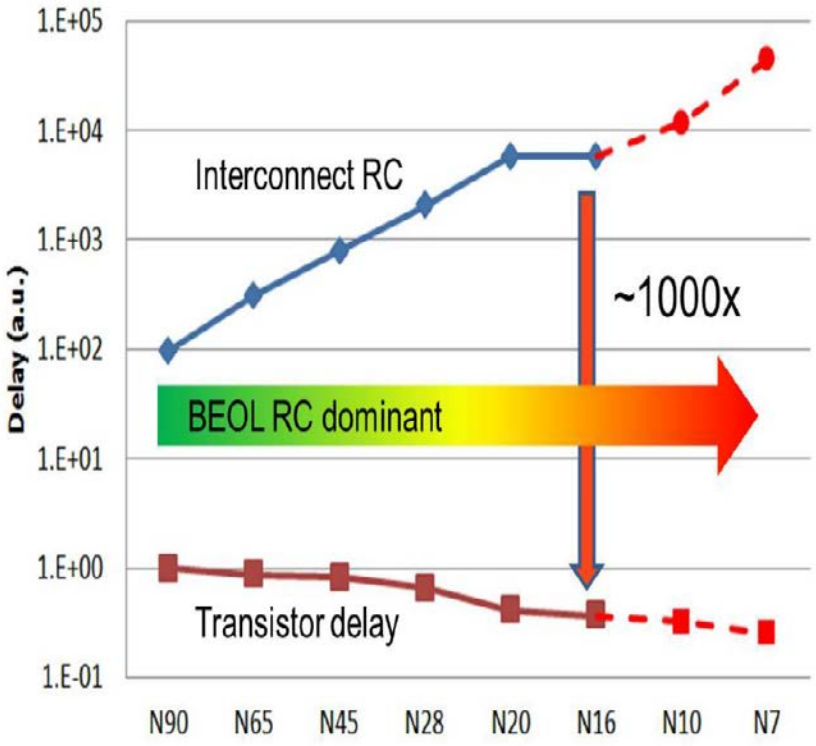

Fig. 17: BEOL performance/area/cost scaling is the foremost issue for 10nm/7nm nodes.

“Monolithic 3D (M3D) is an emerging integration technology poised to reduce the gap significantly between transistors and interconnect delays to extend the semiconductor roadmap way beyond the 2D scaling trajectory predicted by Moore’s Law.”

Geoffrey Yeap,
VP of Technology at Qualcomm,
Invited paper, IEDM 2013

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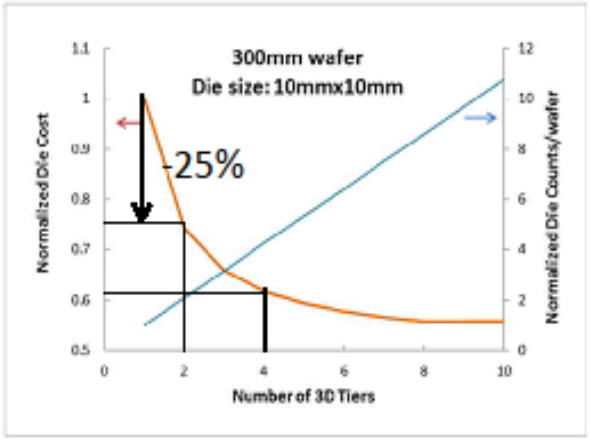
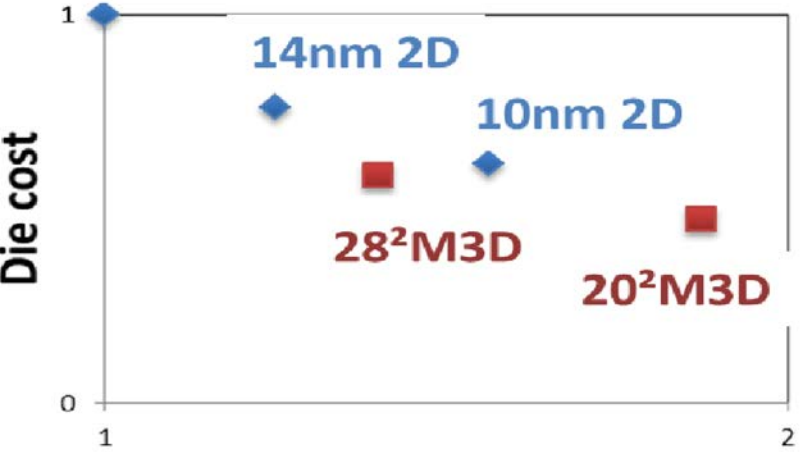
Interest for M3D

Source: G. Bartlett, Global Foundries, SMC 2013

Source: R. Gilmore, Qualcomm VP, ESSIRC 2012

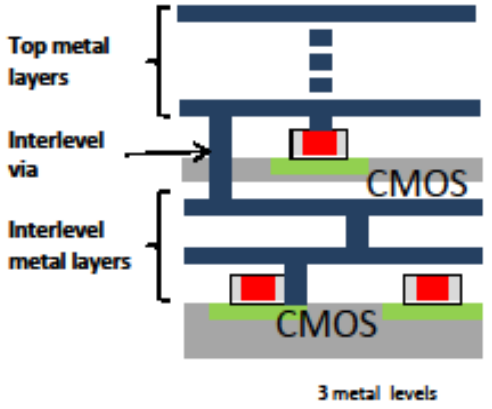


Without scaling avoid fab and process costs increase



1 node gain without scaling

Stack 2 layers: 25% die cost reduction



MONOLITHIC
10,000x the Vertical Connectivity of TSV

	TSV	Monolithic
Layer Thickness	~50µ	~50nm
Via Diameter	~5µ	~50nm
Via Pitch	~10µ	~100nm

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The Monolithic 3D Challenge
Why is it not already in wide use?

- *Processing on top of copper interconnects should not make the copper interconnect exceed 400^{o}C*
  - How to bring mono-crystallized silicon on top at less than 400^{o}C
  - How to fabricate state-of-the-art transistors on top of copper interconnect and keep the interconnect below at less than 400^{o}C

- *Misalignment of pre-processed wafer to wafer bonding step ~~is~~ was ~1µm*
  - How to achieve 100nm or better connection pitch
  - How to fabricate thin enough layer for inter-layer vias of ~50nm

MonolithIC 3D - Precision Bonder Flow

- **RCAT** *(2009)* – Process the high temperature on generic structures prior to ‘smart-cut’, and finish with cold processes – Etch & Depositions
- **Gate Replacement** *(2010)* (=Gate Last, HKMG) - Process the high temperature on repeating structures prior to ‘smart-cut’, and finish with ‘gate replacement’, cold processes – Etch & Depositions
- **Laser Annealing** *(2012)* – Use short laser pulse to locally heat and anneal the top layer while protecting the interconnection layers below from the top heat
- **Precise Bonder** (2014) – Use precision bonder and prior techniques such as ‘gate replacement’. Offers low cost flow with minimal R&D

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Skills

- Be Curious – don't leave home without it!
- Energy – science is hard work
- Collaboration

Curiosity + Energy = Passion

- Scientific Notation, the scale of things
  - *back-of-the-envelope*
- Broad knowledge and Interests
- Tolerance for and embrace ambiguity
- Practice Pareto (80/20)

More Skills

- Engineering ethics
- Statistics, process control
  - Don't get caught-up in it!
- Communication: Personal and written (papers, presentos)
- Study & practice lateral thinking, innovation
  - (bean bags+table)
- Be a Life Learner and…
  - Teach it/pass it on
- Embrace social media, to a point….

Some Resources

- Overall 3D-IC: Garrou, P., et al., *Handbook of 3D Integration: Technology and Applications of 3D Integrated Circuits*, 2008 Wiley-VCH Verlag GmbH & Co.
- www.ieee.org, Powers of Ten – Eames,
- History of SV:
  - Malone, M.S., *The Big Score: The Billion Dollar Story of Silicon Valley*, 1985 Doubleday & Company, New York.
  - Stories of SV: Malone, M.S., *The Valley of Heart's Delight: A Silicon Valley Notebook 1963-2001*, 2002 John Wiley & Sons, New York.
  - Intel's History of the Transistor
- Moore's Law
  - Gordon Moore speech on 40th Anniversary of Moore's Law
  - Gordon Moore talk on Microchip History
  - Mythbusters - Moore's Law
- The making of an integrated circuit in poetry
- Robert Dennard: Inventor of the DRAM and Transistor Scaling Laws
- More on wafer fab: Intel Chandler Wafer Fab (45nm)
- More on processing: Sand to Si to pkg Intel 2min, 10min Si processing,old, Science Channel how to make an IC
- Making an IC at home: 8min vid Jeri Ellsworth making NMOS xtor at home
- Harvard: ipod to biochips