Gullipalli Durga Siva Sai Venkata Avinash

20551a04e9.gdssvavinash@gmail.com 06301288794 Chintalapudi,Andhra Pradesh, India
GULLIPALLI DURGA SIVA SAI VENKATA AVINASH

OBJECTIVE

Dynamic M.Tech in VLSI Design fresher with a strong foundation in Digital Electronics and Verilog, along with basic knowledge of SystemVerilog and UVM methodology. Passionate about front-end design and verification, eager to apply academic knowledge, and contribute effectively to a progressive team in the semiconductor industry.

EDUCATION

Mtech, VLSI Design 08/2024 – present
Amrita Vishwa Vidyapeetham Amritapuri, Kerala, India
cgpa 7.86

Btech, ECE[Electronics and Communication Engineering] 2020 – 2024
Godavari Institute of Engineering and Technology rajamahendravaram, India
cgpa 8.12
76%-Passed in First class with Distinction

Intermediate MPC [Mathematics, Physics, and Chemistry] 2018 – 2020
Sri Chaitanya Junior College vijayawada, India
cgpa 8.57
80%-Passed in First class with Distinction

10 class 2017 – 2018
Sri Chaitanya School Chintalapudi, India
cgpa 10
95%-Passed in First class with Distinction

PROJECTS

UART
[Universal Asynchronous Receiver Transmitter]
*Designed and implemented a UART communication system using Verilog HDL.
*Verified and simulated the UART design using Questa Sim to ensure functionality.
*Developed mechanisms for Tx and Rx, Baud clock generator,parity bits and data frames and error-checking.
*Tools Used:Verilog HDL
*Simulation and Verification Tool: Questa-Sim

FPGA Implementation on SPI Data Communication Protocol
*Designed and Implemented a SPI Data Communication protocol using verilog HDL.
*Tools Used**:**Verilog HDL
*Simulation and Verification Tool: Questa-Sim
*FPGA Platform: XILINX

CERTIFICATES

Internship in Embedded Systems
(APSSDC, Online),Rajamahendravaram

VLSI-Design &Verification
(VLSI FIST, Hyderabad)

COURSES

Apprenticeship in VLSI-Design &Verification 12/2023 – 06/2024
VLSI FIRST,Hyderabad Hyderabad, India

Internship in Embedded Systems 05/2023 – 07/2023
Andhra Pradesh State Skill Development Corporation (Online) Rajamahendravaram, India

SKILLS

Technical:
Digital Electronics,HDL Verilog, System Verilog(Basic Knowledge),Familiar python(Basics)

Methodology:
Basic understanding of Universal Verification Methodology [UVM LEVEL 1]

Tools:
Questa-sim, GVIM,vivado-Xilinx, LTSpice

Protocols:
UART protocol,SPI protocol

Soft Skills:
Team Collaboration, Positive Attitude, Better Communication, Problem Solving.

FPGA implementation.

LANGUAGES

English

Telugu

Hindi

INTERESTS

Community Involvement | playing cricket | Listening to music