Basavaraj Sheelvant

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Profile

VLSI Engineer with a year of experience in the Semiconductor domain, having a strong understanding of the overall VLSI Design flow, including RTL Design, Verification and FPGA development. Currently pursuing a Master's in VLSI Design, seeking an opportunity to advance skills and contribute to innovative Chip Design projects.

Professional Experience

10/2023 – 08/2024
Bengaluru, India

FPGA Design Engineer, LRDE-DRDO[Cadmaxx Solutions Pvt Ltd]

- Designed and Impemented FPGA logic for Waveform generation module used for Radar Exiter and Receiver Module.
- Conducted RF Testing using test equipments like Spectrum Analyzers, Mixed Signal Oscilloscope, Signal Generator and JTAG for Exiter and Receiver modules to ensure accuracy and performances
- Assisted in calibration of Radar Receivers and contibuted to the Development of Radar by debugging and Integrating Radar subsystems.

05/2023 – 09/2023
Bengauru, India

Project Intern-RTL Design, Maven Silicon Softech Pvt Ltd

- Worked with Design team to provide quality mentorship to the trainees on RTL Design, Code Coverage, and Lint Checks using latest EDA Tools and mentored throughout their project and lab.

Professional Training

2022 – 2023
Bengaluru, India

Advanced VLSI Design and Verification
Maven Silicon-VLSI Training

Projects

AHB to APB Bridge IP Core Verification
Maven Silicon Softech Pvt Ltd

Crop Recommender System
Jain(Deemed-to-be University)

Router 1x3 | RTL Design, Verification and Code Coverage
Maven Silicon Softech Pvt Ltd

Education

2024 – Present
Bengaluru, India

M.Tech in VLSI Design, ASE, Amrita Vishwa Vidyapeetham
Major Subjects: Digital Systems and Circuits, Verilog HDL, Functional Verification, CMOS VLSI Design, Machine Learning
Grade: 7.0 GPA

2019 – 2022
Bengaluru, India

B.Tech in Electronics and Communication Engineering, Jain(Deemed-to-be University)
Major Subjects: ASIC Design , Embedded Systems, Fundamentals of Python
Grade: 8.4 GPA
Achievements: Awarded with 2nd Best Project in the Department of ECE for AY 2021-2022

2016 – 2019
Bengaluru, India

Diploma in Electronics, Nettur Technical Training Foundation[NTTF]
Major Subjects: Digital and Analog Electronics, C, C++, IoT
Grade: 8.9 GPA

Skills

HDL-Verilog | HVL-System Verilog | Programming Languages-C, Python | Hardware-Xilinx Kintex Ultra Scale FPGA | RTL Development | Lint Checks | Code Coverage | OS Platform-Linux, Windows

Tools

EDA Tools
Simulation Tools:
1. Questasim. 2. Synopsys VCS. 3. Modelsim. 4. Xilinx Vivado. 5. Cadence Virtuoso
Synthesis Tools:
1. Quartus Prime. 2. DC Compiler.
Linter Tool:
1. VC SpyGlass

Certifications

1. System Design Through Verilog-NPTEL, IIT-Guwahati. 2. Python-LinkedIn Learning