B JAYAKRISHNAN

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Determined and passionate aspiring VLSI Engineer with a proven track record and a strong foundation in Physical Design, Static Timing Analysis, Clock Tree Synthesis, CMOS Fundamentals, and ASIC design flows. Skilled in RTL coding, synthesis, timing analysis, and open-source EDA tools. Eager to tackle complex VLSI design challenges and continuously expand skills through hands-on experimentation and self-learning.

SKILLS

Coreskills	Verilog, Tcl Scripting, C, Python, ARM Assembly
Tools/Platforms	Modelsim RTL Simulator, Xilinx Vivado, Static Timing Analysis, Clock Tree Synthesis, VLSI Design Flow, Yosys Synthesis Tool, OpenSTA, ISE Design Suite, Questasim, Cadence Virtuoso, Bambu HLS, Xilinx Vitis HLS, LTSpice, Keil, Spartan 6, Basys3, Lattice ICEStick
Softskills	Communication, Problem Solving, Teamwork, Leadership, Time Management, Adaptability, Mentoring

PROJECTS

Implementation of RISC V Processor on FPGA
Designed and implemented a custom RISC-V processor on Spartan 6 FPGA using Verilog, gaining a deep understanding of the RISC-V ISA and optimizing performance for efficient hardware acceleration.

FPGA-Based custom ANN Implementation for Vision Applications
Designed a Artificial Neural Network (ANN) for digit recognition using the MNIST dataset on Xilinx FPGA. Created custom neuron modules in Verilog and optimized the network for hardware deployment. Delivered a resource-efficient, high-performance solution for vision applications.

Machine Learning Assisted Check-In System
Collaborated on developing a real-time device detection system for examination halls. Integrated the model on Raspberry Pi and delivered a custom dataset of 1300+ annotated images, publicly shared on Roboflow.

UAV Hunting Drone
Prototyped an autonomous drone system for detecting unauthorized UAVs, utilizing MobileNet SSD for object detection and a Python-based tracking algorithm. Deployed the solution on Raspberry Pi and Pixhawk streamlined for real-time airspace security operations.

KNN Implementation on FPGA
Implemented a hardware-accelerated k-Nearest Neighbors (KNN) algorithm on Basys3 FPGA, optimizing performance, area, and power. Integrated KNN for real-time classification in machine learning applications.

Design and Simulation of APLL Using LTSpice
Designed and simulated an Analog Phase-Locked Loop(APLL) in LTSpice (45nm), using a multiplier-based phase detector, low-pass filter, and VCO with inverters. Analyzed its role in precise frequency control and signal synchronization.

EDUCATION

Amrita School of Engineering, Amritapuri	*MTech in VLSI Design*	CGPA : **9.67** / 10	2026
Government Engineering College Wayanad	*BTech in Electronics and Communications*	CGPA : **8.48** / 10	2024
Government Engineering College Wayanad	*BTech (Minor) in Computer Science and Engineering*		2024
Clemis School, Chingavanam, Kottayam	*Class XII, CBSE (Computer Science Stream)*	**92.2%**	2020

SELF-INITIATED LEARNING

NPTEL 12 week Online Course by IIIT Delhi	**VLSI Design Flow: RTL to GDS**
NPTEL 12 week Online Course by IIT Guwahati	**C-Based VLSI Design**
NPTEL 12 week Online Course by IIT Hyderabad:	**Deep Learning for Computer Vision**

STUDENT CLUBS AND ACTIVITIES

G-Bot Robotics Club, *Chief Technical Officer* Feb 2023 - Feb 2024

- Co-founded the club, growing membership by 350% and increasing financial standing by 90%.
- Led outreach activities to engage rural school students and organized 15 events.

ISTE, *Technical Head* Sept 2022 - Sept 2023

- Led team to win Best Emerging ISTE Chapter Award 2023.

IEEE, *Executive Member* Jan 2022 - Feb 2024

- Contributed to Best IEEE Chapter wins (Malabar Section 2023, Kerala Section 2022).