VLSI DESIGN (ECE 6346)

Project Report

Design of Energy economized transistor logic (EEPL) multiplexer and Differential Cascode Voltage Switch logic with Pass gate (DCVSPG) multiplexer.

D flip-flop designed by connecting to LEAP multiplexer and EEPL multiplexer.

Project by

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INDEX

Contents

1. Project Aim
2.Introduction
2.1. Multiplexer (MUX)
2.2. D flip-flop

3. Introduction to Energy economized transistor logic (EEPL) MUX and Differential Cascode Voltage Switch logic with Pass gate (DCVSPG) MUX. -----
3.1Energy economized transistor logic (EEPL) MUX
3.2. Differential Cascode Voltage Switch logic with Pass gate (DCVSPG) MUX

4. Introduction to D flip flop designing by connecting to LEAP mux and EEPL mux.

5. Steps involve in designing schematic circuit and simulation using cadence:

6. Design, schematic, simulation, and results for EEPL mux.
6.1. Design of Energy economized transistor logic (EEPL).
6.2. Schematic circuit of energy economized transistor logic (EEPL) mux using cadence.
6.3. Area of the EEPL mux.
6.4. Results.

7. Design, schematic, simulation, and results for Differential Cascode Voltage Switch logic with Pass gate (DCVSPG) MUX.

7.1. Design of Differential Cascode Voltage Switch logic with Pass gate (DCVSPG) MUX.

7.2. Schematic circuit of Differential Cascode Voltage Switch logic with Pass gate (DCVSPG) MUX using cadence.

7.3. Area of the DCVSPG mux

7.4. Results

8. D flip flop design

8.1. D flip flop by connecting LEAP mux and EEPL mux.

8.2. Schematic, simulation, and results for D flip flop using LEAP and EEPL.

8.3. Area of the above D flip flop.

8.4. Results

1.Project Aim

1. Design of energy economized transistor logic (EEPL) MUX and differential cascade voltage switch logic with pass gate (DCVSPG) MUX using cadence simulating tool and simulating that design works as a MUX.
2. Design of D flip-flop using LEAP and EEPL MUX runs at atleast 1.5 GHz Clk with Full swing from Vlow = 0V, Vhigh = 1.8V, at output using Cadence simulating tool.

2. Introduction.

Electronic gadgets have become an essential component of daily living in the modern world. They're utilized for everything from communication to entertainment to medical science. In such a case, the design and development of an efficient multiplexer (MUX) is essential for the proper operation of various electronic systems. Recognizing this expanding demand, energy economized transistor logic (EEPL) MUX and differential cascade voltage switch logic with pass gate (DCVSPG) MUX, created a high-quality MUX with enhanced functionality fit for modern-day applications.

2.1. Multiplexer (MUX):

A Multiplexer (MUX) is a digital circuit that selects one of numerous input signals and transmits it on a single output line depending on a select input. Any number of inputs can be used in a multiplexer, but the most frequent are two-to-one, four-to-one, and eight-to-one. A two-to-one multiplexer, for example, has two input lines and one output line. It is frequently used in digital circuits for data selection, signal routing, clock selection, address decoding, and other purposes

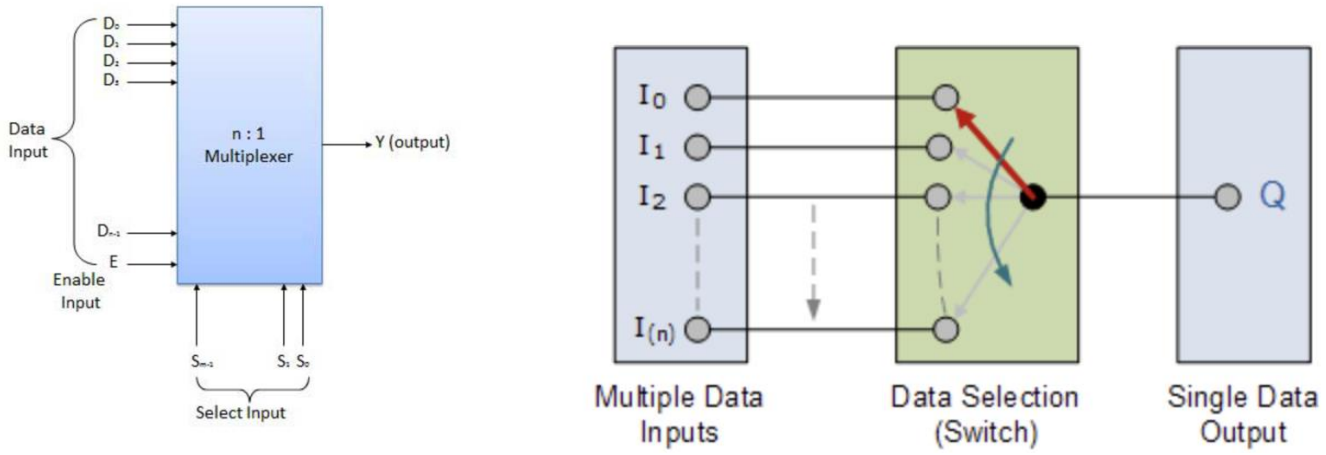

Fig-1

2.2. D flip-flop:

A D flip-flop is also a type of digital circuit that stores a single bit of data. It is referred to as a "flip-flop" because it has two stable states that may be "flipped" between. The "D" in D flip-flop stands for "data," and it refers to the input that is used to set the state of the flip-flop. The basic working of D flip-flop is when the clock signal is high, the current state of the flip-flop is retained; when the clock signal is low, the input data (D) is sampled and stored as the new state of the flip-flop. The flip-flop output is the stored state and its counterpart. D flip-flops can be constructed using various types of logic gates, such as AND gates, NOR gates, and

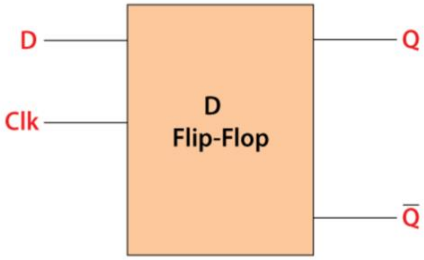

Fig-2

NAND gates. They can also be constructed using multiplexers (MUXes) and inverters.

3. Introduction to Energy economized transistor logic (EEPL) MUX and Differential Cascode Voltage Switch logic with Pass gate (DCVSPG) MUX.

EEPL MUX (Energy economized transistor logic**)** and DCVSPG MUX (Differential Cascode Voltage Switch logic with Pass gate) are two circuit designs that are used to construct low-power, high-speed multiplexers. To reduce power consumption while maintaining high-speed operation, EEPL MUX employs pass-transistors logic and inverters. The DCVSPG MUX circuit employs differential cascode voltage switch logic with pass gates to improve power consumption by reducing the number of transistors utilized. Both circuit designs are appropriate for battery-powered gadgets and applications with limited power consumption. These circuit designs can considerably reduce power consumption, hence prolonging device battery life and lowering power usage in other applications.

3.1. Energy economized transistor logic (EEPL) MUX

Energy economized transistor logic (EEPL) is a form of digital logic circuit designed to allow high-speed operation while consuming little power. It's technique for digital circuits reduces power consumption. This is done by lowering the number of transistors in the circuit while maintaining functionality. Pass transistors and inverters are used in EEPL logic gates to minimize the number of transistors in the circuit. A pass transistor is a kind of transistor that acts as a switch, allowing or preventing current flow based on the voltage applied to its gate.

MUXs are digital circuits that choose one of numerous input signals and route it to a single output line. Here we build an EEPL MUX using a pass transistor and an inverter. Traditional MUX circuits use more power than the EEPL MUX circuit, which uses a pass transistor and an inverter. This is because it uses fewer transistors and only activates the pass transistor when necessary, resulting in a reduced total power consumption.

It has been utilized in the design of numerous digital circuits, including multiplexers, adders, and registers, flip flops and has been found to lower power consumption while maintaining high performance.

Overall, the EEPL MUX is a useful and efficient circuit design for low-power and high-speed applications. Its low power consumption and quick speed make it a good potential for some applications, particularly those that are battery-powered or have power limits.

3.2. Differential Cascode Voltage Switch logic with Pass gate (DCVSPG) MUX

The Differential Cascode Voltage Switch logic with a pass gate (DCVSPG) achieves high-speed and low-power operation by combining differential cascode voltage switch (DCVS) and pass gate logic approaches. The DCVS approach uses a differential amplifier to detect the input signals, allowing for high-speed operation while reducing the effects of noise and interference. The pass gate logic approach uses pass transistors to regulate the flow of data through the circuit, which minimizes the circuit's power usage. The input signals are applied to the gates of pass transistors in the DCVSPG MUX, which govern the flow of data through the circuit.

The DCVSPG MUX may operate at high speeds while consuming little power, making it a desirable choice for a wide range of digital applications. It is also an adjustable circuit that may be utilized in a

variety of configurations, including differential and single-ended modes, and is easily adaptable to other input/output combinations.

In overall, the DCVSPG MUX is a strong digital circuit that combines the benefits of DCVS and pass gate logic approaches to deliver high-speed and low-power operation. It is commonly used in digital systems where low power consumption and rapid data transfer are essential design concerns.

4. Introduction to D flip flop designing by connecting to LEAP mux and EEPL mux.

A D- flip flop is a basic sequential logic circuit that is widely used in digital circuits. It is often used in applications such as register banks, counters, and state machines to store one bit of data. A D flip flop has two inputs: one for data and one for the clock signal (CLK). It also has two outputs: the Q output, which represents the stored value, and the Q' output, which represents the complement of the stored value. To create a D flip flop using a LEAP mux and an EEPL mux, we may begin by utilizing the LEAP mux as a selector to choose between the input data D and the current state of the flip flop Q. The LEAP mux accepts as inputs the data input D and the current state of the flip flop Q, and chooses one of these inputs based on the value of the select signal S.

The output is then transferred to the EEPL mux after the LEAP mux has picked the data input or the current state of the flip flop. The EEPL mux functions as the flip flop, conducting the logic processes required to store the specified input data in the flip flop. The EEPL mux is made up of four pass transistors and an inverter, allowing for more efficient transistor utilization and lower power consumption as compared to typical flip flop systems.

The combination of LEAP mux and EEPL mux provides for an efficient and low-power D flip flop implementation, making it a common choice in many digital circuits.

5. Steps involve in designing schematic circuit and simulation using cadence:

i. **Create a new project**: Begin a new project in Cadence Virtuoso. Configure project parameters such as the project name, location, and simulation settings.

ii. **Create a new schematic cell:** Create a new schematic cell in the project hierarchy and name it after your mux. You will create your mux circuit here.

iii. **Add components:** Add the necessary components to your schematic cell. For an EEPL and DCVSPG mux, we will need transistors, pulse votlage, and voltage sources. Make sure to choose EEPL and DCVSPG components to minimize the number of transistors used.

iv. **Connect the components**: Connect the components together using wires. Place the components in a logical way to make the schematic clear and easy to understand.

v. **Add labels:** To make the schematic simpler to read, label the components, such as input and output signal names.

vi. **Create a symbol**: Make a schematic cell for a mux. This symbol will represent the mux circuit in other schematics or layouts.

vii. **Save the schematic:** Save your mux schematic cell in your project.

viii. **Create a testbench**: Create a testbench to test your mux circuit. The testbench will include voltage sources, input signals, and output signals.

ix. **Simulate the circuit:** mux circuit will be simulated on the test bench. Run a transient simulation to explore how the mux functions over time in the Cadence simulator.

x. **Analyze the results:** Analyzing the simulation data will show whether the mux is functioning properly. Make that the output signal's waveform matches the expected output signal by inspecting it.

6. Design, schematic, simulation, and results for EEPL mux:

6.1. Design of Energy economized transistor logic (EEPL).

Designing an Energy Economized Transistor Logic (EEPL) entails several processes, including:

- **Identify the logic function**: The first step in building an EEPL circuit is determining which logic function must be implemented.
- **Determine the input and output signals**: After identifying the logic function, the input and output signals must be determined. These signals will be utilized to define the behavior of the circuit.
- **Design the pass transistor network**: The pass transistor network is the core of the EEPL circuit. It is made up of a sequence of transistors that regulate the flow of current between the input and output signals. The number of transistors utilized in the pass transistor network is determined by the complexity of the logic function being implemented.
- **Design the inverter**: The inverter is used for enhancing the output signal of the pass transistor network.

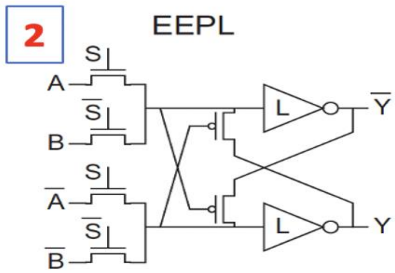

Fig-3

- **Connect the pass transistor network and the inverter**: After designing the pass transistor network and the inverter in cadence tool, they must be linked to form the entire EEPL circuit as shown. The input signals are routed through the pass transistor network, while the output signals are routed through the inverter.

6.2. Schematic circuit of energy economized transistor logic (EEPL) mux using cadence.

Energy economized transistor logic (EEPL) is a type of digital logic circuit that reduces transistor switching activity to save power consumption. This is done by employing techniques like as precharging and reusing charge on internal nodes.

Below is the schematic circuit of energy economized transistor logic (EEPL) mux using cadence where date inputs are A, B and select input is S and outputs are Y and Y'. Depend on the Select input S, signal A or signal B passes to output.

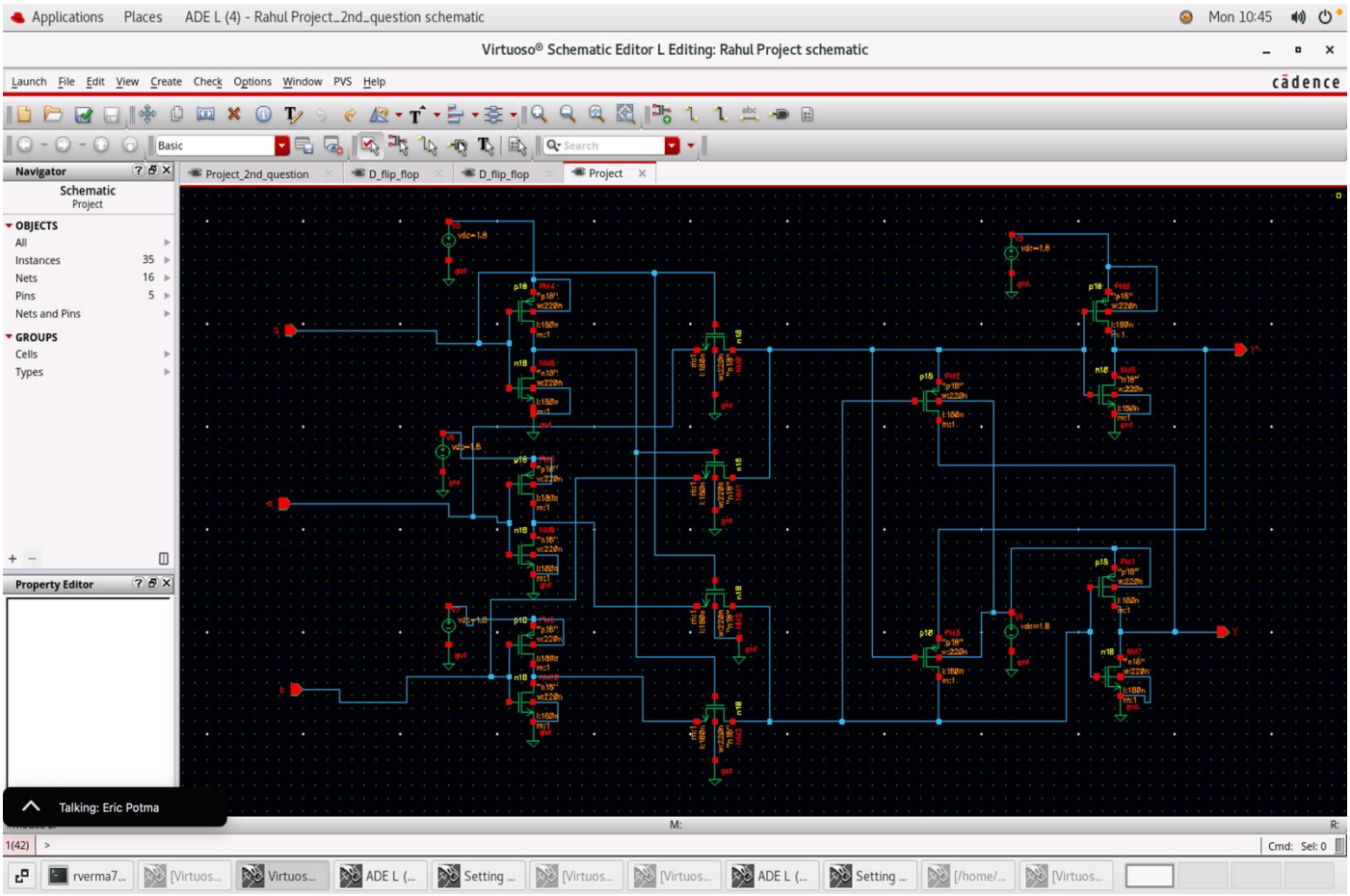

Fig-4

Now, below schematic is the symbol of EEPL mux where all the component of fig-4 enclosed. Here we connect the input VPULSES to data input A and B and to select input S.

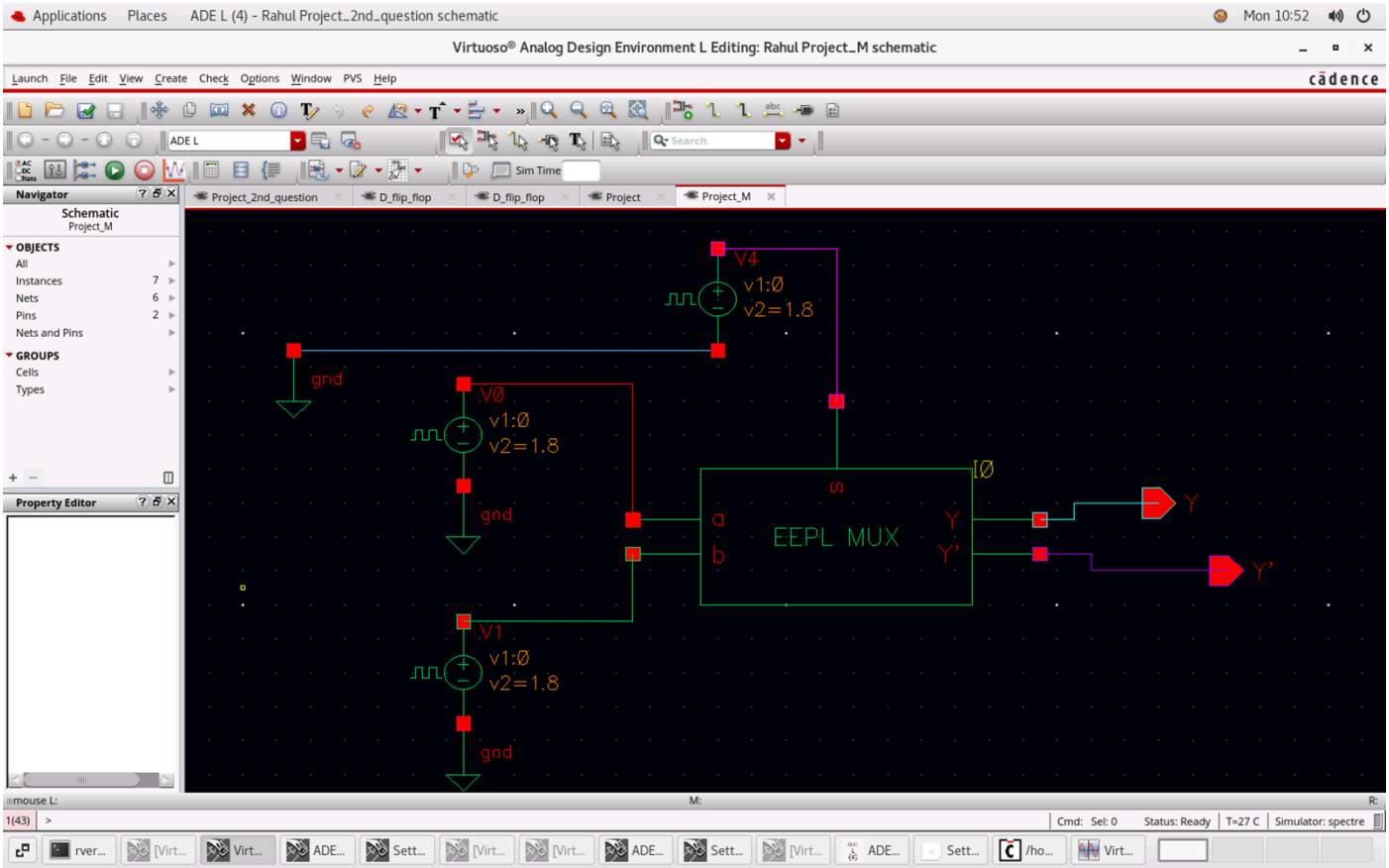

Fig-5

Now in this case there are two data inputs (A and B) and one select input (S). When S is zero, input B is sent to the output Y and Y invert to Y'; when S is one, input A is sent to the output Y and Y invert to Y'. Depending on the value of the select input S, the output waveform will be a duplicate of either input A or input B.

Output waveform:

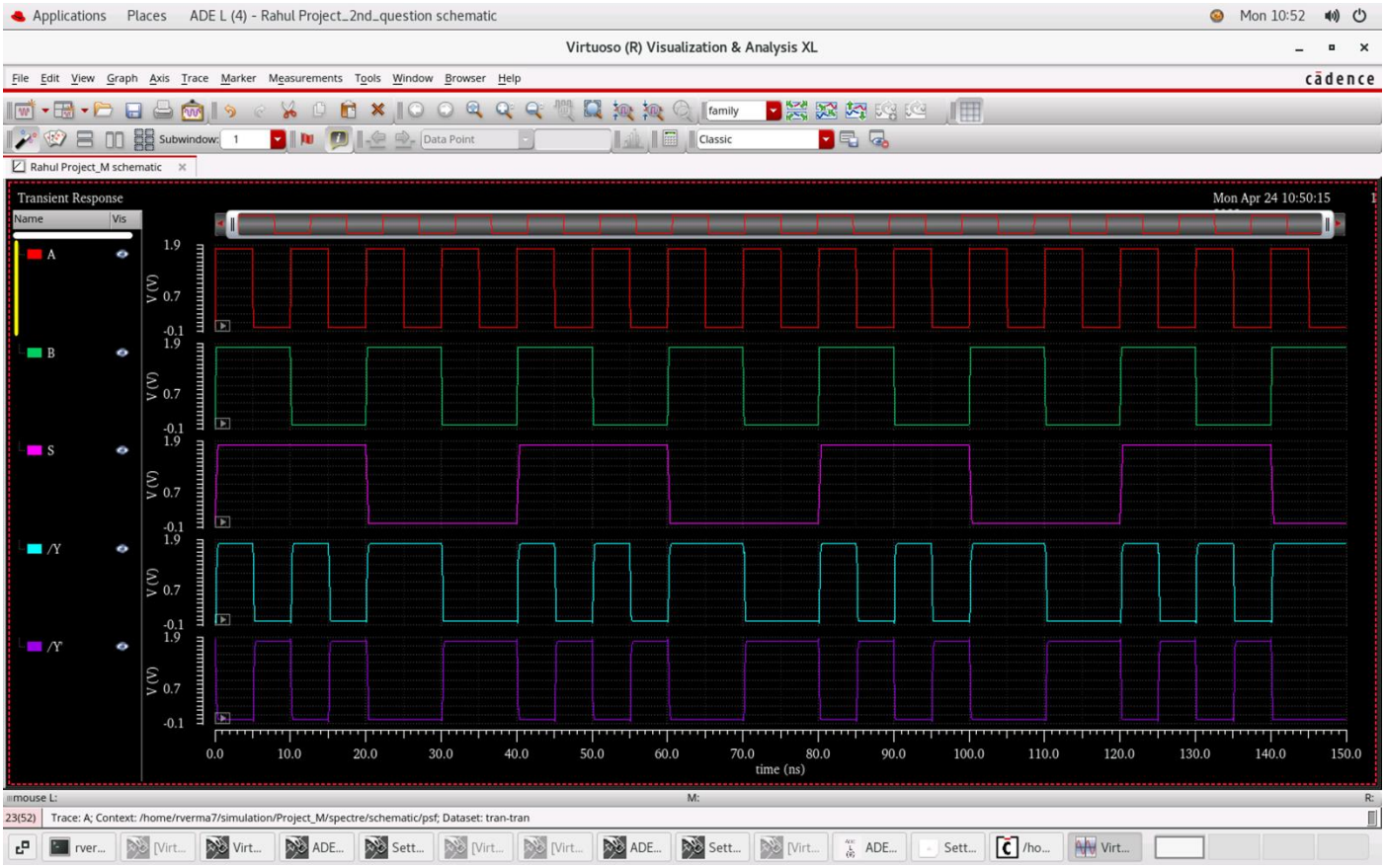

Fig-6

6.3. Area of the EEPL mux:

Area=Length x width of the transistor.
Total Area=Length x Width of the transistor x Number of transistor.

Length= 180n m
Width= 220n m
Number of transistors = 16
Area = 180 x 220 x16 = 633600

6.4. Results:

Therefore, in conclusion we can say above schematic works as a EEPL multiplexer that is when select input S is high, input A passes to output Y and inverts to Y' and input S is low, input B passes to output Y and inverts to Y'.

7. Design, schematic, simulation, and results for Differential Cascode Voltage Switch logic with Pass gate (DCVSPG) MUX.

7.1. Design of Differential Cascode Voltage Switch logic with Pass gate (DCVSPG) MUX.

Designing a Differential Cascode Voltage Switch logic with Pass gate (DCVSPG) entails several processes, including:

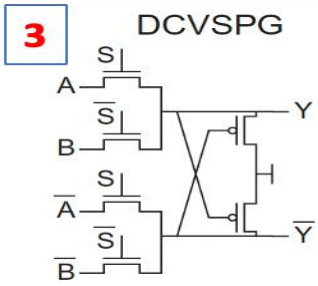

Fig-7

- **Determine the circuit's requirements:** First and foremost, we have to evaluate the number of inputs and outputs necessary for the circuit and their voltage levels.
- **Design the basic DCVSL logic gate:** To design the basic DCVSL logic gate, we begin by designing the NMOS and PMOS transistors that will be used in the circuit. The NMOS transistor is commonly used as a switch to link or disconnect the output from the input. When the NMOS is turned off, the PMOS transistor acts as a pull-up switch, keeping the output at a high level. The transistors are then coupled in differential pair mode, which provides excellent noise immunity. A cascode transistor is attached to the differential pair to improve the circuit's gain and speed.
- **Add pass gates to the circuit:** Now we have to connect NMOS pass transistors to the circuit's input and circuit's output is connected to PMOS pass transistors. Hence in this way, pass gates are connected to the circuit.
- **Design the differential cascode voltage switch logic with pass gate (DCVSPG):** Connect two DCVSL gates in parallel to produce the differential pair. Then this differential pair is connected with a cascode transistor and the output of the cascode transistor is connected to the pass gates.
- **Verify the design:** Simulate the design and make any necessary changes to design to improve the performance.

7.2. Schematic circuit of Differential Cascode Voltage Switch logic with Pass gate (DCVSPG) MUX using cadence.

DCVSPG Mux is a multiplexer circuit that uses DCVSPG logic to choose one of numerous input signals and output it on a single line. Input buffers, pass gates, and a DCVSPG logic gate are all components of it. The pass gates control transmission to the DCVSPG logic gate, which selects and outputs one of the input signals. The DCVSPG Mux is well-known in digital systems for its fast-speed operation, low power consumption, and strong noise immunity.

Below is the schematic circuit of Cascode Voltage Switch logic with Pass gate (DCVSPG) MUX using cadence where date inputs are A, B and select input is S and outputs are Y and Y'. Depend on the Select input S, signal A or signal B passes to output.

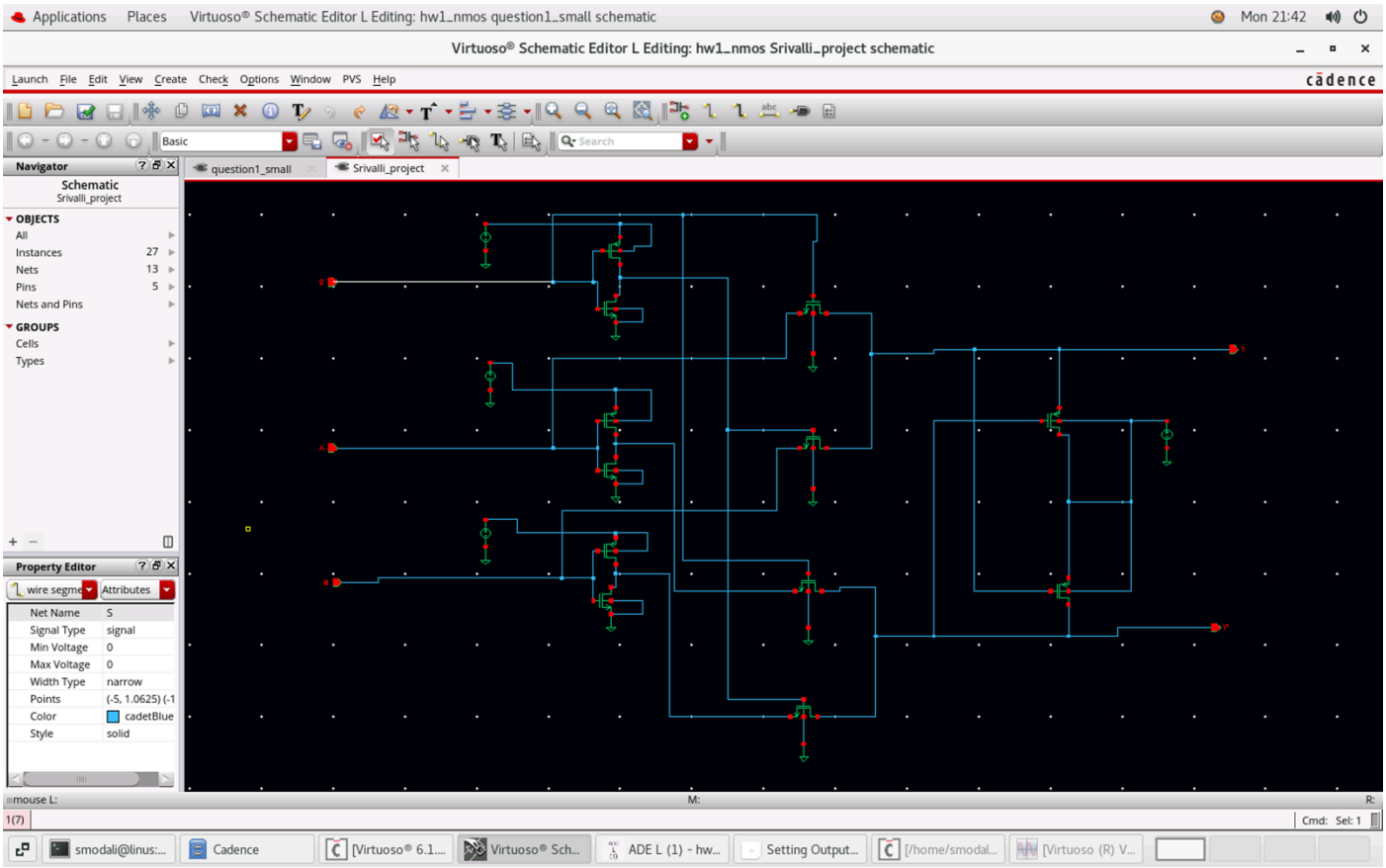

Fig-8

Now, below schematic is the symbol of EEPL mux where all the component of fig-4 enclosed. Here we connect the input VPULSES to data input A and B and to select input S.

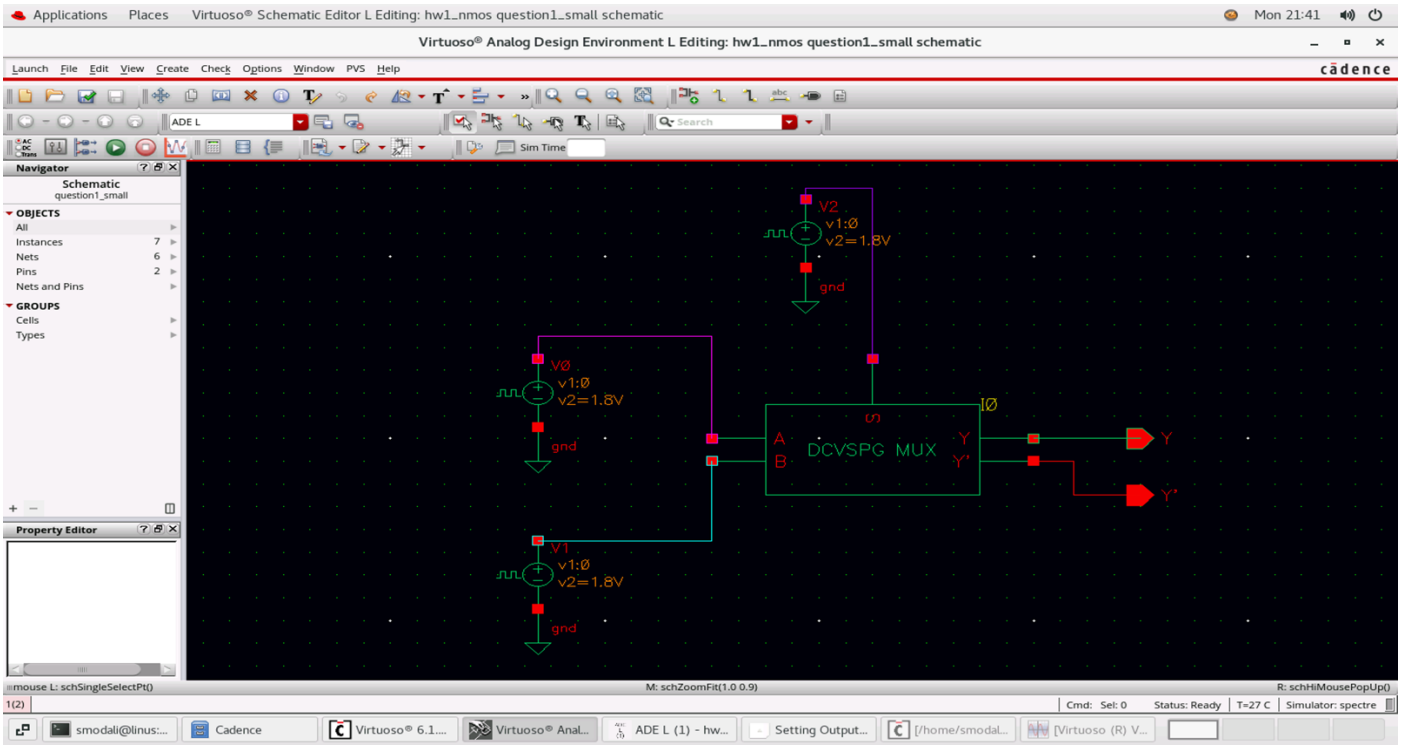

Fig-9

Now in this case there are two data inputs (A and B) and one select input (S). When S is zero, input B is sent to the output Y and Y invert to Y'; when S is one, input A is sent to the output Y and Y invert to Y'. Depending on the value of the select input S, the output waveform will be a duplicate of either input A or input B.

Output waveform:

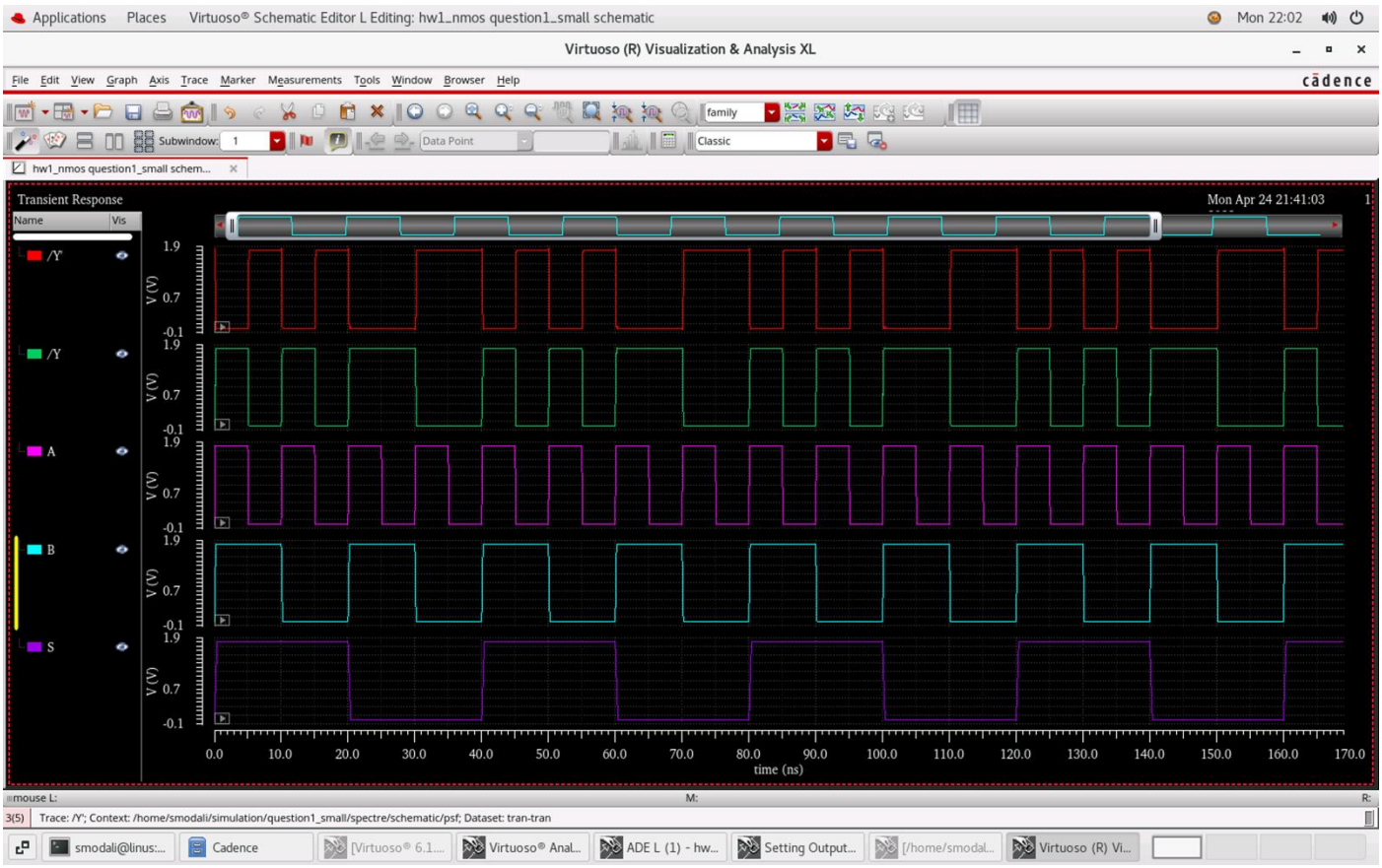

Fig- 10

7.3. Area of the DCVSPG mux:

Area=Length x width of the transistor.
Total Area=Length x Width of the transistor x Number of transistor.

Length= 180nm
Width= 220 nm
Number of transistors = 12
Area = 180 x 220 x12 = 475200

7.4. Results:

Therefore, in conclusion we can say above schematic works as a DCVSPG multiplexer that is when select input S is high, input A passes to output Y and inverts to Y' and input S is low, input B passes to output Y and inverts to Y'.

8. D flip flop design

8.1. D flip flop by connecting LEAP mux and EEPL mux.

To design a D flip-flop using a combination of LEAP mux and EEPL mux, we can follow these steps:

Design the LEAP mux: First, we need to design the LEAP mux using Cadence Virtuoso. The LEAP mux can be designed with data inputs A and B, and a select input S. The output of the LEAP mux will be connected to the data input of the EEPL mux.

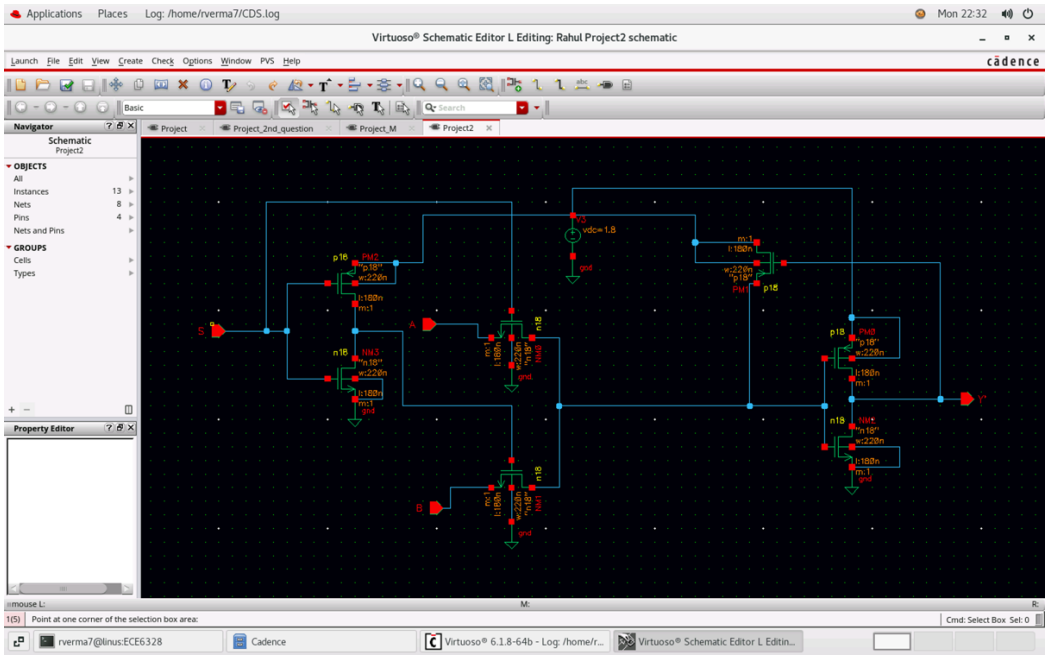

Fig-11

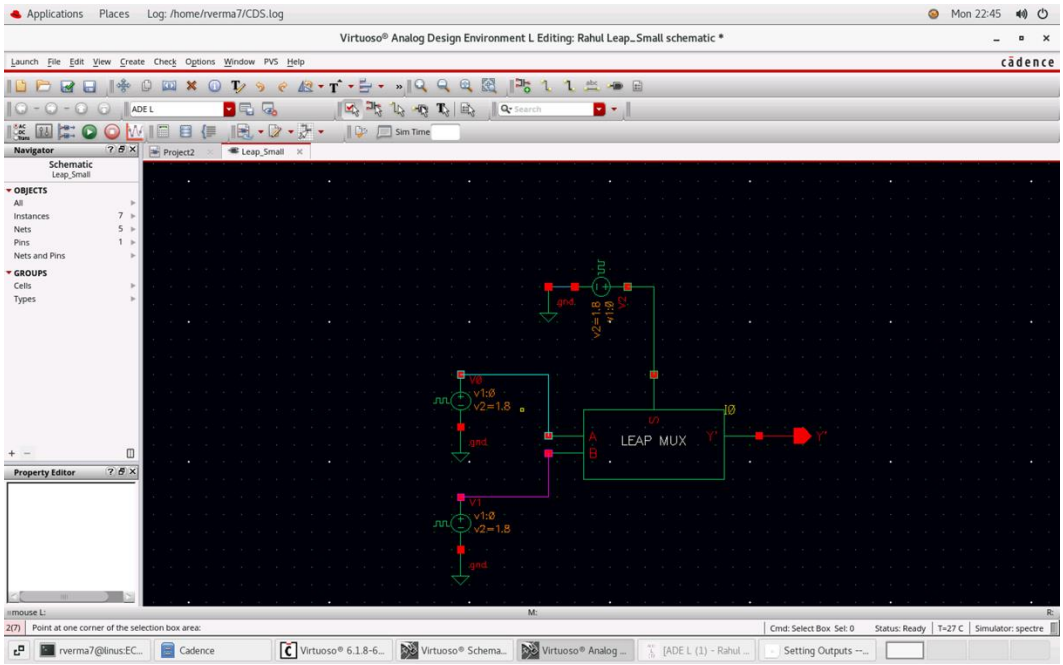

Fig-12

Design the EEPL mux: Next, we need to design the EEPL mux using Cadence Virtuoso. The EEPL mux with data inputs A and B, and a select input S. The output of the LEAP mux will be connected to the input of the EEPL mux.

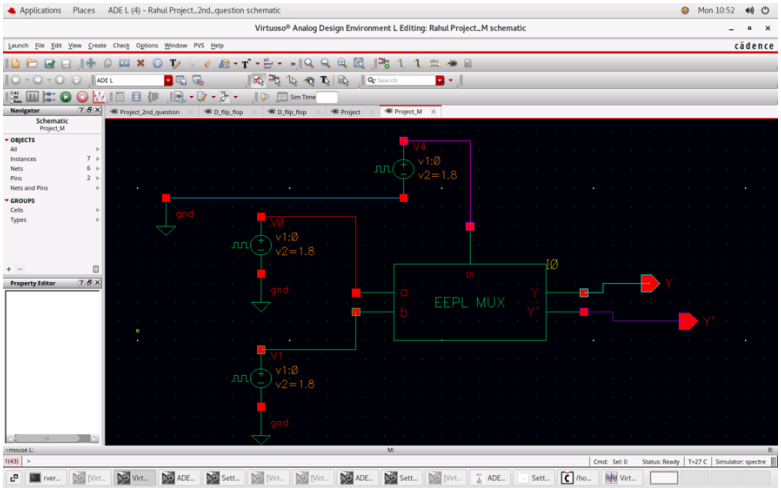

Fig-13

Connect the LEAP and EEPL muxes: The output of the EEPL mux should be connected to the data input of the LEAP mux. The select input of the EEPL mux should be connected to the complement of the select input of the LEAP mux.

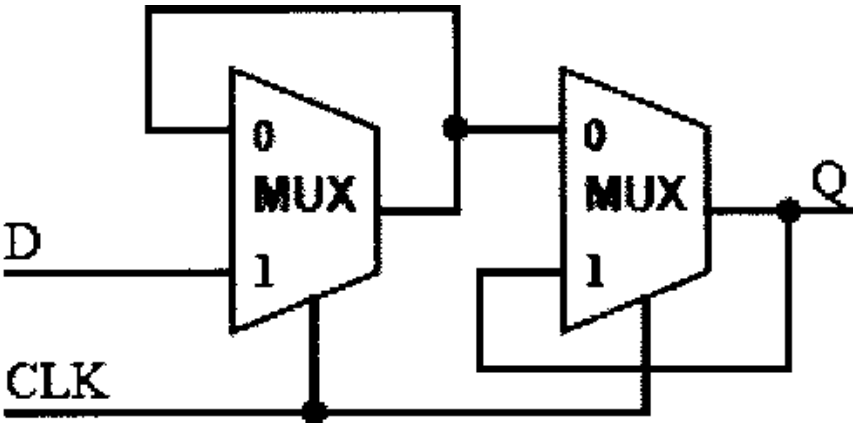

Fig-14

Connect the clock input: The clock input should be connected to the select input of the LEAP and same complement input connect to EEPL mux.

Connect the feedback loop: The output of the LEAP mux should be connected to the data input of the EEPL mux, and the complement of the output of the LEAP mux should be connected to the input of the EEPL mux.

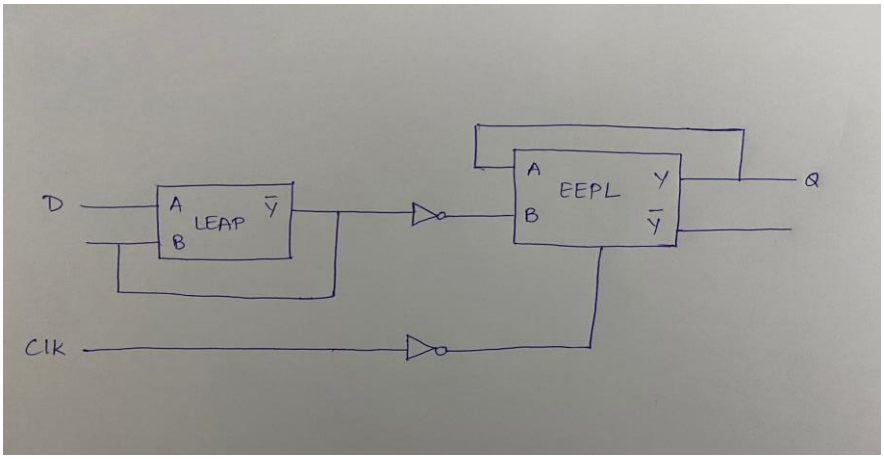

Fig-15

Add power supply and pulse voltage: Finally, we need to add power supply and bias pulse voltage to ensure that the D flip-flop operates correctly.

Once the design is complete, we can simulate the D flip-flop using Cadence virtuoso to ensure that it meets the desired specifications.

8.2. Schematic, simulation, and results for D flip flop using LEAP and EEPL.

The schematic shows the basic circuit diagram for a D flip flop using LEAP mux and EEPL mux. The flip flop's output terminals are Q and Q'. The flip flop's state is represented by Q, whereas its counterpart is represented by Q'.

The flip flop is controlled by a clock signal, CLK. The clock signal determines when the input signal, D, is sampled and stored in the flip flop. The input signal, D, is sampled on the rising edge of the clock signal. When the clock signal is high, the flip flop's output is held constant.

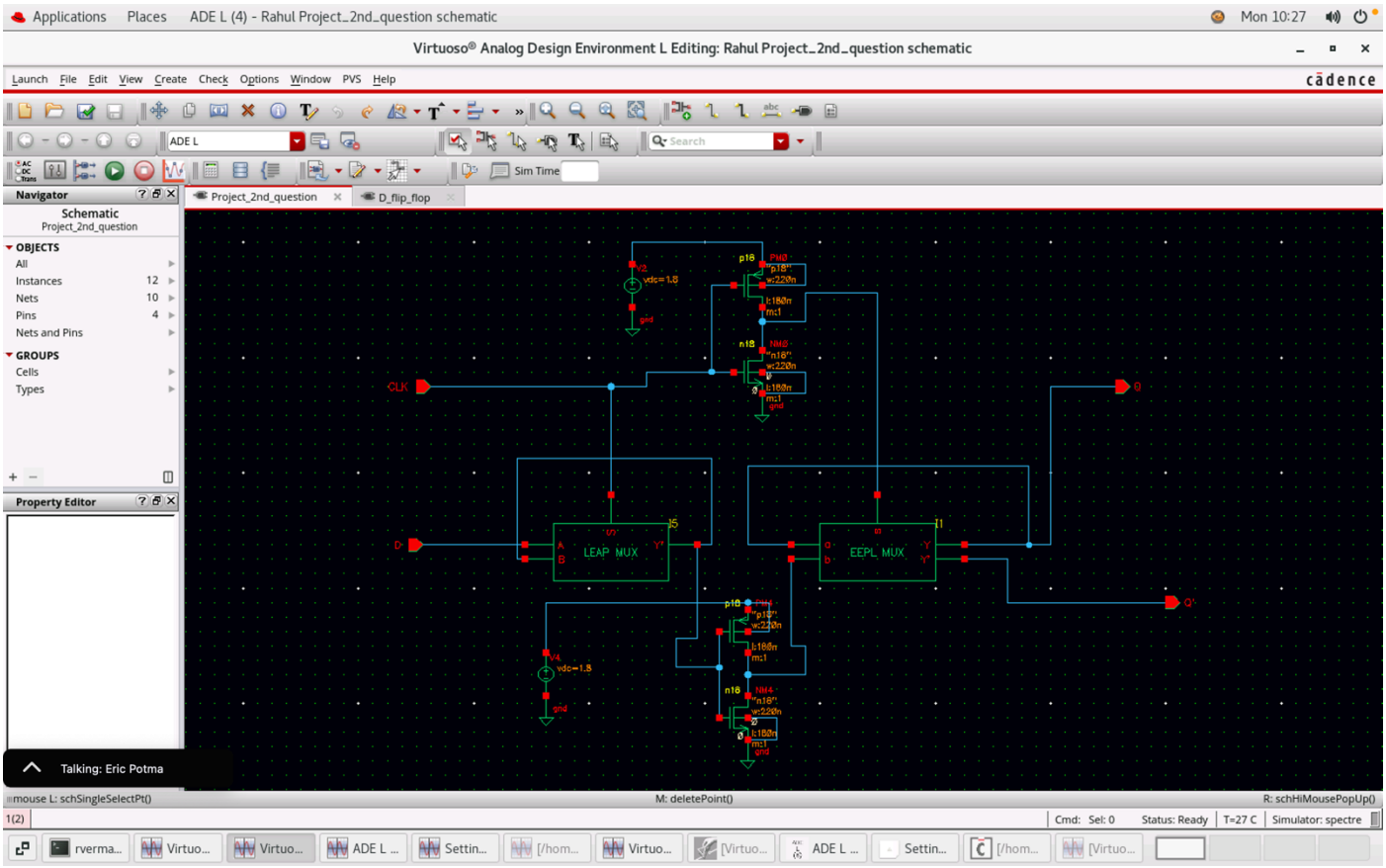

Fig-16

Now, below schematic is the symbol of D flip flop mux where all the component of fig-10 enclosed. Here we connect the input VPULSES to data input D and to select or clock input CLK.

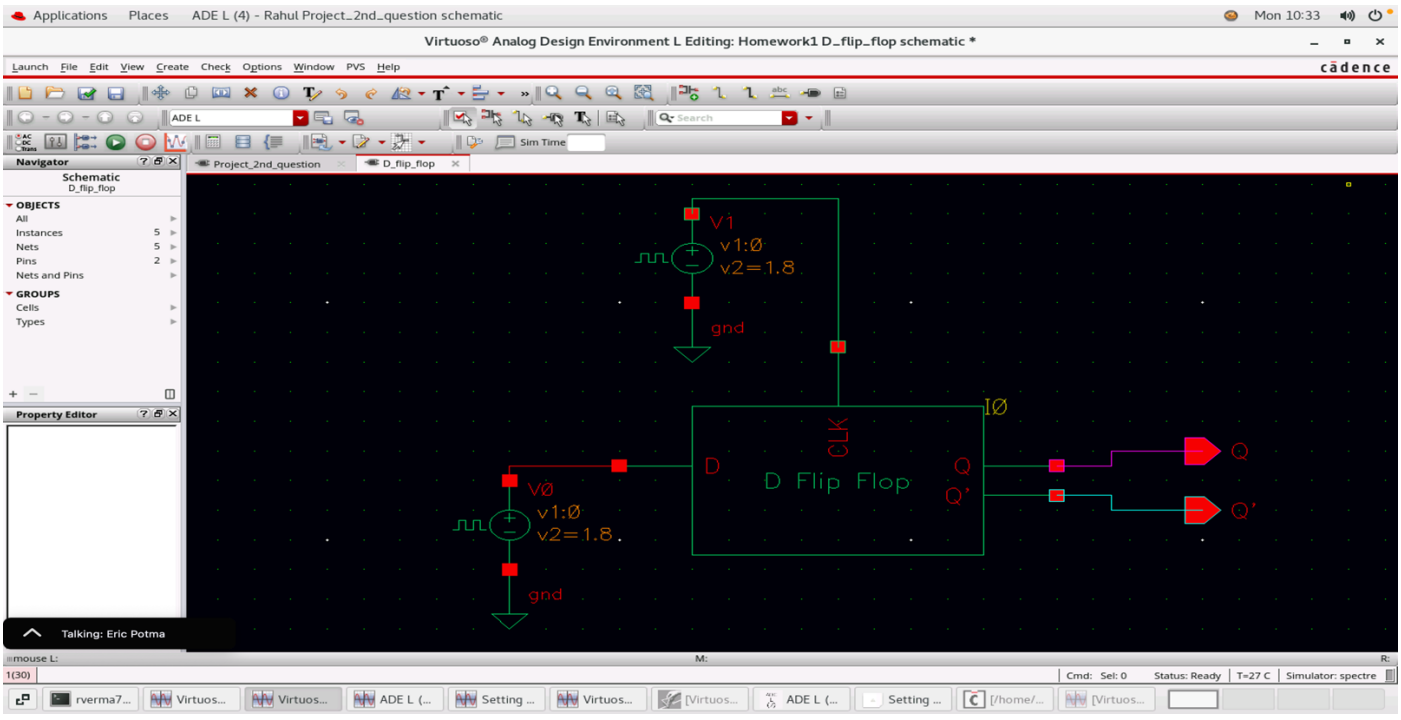

Fig-17

Fig- 18

8.3. Area of the above D flip flop:

Area=Length x width of the transistor.
Total Area=Length x Width of the transistor x Number of transistor.

Length= 180nm
Width= 220nm
Number of transistors = 23
Area = 180 x 220 x23 = 910800

8.4. Results:

Therefore, in conclusion we can say above schematic works as D flip flop that is when the value of the D input is transmitted to the flip-flop's output Q when the clock input is high (logic 1). When the clock input is low (logic 0), the flip-flop's output Q remains unchanged regardless of the D input value.

Thank you