CS5363: Advanced Computer Architecture

End Sem Eaxm, 07 Questions, 80 Marks.
Time: 110 Minutes Pages: 2

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Hyderabad, India
(28th Nov. 2024)

Instructions: If a question suggests answering step-by-step, please follow that instruction accordingly. All the abbreviations used in this question paper have been frequently used in lectures, and I am assuming you are already familiar with them. Do not write unnecessary long answers.

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1. 10

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Inst 1: LD     F6, 34(R2) | Inst 2: MUL.D  F0, F2, F6 | Inst 3: SUB.D  F2, F3, F4
Inst 4: DIV.D  F9, F3, F6 | Inst 5: ADD.D  F9, F3, F5 |
```

Consider a processor using **scoreboarding** technique to execute the above mentioned MIPS program. The functional units available are: 1 integer unit (1 cycle), 2 FP multiplier (4 cycles), 1 FP divider (8 cycles) and 1 FP adder (2 cycles). The execution cycles required for each unit is given in parenthesis. Show the snapshot of the scoreboard after completing the 10th cycle of execution.

Note: If you know **Tomasulo** but not **scoreboarding** then also you can answer but one mark will be deducted at the beginning. *You can use pencil and eraser to update the corresponding scoreboard tables.*

2. Answer the following questions related to Row Hammer attack 10

   a) The easiest way to detect a row hammer attack is to maintain one counter for each row. However, such a naive design has significant hardware overheads. Explain how TWICE solved this problem with a limited number of counters? No need to explain the complete procedure of TWICE, only write whatever is necessary to answer the question. *[5 Marks]*

   b) What is the basic difference between the row hammer mitigation technique of CROW and RHLM? **Hint: Think about the indirect impact of row hammer attack.** *[5 Marks]*

3. Answer TRUE/FALSE and explain your answer in 1-2 lines. No marks will be given if the explanation is not appropriate. Also, no partial marking. 20

   a) Hawkeye has less hardware overhead as compared to SRRIP. F
   b) Implementing SRRIP does not require the concept of Dynamic Set Sampling (DSS). T
   c) Local utilization issue in TCMP means the LLC banks are not using uniformly. T
   d) UCP based cache partitioning is applied on each set separately. F
   e) Commodity DRAM cell is destructive for read operation. T
   f) The Tomasulo's algorithm allows the load/store instructions to enter in the execution stage out of order. T
   g) Pre-charge operation is not always required before accessing a block from the DRAM based main memory. F
   h) The RH detection mechanism of TWICE is implemented inside the memory controller. False
   i) $tRFC > tRC$ F
   j) The XY routing in the NoC of a TCMP is an example of adaptive routing. False

4. Consider an 8x8 Tile-based Chip Multi-Processor (TCMP) with a shared Last Level Cache (LLC). In this architecture, when a core (e.g., from tile T_s) requests a data block that is not found in its L1 cache, the request may traverse the Network-on-Chip (NoC) to retrieve the block from another tile (e.g., T_d). The response packet sent from T_d to T_s contains the requested data block. Now, assume there is a Hardware Trojan (HT) embedded in a NoC router (e.g.,in router R_{ht}) that sporadically modifies the destination tile number in the head flit of certain packets. For instance, a request 10

packet p, originally destined for tile T_{d1}, has its destination altered by the HT to the tile T_{d2} while passing through R_{ht}. Given this scenario, analyze whether the following attacks can be achieved by the HT:

- **Information Stealing:** Can the application running on the core of T_{d2} access or read the altered packet that was originally intended for T_{d1}? *[5 Marks]*
- **Denial of Service (DoS) Attack:** Can the HT cause congestion in the NoC, leading to an increase in the average packet latency of the TCMP? *[5 Marks]*

For each attack, indicate whether it is feasible and support your reasoning with appropriate arguments. Assume no encryption or decryption mechanisms are implemented in the TCMP. Use your understanding of how the LLC controller handles LLC misses to justify your arguments.

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5. Answer the following two questions about randomized cache:

   - What is the primary distinction between Mirage and Maya Cache? Provide your answer in 4-5 lines. *[3 Marks]*
   - Among the following parameters — *performance, security,* and *hardware overhead* — which ones show improvement in Maya Cache compared to Mirage? Explain each parameter separately, detailing how Maya Cache performs relative to Mirage. *[7 Marks]*

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6. Both randomization and partitioning are used as countermeasures against LLC conflict-based attacks. Assume an LLC is partitioned set-wise among cores, with the partitions dynamically adjustable based on application behavior. What additional challenges might arise in implementing the **Hawkeye replacement** policy on this dynamically partitioned LLC design? Suggest an idea to address these challenges.

   Note: You do not need to explain the set-based partitioning or its remapping requirements. Assume these can be handled using remapping tables. *[5 + 5 Marks]*

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7. Consider the following two MIPS programs:

Assumption: The value of X10 is already set. The registers X1 and X2 are used for indexing the loop. BNEQ means "branch not equal to".

Program-1:

```
L: LD X3, 0(X1)
   LD X4, 8(X1)
   LD X5, 16(X1)
   ADD X3, X3, X4
   ADD X3, X3, X5
   SD X3, 0(X2)
   ADDI X1, X1, #32
   ADDI X2, X2, #8
   BNEQ X1, X10, L
```

Program-2:

```
L:LD X3, 0(X1)
  ADD X3, X3, X0
  ADD X4, X3, X3
  SD X4, 0(X2)
  SD X3, 8(X2)
  SD X3, 16(X2)
  ADDI X1, X1, #8
  ADDI X2, X2, #32
  BNEQ X1, X10, L
```

Both programs have an equal number of instructions. Consider a single-core processor, C1, where the LLC is designed with STTRAM. Also, assume that all the data request gets hit in LLC because of an efficient prefetcher.

a) Which of the program shows more performance degradation in C1, as compared to a similar processor having SRAM-based LLC? Explain in 4-5 lines. *[5 Marks]*

b) Let the answer of part a) is **Program-x**. Discuss a technique that can enhance the performance of the STTRAM LLC such that **Program-x** can show better performance. *[5 Marks]*