The topics that I will cover next are:

- Multicycle pipeline.
- Out-of-order execution (O3)
- Pipeline scheduling.

Tomasulo:

Instruct	Issue	Execute	Writeback
LD F6, 32(R2)	✓	✓	
LD F2, 44(R3)	✓		
MULD F0, F2, F4	✓		
SUBD F8, F2, F6	✓		
DIVD F10, F0, F6	✓		
ADDD F6, F8, F2	✓		

Name	Busy	Op	Vj	Vk	Qj	Qk	A
Load 1	Yes	LD					32+Reg(R2)
Load 2	Yes	LD					44+Reg(R3)
Add 1	Yes	SUBD			Load 2	Load 1	
Add 2	Yes	ADD D			Add 1	Load 2	
Add 3	No						
Mul 1	Yes	MulD		Reg(F4)	Load 2		
Mul 2	Yes	DivD			Mul 1	Load 1	

F0	F2	F4	F6	F8	F10
Mul 1	Load 2	0	Load 1 ? Add 2	Add 1	Mul 2

→ Scoreboarding & Tomasulo same?
→ How to do issue, execute and WB?
→ How many cycle for each?
→ Once Q becomes available, what to write in V?
→ How to know mul. D is ready to write?
→ Will loop come?
→ What is DADDIU & BNE?
→ Will you give # reservation stations?
→ What to if all values are available? Should we still put in station?
→ When to write Mem[Reg] & When to write Reg?
→ Temp variable?
→ WAW & WAR hazards where? → Two WB at the same time?

→ Page 180, code.

Cycle
X Z $ ..

Inst	Issue	Execute	WB
2 LD F6, 32(R2)	✓1	2-3	4
LD F2, 44(R3)	✓2	3-4	5
MULD F0, F2, F4	✓3		
SUBD F8, F2, F6	✓		
DIVD F10, F0, F6	✓		
ADDD F6, F8, F2	✓		

Reservation station

	Busy	op	Vj	Vk	Qj	Qk	A
Load 1	Yes ✓	LD ✓					32+Reg[R2] ✓
Load 2	Yes ✓	LD ✓					44+Reg[R3] ✓
Add 1	Yes ✓	SubD ✓			Load2 ✓	Load 1 ✓	
Add 2	Yes ✓	AddD ✓			Add 1	Load 2	
Add 3	No ✓						
Mul 1	Yes ✓	MulD ✓		Mem[Reg[F4]] ✓	Load 2 ✓		
Mul 2	Yes ✓	Div d			Mul 1	Load 1 ✓	

Register Status

F0	F2	F4	F6	F8	F10
Mult1	Add2	0	~~Load1~~ Add2	Add1	Mult2