Hardware Architecture for Deep Learning - CS6490. Spring 2023-24.
Dept. of CSE, IIT Hyderabad
Quiz-2

Total marks: 10 **Time: 10 minutes**

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1. Systolic arrays can be implemented on (choose correct ones): [1]
   a. CPU with Vector instructions
   b. GPU
   c. ASIC
   d. FPGA

2. Which dataflow is depicted by the given code snippet for a 1-D convolution: [1]

```
for (i=0; i<K; i++)
  for (p=0; p<N; p++)
     out[p] += in[i+p] * wt[i]
```

out, in, wt represent the output, input, and weight matrices, respectively.

   a. Input stationary
   b. Output stationary
   c. Weight stationary

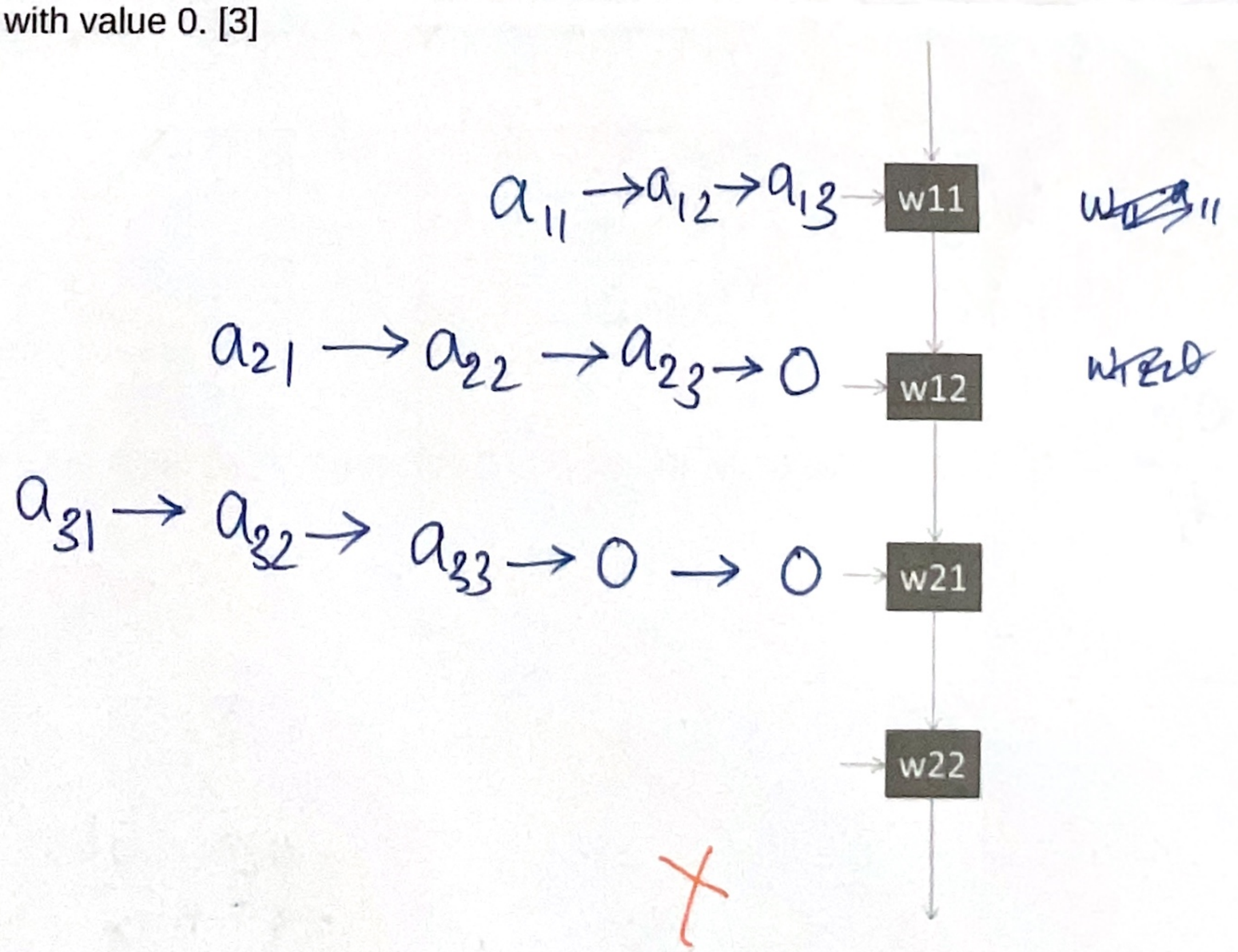
3. Given the systolic design as shown, mark the values to be fed to horizontal and vertical inputs. Any cycle gap can be shown with value 0. [3]

Input:

a11	a12	a13
a21	a22	a23
a31	a32	a33

Kernel:

w11	w12
w21	w22



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4. Consider an application whose 20% time is spent executing sequential portion of the code while 80% time is spent executing parallelizable code on a 1-core CPU. Calculate the maximum possible speedup when executing this application on a 16-core system. [2]

$$\frac{1}{1-0.8+\frac{0.8}{16}} = \frac{1}{\frac{2}{10}+\frac{1}{20}} = 4$$

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5. Perform 3-D convolution of the given 3x3x2 input and 2x2x2 kernel. Assume stride=1. [3]

Input channel-0		
2	3	4
1	2	3
2	1	5

Input channel-1		
1	3	5
2	4	6
0	1	2

Kernel channel-0	
0	1
1	-1

Kernel channel-1	
-1	0
0	1

2	3	+	3	3	=	5	6
3	-1		-1	-2		2	-3

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