Instruction status:

Inst I j k	Issue	Read operand	Execute	Write back
LD F6, 34(R2)				
LD F2, 45(R3)				
MUL F0, F2, F4				
SUB F8, F6,F2				
DIV F10, F0, F6				
ADD F6, F8, F2				

Functional Unit status:

FU	BUSY	OP	Fi	Fj	Fk	Qj	Qk	Rj	Rk
Int									
MULT1									
MULT2									
ADD									
DIV									

Register result status:

	F0	F2	F4	F6	F8	F10	F12
FU							

WAW → Dont w
RAW → Dont
  write
WAR → Dont
  read

Scoreboard: Simulation

Cycle: 1

Instruction status

				Read	Ex	Write
Instr	**Fi**	**Fj**	**Fk**	**Issue**	**Op**	**Done**	**Result**

Instr	Fi Fj Fk	Issue	Op	Done	Result
I1: LD	F6, 4+, R2	1	2	3	4
I2: LD	F2, 8+, R3	5	6	7	8
I3: MULTD	F0, F2, F4	6	9	10-19	20
I4: SUBD	F8, F6, F2	7	9	10-11	12
I5: DIVD	F10, F0, F6	8	21	22-61	62
I6: ADDD	F6, F8, F2	13	14	15-16	22

RAW
RAW

WAR → Dont write
WAW → Dont issue
RAW → Dont read.

Functional unit status

FU Name	Busy	Op	Dest Fi	S1 Fj	S2 Fk	FU→j Qj	FU→k Qk	Fj Rj	Fk Rk
Integer									
Mult 1									
Mult 2									
FP Adder									
Divider									

Register result status

	F0	F2	F4	F6	F8	F10	F12	....	F30
FU						DIV			