

CS5363: Advanced Computer Architecture
Mid Sem Exam, 08 Questions, 90 Marks.
Time: 120 Minutes Pages: 2

IIIT
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- If a question suggests answering step-by-step, please follow that instruction accordingly.
- Two key abbreviations to note: Last Level Cache (LLC) and Covert-Channel Attack (CCA).
- Other abbreviations mentioned in this exam have been frequently used in lectures, and I am assuming you are already familiar with them.
- TimeCache, V-Way, ZCache, and CEASER are the research papers already discussed in class.
- Do not write unnecessary long answers.

1. Explain the attack for which a countermeasure is proposed in TimeCache. How does TimeCache prevents the attack? Do you think implementing TimeCache on STT-RAM LLC has additional performance challenges? Justify your answer with 2-3 lines. [Marks: 3+4+3] ✓
N/A 10
2. Explain the remapping policy of CEASER step-by-step? What is the additional overhead of implementing CEASER on top of an STT-RAM LLC? Explain why CEASER is not guaranteed to prevent the attack that TimeCache prevents? [Marks: 4+3+3] ✓
X 10
3. Dynamic partitioning can be misused to perform CCA. Please discuss (step-by-step) an idea to prevent this attack? **Note:** Your idea should allow performing dynamic partitioning without any security issues. Please do not consider static partitioning as a solution here. The marking will be given based on the practicality of your idea. ✓
X 10
4. The Prime+Probe attack on the Last Level Cache (LLC) was covered in class. To execute the attack, the attacker needs to understand the cache's mapping policy in order to create eviction sets. With this knowledge, do you foresee the possibility of a different type of attack (not necessarily related to information theft) targeting STT-RAM LLC? Provide a step-by-step justification for your answer. ✓
X 10
5. The V-Way concept was discussed in class. Using an example, explain why having only forward pointers (from tags to data) is insufficient, and why backward pointers (from data to tags) are also essential. Additionally, why is the number of valid data entries always equal to the number of valid tag entries in V-Way, even though the tag array contains twice as many entries as the data array? [Marks: 7+3] ✓
X 10
6. Implementing Z-Cache on an STT-RAM-based Last Level Cache (LLC) introduces additional overheads compared to its SRAM counterpart. What are these overheads? Propose an idea to address this issue, involving changes to the fundamental policy of Z-Cache. **Note:** Although this specific idea was not discussed in class, by combining concepts and papers reviewed during lectures, you can formulate a solution. ✓
X 10
7. Assume that two computer manufacturing companies are manufacturing processors with RISC-V ISA. Consider Processor-X is manufactured by the first company and Processor-Y is manufactured by the second company. Processor-X has a clock cycle time of 250ns and a CPI of 1.7. Processor-Y has a clock cycle time of 500ns and a CPI of 1.2. Which processor is faster? Explain. ✓
X 10

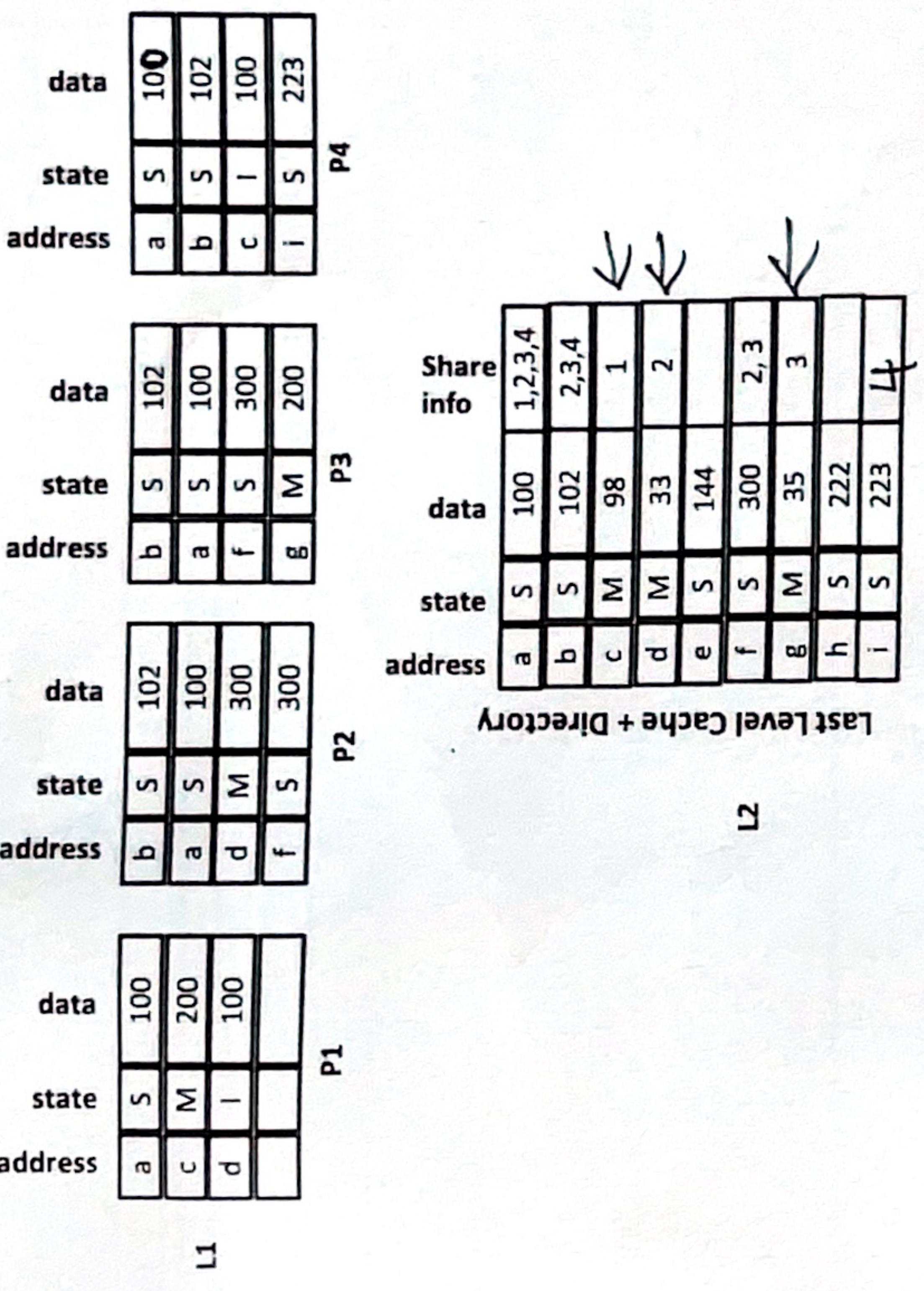


Figure 1: MSI protocol snapshot.

- ① 8. Consider a multicore system with 4 cores. Each core has its own L1 cache and all the cores share a common large L2 cache as LLC. The L1 caches maintain a directory coherence protocol; the directory information of each block is stored in L2 along with the block. [20]

The above figure shows the current status of the memory system (L1 cache and the L2 cache). **All the caches are fully associative using LRU as replacement policy.** For L1 cache, each cache block stores the *address*, *coherence state* and the *data*. While each block in L2 stores *address*, *coherence state*, *data* and the *directory information* (i.e. sharers info).

For simplicity the block address are given as a, b, \dots, i, j . Note that the state **I** means the location is currently empty. A block in L2 without any sharer information means the block is only available in L2. *In each cache, assume that the block placed at the bottom position (in the diagram) is the LRU block.*

Considering MSI coherence protocol show the status of the memory system (shown in Figure 1) after executing all these operations sequentially.

- a) P1: Write *a*. //The value of *a* in P4 is wrongly written as 101. Please make it 100 first and then start answering.

b) P1: Read *b*.

c) P3: Read *e*.

d) P1: Read *j*.

e) P2: Read *a*.

Showing the cache status means you need to draw the updated figure in your answer sheet. For partial marking show the cache status separately after each operation sequentially. You can also show only the final cache status but in that case no partial marking will be awarded in case of any mistake.