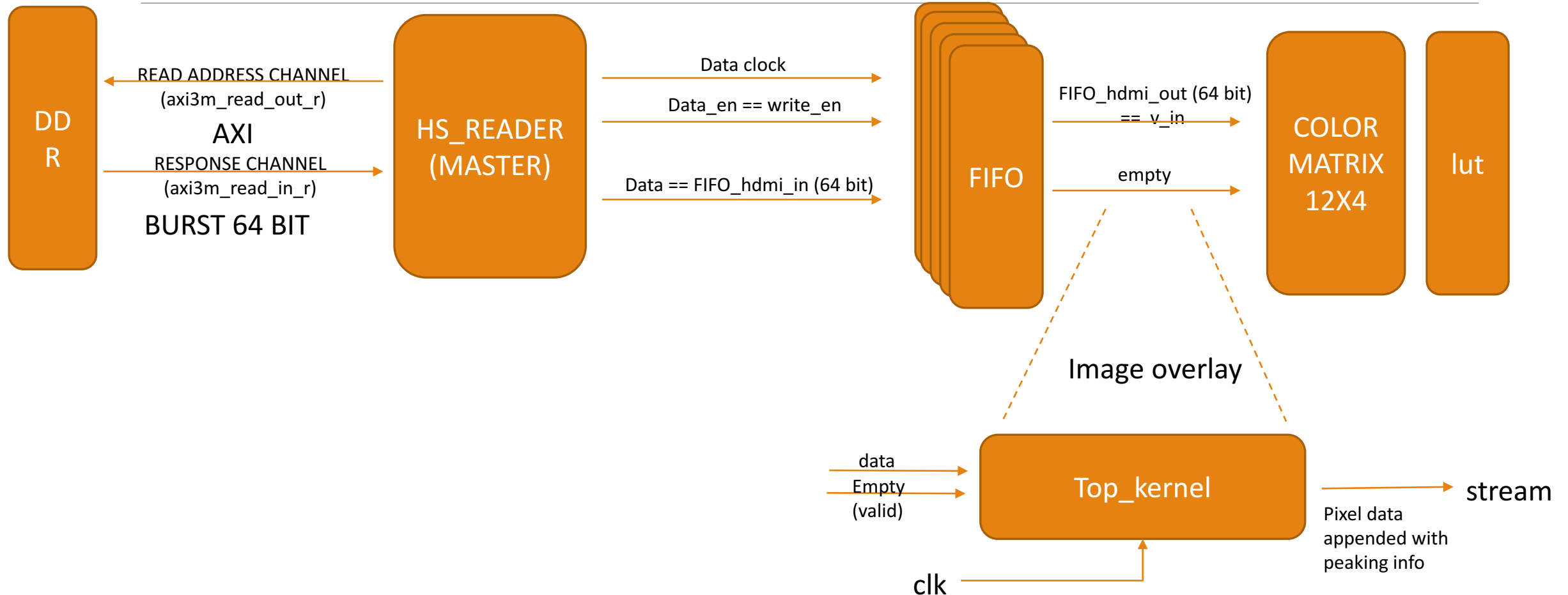


# Real-time Focus Peaking

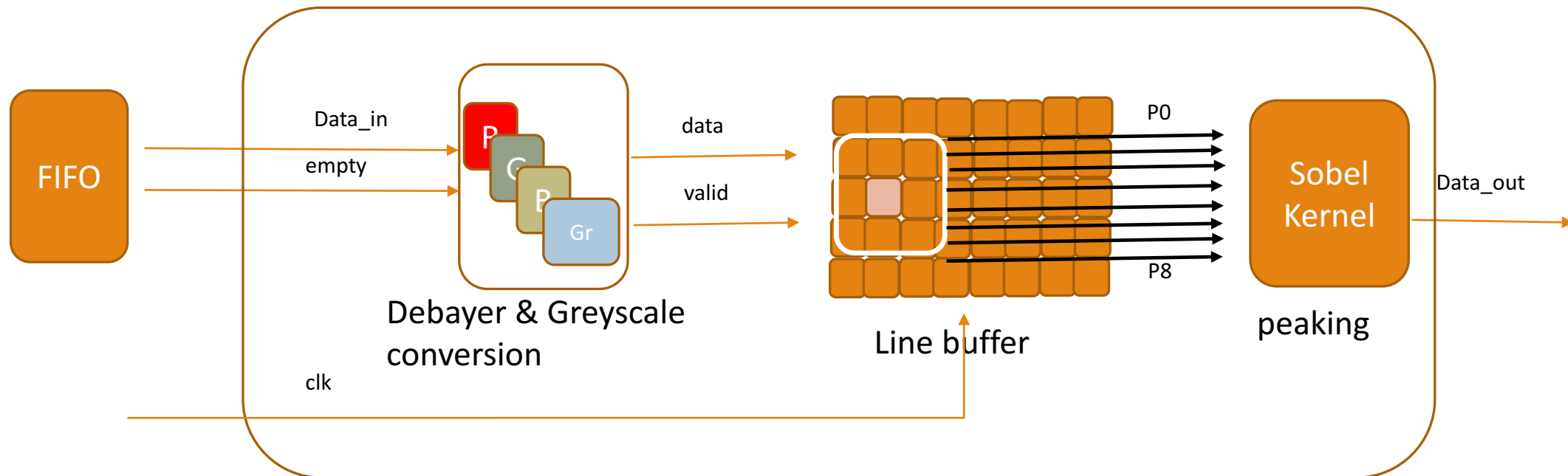
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VHDL BASED KERNEL

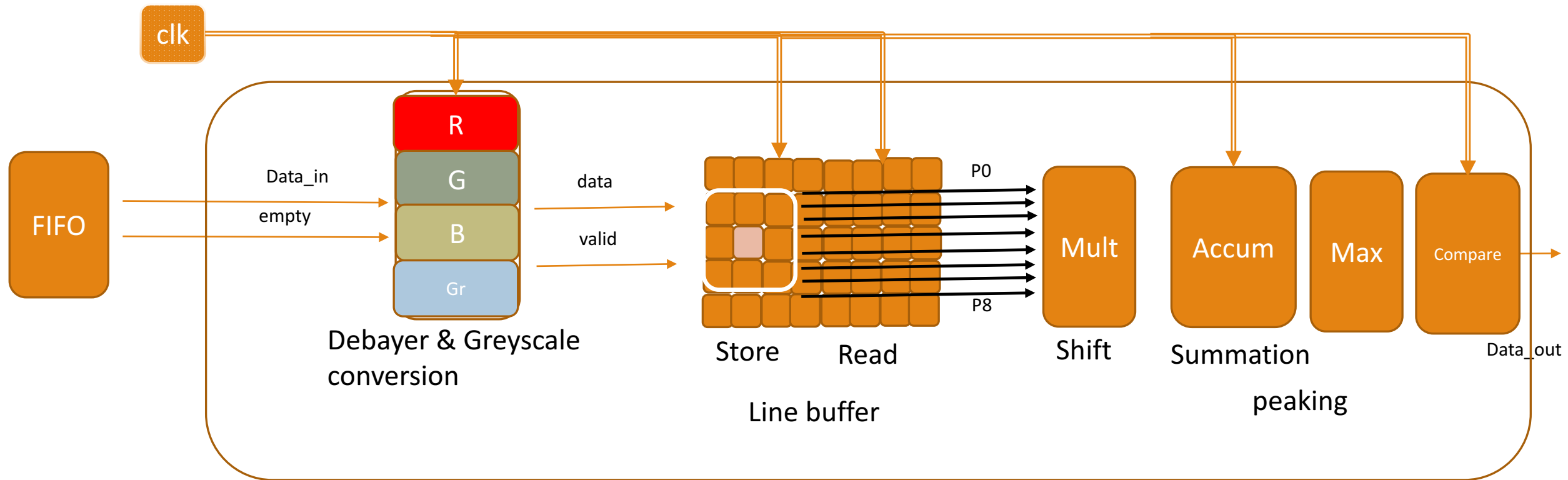
# Output Image Processing Pipeline



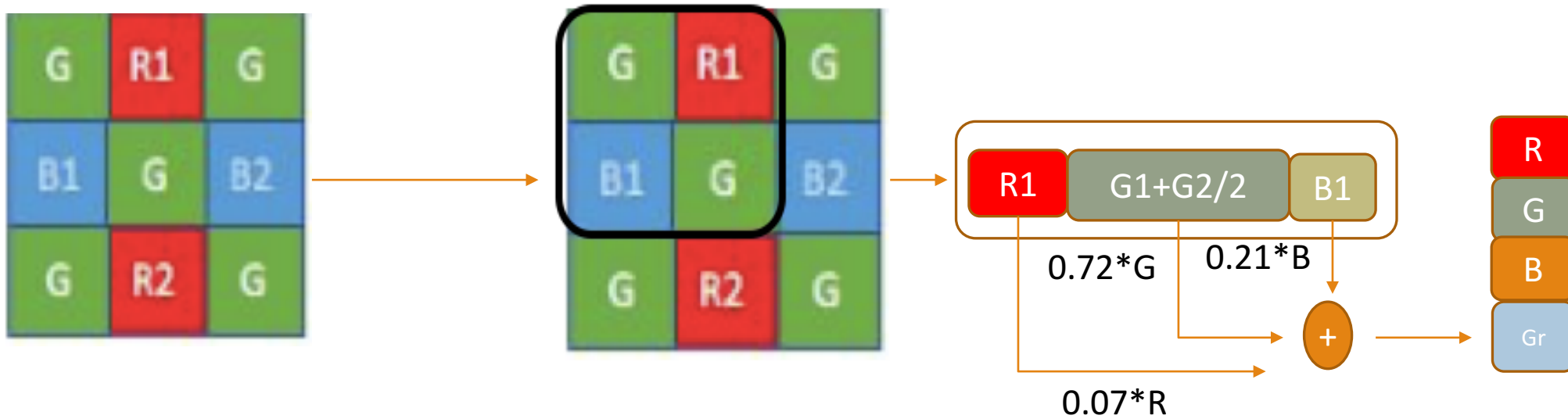
# Top Module



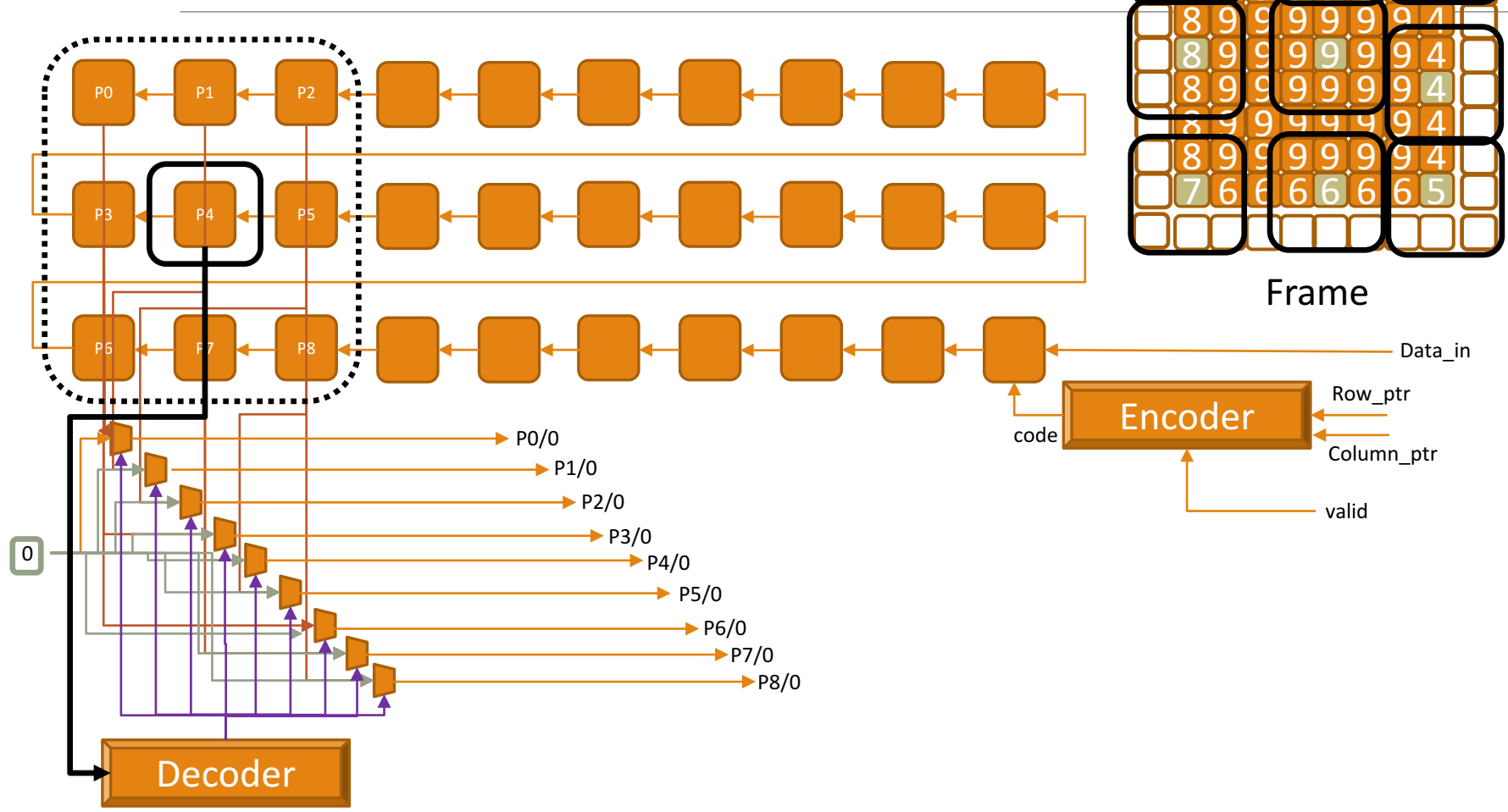
# Top Module



# GRB Gr Module



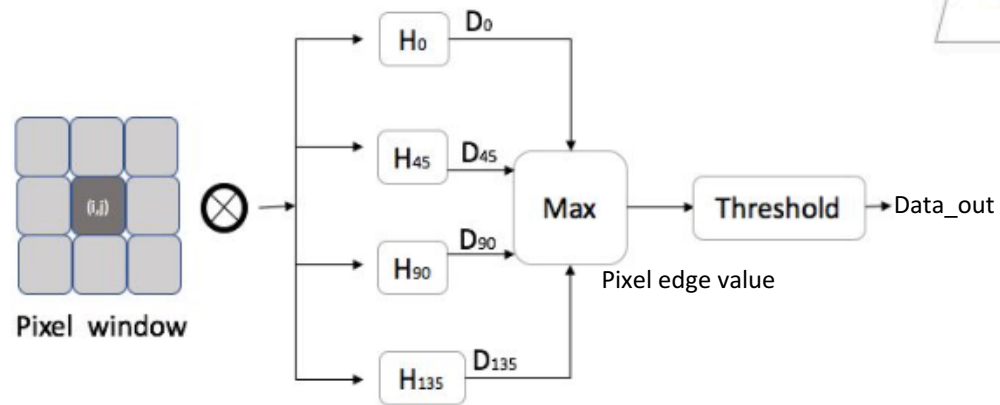
# Line buffer



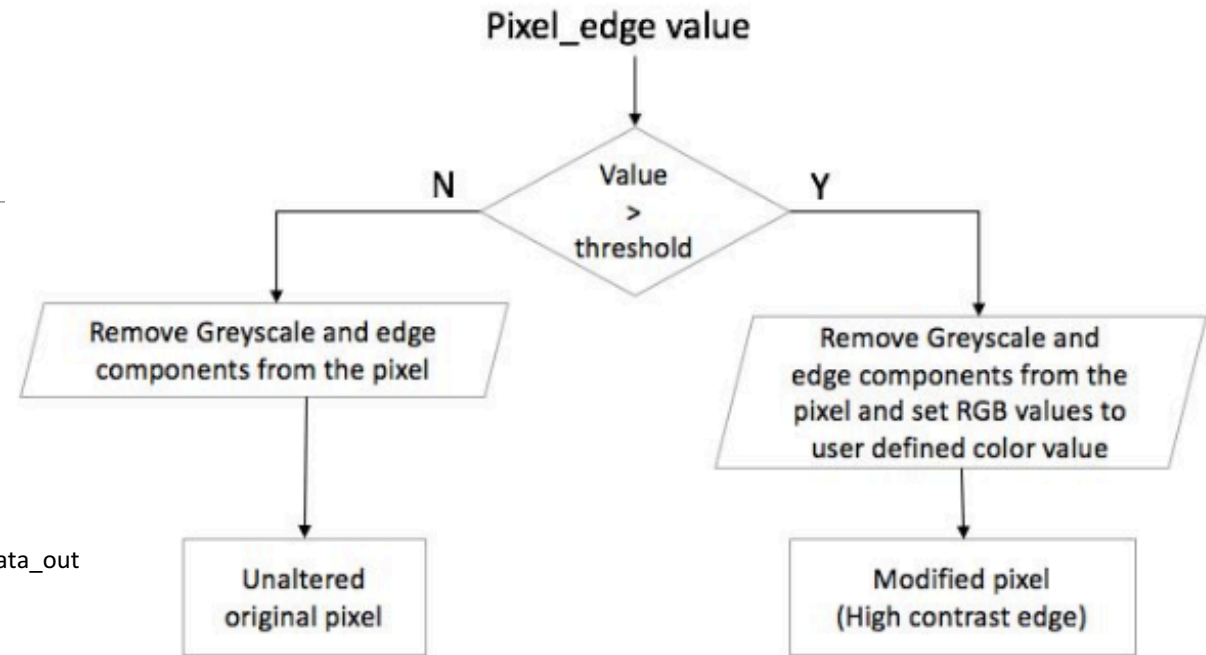
Case	Code	Condition
C1	1000	$L\_ptr=0 \ \& \ c\_ptr=0$
C2	1001	$L\_ptr=0 \ \& \ c\_ptr \neq 0 \ \& \ c\_ptr \neq (columns-1)$
C3	1010	$L\_ptr=0 \ \& \ c\_ptr \neq (columns-1)$
C4	1011	$L\_ptr \neq 0 \ \& \ L\_ptr \neq 0(Rows-1) \ \& \ c\_ptr \neq (columns-1)$
C5	1100	$L\_ptr \neq 0(Rows-1) \ \& \ c\_ptr \neq (columns-1)$
C6	1101	$L\_ptr \neq 0(Rows-1) \ \& \ c\_ptr=0 \ \& \ c\_ptr \neq (columns-1)$
C7	1110	$L\_ptr \neq 0(Rows-1) \ \& \ c\_ptr=0$
C8	1111	$L\_ptr=0 \ \& \ L\_ptr \neq 0(Rows-1) \ \& \ c\_ptr=0$
C9	0001	Normal case
	0000	NO ACTION

$L\_ptr$  = Row pointer  
 $C\_ptr$  = Column pointer

# Sobel kernel



$$H_0 = \begin{bmatrix} -1 & -2 & -1 \\ 0 & 0 & 0 \\ 1 & 2 & 1 \end{bmatrix} \quad H_{45} = \begin{bmatrix} -2 & -1 & 0 \\ -1 & 0 & 1 \\ 0 & 1 & 2 \end{bmatrix} \quad H_{90} = \begin{bmatrix} -1 & 0 & 1 \\ -2 & 0 & 2 \\ -1 & 0 & 1 \end{bmatrix} \quad H_{135} = \begin{bmatrix} 0 & 1 & 2 \\ -1 & 0 & 1 \\ -2 & -1 & 0 \end{bmatrix}$$



Multiplying by:-

-1 = 2s compliment

-2 = left shift and 2s compliment

2 = left shift

# Second Evaluation

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# tasks

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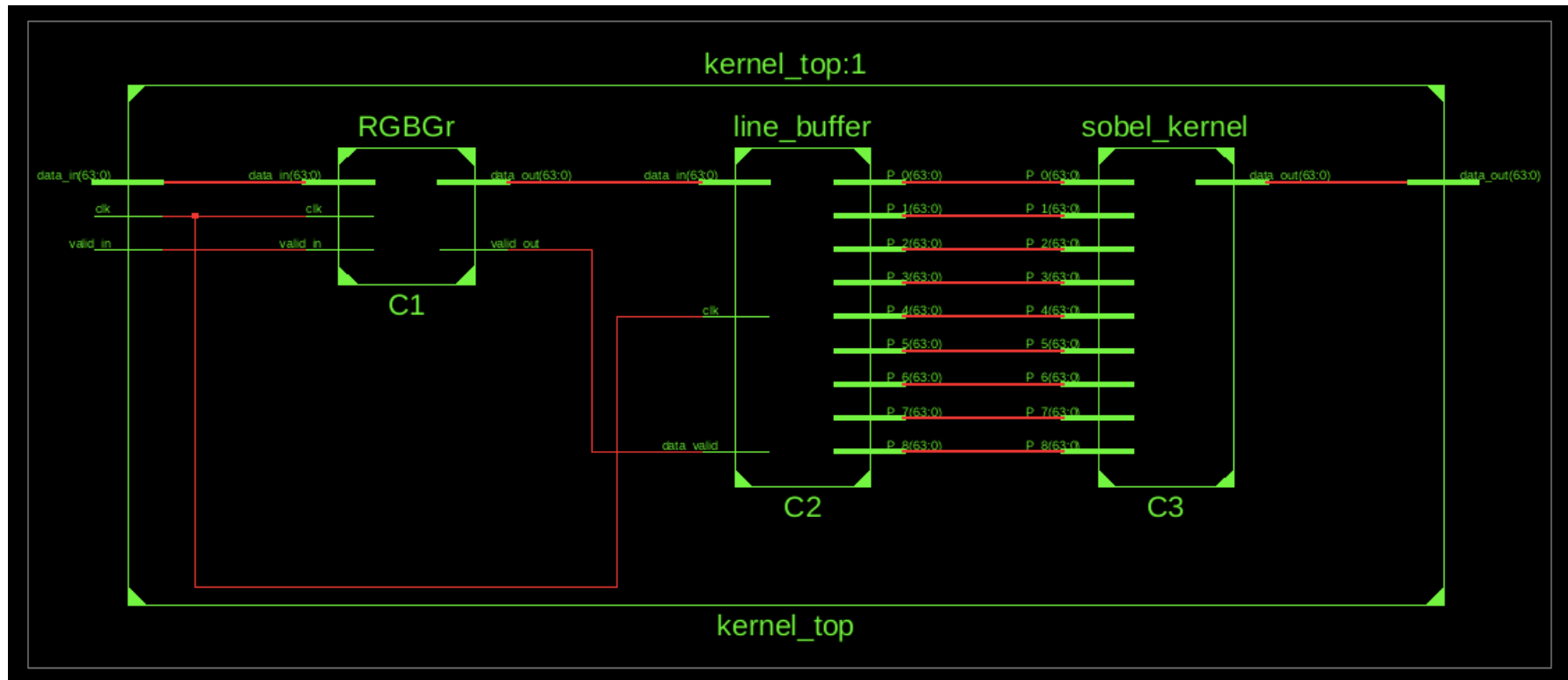
- 1: Simulate the IP from top level to the structural level
- 2: Instantiate the IP into the AXIOM pipeline

# Simulation

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- To Simulate the IP the main structure was the line buffer.
- To test the line buffer, external signals in form of random pixel values were forced on the line buffer (5x5 for testing purpose) over a period of time so that all the pixels streams through the pipeline.
- The result of the pipeline was observed and the generated window pixels were compared so as to verify the correct functioning of the pipeline.
- The top module was tested to see if the output stream removes the blue and green component from the incoming pixels whose grey value was below a preset thresh hold.



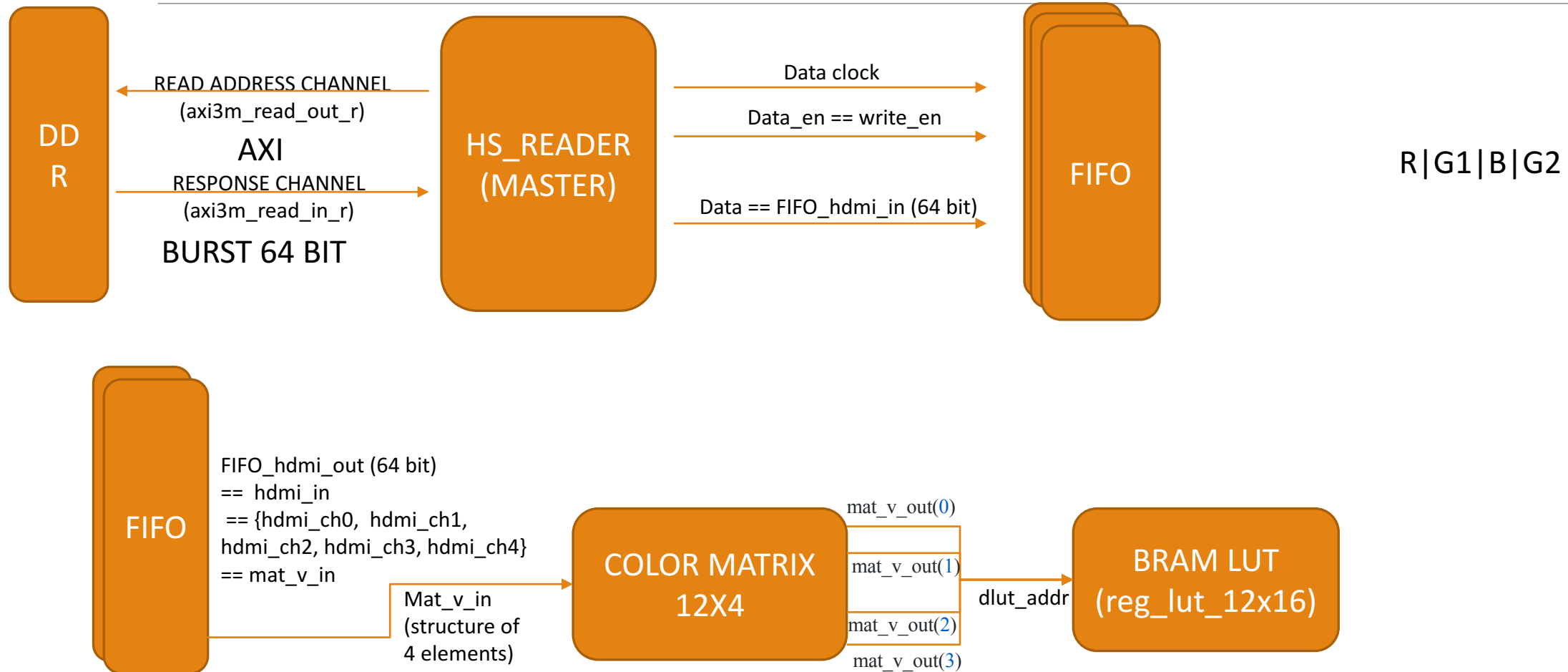


RTL schematic of the IP

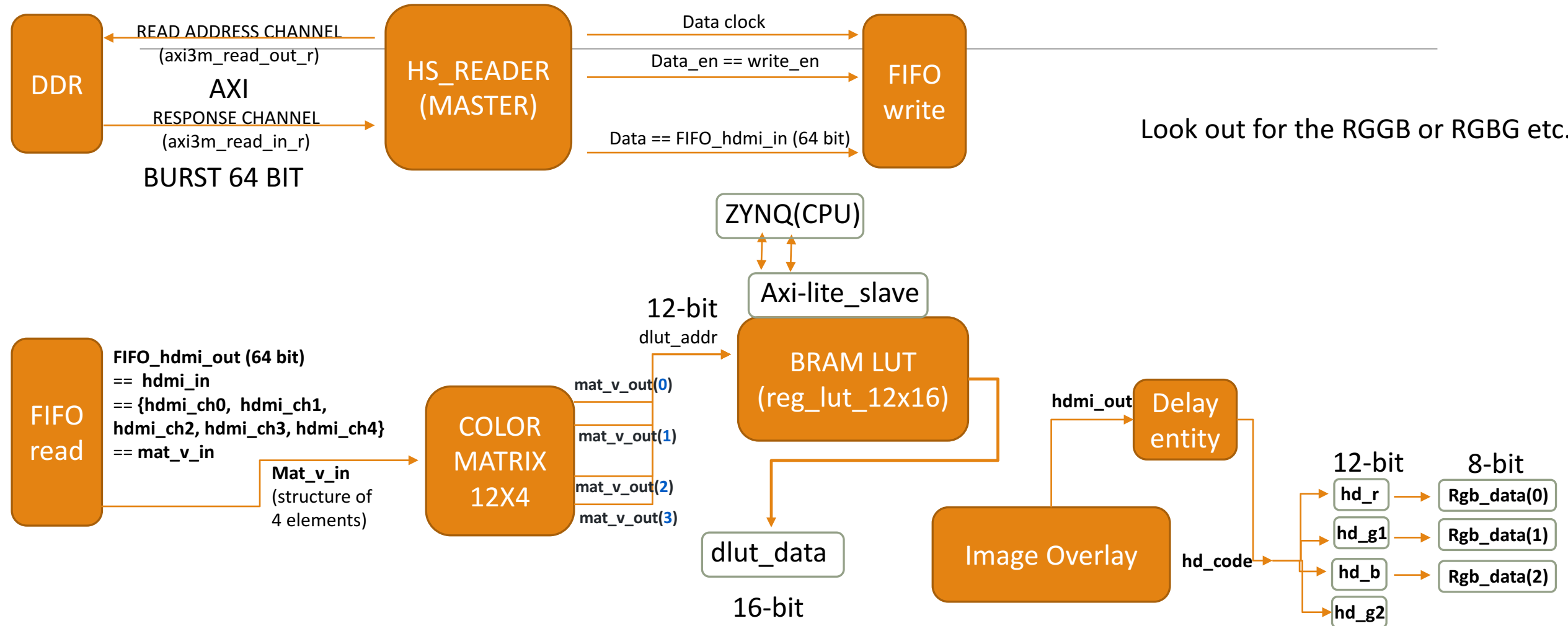
# Instantiation

INSTANTIATE THE IP INTO THE AXIOM PIPELINE

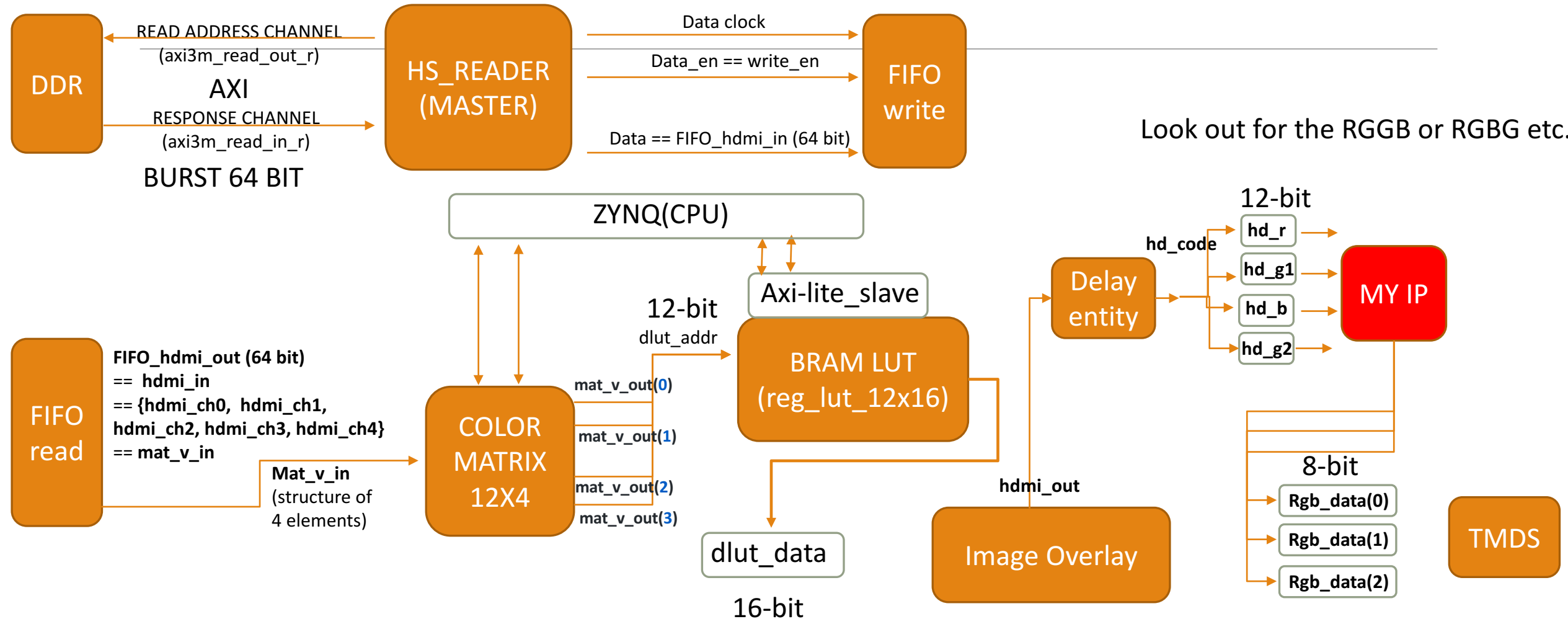
# Output Image Processing Pipeline



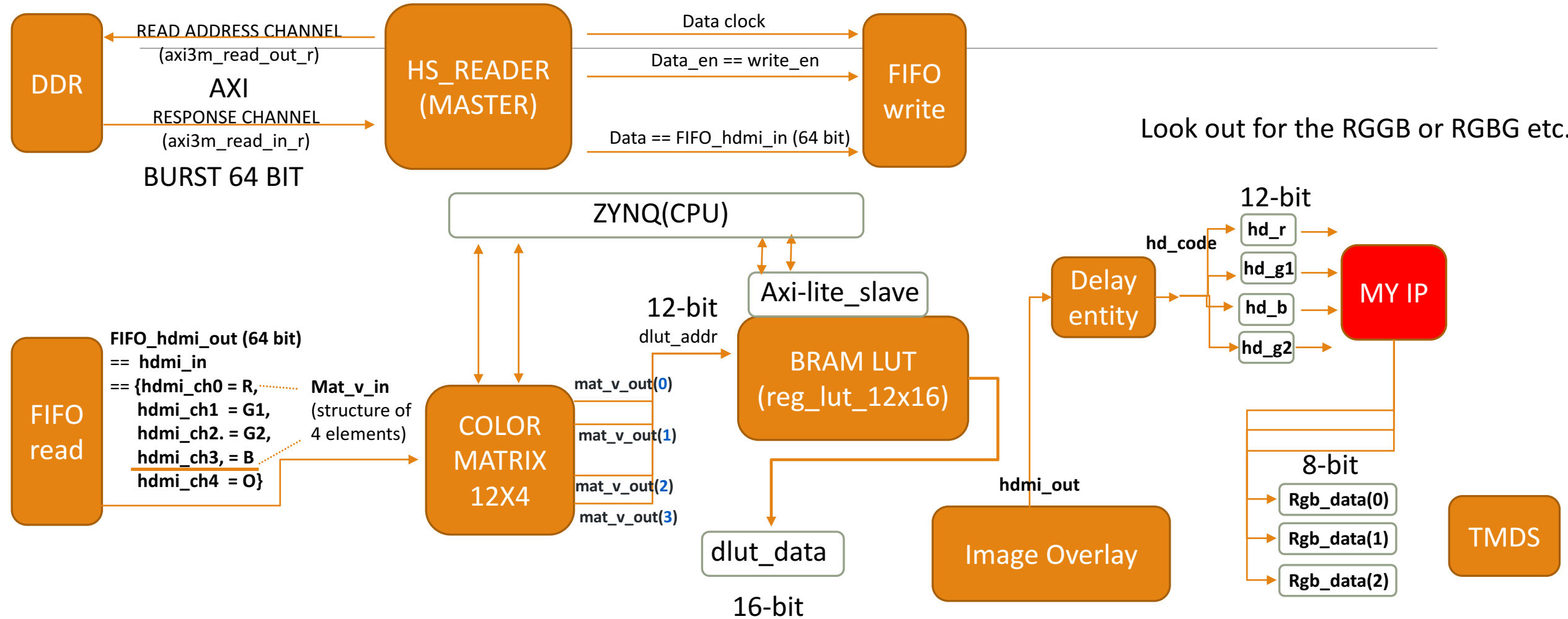
# Output Image Processing Pipeline



# Output Image Processing Pipeline

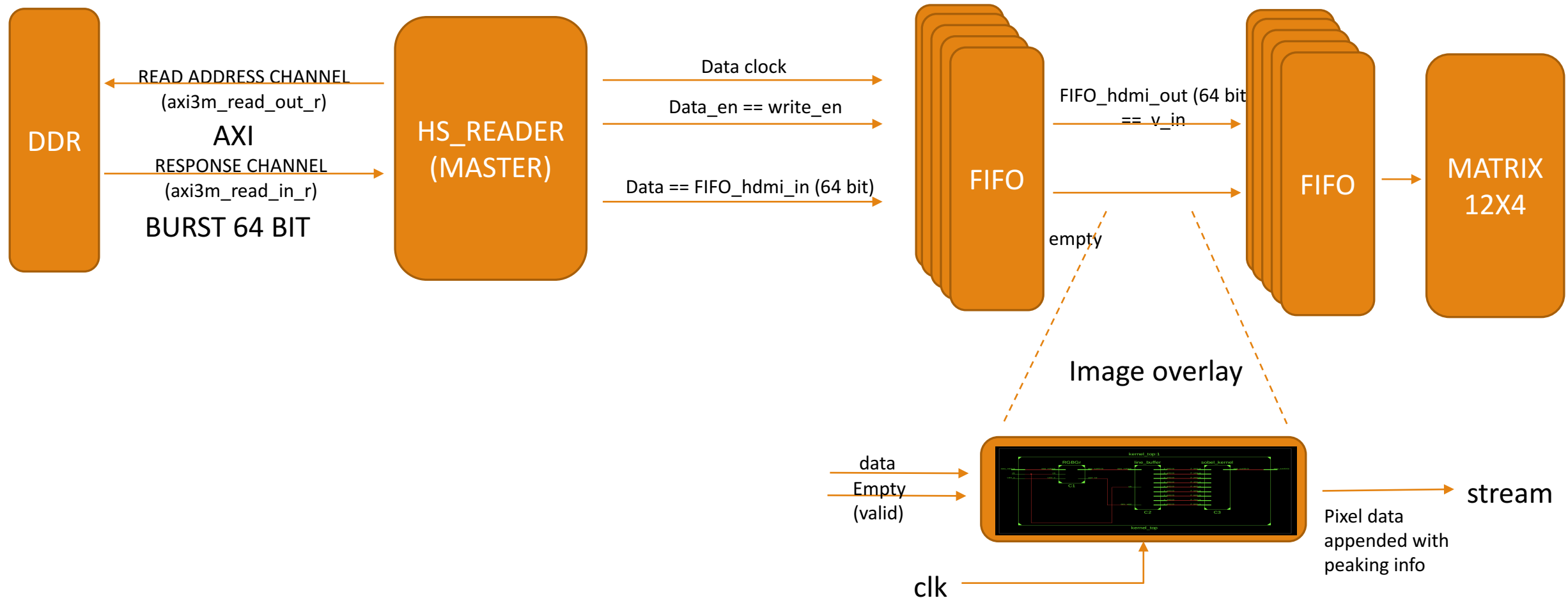


# Output Image Processing Pipeline-new

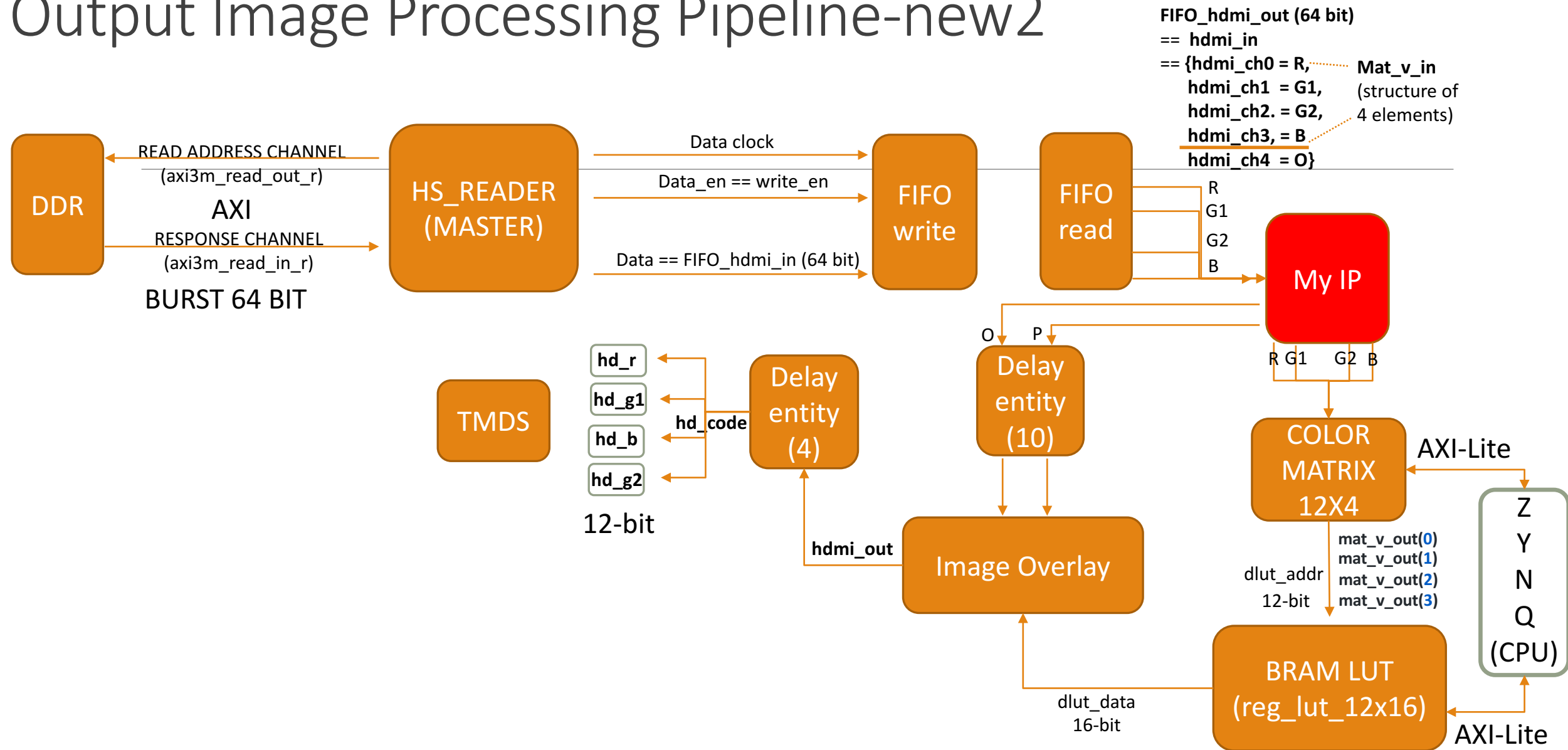




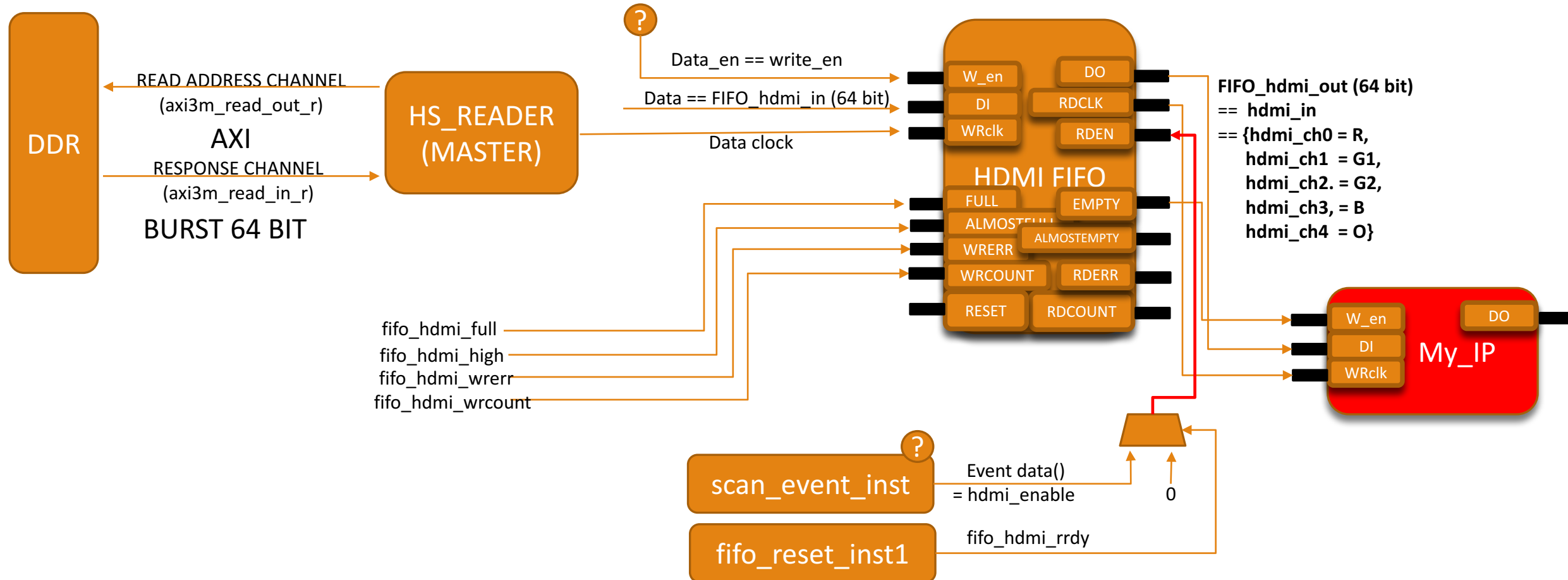
# Output Image Processing Pipeline (new)



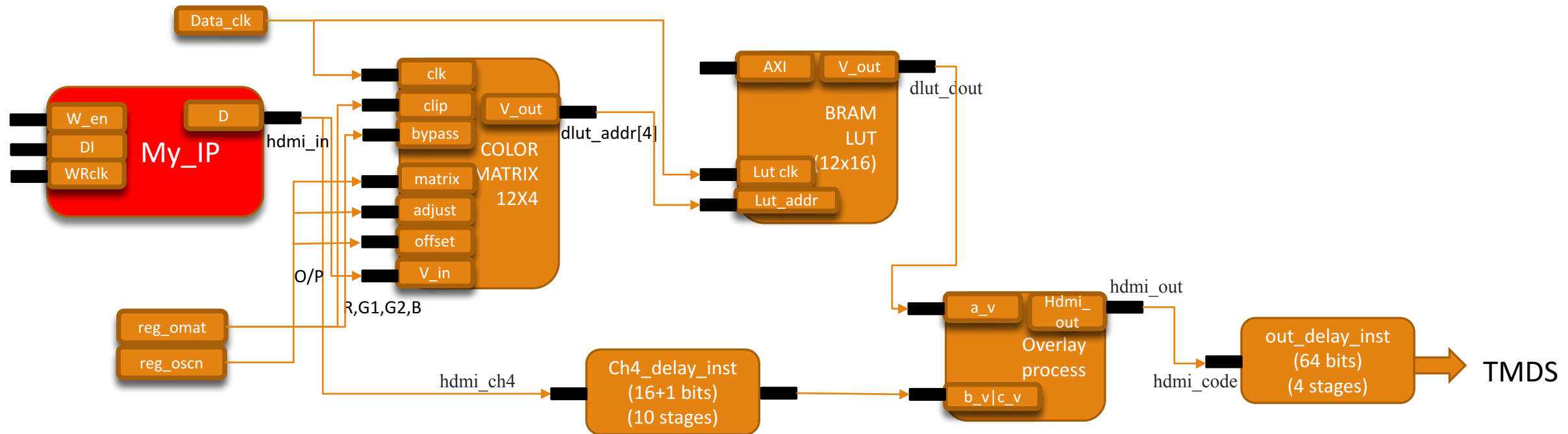
# Output Image Processing Pipeline-new2



# Output Image Processing Pipeline (IP input)



# Output Image Processing Pipeline (IP input)



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- Didn't understand the functioning of the HDMI/RGB scan...that handles the timing...because first of all im not able to find data\_valid signal flowing through the stream lps like thematrix ...LUTs....secondly without EOL and SOF im not able to see how are the timing like blank and sync signals being generated...and how address is being generated for the HP\_reader