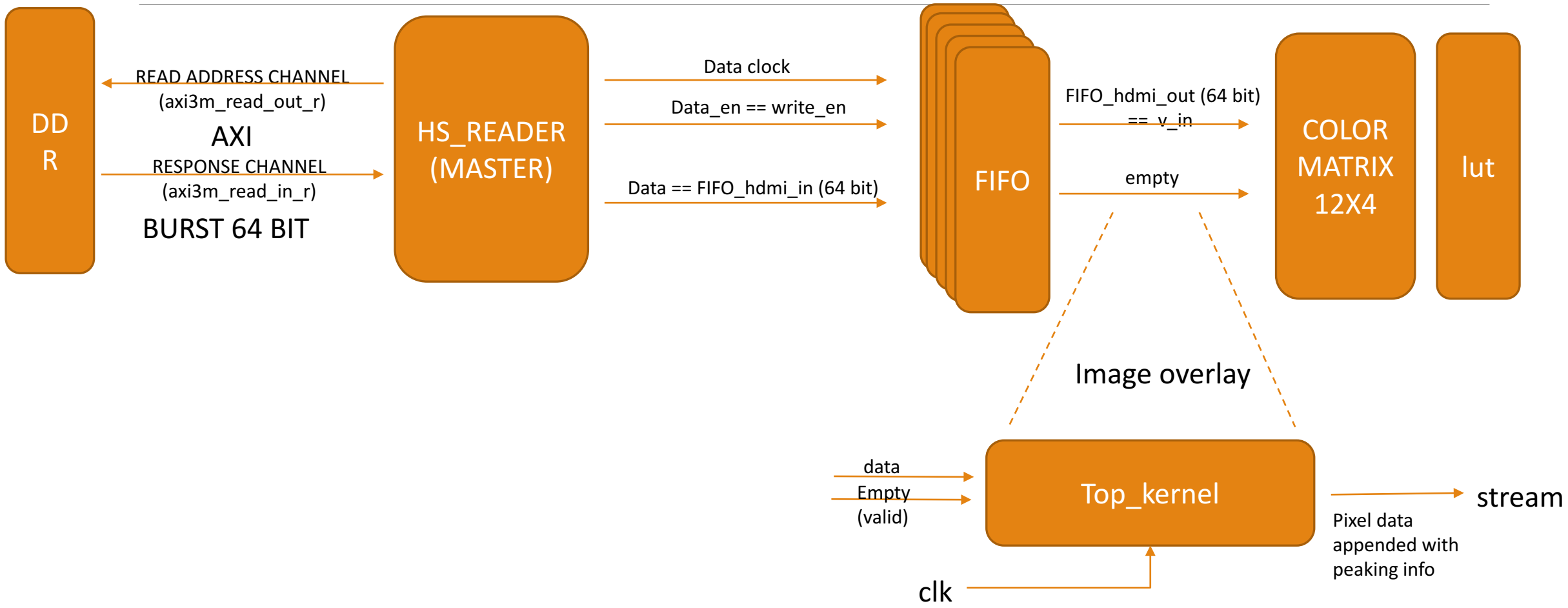
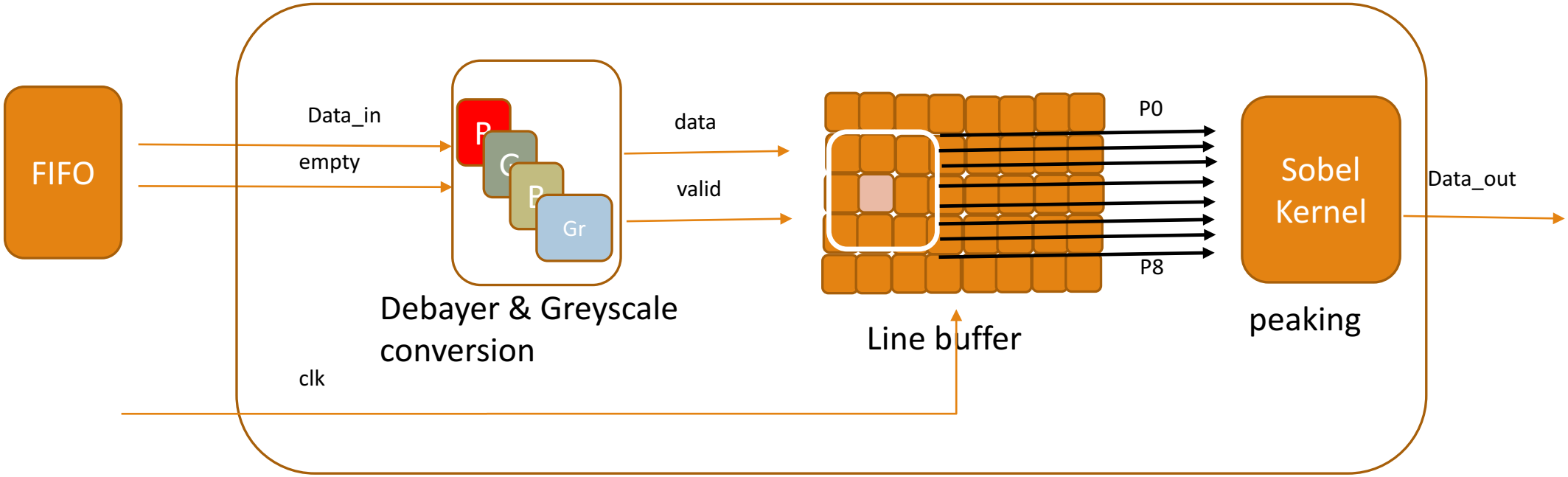
Real-time Focus Peaking

VHDL BASED KERNEL

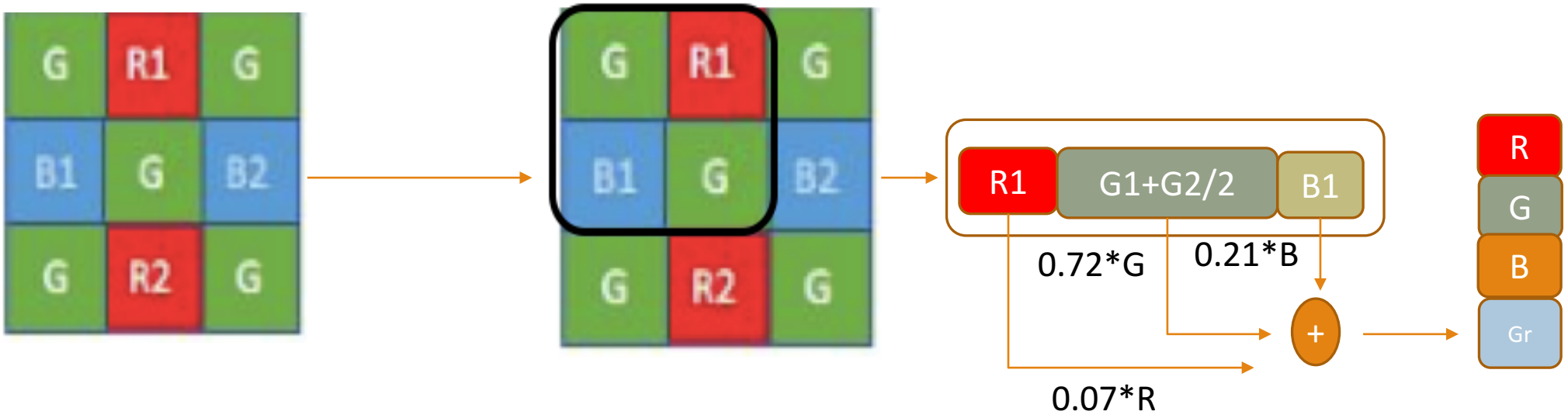
Output Image Processing Pipeline



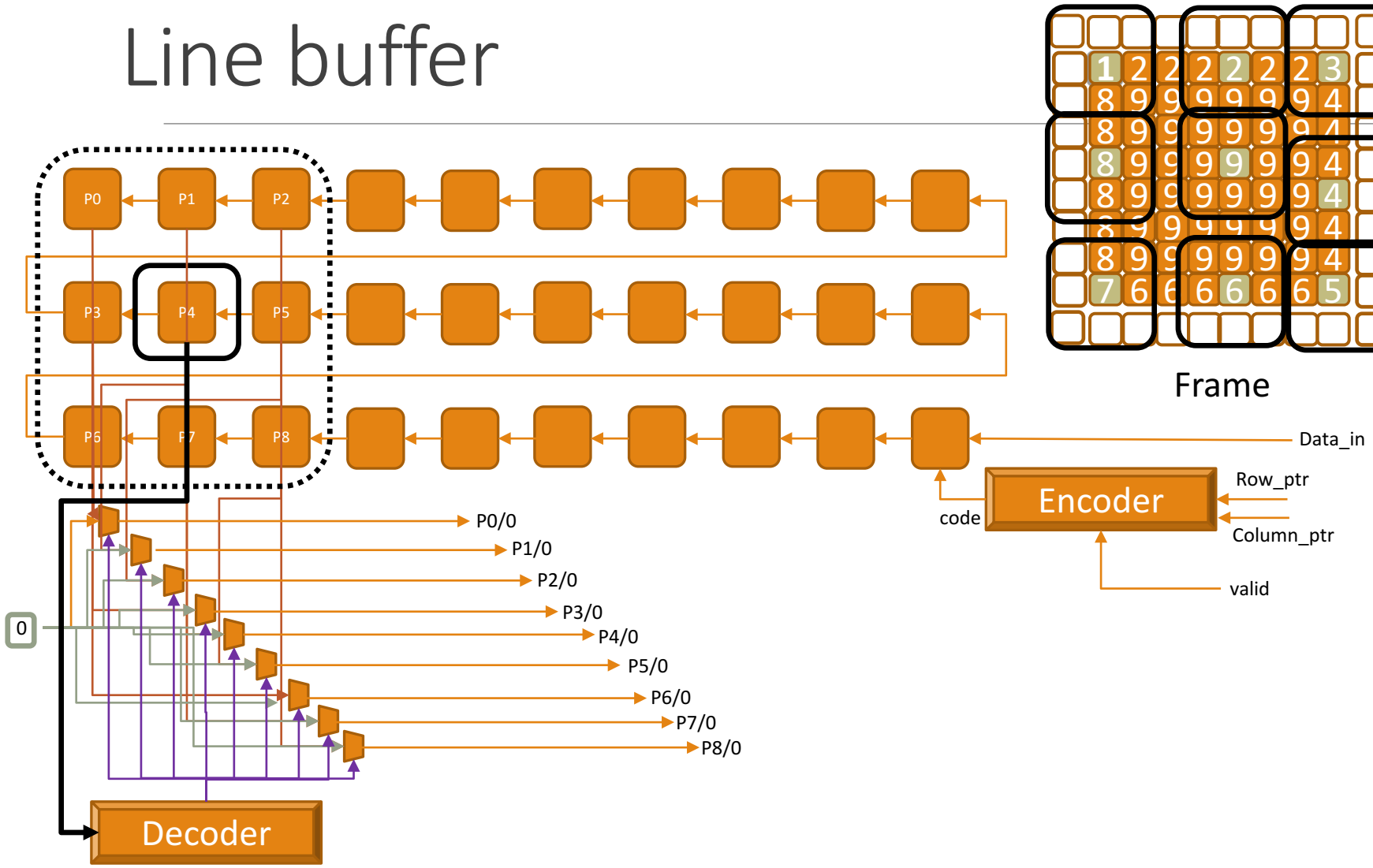
Top Module


FIFO
Data_in
empty
clk
R
G
B
Gr
Debayer & Greyscale conversion
data
valid
P0
P8
Line buffer
Sobel Kernel
peaking
Data_out

GRB Gr Module



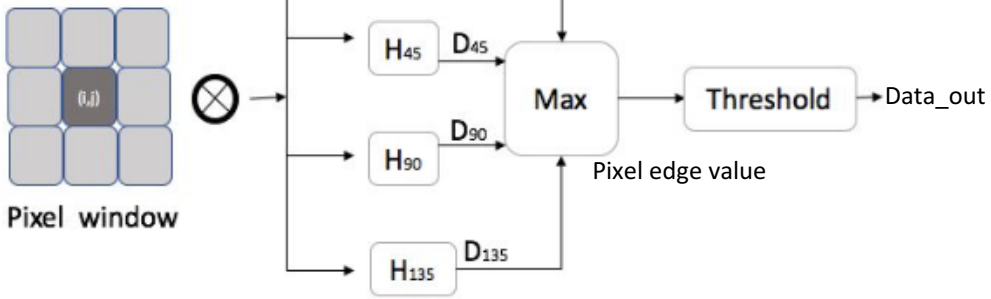
Line buffer

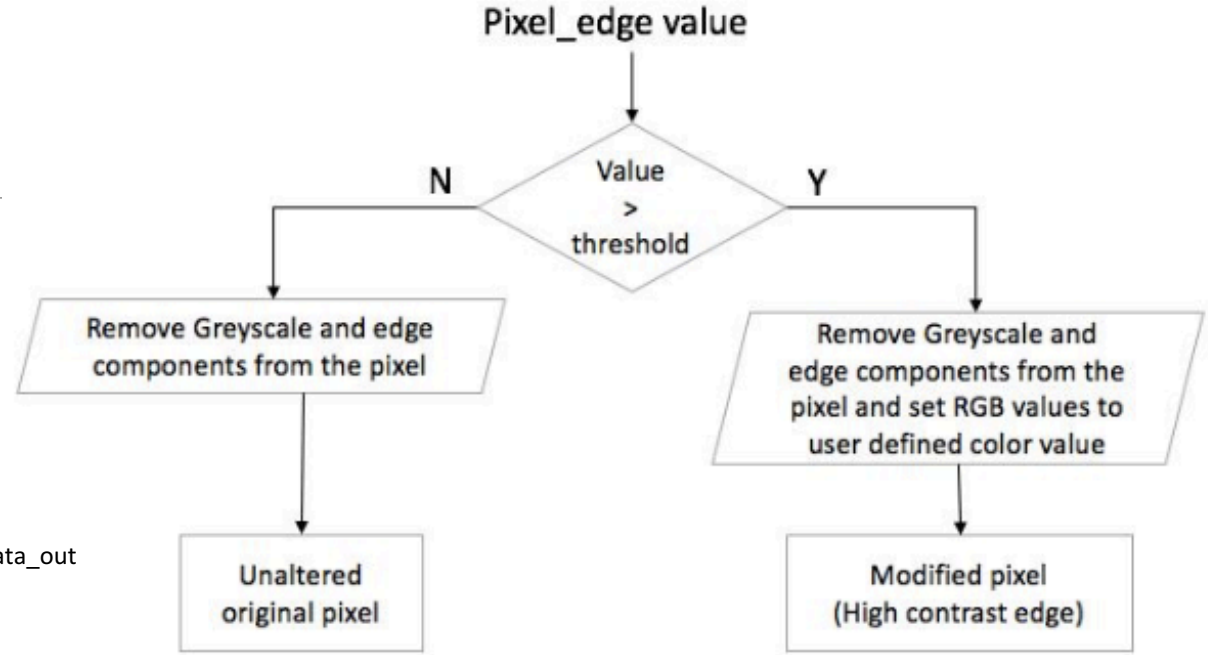


Case	Code	Condition
C1	1000	L_ptr=0 &c_ptr=0
C2	1001	L_ptr=0 &c_ptr/=0 &c_ptr /= (columns-1)
C3	1010	L_ptr=0 & c_ptr /= (columns-1)
C4	1011	L_ptr/=0 & L_ptr/=0(Rows-1) & c_ptr /= (columns-1)
C5	1100	L_ptr/=0(Rows-1) & c_ptr /= (columns-1)
C6	1101	L_ptr/=0(Rows-1) & c_ptr/=0 & c_ptr /= (columns-1)
C7	1110	L_ptr/=0(Rows-1) & c_ptr/=0
C8	1111	L_ptr/=0 & L_ptr/=0(Rows-1) & c_ptr/=0
C9	0001	Normal case
	0000	NO ACTION

L_ptr = Row pointer
C_ptr = Column pointer

Sobel kernel





$$H_0 = \begin{bmatrix} -1 & -2 & -1 \\ 0 & 0 & 0 \\ 1 & 2 & 1 \end{bmatrix} \quad H_{45} = \begin{bmatrix} -2 & -1 & 0 \\ -1 & 0 & 1 \\ 0 & 1 & 2 \end{bmatrix} \quad H_{90} = \begin{bmatrix} -1 & 0 & 1 \\ -2 & 0 & 2 \\ -1 & 0 & 1 \end{bmatrix} \quad H_{135} = \begin{bmatrix} 0 & 1 & 2 \\ -1 & 0 & 1 \\ -2 & -1 & 0 \end{bmatrix}$$

Multiplying by:-
-1 = 2s compliment
-2 = left shift and 2s compliment
2 = left shift

Second Evaluation

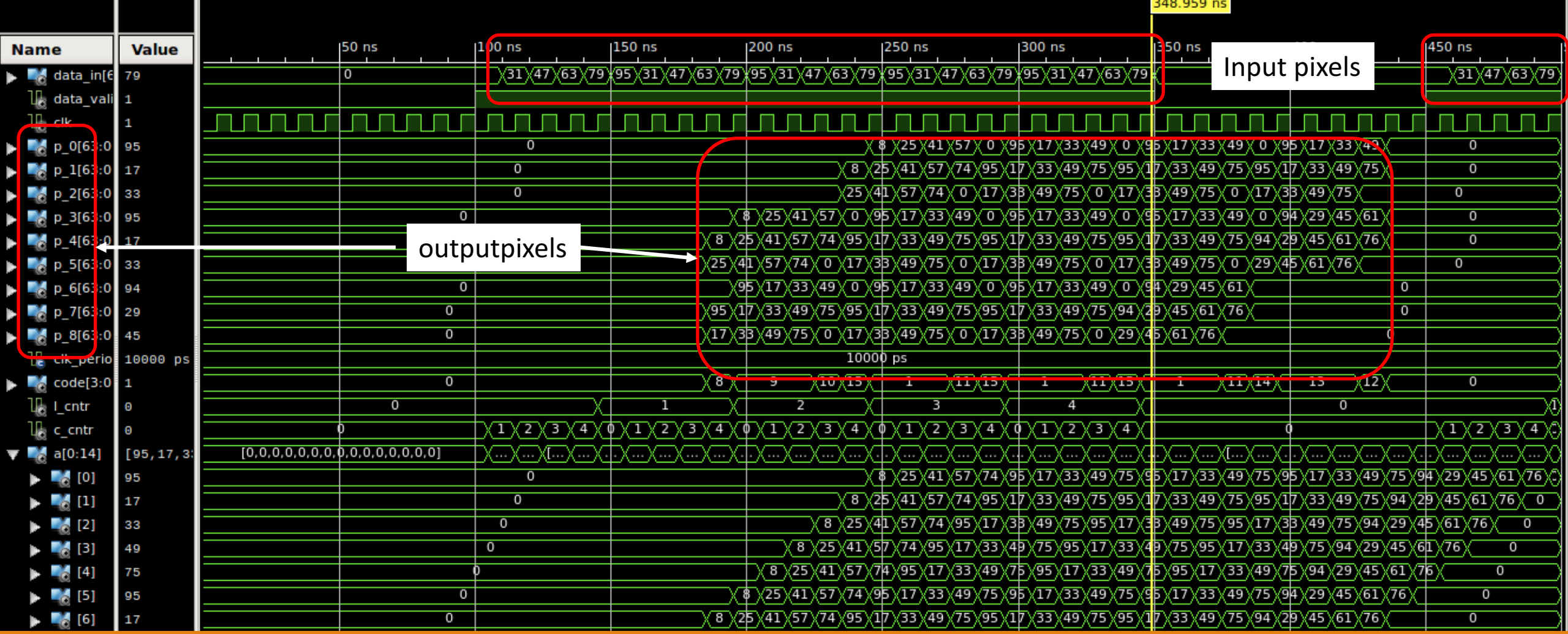
tasks

1: Simulate the IP from top level to the structural level

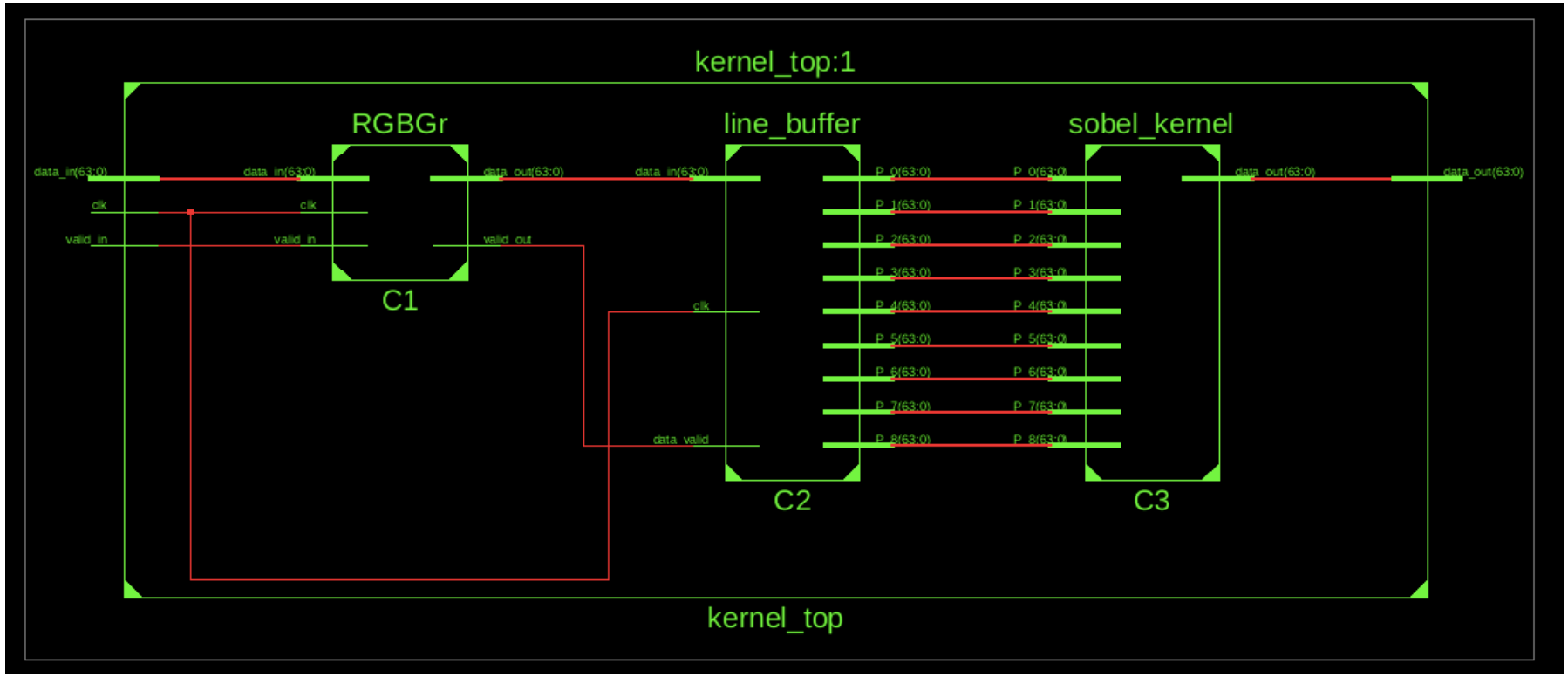
2: Instantiate the IP into the AXIOM pipeline

Simulation

- To Simulate the IP the main structure was the line buffer.
- To test the line buffer, external signals in form of random pixel values were forced on the line buffer (5x5 for testing purpose) over a period of time so that all the pixels streams through the pipeline.
- The result of the pipeline was observed and the generated window pixels were compared so as to verify the correct functioning of the pipeline.
- The top module was tested to see if the output stream removes the blue and green component from the incoming pixels whose grey value was below a preset thresh hold.



Simulation result for line buffer



RTL schematic of the IP

Instantiation

INSTANTIATE THE IP INTO THE AXIOM PIPELINE

Output Image Processing Pipeline (new)