Project Name: Design a 8*3 Encoder Using Candence Virtuoso.

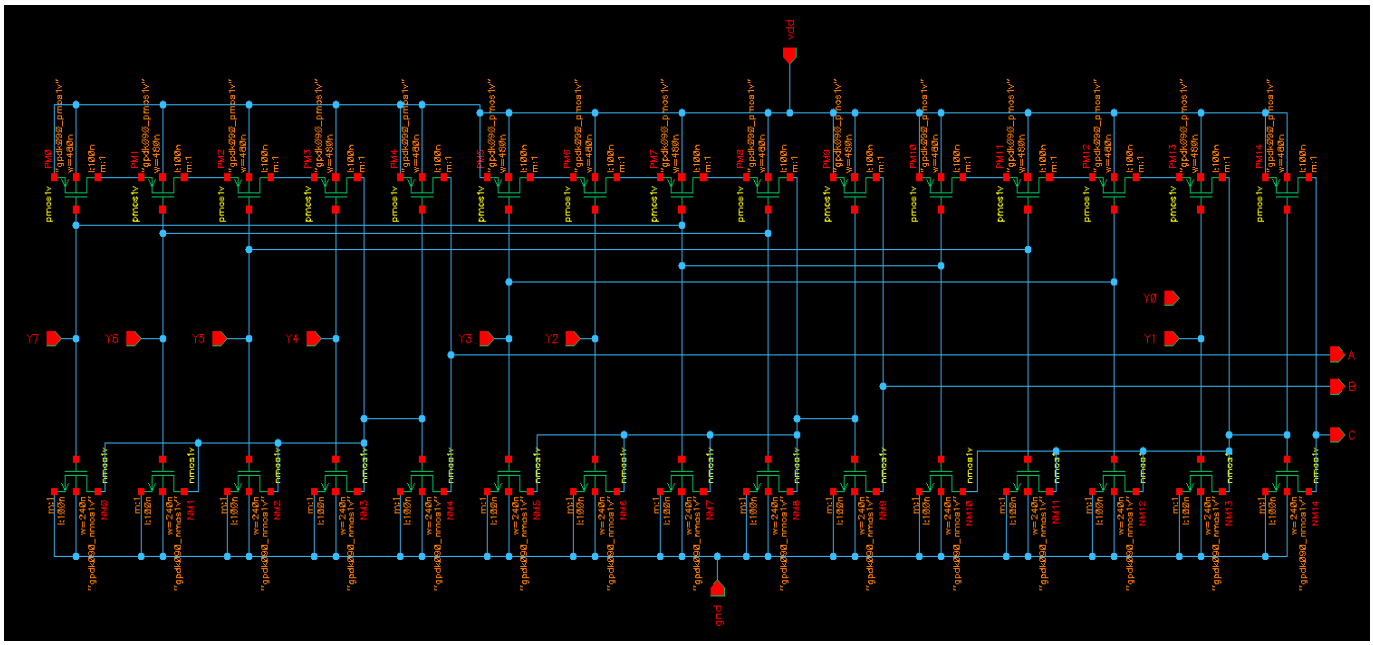

Fig.01: Schematic view of designed 8*3 Encoder using Cadence Virtuoso.

This diagram shows the schematic design of an 8-to-3 encoder in Cadence Virtuoso. Here, inputs Y0 to Y7 represent the 8 decimal values, while outputs A, B, and C form the 3-bit binary code, with A as the most significant bit and C as the least significant bit.

Fig.02: ADE Simulation output of 8*3 Encoder.

This Fig.02 illustrates the simulation of the 8-to-3 encoder in the Analog Design Environment (ADE) to verify its functionality. The output confirms the correct encoding of decimal inputs to binary outputs.

Fig.03: ADE Simulation with power usage.

This diagram extends the ADE simulation to include power usage analysis, providing insight into the encoder's power efficiency during operation.

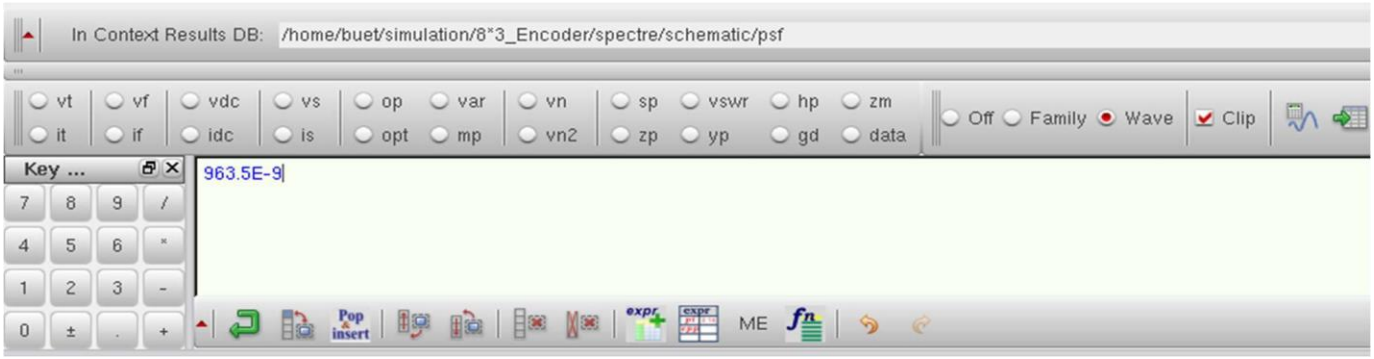

Fig.04: Measured power draw.

Here, the power usage of the 8-to-3 encoder is calculated using Cadence's calculator tool. This step is crucial for evaluating the power efficiency of the encoder design.

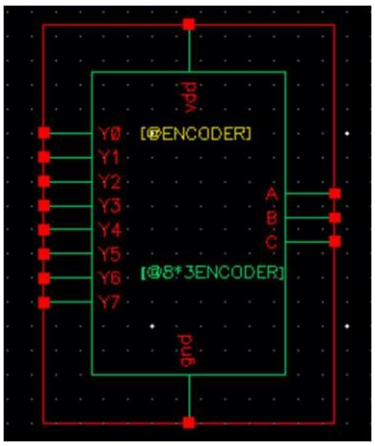

Fig.05: Symbol view of 8*3 Encoder.

Fig.05 is the symbol view of the encoder, representing its functionality in a simplified, icon-based form, which can be used for hierarchical designs in Cadence.

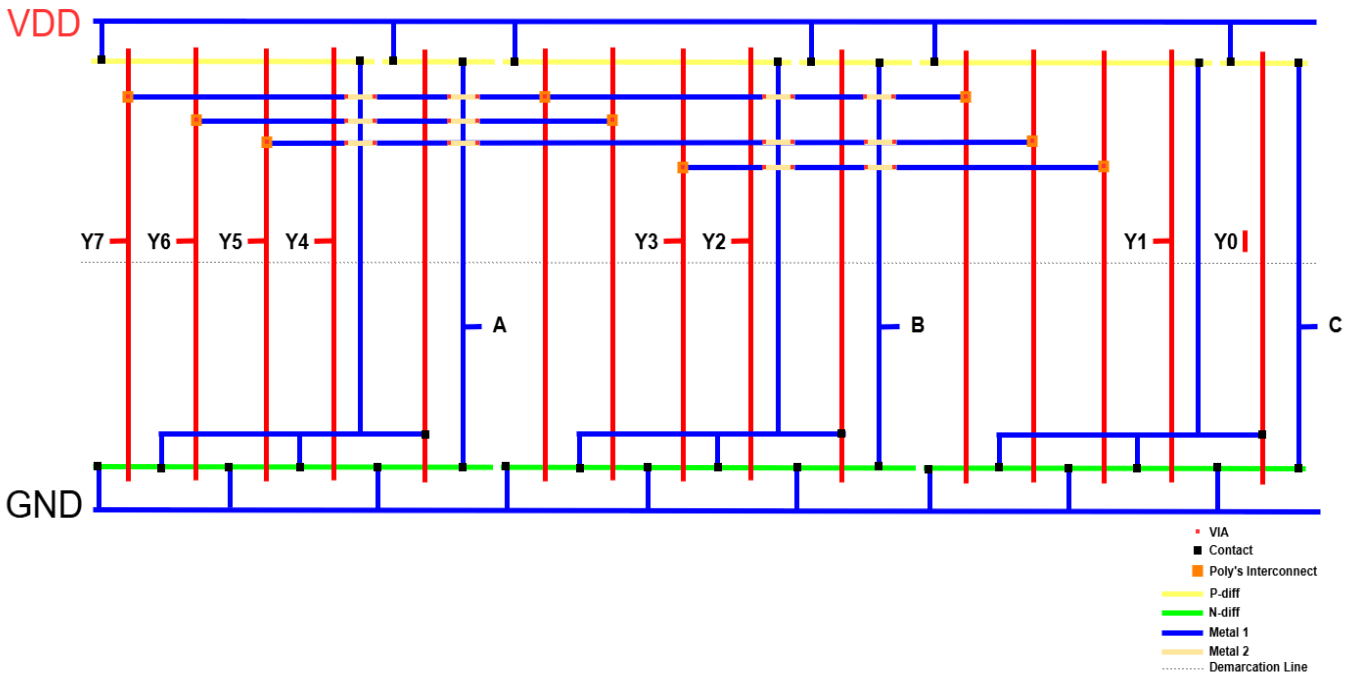

Fig.06: Stick Diagram of Designed 8*3 Encoder.

This stick diagram visually represents the layout of the encoder's transistors and connections, providing a basic view of the physical design before layout implementation.