EE 648 – VLSI Design

Binary Coded Hexadecimal for a 7 Segment Display

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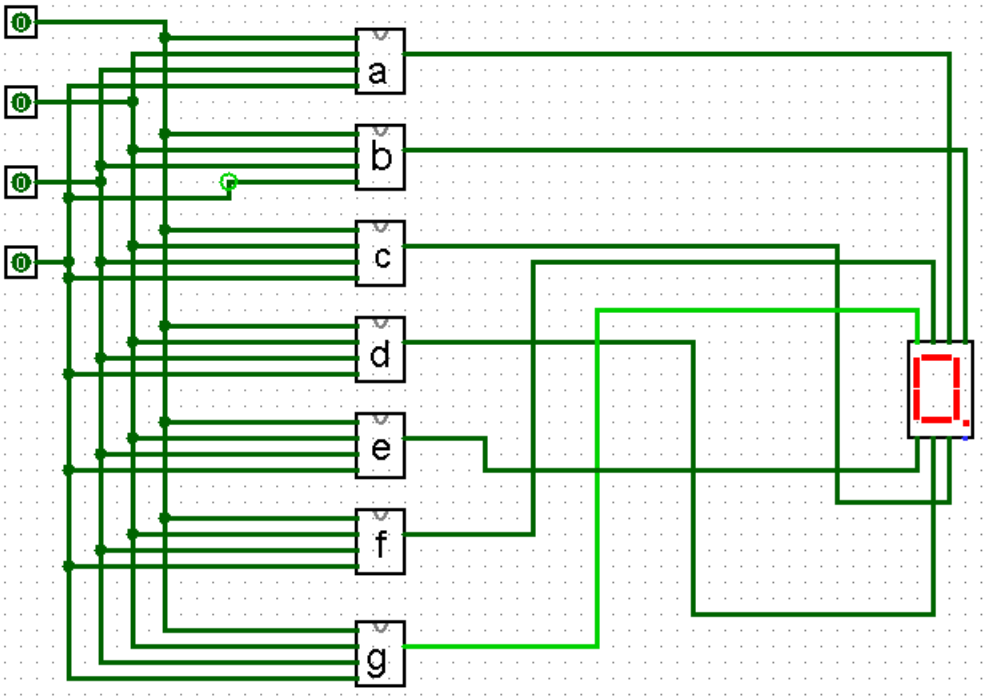

Figure 1: Circuit top level layout

$$a = \overline{(\bar{A}\bar{B}\bar{C}D)}\,\overline{(\bar{A}B\bar{C}\bar{D})}\,\overline{(A\bar{B}CD)}\,\overline{(AB\bar{C}D)} \tag{1}$$

$$b = \overline{(\bar{A}B\bar{C}D)}\,\overline{(B\bar{C}\bar{D})}\,\overline{(\bar{A}CD)}\,\overline{(AB\bar{D})} \tag{2}$$

$$c = \overline{(\bar{A}\bar{B}C\bar{D})}\,\overline{(AB\bar{D})}\,\overline{(ABC)} \tag{3}$$

$$d = \overline{(\bar{B}\bar{C}D)}\,\overline{(\bar{A}B\bar{C}\bar{D})}\,\overline{(B\bar{C}D)}\,\overline{A\bar{B}C\bar{D}} \tag{4}$$

$$e = \overline{(\bar{A}D)}\,\overline{(\bar{B}\bar{C}D)}\,\overline{(\bar{A}B\bar{C})} \tag{5}$$

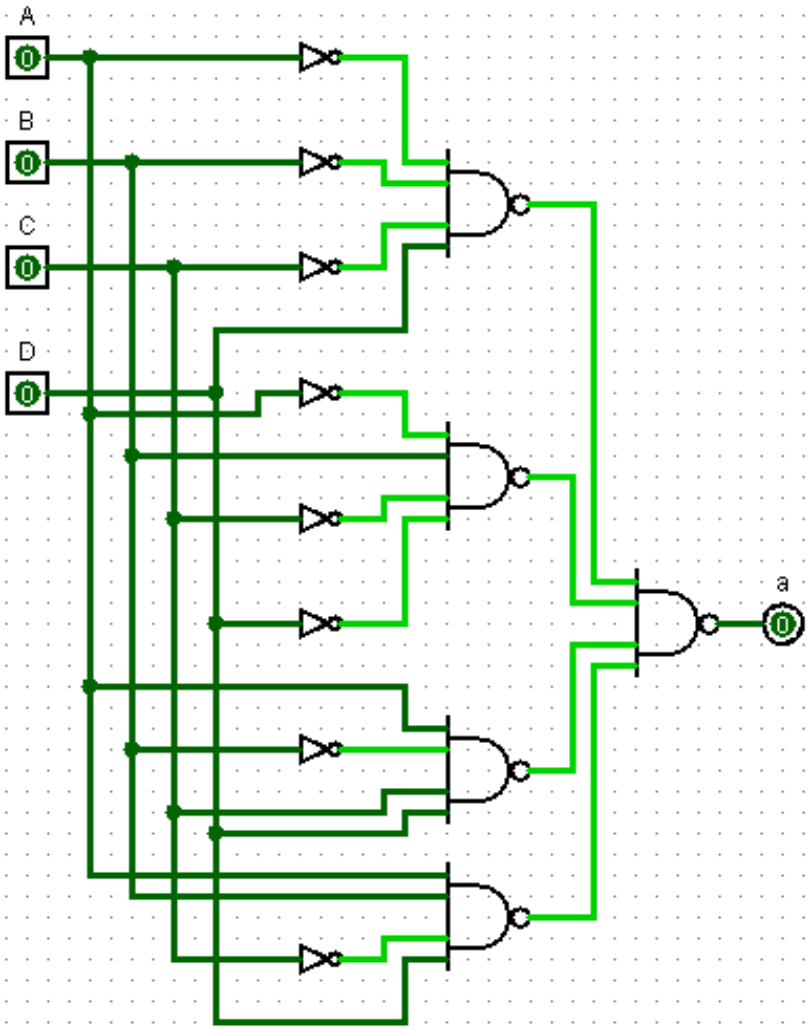

Figure 2: Block a Gate Level Schematic

$$f = \overline{\overline{(\bar{A}\bar{B}D)}\,\overline{(\bar{A}\bar{B}C)}\,\overline{(\bar{A}CD)}\,\overline{(A\bar{B}\bar{C}D)}} \tag{6}$$

$$g = \overline{\overline{(\bar{A}\bar{B}\bar{C})}\,\overline{(\bar{A}BCD)}\,\overline{(AB\bar{C}\bar{D})}} \tag{7}$$

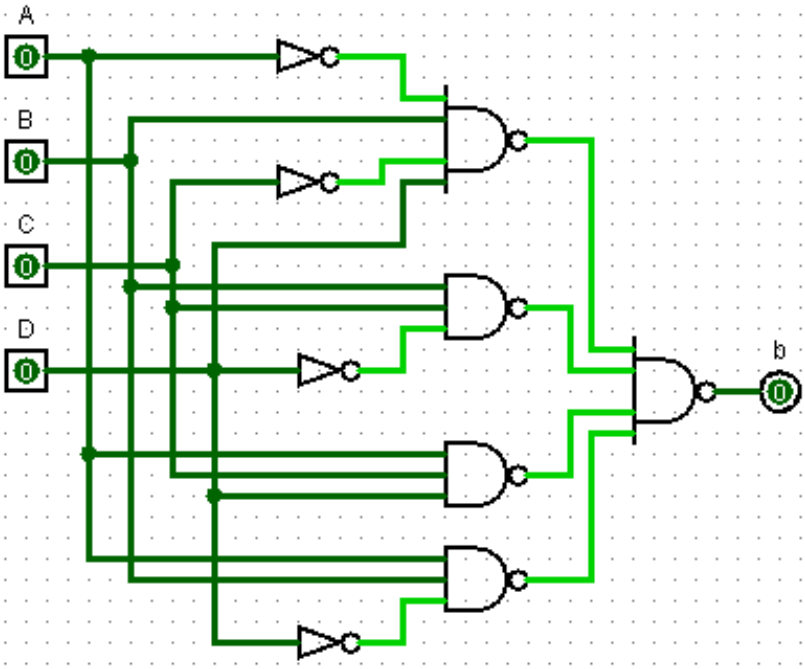

Figure 3: Block b Gate Level Schematic

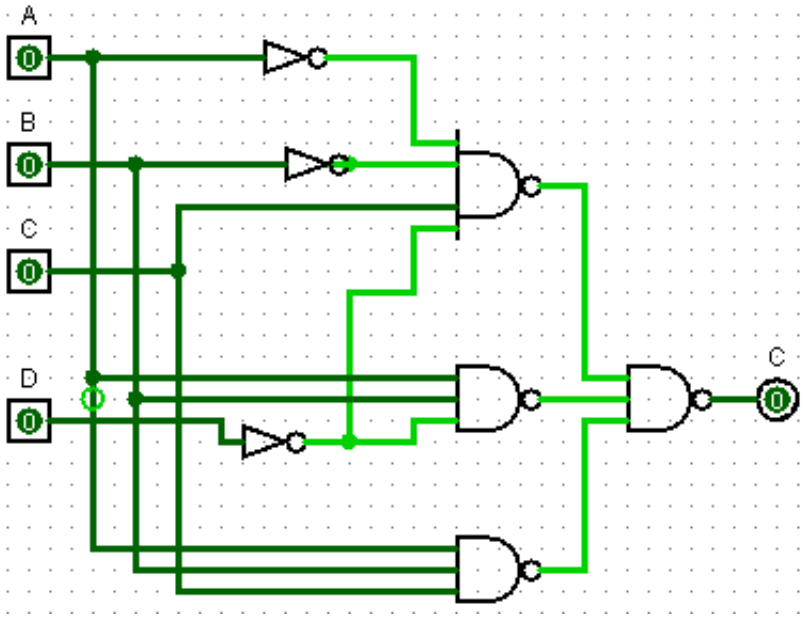

Figure 4: Block c Gate Level Schematic

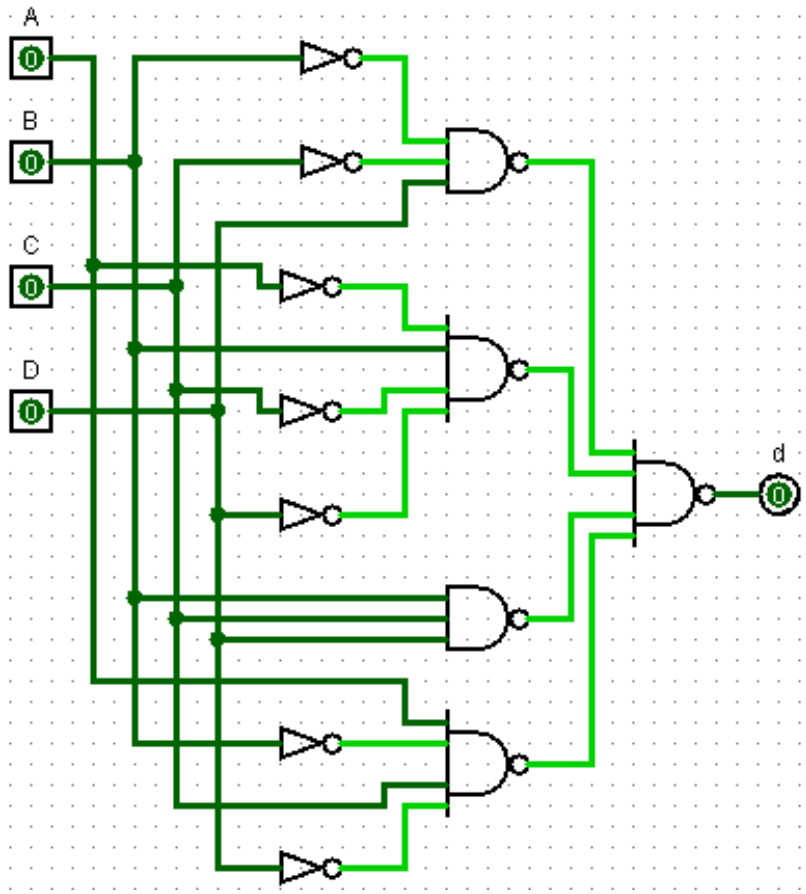

Figure 5: Block d Gate Level Schematic

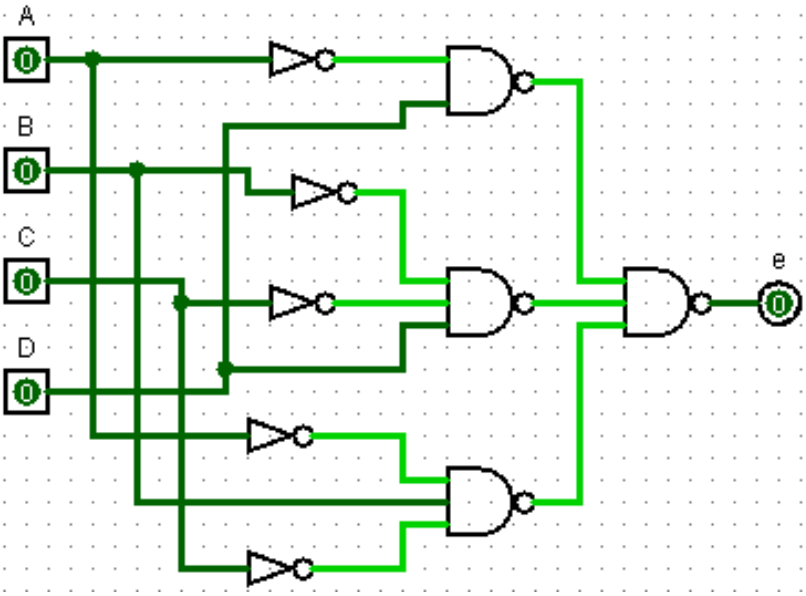

Figure 6: Block e Gate Level Schematic

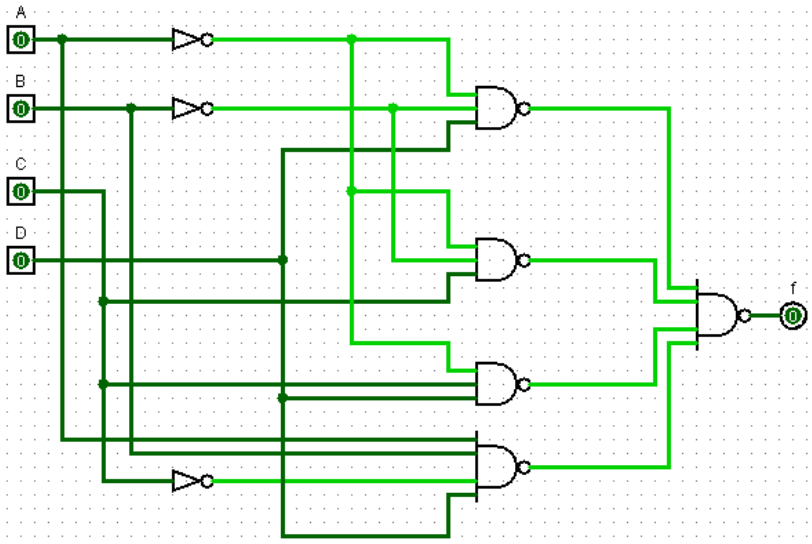

Figure 7: Block f Gate Level Schematic

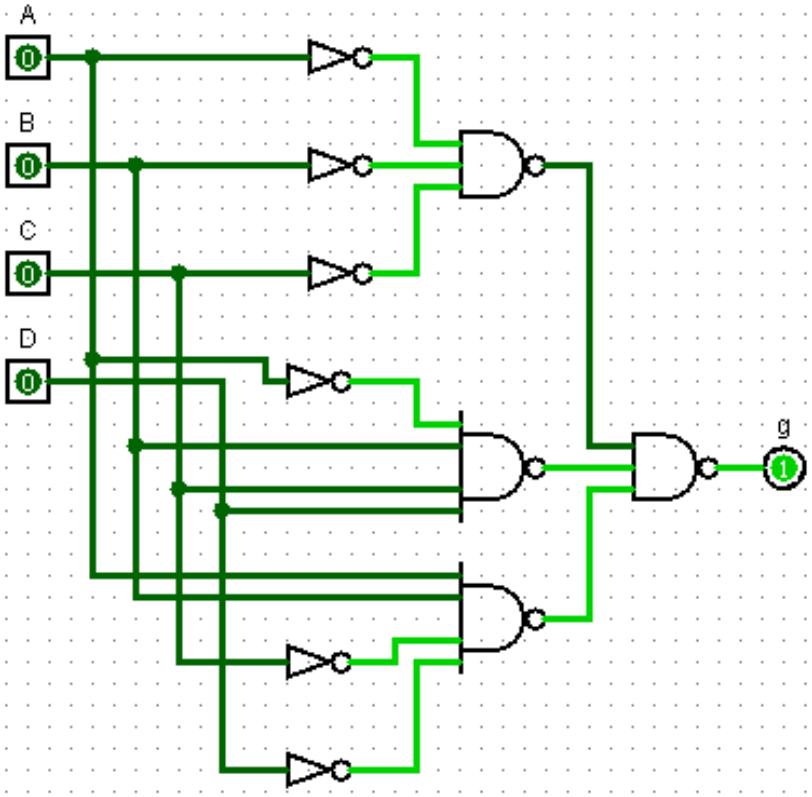

Figure 8: Block g Gate Level Schematic