EE 648 – VLSI Design

Binary Coded Hexadecimal for a 7 Segment Display

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1 Introduction

The goal of this project is to design and fabricate a chip that will use 4 input bits to control a 7 segment display. An integrated circuit such as this can be used to connect a 7 segment display to a microcontroller, reducing the number of output pins required to drive the display. Four output pins of the controller are used to input the number to the IC, which then uses open collector outputs to pull down the cathodes of the 7 segment display.

2 Top Level Design

The general strategy with the design is to separate the logic for each segment into its own module. Each module will be routed to an output pin through an open collector transistor to drive the 7 segment display. The top level diagram is shown in Figure 1.

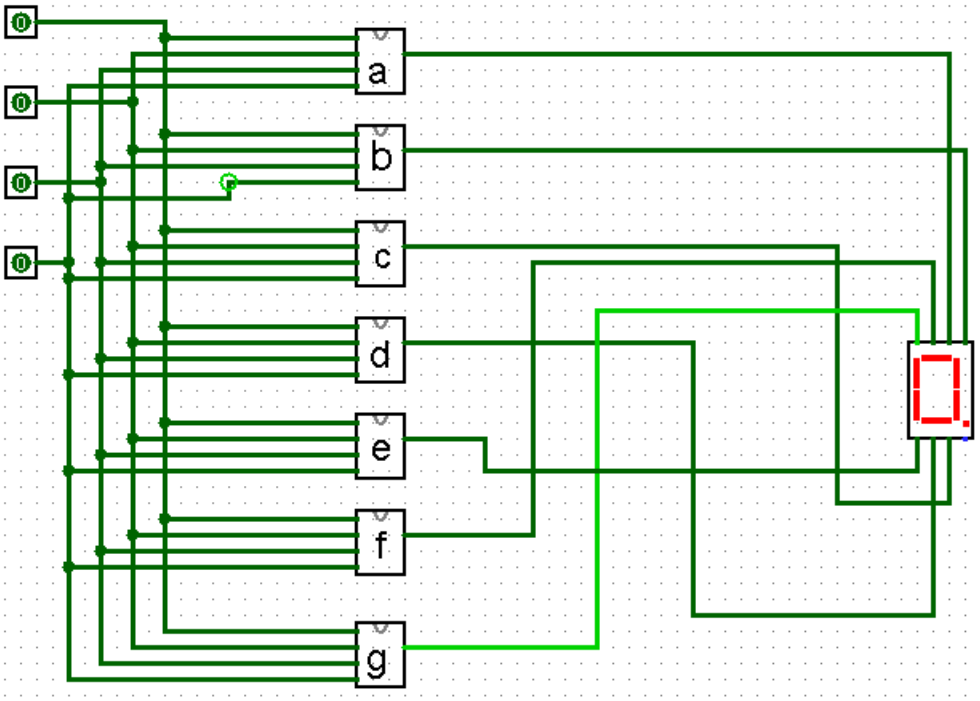

Figure 1: Circuit top level layout

Many of the gate level circuits use the inputs as well as their complements. To reduce the number of gates in the final design, the inputs will each be inverted before being to the logic circuitry. This will minimize redundancies in the gate layout. This has not been included in

this iteration of the design.

3 Detailed Design

3.1 Gate Level

The truth table for the four inputs and all seven outputs was created, it is shown in Figure 2.

Inputs				Outputs						
A	B	C	D	a	b	c	d	e	f	g
0	0	0	0	0	0	0	0	0	0	1
0	0	0	1	1	0	0	1	1	1	1
0	0	1	0	0	0	1	0	0	1	0
0	0	1	1	0	0	0	0	1	1	0
0	1	0	0	1	0	0	1	1	0	0
0	1	0	1	0	1	0	0	1	0	0
0	1	1	0	0	1	0	0	0	0	0
0	1	1	1	0	0	0	1	1	1	1
1	0	0	0	0	0	0	0	0	0	0
1	0	0	1	0	0	0	1	1	0	0
1	0	1	0	0	0	0	1	0	0	0
1	0	1	1	1	1	0	0	0	0	0
1	1	0	0	0	1	1	0	0	0	1
1	1	0	1	1	0	0	0	0	1	0
1	1	1	0	0	1	1	0	0	0	0
1	1	1	1	0	1	1	1	0	0	0

Figure 2: Circuit Truth Table

The truth table was transferred to the free software Logisim one output at a time. Logisim analyzed the truth table for each output bit and generated a minimized NAND Boolean expression. Utilizing inverting logic will reduce the number of inverters required to realize the circuit. Note that a zero in the output represents an active segment. The equivalent set of logic equations is shown in Appendix B.

Each logic equation represents a block on the top level diagram, and has a corresponding series of gates. The gate level design of these blocks is included in Appendix A.

3.2 Transistor Level

By optimizing the design to use only NAND gates the overall complexity is reduced. Efficient 2, 3, and 4 input NAND gates can be designed once and reused in block form. Apart from the NAND gates, an inverter will also be required. The transistor level design of these gates is shown in the figures below.

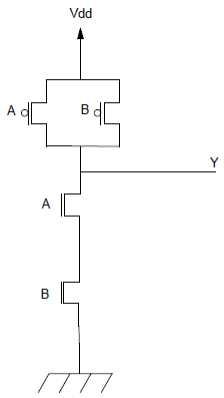

Figure 3: Circuit Truth Table

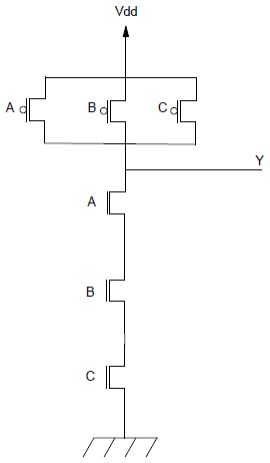

Figure 4: Circuit Truth Table

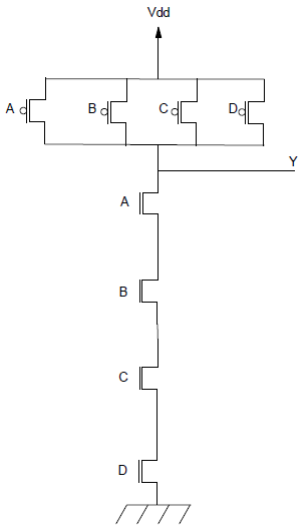

Figure 5: Circuit Truth Table

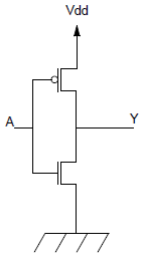

Figure 6: Circuit Truth Table

A Segment Logic Diagrams

A.1 Segment a

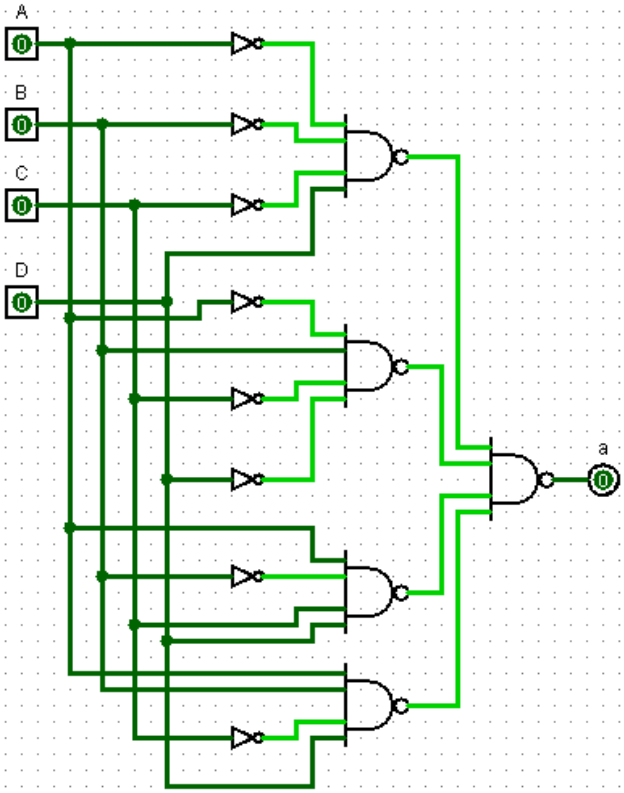

Figure 7: Block a Gate Level Schematic

A.2 Segment b

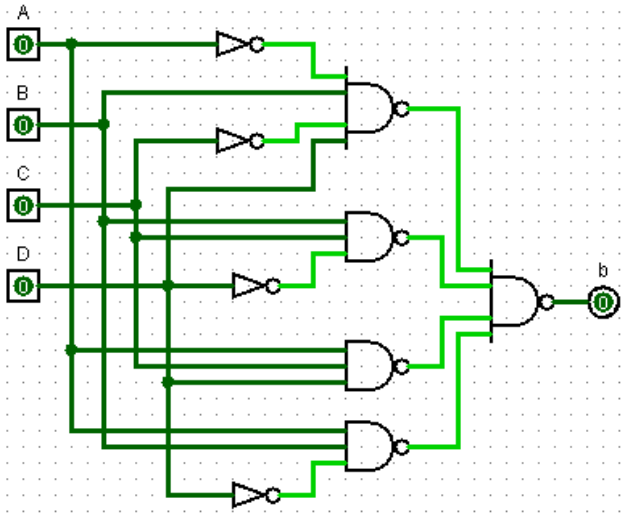

Figure 8: Block b Gate Level Schematic

A.3 Segment c

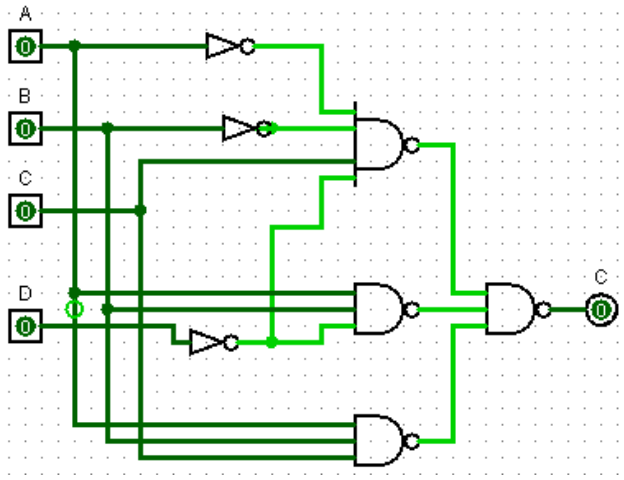

Figure 9: Block c Gate Level Schematic

A.4 Segment d

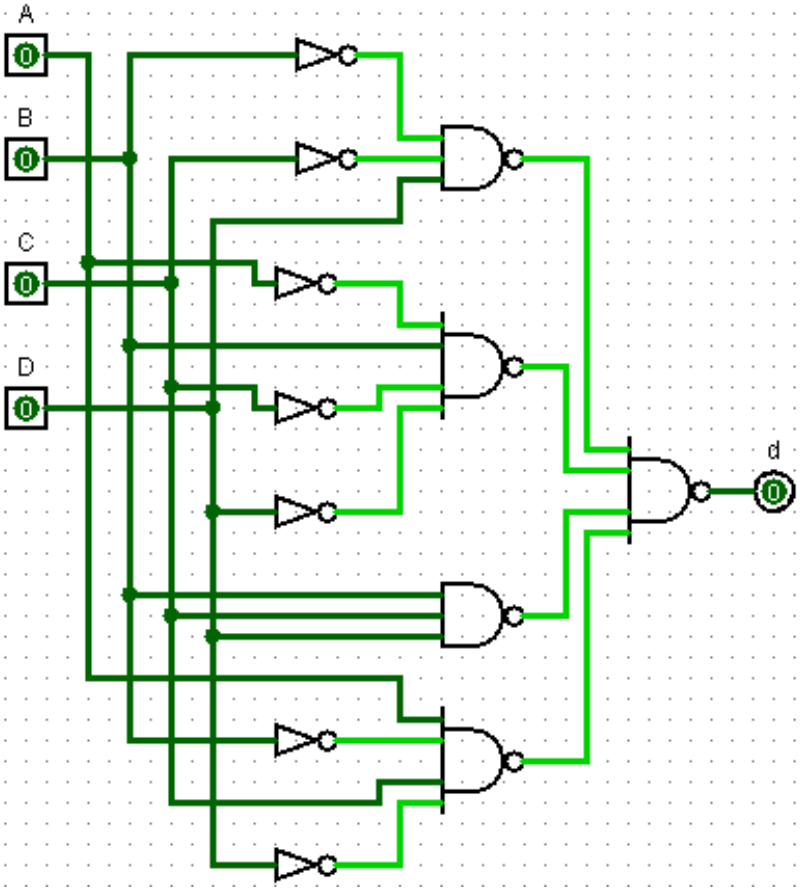

Figure 10: Block d Gate Level Schematic

A.5 Segment e

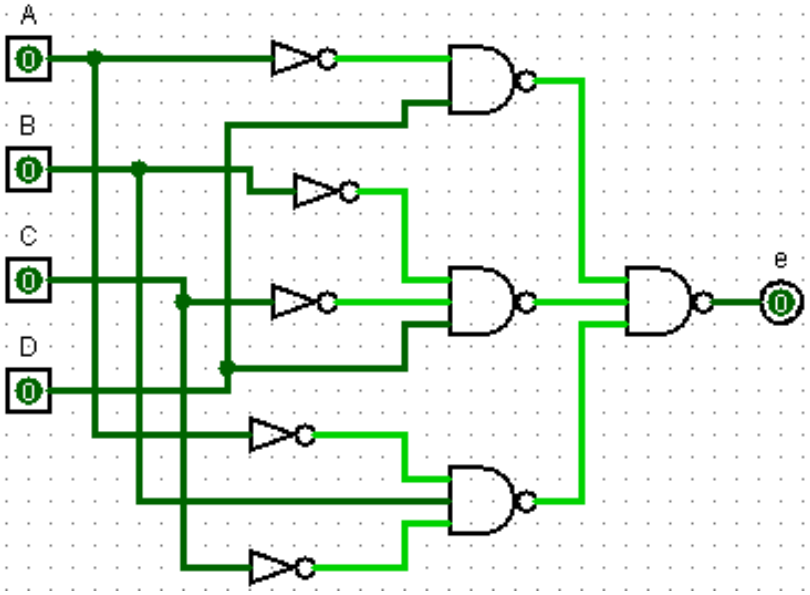

Figure 11: Block e Gate Level Schematic

A.6 Segment f

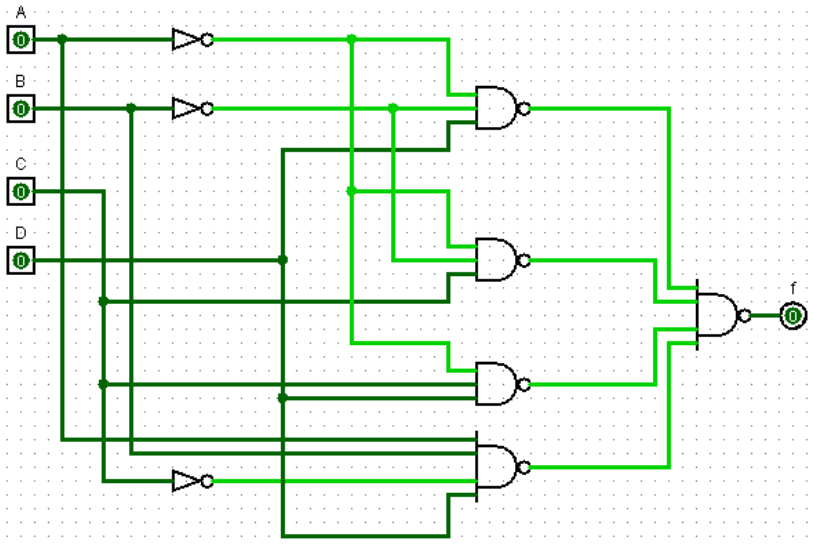

Figure 12: Block f Gate Level Schematic

A.7 Segment g

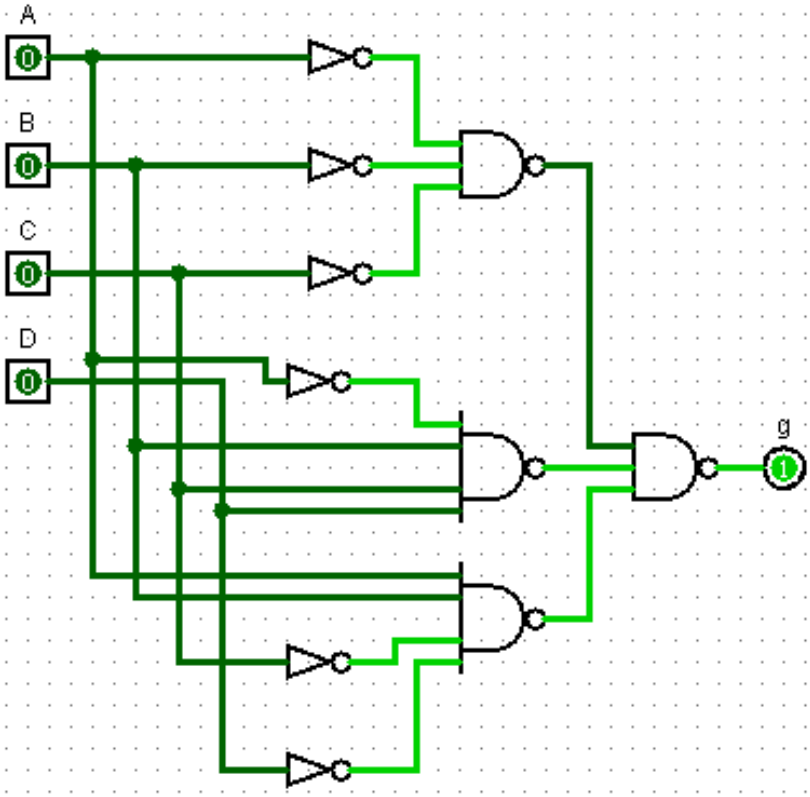

Figure 13: Block g Gate Level Schematic

B Logic Equations

$$a = \overline{\overline{(\bar{A}\bar{B}\bar{C}D)}\,\overline{(\bar{A}B\bar{C}\bar{D})}\,\overline{(A\bar{B}CD)}\,\overline{(AB\bar{C}D)}} \tag{1}$$

$$b = \overline{\overline{(\bar{A}B\bar{C}D)}\,\overline{(BC\bar{D})}\,\overline{(\bar{A}CD)}\,\overline{(AB\bar{D})}} \tag{2}$$

$$c = \overline{\overline{(\bar{A}\bar{B}CD)}\,\overline{(AB\bar{D})}\,\overline{(ABC)}} \tag{3}$$

$$d = \overline{\overline{(\bar{B}\bar{C}D)}\,\overline{(\bar{A}B\bar{C}\bar{D})}\,\overline{(BCD)}\,A\bar{B}C\bar{D}} \tag{4}$$

$$e = \overline{\overline{(\bar{A}D)}\,\overline{(\bar{B}\bar{C}D)}\,\overline{(\bar{A}B\bar{C})}} \tag{5}$$

$$f = \overline{\overline{(\bar{A}\bar{B}D)}\,\overline{(\bar{A}\bar{B}C)}\,\overline{(\bar{A}CD)}\,\overline{(AB\bar{C}D)}} \tag{6}$$

$$g = \overline{\overline{(\bar{A}\bar{B}\bar{C})}\,\overline{(\bar{A}BCD)}\,\overline{(AB\bar{C}\bar{D})}} \tag{7}$$